DESIGN CONSIDERATIONS FOR AN ECONOMICAL COMPACT MICROWAVE RECEIVER

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INTRODUCTION

The general trend in electronic equipment can be summarized by two words: smaller and smarter. Surveillance receivers are no exception to this rule. VHF and UHF surveillance receivers have undergone an especially rapid evolution in recent years. They have become smaller and more capable, in large part due to the use of microprocessors. Frequency synthesis and formally exotic functions, such as computer control, have become commonplace. Surprisingly, increased performance has generally been accompanied by decreased price. On the other hand, microwave receivers have not advanced quite as rapidly.

The purpose of this paper is to explore recent trends in receiver design and to examine how they might be applied towards the design of a compact and capable, yet inexpensive microwave receiver. The receiver considered in this paper is presumed to tune over the range of 1 to 26 GHz.

RECEIVER ARCHITECTURE

Receiver architecture is influenced by several contradictory requirements which include tuning range, noise figure, elimination of spurious responses, and dynamic range. The wide tuning range of the receiver considered in this paper presents a special problem and will be considered first.

Superheterodyne receivers have traditionally employed down conversion to a first intermediate frequency somewhere below their tuning range. For example, all home FM broadcast receivers use an intermediate frequency of 10.7 MHz, roughly 10 percent of the tuned frequency. Recently, up conversion, the use of a first intermediate frequency above the receiver tuning range, has become popular. Up conversion has become practical with the advent of frequency synthesizers with adequate performance. One compact surveillance receiver tuning from 20 to 500 MHz up converts to a first intermediate frequency of 555 MHz. Since high quality filters are still easier to implement at lower frequencies, up conversion usually implies multiple conversion.

Both techniques have serious limitations when applied to the design of a broad frequency coverage microwave receiver. Image rejection considerations rule out down conversion, and up conversion requires very expensive high frequency (greater than 30 GHz) components.

Best microwave amplifier and filter performance is obtained in the 1 to 6 GHz range making a first intermediate frequency (IF) in this range attractive. A superheterodyne receiver, however, cannot tune through its own first intermediate frequency so two different first intermediate frequencies are required. The additional IF provides coverage at those frequencies for which the other IF cannot be used.

Figure 1 is a block diagram of a microwave receiver capable of tuning from 1 to 26 GHz. The first intermediate frequencies are 1940 and 4360 MHz. The second intermediate frequency is 1210 MHz, and the third conversion is to the standard intermediate frequency of 160 MHz in order to be compatible with existing signal monitoring and processing equipment. Wideband (10 to 100 MHz bandwidth) IF filtering and detection also takes place at 160 MHz. Narrowband (10 kHz to 10 MHz) signal processing is easier to realize at a lower frequency, so an additional frequency conversion to 21.4 MHz is required. The local oscillator for the last conversion is generated by a frequency synthesizer tuning from 138.1 to 139.1 MHz.

Careful selection of the intermediate frequencies can simplify the overall receiver design. All local oscillator signals, with the exception of the first local oscillator, are derived from a single fixed frequency multiplier chain. A low phase noise 50 MHz frequency reference provides the starting point for the frequency multiplier chain. This reference can be phase locked to an external standard if desired. Frequency multiplication by seven produces a signal at 350 MHz. A second multiplication by three generates the 1050 MHz conversion signal. Tripling once again produces the 3150 MHz local oscillator signal required by the second mixer. Schottky and step recovery diodes perform the frequency multiplication without the phase noise degradation often introduced by active frequency multipliers. Careful filtering is required throughout the frequency multiplier chain to preserve the spectral purity essential for spur-free operation. Filtering requirements are reduced by the use of a balanced multiplier for the initial multiplication that suppresses even order harmonics. This conversion scheme minimizes the conversion oscillator circuitry and reduces the number of spurious responses.

The receiver tuning range and the first intermediate frequency determine the local oscillator (LO) tuning range. In this receiver, the first LO signal is generated by a frequency synthesizer. Table 1 shows the combinations of local oscillator and first intermediate frequencies employed to tune from 1 to 26 GHz. The frequency synthesizer tunes from 4 to 8 GHz in 1 MHz steps. Finer tuning resolution is provided further down the receiver conversion chain by a second frequency synthesizer. The 1.94 GHz IF allows the receiver to tune through the portion of the spectrum occupied by the primary 4.36 GHz IF. Use of both high side and low side injection enables the receiver to cover 1 to 12 GHz while the first LO tunes only 4 to 8 GHz.

Above 12 GHz, the 4.36 GHz IF is used exclusively. The microwave synthesizer output is doubled or tripled to produce the necessary local oscillator signal. Doubling the synthesizer frequency permits coverage from 12 to 20 GHz, while tripling is used in the 18 to 29 GHz band. The synthesizer reference frequency is reduced by one half and one third, respectively, when tuning above 12 GHz in order to maintain consistent 1 MHz tuning resolution.

MICROWAVE FREQUENCY SYNTHESIZER

Frequency synthesis has a major impact upon the cost and performance of modern receiving systems. Frequency synthesizers provide good stability and lend themselves to easy remote control; however, a poorly designed synthesizer can degrade the performance of the entire receiver. In addition, the frequency synthesizer may represent a substantial portion of the overall receiver price. For these reasons, it is worthwhile to discuss a design approach that might be employed in the design of the phase locked loop synthesizer intended for use in a microwave receiver.

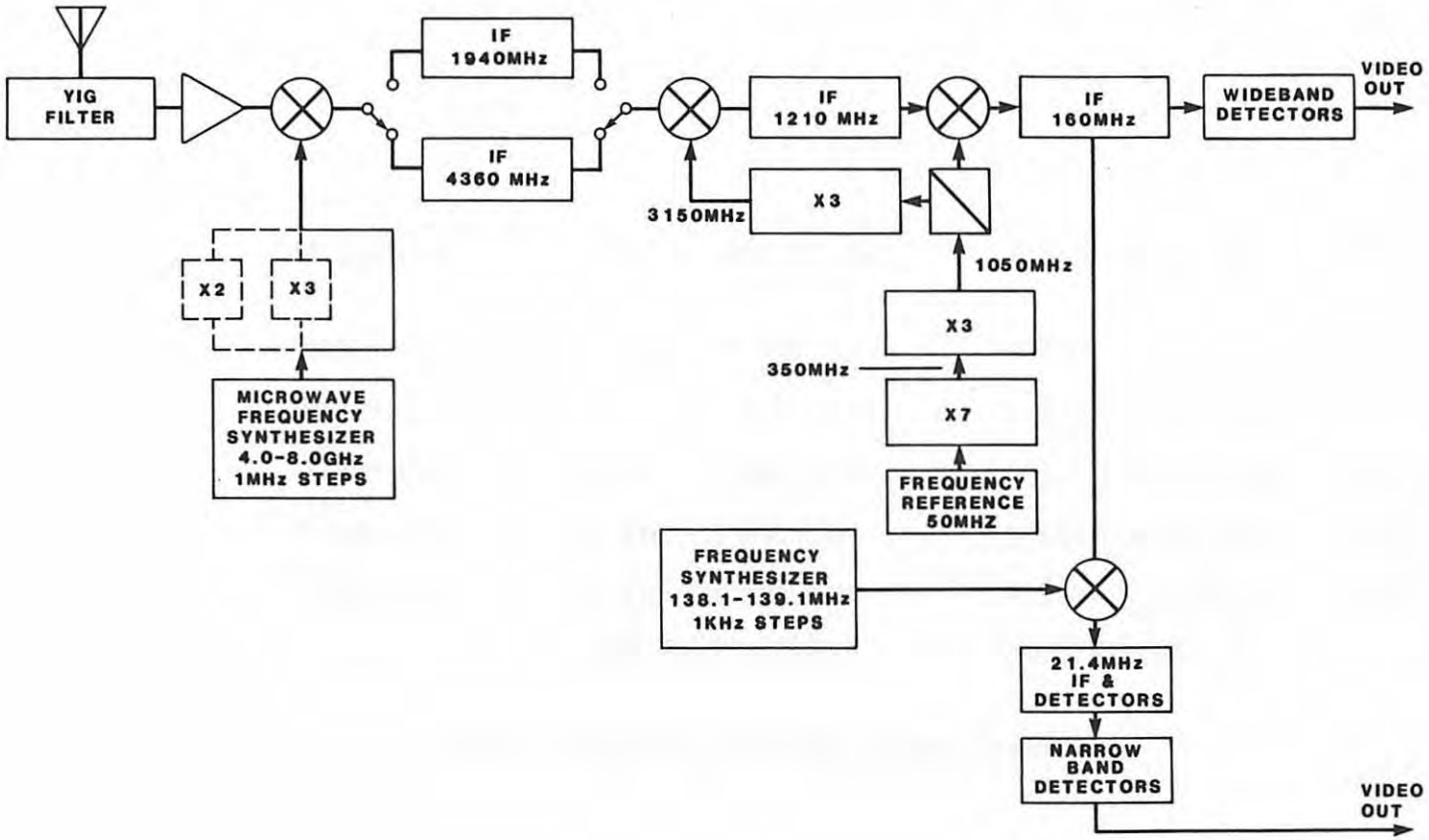

Figure 1. Microwave Receiver Block Diagram

Table 1. Receiver Frequency Conversion Scheme

Received Frequency	First IF	First Local Oscillator	Image Frequency	Comments
1 - 3 GHz	4.360 GHz	5.360 - 7.360 GHz	9.720 - 11.720 GHz	High Side Injection
3 - 6 GHz	1.940 GHz	4.940 - 7.940 GHz	6.880 - 9.88 GHz	High Side Injection
6 - 9 GHz	1.940 GHz	4.060 - 7.060 GHz	2.120 - 5.120 GHz	Low Side Injection
9 - 12.36 GHz	4.350 GHz	4.640 - 8.000 GHz	0.280 - 3.640 GHz	Low Side Injection
12.36 - 20.0 GHz	4.360 GHz	8.000 - 15.640 GHz	3.640 - 11.28 GHz	Low Side Injection YIG Frequency x 2
18.0 - 29 GHz	4.360 GHz	13.640 - 23.640 GHz	9.28 - 19.28 GHz	Low Side Injection YIG Frequency x 3

Random short term frequency deviations of any oscillator are responsible for the phenomena of phase noise; an important measure of synthesizer performance. The local oscillator phase noise can limit the maximum signal to noise ratio that can be achieved during the reception of frequency modulated (FM) or phase modulated (PM) signals. It can also increase the bit error rate experienced during reception of phase shift keyed (PSK) signals and limit the maximum noise power ratio in FM/FDM (frequency division multiplex) systems. Reciprocal mixing can degrade receiver selectivity by causing an increase in the noise floor when a strong signal appears just outside the receiver passband. This effect limits the ability of a receiver to recover weak signals in the presence of interference. The performance degradation listed above can only be overcome by reducing the synthesizer phase noise.

One way to limit synthesizer phase noise is to use a low noise voltage tuned oscillator (VCO). At microwave frequencies, only YIG (Yttrium Iron Garnet) oscillators offer the combination of low noise operation and wide tuning range needed for a high performance receiver local oscillator. This is largely due to the excellent Q presented by the YIG resonator. Varactor tuned oscillators lack this high Q resonant circuit and are consequently fairly noisy. Cavity resonators make very fine low noise oscillators, but their electrical tuning range is restricted to a few percent at most. YIG oscillators have the disadvantage of being somewhat bulky and expensive. Also, the YIG tuning coil and heater consume a fair amount of electrical power.

The oscillator phase noise can be further reduced by phase locking. The phase locked loop (PLL) sees oscillator phase noise inside its loop bandwidth as short term frequency variations. The loop cancels these variations by introducing a correction of equal magnitude but of opposite sign. The PLL determines oscillator frequency (or phase) deviations by comparison against a stable reference frequency. Because the phase detector cannot distingush between VCO and reference frequency variations, the degree of phase noise improvement is limited by the noise performance of the reference. Reference frequency disturbances are transferred directly to the VCO. This process replaces the close in VCO noise with the corresponding reference spectra.

In a single loop synthesizer, the VCO operates at an integer multiple of the reference frequency and is divided down for phase comparison. As a rule, the locked VCO exhibits the same close in noise performance that would be expected if the reference were multiplied up to the VCO frequency; however, dividers are not noise free. For example, TTL dividers exhibit noise levels in the vicinity of -155 dBc. The noise is largely due to the uncertainty in the determination of the exact moment at which the input changes state. The divider noise contribution can become significant if the divisor is sufficently large. Heterodyne techniques can be used to lower the VCO frequency before division, thereby alleviating the need for large divisors.

MICROWAVE FREQUENCY SYNTHESIZER IMPLEMENTATION

Figure 2 is a simplified block diagram of a microwave receiver first local oscillator. It is a frequency synthesizer that tunes from 4 to 8 GHz in 1 MHz steps using the techniques discussed earlier to achieve good phase noise performance. A YIG oscillator forms the heart of the synthesizer. Frequency heterodyning and division convert a portion of the YIG output to 1 MHz for phase comparison with a 1 MHz reference. Figure 3 illustrates the two

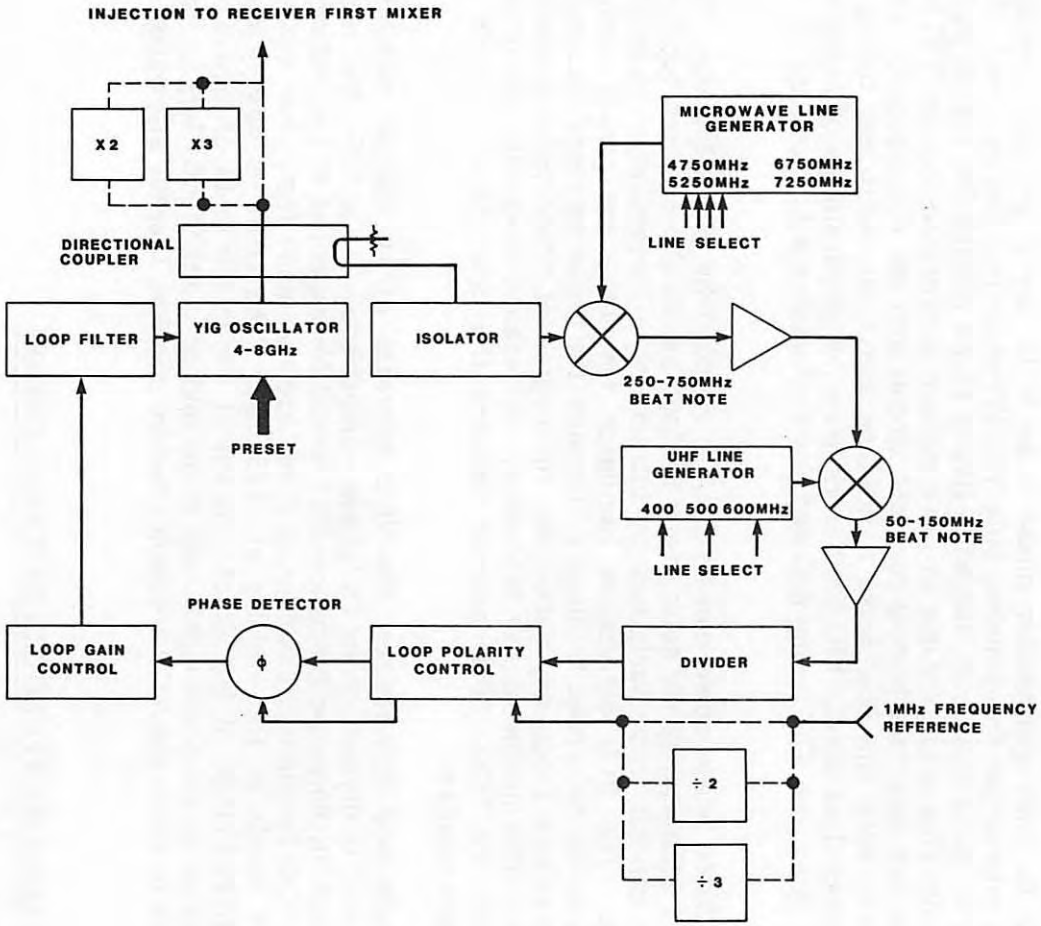

Figure 2. Block Diagram of First LO Frequency Synthesizer

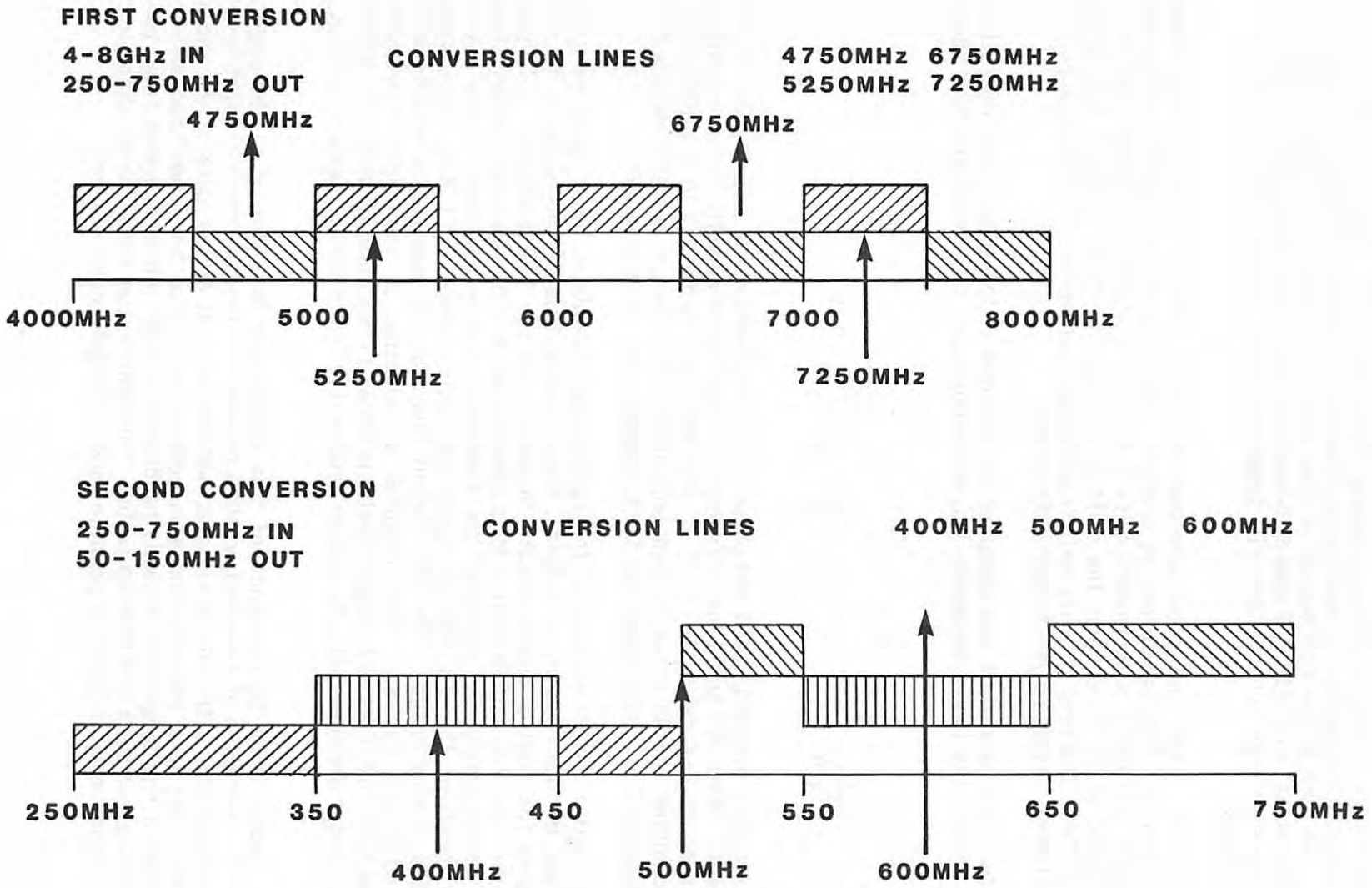

Figure 3. First Synthesizer Frequency Conversion

step heterodyning process. The first conversion uses one of four microwave lines to mix the YIG output to an intermediate frequency ranging from 250 to 750 MHz. After filtering and amplification, a second conversion is performed creating a second intermediate frequency from 50 to 150 MHz. The rest of the synthesizer follows traditional lines. A digital divider lowers the 50 to 150 MHz signal to 1 MHz for phase comparison against a 1 MHz reference signal. The phase detector error voltage controls the YIG frequency after passing through the loop filter and gain control blocks.

Since both upper and lower side beat notes are used in the frequency conversion process, the loop polarity may sometimes be reversed. As a result, an upward drift in the YIG oscillator frequency will cause a downward drift in the signal seen by the phase detector. The loop will try unsuccessfully to correct the drift by forcing the YIG higher in frequency. To overcome this problem, the loop polarity switch exchanges the signal and reference ports of the phase detector, thereby inverting the polarity of the loop.

Proper loop bandwidth and damping are essential to low phase noise operation. The equations below define the loop bandwidth, Wn, and damping, ξ, for second order phase lock loops:

$$W_n = \sqrt{\frac{K}{\tau_1 N}} \qquad \xi = \frac{\tau_2}{2}\sqrt{\frac{K}{\tau_1 N}}$$

where K is the loop gain including VCO and phase detector sensitivities, and τ_1 and τ_2 are the loop time constants. Both Wn and ξ are a function of the loop divisor N. In this synthesizer, N varies over a three to one ratio ($50 \leq N \leq 150$) and will cause a 3 to 1 variation in both bandwidth and damping factor unless a complementary gain change is made elsewhere in the loop. The loop gain control circuit provides the necessary gain compensation.

The digital divider section of the synthesizer accepts an input signal ranging from 50 to 150 MHz and divides it down to 1 MHz. Phase comparison of this signal with a 1 MHz reference produces the control signal needed to phase lock the YIG oscillator. Changing the division ratio moves the YIG oscillator in 1 MHz steps across a 150 MHz band. Wider frequency transitions are accomplished by changing the frequency conversion lines in the heterodyne section. Taken together, the YIG can be tuned and phase locked in 1 MHz steps across its entire 4 to 8 GHz tuning range. The YIG output frequency is doubled or tripled when the receiver is tuned above 12 GHz. This requires a reduction in the synthesizer reference frequency by one half and one third, respectively, in order to maintain consistent 1 MHz tuning resolution. The divider division ratio, N, is also doubled ($100 \leq N \leq 300$) or tripled ($150 \leq N \leq 450$) in this case.

The phase noise performance of this synthesizer is achieved at the expense of control complexity. For each of the 4000 possible output frequencies, the YIG must be preset, the proper microwave and UHF lines activated, and the correct divisor determined and loaded into the counters. The loop polarity and gain control must also be determined and set up. Fortunately, a task of this magnitude is easily handled by a small microprocessor and a hand full of relatively simple algorithms and look-up tables. This synthesizer serves as an example of the RF performance improvements that are possible under microprocessor control.

138 MHz Frequency Synthesizer

The final frequency conversion in the receiver is from 160 MHz to 21.4 MHz. A single loop frequency synthesizer tuning from 138.1 to 139.1 MHz in 1 kHz steps serves as the local oscillator. Like the microwave synthesizer discussed earlier, this synthesizer must exhibit good phase noise characteristics. A lower operating frequency and recently developed integrated circuits help to simplify the design of this synthesizer and reduce its power consumption, size, and cost. Figure 4 is a block diagram of the synthesizer. The VCO operates at eight times the desired output frequency. Division by eight improves the overall synthesizer phase noise performance by 20 LOG(8) or 18 dB and reduces the loop lock time. As before, synthesizer phase noise is minimized by keeping the loop division ratio as low as possible. This goal is met by heterodyning a portion of the VCO output with a 1150 MHz note creating a beat note ranging from 37.2 to 45.2 MHz. The 1150 MHz note is generated by frequency multiplication of the 10 MHz reference frequency. Schottky and step recovery diodes are used to minimize the noise contribution of the frequency multiplier chain. The dual modulus control circuitry, a reference frequency divider and a phase detector are all contained on a single frequency synthesizer integrated circuit. Five integrated circuits are used by this synthesizer, contrasting with the 15 to 20 required to perform the same function in the past.

CONCLUSION

Recent developments in receiver design can be extended to include microwave receivers. A simple, yet versatile, receiver architecture allows broad frequency coverage and high performance in a small package. This architecture also reduces the amount of microwave circuitry thereby lowering cost and improving reliability. Heterodyning and microprocessor control techniques are valuable tools in the design of a low phase noise microwave frequency synthesizer.

ACKNOWLEDGMENT

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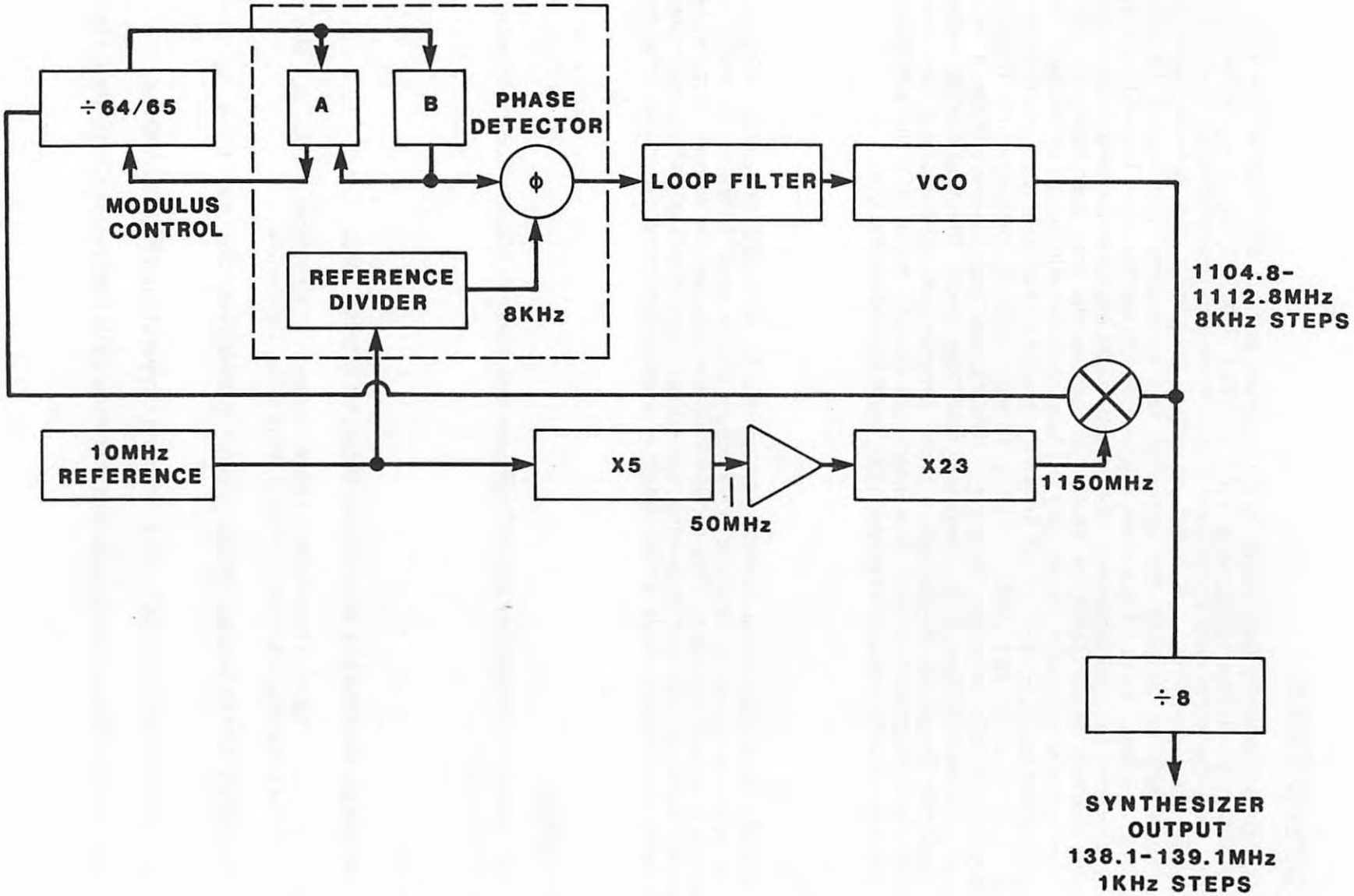

Figure 4. Block Diagram of 138 MHz Frequency Synthesizer

APPENDIX

The digital divider section of the microwave frequency synthesizer outlined in this paper must accept input signals ranging from 50 to 150 MHz. Unfortunately, fully programmable counters are not generally capable of operation above 50 MHz. Conventional dual modulus counters are capable of high frequency operation, but also have minimum divisor limitations that prohibit their use in this application. The solution to the problem is an unusual dual modulus counter that represents a significant departure from standard practice.

Dual modulus counters offer a way of circumventing the speed limitations of conventional programmable counters. Dual modulus counters are not fully programmable, but are capable of division by two different numbers or moduli, often 10 and 11 or 15 and 16. Restricting division to two divisors allows much faster operation over what could otherwise be achieved. A dual modulus counter together with two slower programmable counters can mimic a single high speed programmable counter. Its operation can be easily understood if one remembers division is really a special case of counting. Division by 113, for example, can be accomplished by generating one output pulse for every 113 input pulses. A conventional counter starts at 113 and decrements with each input pulse. When zero is reached, a reset pulse is generated and the counter is reset to 113 for the next cycle. The time required to decrement the counter and generate the reset pulse imposes a speed limitation.

A dual modulus prescaler performs division somewhat differently. Consider the 10/11 dual modulus prescaler shown in Figure A1. For division by 113, the B and A counters are preset to 11 and 3, respectively, and the dual modulus counter is set up to divide by 11 initially. At first, the A and B counters are both decremented by one for every eleven pulses into the prescaler. After 33 inputs have arrived, the A counter reaches zero and changes the modules of the prescaler to ten. The prescaler then continues to count until the B counter is decremented to zero. This occurs after 80 additional input pulses at which point both A and B counters are reset and the cycle repeats. The division ratio N of a P/P+1 dual modules prescaler is given by:

$$N = BP + A$$

Where B and A are the values set into the B and A counters. For a division ratio of 113, the 10/11 prescaler counts by eleven three times giving 33 counts, and counts by ten eight times for a count of 80. The sum of the two counts is the desired divisor, 113.

For this system to work, the B counter must not reach zero before the A counter does. To meet this condition, the B counter value must equal or exceed the A counter value making some divisors impossible. A P(P+1) dual modulus prescaler is capable of all division ratios greater than P(P-1), and some, but not all, ratios less than P(P-1). For example, a 10/11 prescaler cannot divide by 89 (P(P-1) = 90) since this divisor requires nine counts to eleven (A=9). Division by 88 is possible, however, by setting both A and B counters to eight.

In many cases, small division ratios are not desired and the minimum division limitation never arises. But in the synthesizer under discussion, an effort has been made to keep the division ratio small ($50 \leq N \leq 150$), and the minimum divisor limitation becomes a major problem. One solution is to select the prescaler, P, so that all desired divisions are possible. A 7/8 prescaler meets this criteria and is available, but presents a different problem. A 6/7 prescaler requires operation of associated A and B counters at frequencies as high as 25 MHz (150 MHz divided by 6). Propagation time considerations must rule out the use of TTL

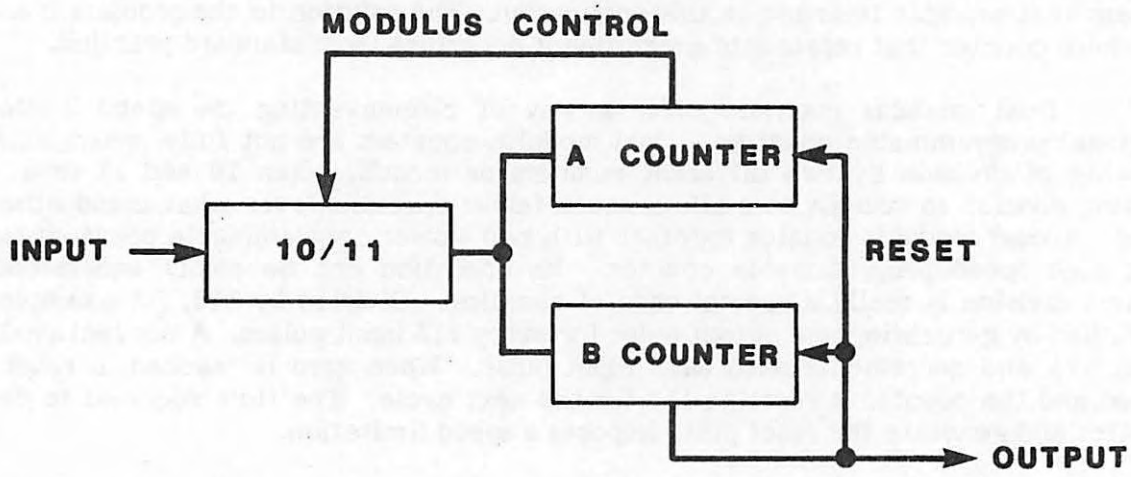

Figure A1. Block Diagram 10/11 Dual Modulus Prescaler

counters and force the implementation of the entire dual modulus circuit in ECL with considerably increased power consumption and parts cost.

Examination of Table 2, which lists all forbidden division ratios for both 10/11 and 8/9 prescalers, reveals a more suitable solution. Divisors missed by the 10/11 counter are covered by the 8/9 counter. All divisors greater than 47 are possible by combining both dual modulus counters into one circuit. Figure A2 shows a block diagram of this double modulus technique. The two dual modulus counters are low power ECL, the remaining components can be TTL or CMOS. The control code for the A and B counters is somewhat more complex as compared to ordinary dual modulus counters. This problem however is easily overcome by the microprocessor used to control the synthesizer. The final result is a divider circuit capable of operation in excess of 200 MHz for all divisors greater than 47 that consumes only 350 milliwatts.

Table A1. Forbidden Prescaler Divisors

10/11

A \ B	9	8	7	6	5	4	3	2	1	0
9	99	98	97	96	95	94	93	92	91	90
8	89	88	87	86	85	84	83	82	81	80
7	79	78	77	76	75	74	73	72	71	70
6	69	68	67	66	65	64	63	62	61	60
5	59	58	57	56	55	54	53	52	51	50
4	49	48	47	46	45	44	43	42	41	40
3	39	38	37	36	35	34	33	32	31	30
2	29	28	27	26	25	24	23	22	21	20
1	19	18	17	16	15	14	13	12	11	10
0	9	8	7	6	5	4	3	2	1	

8/9

A \ B	7	6	5	4	3	2	1	0
7	63	62	61	60	59	58	57	56
6	55	54	53	52	51	50	49	48
5	47	46	45	44	43	42	41	40
4	39	38	37	36	35	34	33	32
3	31	30	29	28	27	26	25	24
2	23	22	21	20	19	18	17	16
1	15	14	13	12	11	10	9	8
0	7	6	5	4	3	2	1	

Divisors in the lower left hand corner are not possible since the A counter value is less than the B counter value.

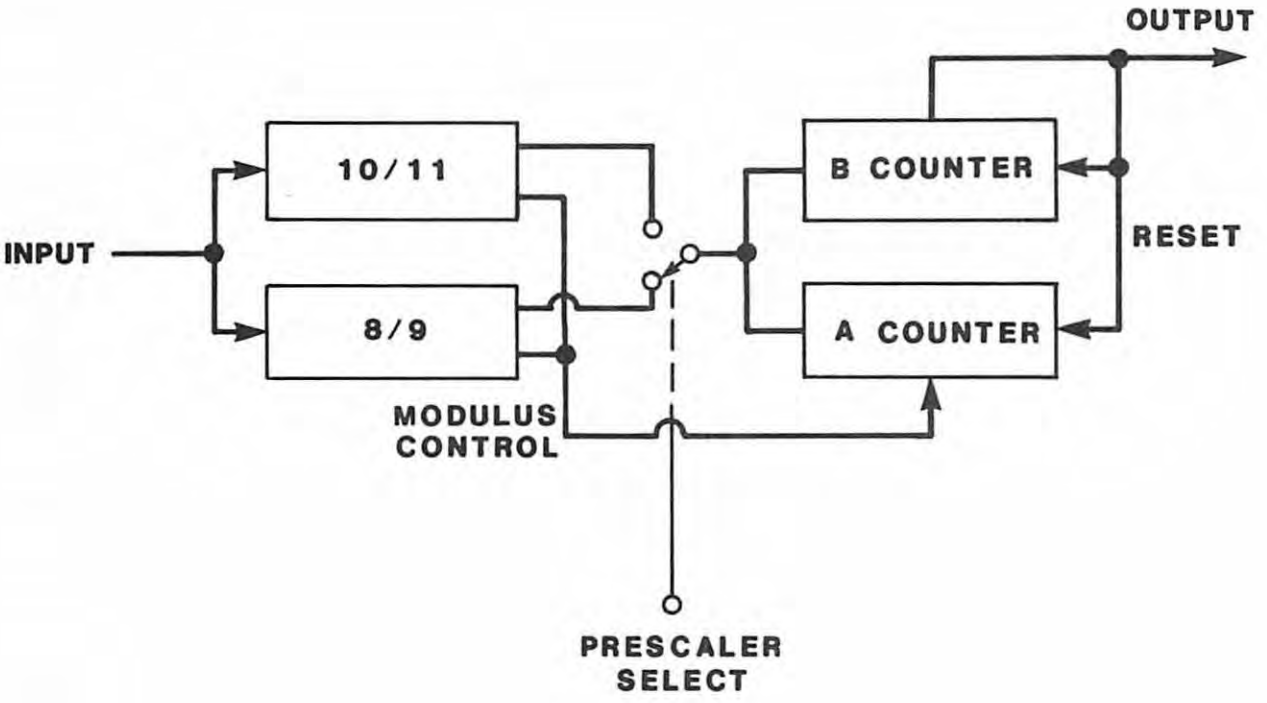

Figure A2. Block Diagram 10/11, 8/9 Double Dual Modulus Prescaler

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4.1.2 The RF Sub-system in the IC (INTERCEPT CENTER)

The *RF* Sub-system will consist of a number of intercept operator's receivers, search receivers, an analysis receiver together with associated controls, displays, antennas communication and other equipment. These items will be distributed as appropriate between the Intercept, Pilot and Analysis vehicles within the IC.

The PD study will select appropriate hardware and produce a sub-system architecture that will meet the requirement for an automatic search function, a signal classification function, a coarse DF capability and an analysis capability.

Whenever possible standard production Watkins-Johnson receivers will be selected for the IC.

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Searching for emitters within the target spectrum (20-120 MHz) at a channel separation of 10 KHz would require 10,000 steps. To ensure capture of signals of duration of one second would require an effective system step rate of 0.1 milliseconds. The apparent problem of a high tuning speed can be alleviated by assigning portions of the target spectrum to multiple independently scanning receivers. The PD study will determine the trade-off between a sufficient number of signal channel receivers such as the WJ Model XXX and a smaller number of multiple channel receivers such as the WJ Model YYY.

Each receiver will report to a processor included within the RF sub-system which will interface with the data processing sub-system within the pilot vehicle. The DP sub-system will determine network classification and will prioritize entries to the pilots task list.

4.1.2 The RF Sub-system in the Intercept Center

The RF Sub-system will consist of a number of intercept operator's receivers, search receivers, an analysis receiver together with associated controls, displays, antennas communication and other equipment. These items will be distributed as appropriate between the Intercept, Pilot and Analysis vehicles within the Intercept Center (IC).

The PD study will select appropriate hardware and produce a sub-system architecture that will meet the requirement for an automatic search function, a signal classification function, a coarse DF capability and an analysis capability.

Whenever possible standard production Watkins-Johnson receivers will be selected for the IC.

The search function within the 20-120 Mhz frequency band could be performed utilizing a modified WJ-8628-1 receiver and WJ-9195 Digitially Refreshed Display unit combination. The synthesized WJ-8628-1 receiver would scan the 20-120 MHz spectrum in 4 MHz steps. Within the WJ 9195 the 21.4 MHz receiver IF output is continuously swept and calibrated at each 10 KHz frequency increment at a sweep speed yielding less than 100 micro-seconds/step. This would allow for 100% probability of intercept for transmissions of more than one second duration. The log video output of the IF Processor provides 70 dB dynamic range. This is used in conjunction with the calibrated sweep frequency to provide magnitude and frequency data at each 10 KHz frequency step. The information received is processed and correlated as to frequency, amplitude, duration of transmission, and activity. The WJ-8628-1 handles frequencies up to 512 MHz within the standard 1/4 frame assembly. Additional frequency coverage up to 1100 Mhz can be incorporated with the addition of one 1/4 frame assembly for each 3 receivers. The DP sub-system would determine network classification and would prioritize entries to the Pilot's task list.

Each search receiver within the RF sub-system will be supported by a processor such as that included in the WJ-9195 unit which will interface with the data processing sub-system within the pilot vehicle.

The estimated level of activity in such an RF environment is expected to be at least 200 emitters per second. This may result in a form of task overload which may be defined as the point at which input from the automatic search function exceeds the

rate at which the pilot interaction or the signal classification function interacts with the task list. The task overload may be alleviated by a combination of:

a) Queuing emitters sequentially to the task list.

b) Establishing precedence of emitters of high priority.

c) Distributing the workload to other intercept centres via the regimental command post (RCP).

d) Slowing/stopping the scan until the workload lessens.

The PD study will evaluate the most effective means of alleviating the overload condition.

Automatic modulation recognition equipment greatly reduces the manual operations usually required in classification of signals detected by automated search systems. This reduction permits more extensive and faster signal intercept tasks using smaller evaluation crews with corresponding reductions in support requirements, training, initial acquisition costs and other life cycle costs. Watkins-Johnson Company manufactures a module for the WJ-9040 receiver system, type MRU-108, that provides up to 90% recognition probability for several modulation formats (including AM, PM, FM and CW signals as well as noise recognition, FSK, SSB and OOK) within a five second time interval or less. Also, NATO "squelch" recognition is a function currently performed by WJ search receivers to enhance the step and scan operation modes.

A section of the PD study would identify the specific operational performance required of the modulation recognition equipment and develop an equipment specification and verification procedure. Additional study efforts would be directed toward evaluation of existing analysis techniques useful in determining if specific encryption equipment or voice scrambling has been applied to the intercepted signal. Recommendations would be made on specific equipment capable of fully meeting the specifications directly or with minor modifications. Such recommendations would provide information for planning the cost and risk assessment areas of the procurement phase. Among other approaches Fourier analysis techniques would be investigated in an attempt to determine encryption presence/recognition and clear voice recognition to approach the one second requirement. Any task overload in the signal classification function area could be alleviated by distributing the classification requirement among multiple signal classification modules.

Direction finding requirements for coarse DF can be provided at the search receiver location with the WJ DF antenna and WJ-8955 DF Processor unit. Bearing accuracies of better than $\pm 2^{o}$ RMS over 360^{o} Horizontal coverage are provided with a frequency coverage of 20-120 MHz. This requirement is however only stated as "desirable" and the key factor which would determine its inclusion will be cost versus benefits. Similarly a suitable WJ receiver such as the WJ-8628 series would be suitable for the intercept function.

With respect to RF reception for the intercept/search/analysis and activity monitoring the alternatives are either to provide individual antennae to each of the intercept vehicles and the pilot vehicle or to provide a single high quality antenna with RF distribution to each of the intercept and pilot vehicles. Two high quality antennae (one as spare) will give improved reception at the risk of central point failure while multiple antennae will give improved reliability at some expense of

reception quality. The WJ-8628-4 receiver could be used as the activity monitor and intercept/analysis receiver which will provide the capability to scan up to 99 preset channels with individual operating parameters for each channel. The WJ-8628-4 also provides for the capability of handing off to slave receivers (WJ-8628-1) any frequency and receiver parameters as assigned by the WJ 8628-4 receiver, operator or controlling computer system. Receiving antennae for the intercept/search/analysis positions will best be accomplished using the WJ-8955 HFA-1, a passive vertically polarized conical monopole antenna. Frequency response is specified from 0.2 to 120 MHz.

4.1.3 DF/PF Subsystem

The PD will determine the modifications required to provide a digital interface for the Vampire DF system and the most efficient way of exploiting the capabilities of the modified Vampires within a processor-controlled system. At a minimum, the system will need to include the means of tasking the Vampire DF stations and of collecting in a coordinated fashion the bearings that they measure.

For the purpose of position fixing, it would be required that the elements within the DF subsystem measure bearings at the same frequency simultaneously in order to distinguish members of a net geographically separated and operating at the same frequency. The system must thus provide the means of synchronizing the activities of the Vampire stations.

The estimated level of activity in such an RF environment is expected to be at least 200 emitters per second. This may result in a form of task overload which may be defined as the point at which input from the automatic search function exceeds the rate at which the pilot interaction or signal classification function interacts with the task list. The task overload may be alleviated by a combination of:

a) Queuing emitters sequentially to the task list.

b) Establishing precedence of emitters of high priority.

c) Distributing the workload to ~~over~~ other intercept centres via the regimental command post.

d) Slowing/stopping the scan until the workload lessens.

The PD study will evaluate the most effective means of overcoming the overlaod condition. The existing modulation recognition capabilities such as that within the W-J 9040 MRU 108 modulation recognizer can provide modulation recognition with up to 90% probability of recognition of AM, PM, FM and CW signals as well as noise recognition, FSK, SSB and OOK within a 5 second interval.

Fourier analysis technique would be investigated in an attempt to decrease the time necessary for modulation recognition and to provide encryption and clear voice recognition to approach the one second requirement. NATO squelch recognition can be performed by existing W-J equipment.

Task overload to the signal classification function could be alleviated by distributing

the classification requirement amongst multiple signal classification modules.

To meet the requirement for activity measurement on up to 40 channels a dedicated stepping receiver of a type within the existing WJ inventory is a favored solution at this time. The requirement for course DF can be met by the provision of a receiver from the existing WJ range with an associated and dedicated antenna. This requirement is however only desirable and thekeyfactor which would determine its provision is cost. Similarly a suitable WJ receiver such as one of the 40/95 series would be used for the intercept function.

With respect to RF reception for the intercept/search/analysis and activity monitoring the alternatives are either to provide individual antennas to each of the intercept vehicles and the pilot vehicle or to provide a single high quality antenna with RF distribution to each of the intercept and pilot vehicles. Two high quality antennas (one as spare) will give improved reception at the risk of central point failure while multiple antennas will give improved reliability at some expense of reception quality to support the coarse DF function of WJ DF antenna would be used.

4.1.3 DF/PF Subsystem

The PD will determine the modifications required to provide a digital interface for the Vampire DF system and the most efficient way of exploiting the capabilities of the modified Vampires within a processor controlled system. The system must include the means of tasking the Vampire DF stations and of collecting the bearings that they measure in a coordinated fashion.

For the purpose of position fixing, the system requires that the elements within the

DF subsystem measure bearings at the same frequency simultaneously in order to distinguish members of a net geographically separated and operating at the same frequency. The system must then provide the means of synchronizing the activities of the Vampire stations.

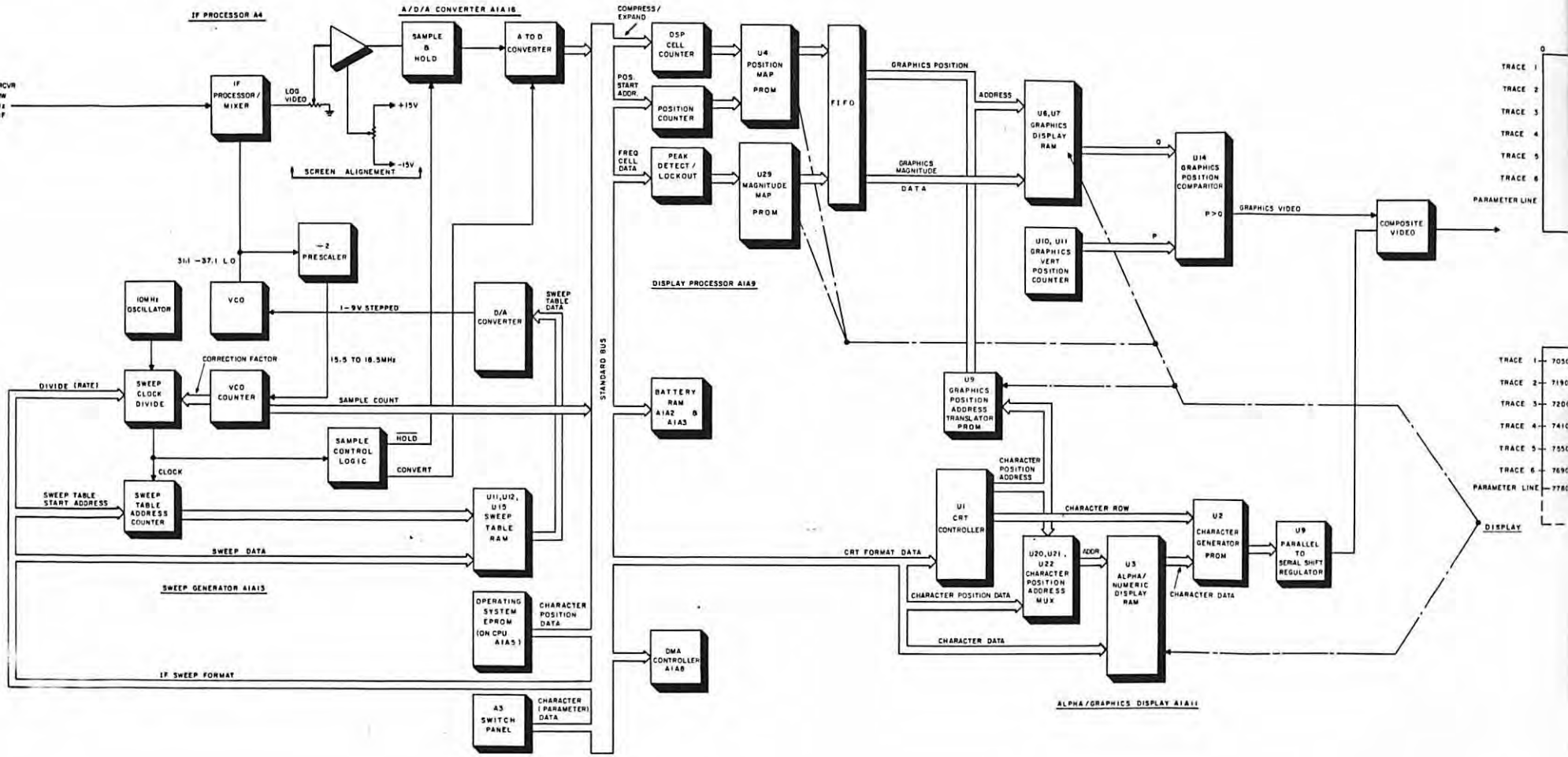
ESTIMATED LABOR FOR DIGITAL CONTROL (AUTOMATIC SEARCH) (SEARCH RECEIVER PROCESSING)

SDec 84'

SUB TASK PHASE	STAFF	PROG EE	SEC	DRAFT MGT ITRT
1. DEFINE PROC TASK	20	80	5	–
2. DEFINE PROC LOAD	20	40	–	–
3. DEFINE PROC STRUCTURE	20	40	–	–
4. DEFINE I/O PROTOCOL	20	40	–	–
5. DEVELOPE HARDWARE BLOCK	20	40	5	20
6. " SOFTWARE "	30	60	5	10
7. EVALATE DESIGN	20	40	–	–
8. ESTIMATE COST & RISK	20	40	5	5
	150	380	20	35

(8–10 week effort)

REVISION 052284



Figure