CHAPTER 1

GENERAL DESCRIPTION

1-1 GENERAL DESCRIPTION.

The WJ-9902-2 Receiver Controller accommodates up to two WJ-8607-88-4 VHF/UHF Surveillance Receivers. It is a half-rack package, occupying the right side of the lower drawer of the R-2541/B Receiver, Barracuda System (Figure 1-1).

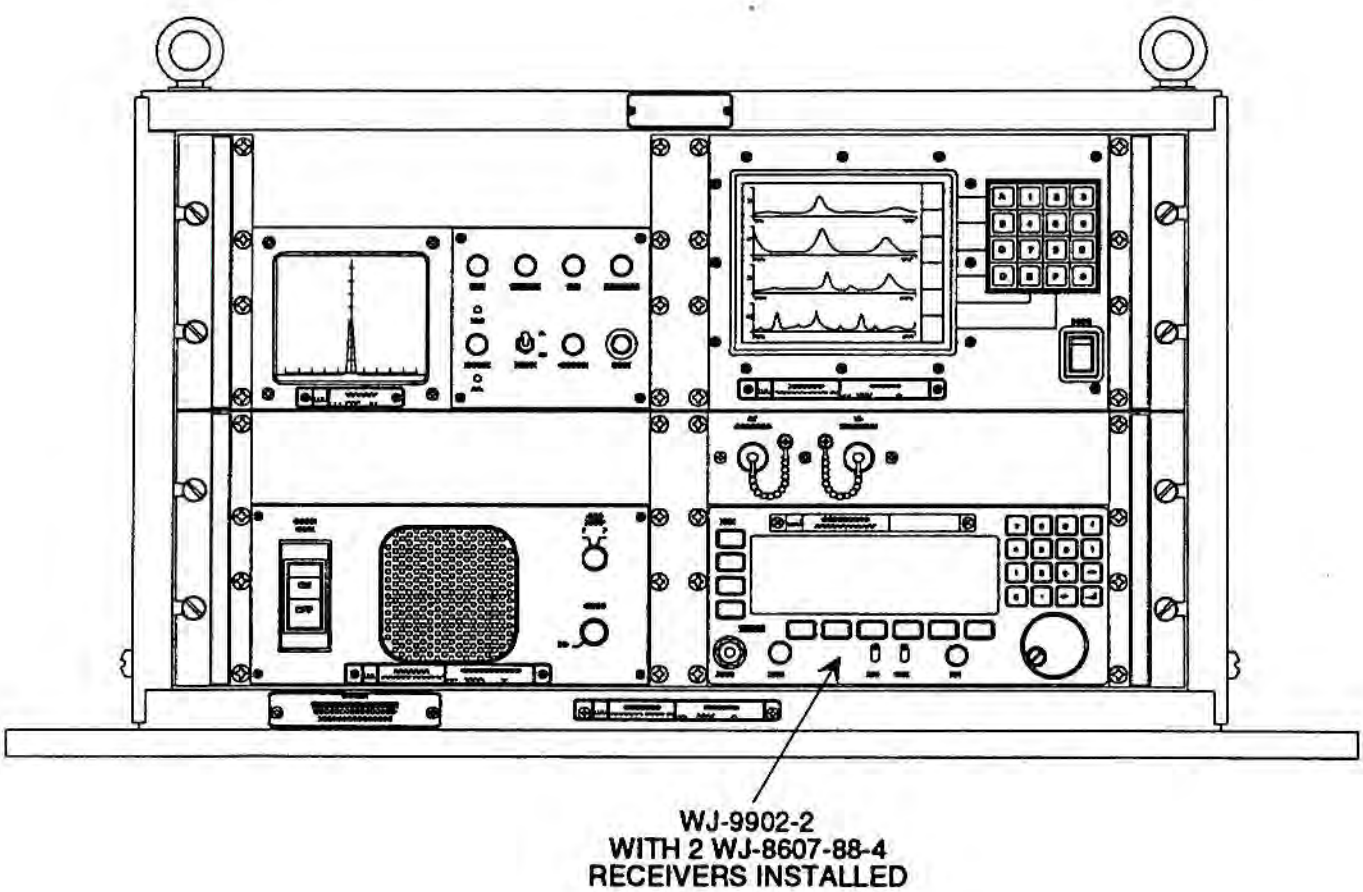


FIGURE 1-1. WJ-9902-2 Equipment Location

1-2 ELECTRICAL CHARACTERISTICS.

The WJ-9902-2 Receiver Controller operates on 110 or 220 Vac, 44-400 Hz power, and provides +12 Vdc power for receiver operation. The WJ-9902-2 provides full front panel operation for the receivers installed within. The front panel provides a back-lit LCD (Liquid Crystal Display) and group of control keys that permit a local operator to exercise all of the capabilities of the installed receivers via the HPIL (Hewlett-Packard Interface Loop) interface of the receivers. In addition, the front panel contains a battery-backed memory that allows the operator to set mission parameters and have them retained for later use. Included in the WJ-9902-2 Receiver Controller is an IEEE-488 host interface which converts the IEEE-488 protocol into HPIL format for use by the receivers. The host interface also converts the RS-232C output of the front panel assembly into the HPIL protocol for use by the receivers.

General specifications for the WJ-9902-2 are listed in Table 1-1.

TABLE 1-1. WJ-9902-2 Receiver Controller General Specifications

Size	3.5 X 8.25 X 20 inches (excluding rear-panel connections and handles)
Weight	20 lbs. nominal (frame with Host interface, Front Panel Unit and two Miniceptors installed)
Power Requirements	110 or 220 Vac, 47-400 Hz
Maximum Power Consumption	50 watts, nominal, fully loaded with two receivers and host interface
Cooling Method	Forced air (internal fan)

1-3 PHYSICAL CHARACTERISTICS.

The WJ-9902-2 Receiver Controller is designed in a half-rack configuration. It occupies 3.5 inches of vertical rack space and measures 8.25 inches in width, permitting two units of similar size to be adjacently mounted in a standard 19-inch equipment rack. The receivers install into mounting trays, accessible from the top and bottom of the unit. All receiver connections except headphone audio are cabled to the rear panel to accommodate the WJ-8907 Receiver System mounting configuration.

With exception of headphone audio which is located on the front panel, all connectors are located on the rear panel of the Receiver Controller, with internal cabling routed directly to the input and output connectors of the two WJ-8607-88-4 receivers.

1-4 EQUIPMENT SUPPLIED.

Equipment supplied with the WJ-9902-2, as configured for the R-2541/B Receiver System, consists of the Receiver Controller and two WJ-8607-88-4 Receivers.

1-5 EQUIPMENT REQUIRED BUT NOT SUPPLIED.

No additional equipment is required to operate the WJ-9902-2 within the R-2541/B Receiver System.

1-6 TOOLS AND TEST EQUIPMENT.

Table 1-2 lists all the tools and test equipment required to maintain the WJ-9902-2 Receiver Controller.

TABLE 1-2. Tools and Test Equipment

SCAT No.	Equipment	NSN-NICN CAGEC/P/N
4207	Oscilloscope Tektronix Model 2465B	6625-01-213-9354 80009-2465B-11
N/A	Flat Blade Screwdriver	N/A
N/A	#2 Phillips Screwdriver	N/A
N/A	6" Adjustable Open end Wrench	N/A
N/A	ESM Maintenance Kit	N/A
N/A	Test Bed - "Known-good" WJ-9902-2 with a 'known-good' WJ-8607-88-4 Receiver	N/A
N/A	Test Cable A	See Figure 4-2
N/A	Test Cable B	See Figure 4-2

1-7 WARRANTY INFORMATION.

The WJ-9902-2 Receiver Controller, Serial Numbers 1-28, are covered by a two-year warranty period that commences on September 30, 1993. This warranty is extended to all Lowest Replaceable Assemblies as defined in paragraph 4-3 of the WJ-9902-2 organizational level maintenance manual. The warranty contains provisions that allow a five-month grace period to report system failures that occur at sea. For more detailed information regarding the warranty, refer to Contract Number MDA904-92-C-1116.

1-8 PREPARATION FOR SHIPMENT OR STORAGE.

1-8.1 Preparation for Shipment. If the unit must be prepared for reshipment, the packaging method should follow the pattern established in the original shipment. Use the best packaging materials available to protect the unit during shipment or storage. When possible, use the original packing container and cushioning materials. If the original packing materials are not available, use the following procedure:

a. Wrap the unit in sturdy paper or plastic.

b. Place the wrapped unit in a strong shipping container and place a layer of shock-absorbing material (3/4-inch minimum thickness) around all sides of the unit to provide a firm cushion and to prevent movement inside the container.

c. Thoroughly seal the shipping container and mark it FRAGILE.

d. Properly address the shipping container for intended destination.

1-8.2 Preparation for Storage. When storing the equipment for extended periods, follow the above packing instructions to prevent damage to the equipment. The safe limits for storage environment are:

Temperature: -40 to +70°C
Humidity: less than 95 percent

CHAPTER 2

INSTALLATION AND OPERATION

2-1 GENERAL.

This section contains the installation procedures and operating procedures for the WJ-9902-2 Receiver Controller.

2-2 UNPACKING AND INSPECTION.

The WJ-9902-2 Receiver Controller is shipped as an integral part of the R-2541/B Receiver System. Refer to the R-2541/B Receiver, Barracuda Operation and Maintenance Manual for instructions on unpacking and inspection of the receiver system and its components.

2-3 INSTALLATION INSTRUCTIONS.

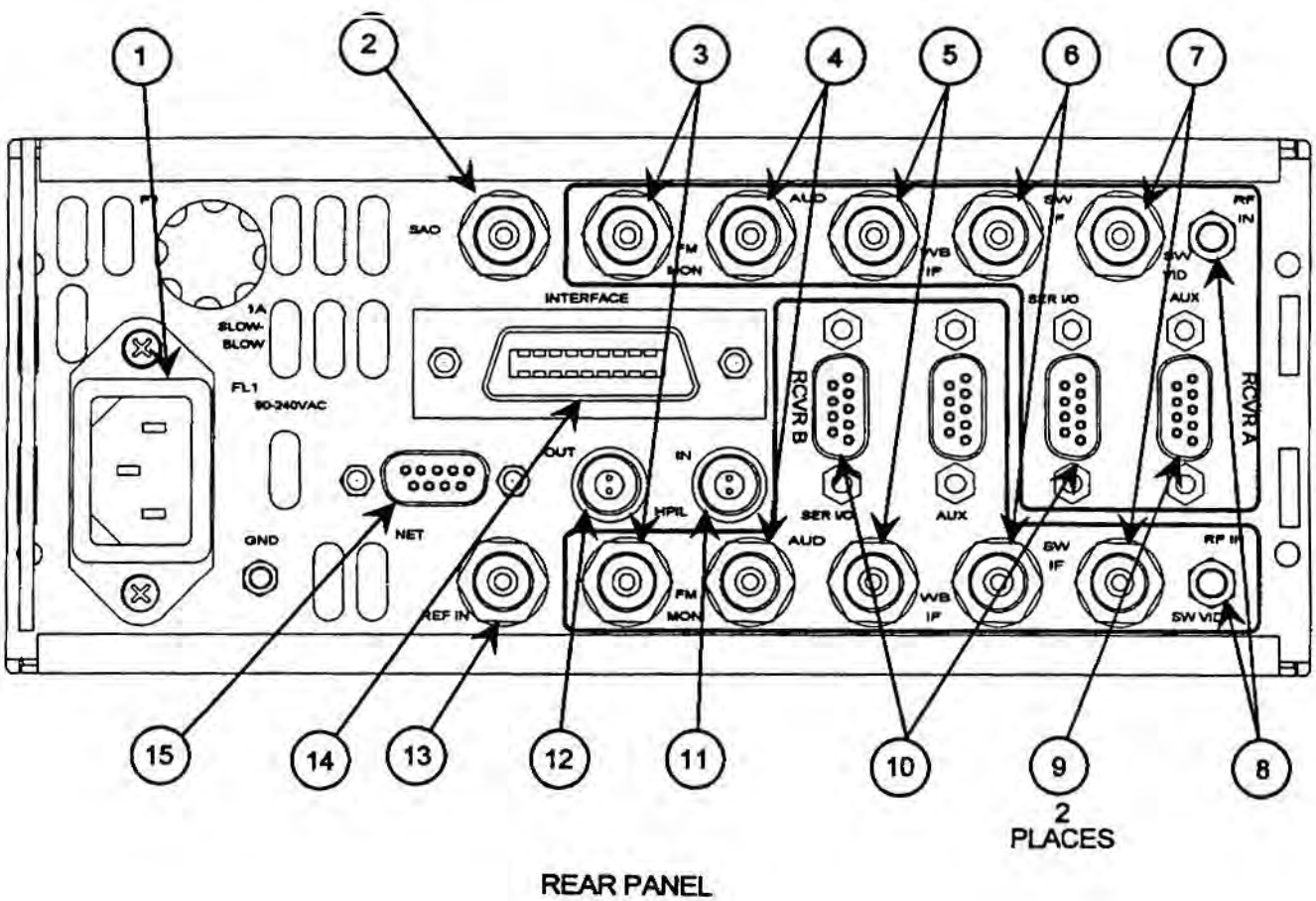
The WJ-9902-2 Receiver Controller is shipped installed in the R-2541/B Receiver System. Figure 2-1 provides a diagram of the WJ-9902-2 Receiver Controller's front and rear panels and their connectors while Table 2-1 lists the connectors. The following paragraphs detail the functioning of each connector. Connectors that connect only to either Receiver A or Receiver B are grouped at the rear panel and labeled as either RCVR A or RCVR B.

2-3.1 PWR IN, AC Power Input, FL1J1. This three-pin SJ type connector (number 1) is used with the detachable AC power cord (supplied with the WJ-8907) to connect the WJ-9902-2 to a 110 or 220 Vac, 44-400 Hz AC power source. In the WJ-8907 Receiving System, the power cord is connected to the WJ-8907 Power Distribution Unit.

2-3.2 SAO, Selected Audio Output Connector, J2. This BNC connector (number 2) routes the parallel-tied SAO outputs of the installed receivers. This allows the selection of the audio output via a remote command of any of the receivers installed within the WJ-9902-2.

2-3.3 RCVR-A FM MONITOR Connector, J9 and RCVR-B FM MONITOR Connector, J17. These BNC connectors (number 3) output a signal from the receiver's FM MON output, which is FM-demodulated. This signal has a limited bandwidth of 100 kHz or half of the selected IF bandwidth filter, whichever is less. This output is present in the AM, FM, and pulse detection modes and is always an FM-demodulated signal regardless of the selected detection mode.

2-3.4 RCVR-A LINE AUDIO Connector, J8 and RCVR-B LINE AUDIO Connector, J16. These BNC connectors (number 4) provide a limited bandwidth audio signal of approximately 3 volts peak-to-peak from a 68 ohm source. This output may be used with any load between 4 ohms and an open circuit. This output is switched based on the absence or presence of a signal above the COR threshold setting of the receiver. The source of this output is the receiver's AUDIO output.



REAR PANEL

FIGURE 2-1. WJ-9902-2 Receiver Controller Connections (Sheet 1 of 2)

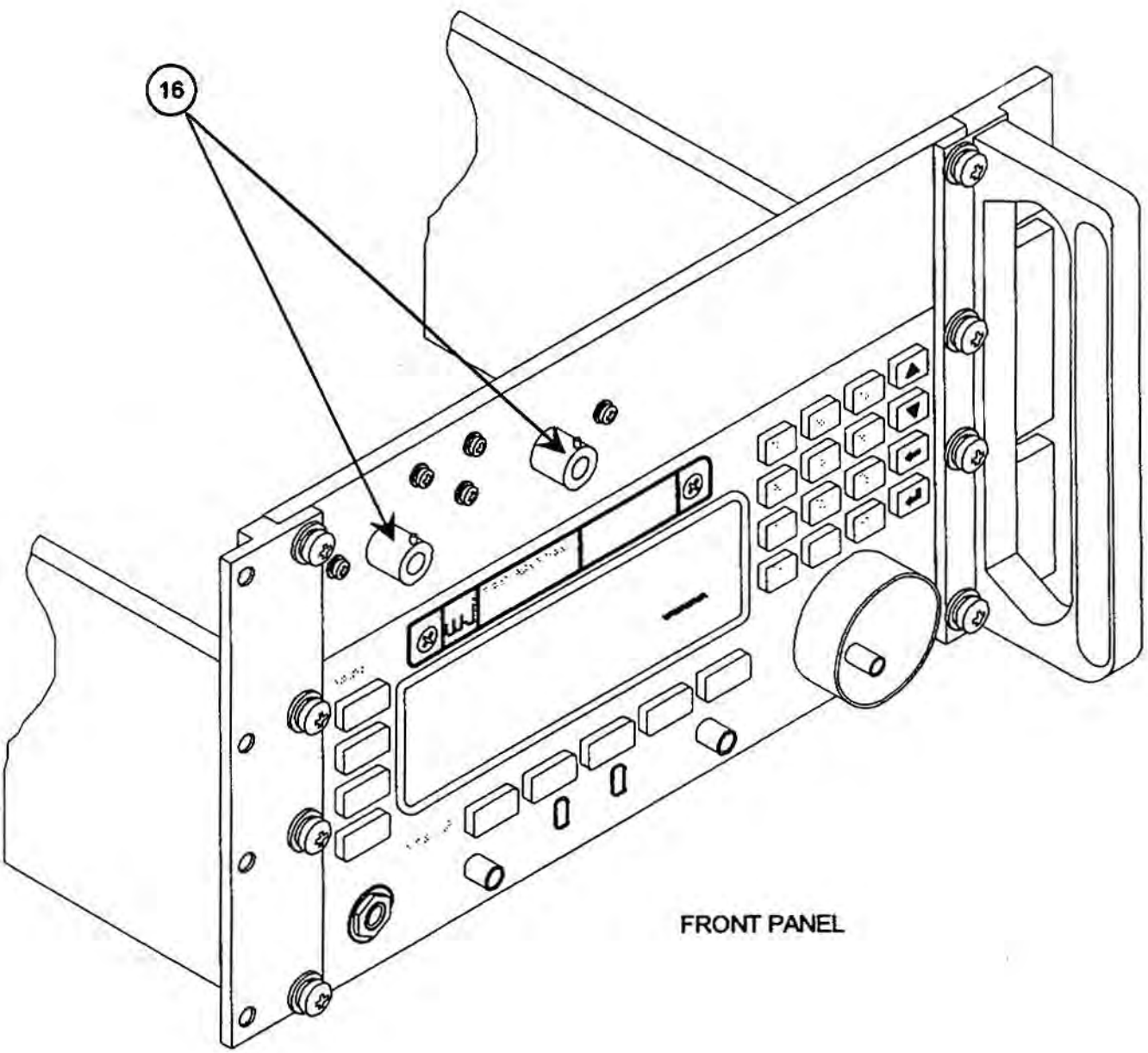


FIGURE 2-1. WJ-9902-2 Receiver Controller Connections (Sheet 2 of 2)

TABLE 2-1. WJ-9902-2 List of Connectors

Category	Connector	Ref Desig	Function
Common	PWR IN	FL1J1	(3-pin SJ) AC Power Input
Common	REF IN	J1	(BNC) Ext. Reference Input
Common	SAO	J2	(BNC) Selected Audio Output
Common	HPIL IN	J3	(Multipin) HPIL Input
Common	HPIL OUT	J4	(Multipin) HPIL Output
Common	REMOTE INTERFACE	A2J1	(Multipin) REMOTE INTERFACE
Common	NET	A2J2	(Multipin) WJ NET
RCVR A	RF IN	J5	(SMA) Receiver A Antenna Input
RCVR A	WB IF	J6	(BNC) Receiver A Wideband IF Output
RCVR A	SW IF	J7	(BNC) Receiver A Switched IF Output
RCVR A	AUD	J8	(BNC) Receiver A Line Audio Output
RCVR A	FM MON	J9	(BNC) Receiver A FM Monitor Output
RCVR A	SW VID	J10	(BNC) Receiver A Switched Video Output
RCVR A	SER I/O	J11	(Multipin) Receiver A Serial I/O Interface
RCVR A	AUX	J12	(Multipin) Receiver A Auxiliary for COR, Spectrum Inversion and Log Display
RCVR B	RF IN	J13	(SMA) Receiver B Antenna Input
RCVR B	WB IF	J14	(BNC) Receiver B Wideband IF Output
RCVR B	SW IF	J15	(BNC) Receiver B Switched IF Output
RCVR B	AUD	J16	(BNC) Receiver B Line Audio Output
RCVR B	FM MON	J17	(BNC) Receiver B FM Monitor Output
RCVR B	SW VID	J18	(BNC) Receiver B Switched Video Output
RCVR B	SER I/O	J19	(Multipin) Receiver B Serial I/O Interface
RCVR B	AUX	J20	(Multipin) Receiver B Auxiliary for COR, Spectrum Inversion and Log Display
RCVR A	SW IF	J21	(BNC) Receiver A Switched IF Output
RCVR B	SW IF	J22	(BNC) Receiver B Switched IF Output

2-3.5 RCVR-A WB IF OUT Connector, J6 and RCVR-B WB IF OUT Connector, J14. These BNC connectors (number 5) provide a sample of the receiver's 21.4 MHz IF signal with a 12 MHz bandwidth. The nominal impedance of the connector is 50 ohms with approximately 14 dB of gain from the antenna input. This signal is routed from the receiver's WBIF connector.

2-3.6 RCVR-A SW IF Connector, J7 and RCVR-B SW IF Connector, J15. These BNC connectors (number 6) provide a nominal -30 dBm IF signal into 50 ohms. The center frequency is 21.4 MHz with a bandwidth equal to the receiver's selected IF bandwidth. This signal is routed from the receiver's SW IF Output.

2-3.7 RCVR-A SW VIDEO Connector, J10 and RCVR-B SW VIDEO Connector, J18. These outputs (number 7) provide a full bandwidth, demodulated signal related to the receiver's selected detection mode. This signal is routed from the receiver's SW VID output. When the receiver's is in FM detection mode, the nominal level of the signal is ±0.5 volts peak-to-peak for +/- a half bandwidth of frequency deviation. When in AM, CW, or SSB detection modes, the nominal level of this signal is 0.5 volts peak-to-peak.

2-3.8 RCVR-A RF IN Connector, J5 and RCVR-B RF IN Connector, J13. These SMA connectors (number 8) accept the RF input from the antenna. Their nominal input impedance is 50 ohms. This signal is routed to the receiver's RF IN, Antenna Input.

2-3.9 RCVR-A AUX Connector, J12 and RCVR-B AUX Connector, J20. This multipin connector, (number 9) shown in Figure 2-2, provides Carrier-Operated Relay (COR), Spectrum Inversion, and LOG Display Outputs. Pins 1 thru 6 of this connector are wired for pin-to-pin compatibility with the receiver's AUX output. Pin 7 is wired to chassis ground and pins 8 and 9 are not used. Pin 3 provides a signal that is a CMOS logic output indicating the presence of energy over the programmed COR level. Pin 1 provides a CMOS logic output indicating spectrum sense of the IF output. In the receiver's tuning range (2-500 MHz), this line is always true. Pin 4 provides a 0.1V to 4.57V output that is a linear representation of the amplitude of the signal in the selected IF bandwidth from 0 to 60 dB.

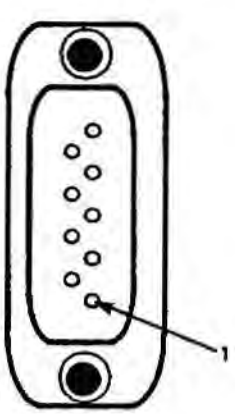


FIGURE 2-2. Pin Locations for the AUX Connector

2-3.10 RCVR-A SER I/O Connector, J11 and RCVR-B SER I/O Connector, J19. These connectors (number 10) provide the Digital Signal Output from each receiver for connection to the WJ-9207 Pan Display, another part of the R-2541/B Receiver. Table 2-2 lists the pins and their respective signals.

TABLE 2-2. SER I/O Connector Signals

Pin	Signal
1	RS-485 +
2	RS-485 -
3	+5.5 VDC
4	Ground
5	RS-232 RXD
6	RS-232 TXD
7	Not connected
8	Not connected
9	Not connected

2-3.11 HPIL IN Connector, J3. This connector (number 11) serves as an input for data on a Hewlett-Packard Interface Loop (HPIL). This connector is physically and functionally shown in Figure 2-3.

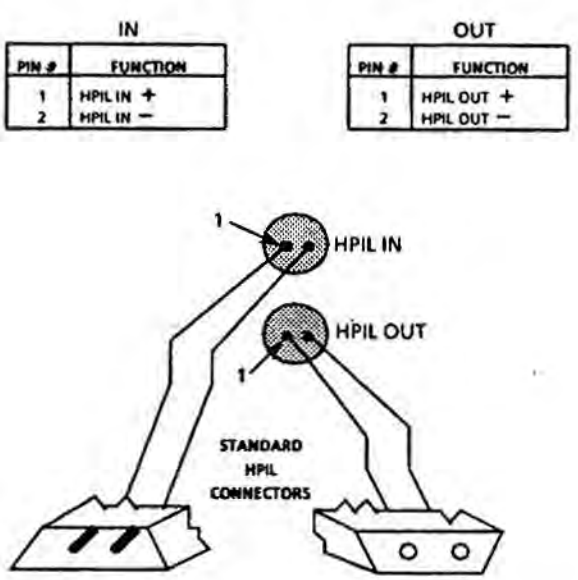


FIGURE 2-3. HPIL Connector Pin Configurations

2-3.12 HPIL OUT Connector, J4. This connector (number 12) serves as an output for data on a Hewlett-Packard Interface Loop. This connector is physically and functionally shown in Figure 2-3.

2-3.13 REF IN Connector, J1. This BNC connector (number 13) allows an external 1 MHz, 5 MHz, or 10 MHz reference, having a level of 0 dBm, to be used as the time base for the installed receivers. The installed receivers must be configured to match the external reference being used.

2-3.14 HOST I/O Connector, A2J1. This multipin IEEE-488 connector (number 14) permits the connection of a host controller to the WJ-9902-2 Receiver Controller. This connector is mounted on the rear panel of the WJ-9902-2. This connector is not used in the R-2541/B Receiver configuration.

2-3.15 NET Connector, A2J2. This multipin connector (number 15) permits connections to the WJ NET. This connector is mounted on the rear panel of the WJ-9902-2. This connector is not used in the R-2541/B Receiver configuration.

2-3.16 RCVR-A SW IF Connector, J21, and RCVR-B SW IF Connector, J22. These BNC connectors (number 16) route to the front panel the SW IF signals from each receiver from the connectors, J7 and J15, discussed in paragraph 2-3.6.

2-4 CONTROLS AND INDICATORS.

All controls and indicators are contained on the Front Panel Unit (FPU), a general-purpose, menu-driven assembly that provides local control of Miniceptor receivers. The FPU controls and display are used to control the co-located Miniceptor receivers. The FPU incorporates a backlit liquid-crystal display which provides a visual representation of all menus and equipment functions. The controller assembly for the FPU features a built-in 16-bit microprocessor and receiver control programs contained in read-only-memory (ROM). In addition, the controller assembly contains battery backed-up random-access-memory (RAM) for memory operations. Control operations are based upon "softkey" access to different menu levels.

All controls for the FPU are shown in Figure 2-4. Toggle switches are provided for turning on and off the power and the backlighting for the LCD display. Control knobs are available to set the audio output level and manually tune the equipment being controlled, with a third knob for control of variable parameters. The LCD display provides the status indicators for all equipment functions; there are no discrete indicator lamps or other displays provided. The following paragraphs explain in detail the function of each control and indicator. The number in parentheses in the paragraph refers to the key in Figure 2-4.

2-4.1 PWR Switch. This two-position, front-panel-mounted, toggle switch (number 1) turns the primary AC power on when in the "up" position.

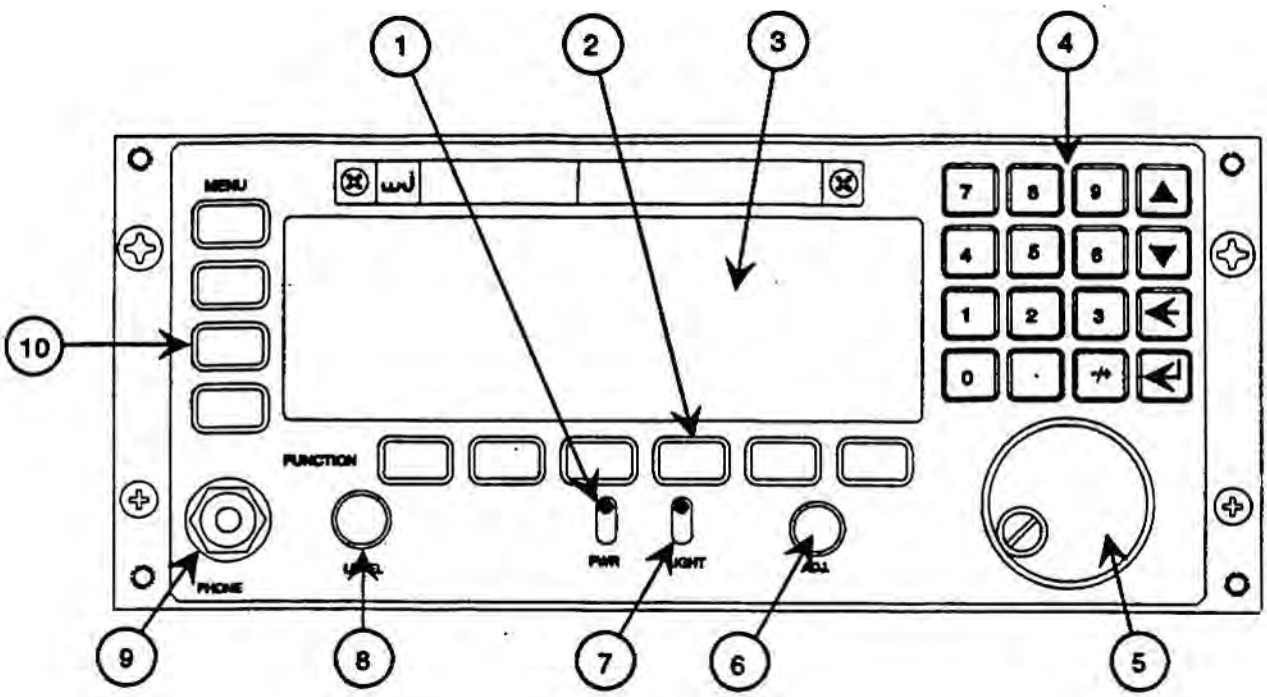


FIGURE 2-4. Front Panel Unit (FPU) Controls and Indicators

2-4.2 LIGHT Switch. This two-position, front-panel-mounted, toggle switch (number 7) energizes backlighting for the LCD front panel display and keyboard when set to the "up" position.

2-4.3 Parameter ADJ.Control. This 24-position, front-panel-mounted, encoded rotary switch (number 6) mimics the use of the UP (↑) and DOWN (↓) keys, and controls variable-parameter subfunctions under software control, such as IF bandwidth select, COR level, etc. Although it can be turned continuously in either direction, software will not "roll over" the control when the end of a subfunction parameter range is reached.

2-4.4 LEVEL Control. This front panel control (number 8) adjusts the left and right audio levels to the front panel PHONE jack (number 9).

2-4.5 Tuning Wheel. The Tuning Wheel (number 5) can be turned continuously in either direction and controls frequency subfunctions. Software will not "roll over" the control when the end of a subfunction parameter range is reached.

2-4.6 Keypad. This front-panel-mounted membrane keypad assembly (number 4) comprises ten numeric (0-9) and six special function keys, all contained in a 4 X 4 square. Specific keys are defined in paragraphs 2-4.6.1 through 2-4.6.4.

2-4.6.1 0 through 9, +/-, . Keys. These keys are used for numeric entry of parameters, or in response to an operator prompt. Subsequent entries after the first are appended to the right of the first entry. Additional entries beyond a full field (as defined for a given parameter) are ignored.

2-4.6.2 Up (↑) and Down (↓) Keys. These keys are used to increment or decrement an active parameter or operator prompt. The amount incremented or decremented is specified by the particular parameter, or is variable in the case of frequency. When one of these keys are pressed for longer than 0.5 second, the auto repeat function is enabled. The parameter continues to increment through its range until the key is released or until the parameter's limit is reached.

2-4.6.3 DELETE (←) Key. This key provides two modes of operation based on the keypad mode. In numeric entry mode (at least one key has been pressed) the DELETE key removes the last entry; if the first numeric entry is deleted, the front panel display reverts to non-numeric entry operation.

Pressing the DELETE key while in the non-numeric entry operation mode returns the front panel display to function selection operation.

2-4.6.4 ENTER (↵) Key. This key provides two modes of operation based on the keypad mode. In numeric entry mode, ENTER causes the entered numeric value to become the new subfunction value. If the entry is valid, the front panel display returns to the subfunction, numeric entry inactive mode; an invalid entry causes a display error prompt that requires operator action.

Pressing the ENTER key while in subfunction, numeric entry inactive mode, reverts the front panel display to the function select mode and causes any valid selections to be entered into the equipment.

2-4.7 MENU Keys. These four software-controlled keys (number 10) enable the operator to select the appropriate menu, as indicated adjacent to each key on the LCD display, to allow the desired function(s) to be performed. MENU keys perform no actual device actions, and do not cause any equipment parameters to be changed.

2-4.8 FUNCTION Keys. The six software-controlled FUNCTION keys (number 2) allow the equipment to be controlled by the operator. Functions available from any displayed menu are shown on the LCD display above the appropriate FUNCTION keys; where more than six functions are available, the far right function key is labeled "more" and allows access to additional functions.

There are two basic definitions related to the FUNCTION keys of the front panel display:

a. Function. A function refers to an operation indicated on the front panel display above one of the horizontal FUNCTION keys; for example, frq (frequency), ibw (IF bandwidth), etc.

b. Subfunction. A subfunction refers to an operation contained within a function, as indicated on the front panel display above one of the horizontal FUNCTION keys after the desired function has been selected. For example, pressing the ibw (IF bandwidth) key causes the display to indicate the six available bandwidths, one above each FUNCTION key. Selecting one of the bandwidths by pressing the appropriate key is therefore a subfunction action.

FUNCTION keys may have an immediate action, such as toggling a function which is a simple "ON-OFF" selection. They may also select a new group of subfunction keys (as described in the note above for ibw selection). Finally, FUNCTION keys for parameters which are not currently displayed access an operator prompt on the function key line.

When a FUNCTION key is pressed, the corresponding display readout of the selected function changes to uppercase letters, and is bracketed on either side by a black rectangle.

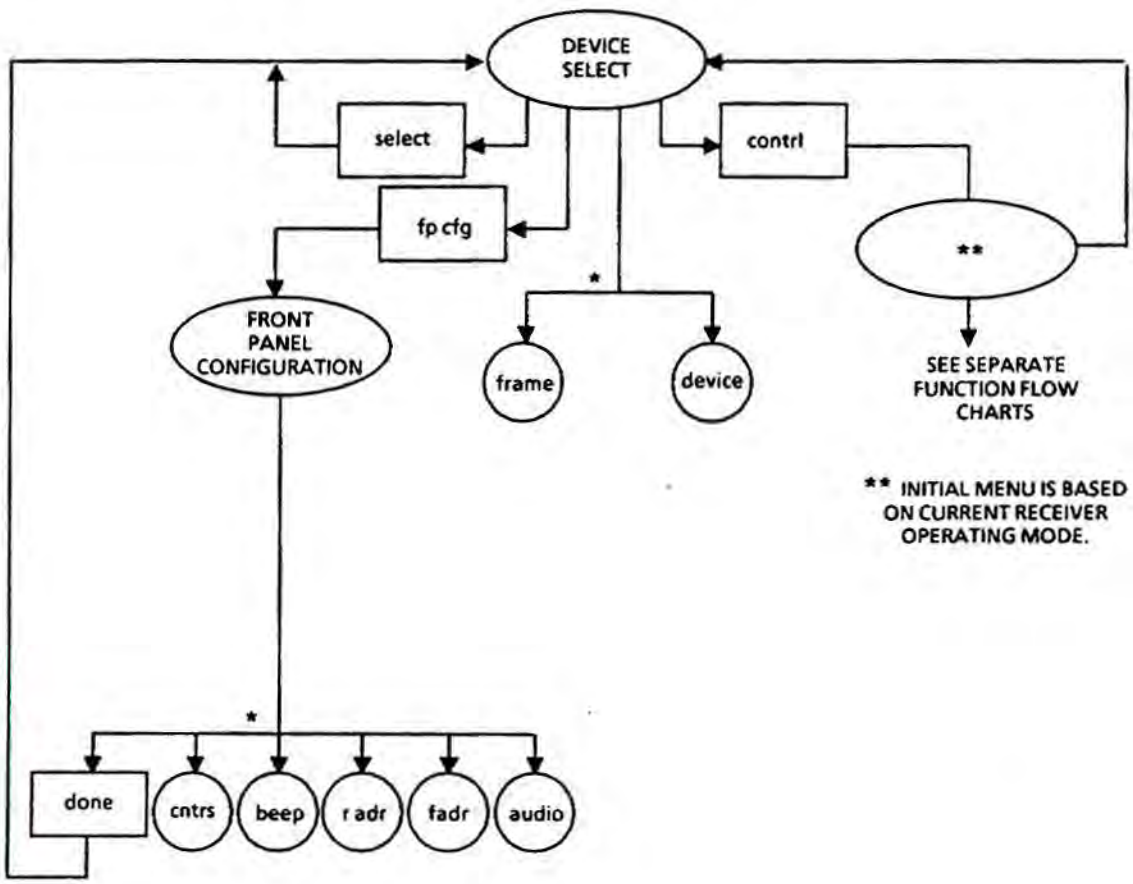
2-4.9 LCD Display. The 4.5" X 1.5" backlit LCD display (number 3) provides visual indication of the status of all equipment functions, labels for the MENU and FUNCTION keys, and operator prompts or error messages.

2-4.10 Menu Displays. The WJ-9902-2 Receiver Controller uses a data display technique which is a system of nested menus. That is, the opening menu leads the operator to a series of functional menus, each of which allows access to various functions and subfunctions. The following paragraphs briefly describe the use of menu flow diagrams, and define common display parameters which are applicable to all operating menus. The remaining sections of this manual describe the operation of specific equipment using the nested menu concept.

2-4.10.1 Menu Flow Diagrams. To more fully describe the operation of the receiver controller, a set of menu flow diagrams has been developed. These diagrams show the flow of operations from menu to function, and provide a road map to allow quick movement among the various displays.

Figure 2-5 is an overall flow chart of menus. As shown in the figure, access to a particular function requires that the operator select the appropriate menu, using the MENU keys arranged vertically on the left side of the LCD display. This, in turn, causes the desired function to appear above one of the FUNCTION keys, which are arranged horizontally just below the LCD display. Subsequent selection of a FUNCTION key either toggles the desired parameter or causes the applicable subfunction(s) to appear on the display above the horizontal keys. Subfunctions are NOT identified on the menu flow diagrams.

Since there are more than four menus and six functions available, one of the MENU and/or FUNCTION keys may be labeled "more". Pressing the "more" key allows access to additional menus, functions, and subfunctions, as appropriate.



LEGEND:

= DISPLAYED MENU

= MENU SOFTKEY

= FUNCTION SOFTKEY

* SEE DESIRED FUNCTION DESCRIPTION FOR PARAMETER CHOICES AND SELECTION PROCEDURE.

FIGURE 2-5. Overall Flow Chart of Menus

2-4.10.2 Operating Menu. Figure 2-6 shows the general operating menu layout including definitions of the fields and indicators. The following paragraphs describe the three types of display cursors, and the signal strength and tuning indicators. For detailed descriptions of other displayed information, refer to paragraph 2-7 on operation.

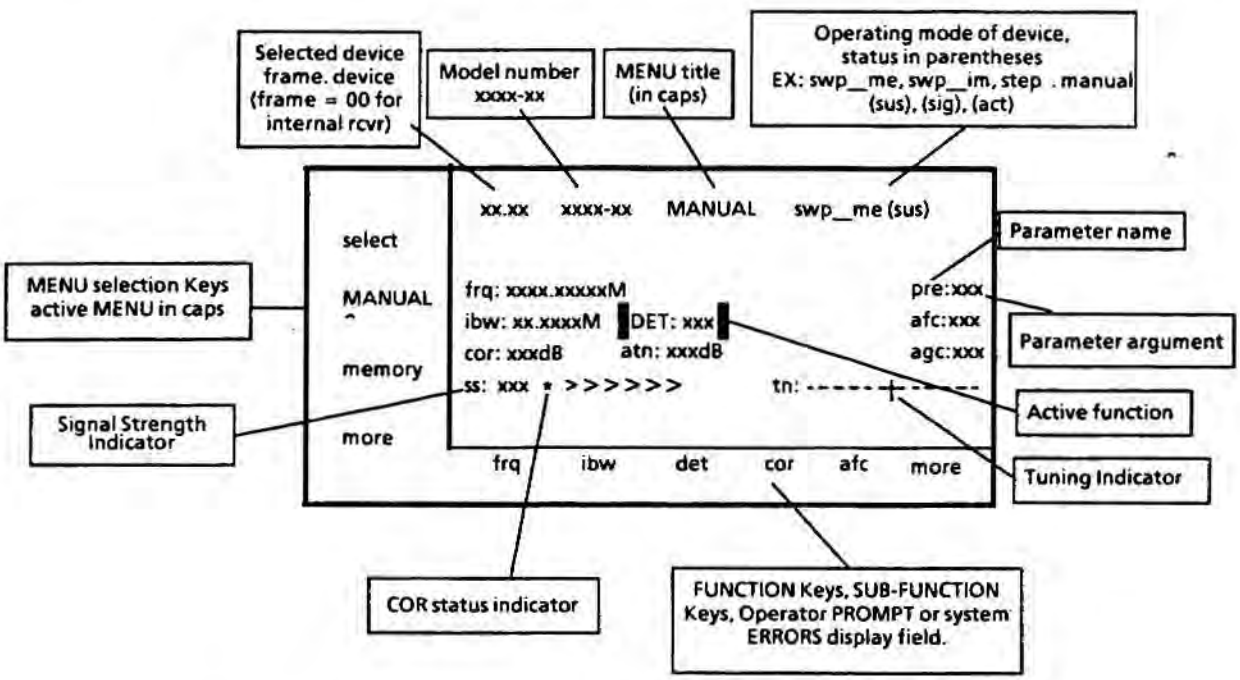


FIGURE 2-6. Receiver Controller Typical Operating Menu

2-4.10.2.1 Display Cursors. Three types of display cursors are used on the LCD display: an active parameter cursor, a tuning resolution cursor, and a numeric entry cursor. The active parameter cursor is used in conjunction with either of the other two cursors; however, the tuning resolution and numeric entry cursors are never active at the same time.

a. Active Parameter Cursor. The active parameter cursor consists of a solid box on each end of the currently active parameter; that is, the parameter selected by a FUNCTION key for immediate control or alteration. This cursor is accompanied by a change from lower case to upper case letters of the parameter name, and is present any time the parameter is active in either the numeric or non-numeric mode.

b. Tuning Resolution Cursor. The tuning resolution cursor indicates the current tuning resolution for a frequency parameter. It consists of a blinking underline beneath the most significant digit of the tuning rate. This cursor is present any time the tuning wheel is active (refer to paragraph 2-4.5 for a description of tuning wheel operation).

c. Numeric Entry Cursor. The numeric entry cursor highlights the current active numeric entry field by causing a solid block to blink over the last entered numeric character. This cursor is only present when the display is in the active numeric entry mode.

2-4.10.2.2 Signal Strength Indicator. The Signal Strength indicator, designated on the Operating Menu by ss, indicates the strength of the received signal in dBm. The row of right-pointing arrows may be used as an analog "peaking" indicator, since the more arrows present, the stronger the signal.

Between the numerical signal strength readout and the right-pointing arrows, an asterisk will appear if the COR is active and the signal level is sufficient to cause it to trip.

When the AGC is turned off, a signal strength too low to provide linear AM demodulation will cause the right-pointing arrows to be replaced with the word "underload." If the signal strength is too high, the word "overload" will appear.

In the event that the receiver is unable to acquire signal strength because of an error, active sweep, or step operation, the SS field will be blank.

2-4.10.2.3 Tuning Indicator. The Tuning Indicator, designated on the operating menu by tn, is only active in AM and FM modes of operation and indicates the relative location of the signal within the selected IF passband. The left and right edges of the tuning indicator bar represent 70 percent below or above the passband center frequency, respectively.

2-5 STARTUP PROCEDURE.

The following startup procedure brings the WJ-9902-2 Receiver Controller to a normal operating state:

a. Energize the receiver controller by moving the PWR switch to the On (up) position.

b. Move the LIGHT switch to the On (up) position.

c. Using the ADJ control, adjust the screen contrast to the desired brightness.

Figure 2-7 shows the receiver controller power-up display.

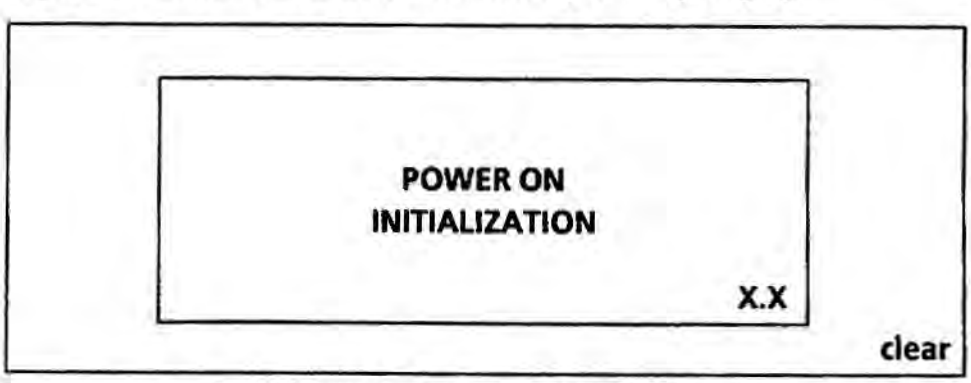


FIGURE 2-7. Power-Up Display

The X.X in the lower right-hand corner of the display indicates the front panel software version number. If the CLEAR key is pressed, it causes all of the battery backed front panel parameters to be reset to their default values. These parameters include contrast, beeper, audio, and the last controlled device and menu. The receiver parameters are unaffected.

During the time this screen is displayed, the receiver controller verifies proper operation with the IEEE-488 Remote Interface (Input-Output Controller - IOC). If an error is encountered, the message "IOC NOT RESPONDING" is displayed.

After the screen shows the power-up display, the receiver controller displays the menu that was in use when the power was last removed. However, in the event of a failure of the battery-backed memory, or if the last FPU-controlled device was not internal to the receiver controller's residing frame, the receiver controller displays the DEVICE SELECT menu.

2-6 INITIAL ADJUSTMENTS.

No initial adjustment procedures are necessary for the WJ-9902-2 Receiver Controller.

2-7 NORMAL OPERATION.

Local operation of a Miniceptor from the receiver controller is accomplished through use of the remaining menus, all of which are accessed from the DEVICE SELECT menu by pressing the menu key labeled contrl. To begin local operation, press the contrl key; the display switches to a menu based on the current receiver operation.

2-7.1 Local Operation Via the DEVICE SELECT Menu. The following paragraphs describe the functions available, and their means of selection, from the DEVICE SELECT menu.

2-7.1.1 The frame Function. Pressing the frame function key on the DEVICE SELECT menu allows selection of either a local frame or external frames. The "frame" readout on the display changes to all capital letters, and the word "FRAME" is bracketed. As frames are selected, the "frame" field indicates the model number, frequency range and software version of the selected device. If the local frame is desired, press the local subfunction key.

2-7.1.2 The device Function. Pressing the device function key on the DEVICE SELECT menu allows selection of either local or external devices to be controlled, depending on the frame selection. Only local devices are controlled in the R-2541/B Receiver System. The "device" readout on the display changes to all capital letters, and the word "DEVICE" is bracketed. As devices are selected, the "model" field indicates the model number, frequency range and software version of the selected device.

Subfunction labels dev1 and dev2, which represent receivers A and B in the selected frame, appears above the two left-most FUNCTION keys. Press dev1 or dev2 to select a receiver in the frame. The "DEVICE" readout on the display reflects the address of the device selected. After making the desired selection, press the ENTER key.

NOTE

Attempting to select a frame/device not installed results in a "NO DEVICE" message in the "model" field of the display.

2-7.1.3 Accessing the Front Panel Configuration Menu (fp cfg KEY). From the opening DEVICE SELECT menu, the operator may enter the Front Panel Configuration Menu by pressing the fp cfg function key. The FRONT PANEL CONFIGURATION menu, which is functionally represented within Figure 2-5, allows operator control of the presentation of information on the display. It is selected by pressing the fp cfg menu key.

a. The Display Contrast Control (cntrs). There are two ways to control contrast. Contrast may be controlled by the parameter adjust knob whenever there is no other parameter under its control. Contrast may also be controlled by pressing the cntrs key on the FRONT PANEL CONFIGURATION menu. This will allow the direct input of the contrast value from 0 to 25. A value of 0 offers the least amount of contrast, while a value of 25 offers the greatest amount of contrast available. Entries outside this range will be ignored. If the numeric keypad is used, press ENTER to enter the value. This parameter is retained in battery backed-up memory.

b. Front Panel Feedback Tone Control (beep). The beep key function on the FRONT PANEL CONFIGURATION menu provides operator control of the front panel feedback tones. The "off" subfunction renders the beeper inactive. The "key" subfunction causes the beeper to sound a short, high tone on valid keypresses and a longer low tone on errors. The "error" subfunction causes the beeper to sound only the error tone.

   To select the desired beeper condition, press the appropriate subfunction key followed by the ENTER key. This parameter is retained in battery backed-up memory.

c. Selecting the Remote Address (r adr). The remote address (r adr) parameter on the FRONT PANEL CONFIGURATION menu allows selection of the installed Remote Interface address. The IEEE-488 General-Purpose Interface Bus is not used in the WJ-8907 Receiving System and this parameter is not applicable.

d. Selecting the Frame Address (f adr). The frame address parameter (f adr) on the FRONT PANEL CONFIGURATION menu allows selection of the WJ NET frame address of the local frame in which the FPU is installed. Since the WJ Net is not used in the WJ-8907 Receiving System, a frame address of 0 should be selected.

e. Selecting the Audio Source (audio). The audio function key on the FRONT PANEL CONFIGURATION menu allows operator selection of the audio source present in each of the front panel headset channels (left and right). Pressing this function key yields the following subfunctions:

   1. dev1. When selected, the audio of Local Device 1 is present in the left side of the headset.

   2. dev2. When selected, the audio of Local Device 2 is present in the right side of the headset.

3. 1L-2R. When selected, the audio of Local Device 1 is present in the left earpiece and the audio of Local Device 2 is present in the right earpiece.

4. 1 and 2. When selected, the sum of the Local Device 1 and Local Device 2 audio outputs is present in both earpieces.

5. auto. When selected, the audio routed to the headset is based on the selected device.

After selecting the desired subfunction, press the ENTER key.

2-7.1.4 Gaining Access to Device Functions (contrl key). Pressing the contrl function key on the opening DEVICE SELECT menu allows entry to the DEVICE menus. These menus allow access to all other functions of the device.

2-7.2 Local Operation Via the Manual Menu. The MANUAL menu, whose receiver parameter functions are summarized in Figure 2-8, allows the operator to control the receiver locally by manual selection of commands and adjustments. No sweep or step operations take place from the MANUAL menu.

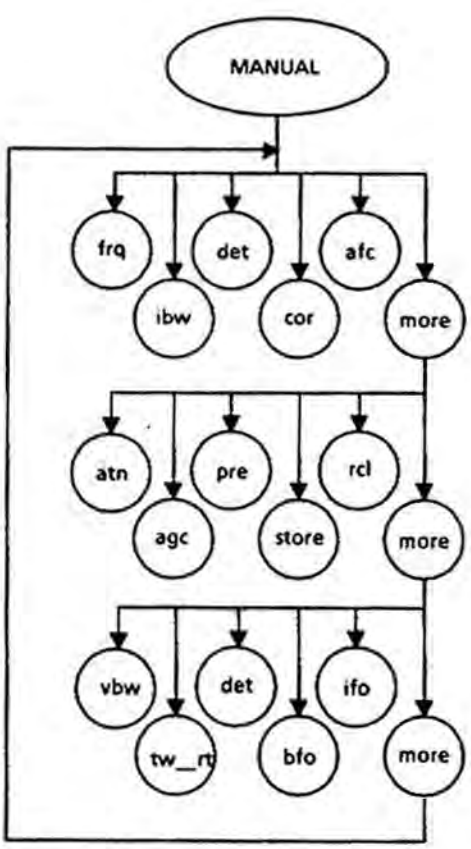


FIGURE 2-8. The MANUAL Menu

The MANUAL menu, which is used to access manual search or analysis operations of the Miniceptor, is selected by pressing the menu key labeled <manual>. The MANUAL menu may only be entered if the Miniceptor is in the manual operating mode, or if sweep or step operations have been suspended. If these conditions are not true, the previous menu generates an error prompt indicating "INCOMPATIBLE MENU."

To re-enter manual mode from another menu, cycle through the menu keys as necessary using the <more> key, and press the <manual> key when it becomes visible on the display. The following paragraphs describe the manipulation of the various functions within the MANUAL menu.

2-7.2.1 Tuning the Receiver (frq). Pressing the frq function key on the MANUAL menu allows selection of receiver tuned frequency, and makes the following subfunctions available:

a. <tw_rate>. Pressing the left arrow (<) or right arrow (>) subfunction keys selects the rate at which frequency is varied by the tuning wheel. The rate is indicated by a flashing underscore below the appropriate digit on the "FRQ" display. If the flashing underscore is below the "M", the tuning wheel and UP/DOWN arrow keys are locked. The ADJ. switch selects the tuning wheel rate in the same manner as the subfunction keys.

b. tw_lk. Locks the tuning wheel and UP/DOWN arrow keys. When locked, the flashing cursor is beneath the "M" in the frequency display. When unlocked, the cursor is below the "tens" (rightmost) frequency digit. This subfunction is exclusive to the frq function.

c. zero. Sets all digits to the right of the "FRQ" display decimal point to zero.

The operating frequency may also be selected by entering the digits sequentially, highest to lowest, using the numeric keypad keys and the decimal point key, and then pressing the ENTER key. After selecting the desired frequency, press the ENTER key again to exit the function.

For example, when the display indicates 145.5150 MHz, entering "26" followed by an ENTER keypress causes the display to indicate 26.00000 MHz.

2-7.2.2 Enabling or Disabling Automatic Frequency Control (afc). Automatic Frequency Control can be toggled on and off by pressing the afc function key in the MANUAL menu. It is not necessary to press the ENTER key.

2-7.2.3 Selecting the Receiver's IF Bandwidth (ibw). Pressing the ibw key while in the MANUAL menu allows selection of receiver IF bandwidth, with subfunction keys indicating the available bandwidth choices. Bandwidths less than 1 MHz are displayed in kHz (suffix "k"). Bandwidths greater than 1 MHz are displayed in MHz (suffix "M"). In the WJ-8907 Receiving System, bandwidths are displayed from left to right as follows:

6.4k 20.0k 75.0k 250k 1.00M 12.0M

(The 12.0 M indicates the Bypass mode.) To select a bandwidth, press the appropriate subfunction key, followed by the ENTER key. Alternatively, the UP/DOWN arrow keys or the parameter adjust knob may be used to step through the available bandwidth choices. When the LSB and USB detection modes are selected, the smallest IF bandwidth is automatically selected. Therefore, the IF bandwidth cannot be changed if the detection mode is LSB or USB.

2-7.2.4 Selecting the Receiver's Detection Mode (det). Pressing the det key while in the MANUAL menu allows selection of receiver detection mode. Available detection modes in the Miniceptor include (displayed subfunction in parentheses): AM (am), FM (fm), Pulse (pls), IFT (ift), CW (cw), LSB (lsb), and USB (usb). To select the desired detection mode, press the appropriate subfunction key, up/down keys, or use the adjust knob.

2-7.2.5 Enabling or Disabling Automatic Gain Control (agc). Automatic Gain Control can be toggled between normal and off by pressing the agc function key in the MANUAL menu. It is not necessary to press the ENTER key.

2-7.2.6 Setting the Carrier-Operated Relay (COR) Threshold (cor). Pressing the cor key is used to set the COR threshold from 0 to 55 dB above the receiver's theoretical noise floor, or to turn the COR function OFF. See the WJ-8607-88-4 Depot Maintenance Manual for a more detailed discussion of COR.

To set the COR level, press the cor function key in the MANUAL menu and select the off subfunction, or the desired level in dB as follows:

a. If using the preset subfunction values, select the value using the parameter adjust knob or the UP/DOWN arrow keys, then press ENTER to enter the value.

b. If using the numeric keypad, select the desired value and then press ENTER to enter the value.

NOTE

Attempting to select a value larger than 55 dB automatically turns the COR to "off."

2-7.2.7 Setting the Receiver's Manual Gain (atn). Pressing the atn function key in the MANUAL menu adjusts the degree of attenuation of receiver manual gain from 0 to 105 dB. For the attenuation adjustment to affect receiver performance, AGC must be turned OFF (see paragraph 2-7.2.5).

To set the attenuation value, press the atn function key and select the desired attenuation using the preset subfunction values, the parameter adjust knob, the numeric keypad, or the UP/DOWN arrow keys.

If the attenuation is increased to the point that signal strength determination is no longer possible, an "<DET" error message appears on the display. Conversely, decreasing attenuation to the point that strong signals exceed the maximum AM detector input causes an ">DET" error message to appear on the display.

2-7.2.8 Storing Current Receiver Parameters in Memory (store). Pressing the store function key in the MANUAL menu stores all current receiver parameters in receiver memory. To utilize this function, proceed as follows:

a. Press the function key labeled store. Display shows the operator prompt "STORE TO CHANNEL: X" in brackets at the bottom of the display screen (X is the last used memory channel number +1).

b. Use the parameter adjust knob, UP/DOWN arrow keys, or numeric keypad to select the desired memory channel (1 through 100). The display indicates the selected channel number.

c. Press ENTER to store the receiver parameters in the selected memory channel. Display returns to the normal MANUAL menu.

To store other than current receiver parameters in memory, refer to paragraph 2-7.3.1.

2-7.2.9 Recalling Receiver Parameters from Memory (rcl). Pressing the rcl function key in the MANUAL menu allows stored receiver parameters to be recalled and used as the current parameters. This function is useful when the operator knows the contents of the memory channel to be recalled. In order to review memory contents before recall, refer to paragraph 2-7.3.1. To utilize the recall function, proceed as follows:

a. Press the function key labeled rcl. Display shows the operator prompt "RECALL FROM CHANNEL: X" in brackets at the bottom of the display screen (X is the last used memory channel number +1).

b. Use the parameter adjust knob, UP/DOWN arrow keys, or numeric keypad to select the desired memory channel (1 through 100). The display indicates the selected channel number.

c. Press ENTER to recall the stored receiver parameters in the selected memory channel. Display returns to the normal MANUAL menu.

2-7.2.10 Adjusting the Beat Frequency Oscillator (bfo). Pressing the bfo function key in the MANUAL menu allows the BFO to be adjusted in 0.25 kHz increments from -4.00 kHz to +4.00 kHz while in CW mode. Select the desired BFO frequency using the parameter adjust knob, UP/DOWN arrow keys, or numeric keypad. BFO can only be adjusted when the CW detection mode is selected.

2-7.2.11 Selecting the Receiver's Video Bandwidth (vbw). Pressing the vbw function key in the MANUAL menu allows selection of receiver video bandwidth, with subfunction keys indicating the available bandwidth choices.

Video bandwidths less than 1 MHz are displayed in kHz (suffix "k"). The following video bandwidths are displayed as subfunctions in ascending order from left to right:

4.2k 13.0k 48.7k 162k 650k bypass

To select a video bandwidth, press the appropriate subfunction key or use the UP/DOWN arrow keys or the parameter adjust knob to step through the bandwidth choices.

NOTE

Default video bandwidths are assigned to each IF bandwidth choice. Although the video bandwidth may be changed using the vbw function key, subsequent selection of a new IF bandwidth causes the video bandwidth to revert to the appropriate default setting.

2-7.2.12 Setting the Resolution of the Tuning Wheel (tw_rt). Pressing the tw_rt key in the MANUAL menu allows selection of the increment used in frequency adjustment with the tuning wheel or UP/DOWN arrow keys. The increment is selected in the same manner as described under the frq function in paragraph 2-7.2.1.

This function is included separately to allow entry of a tuning rate which is not an integral multiple of 10; for example, 25 kHz.

2-7.2.13 Adjusting the IF-to-Baseband (IFT) Oscillator (ifo). Pressing the ifo function key in the MANUAL menu allows adjustment of the conversion oscillator frequency from -2 MHz to +2 MHz to provide the proper baseband output. Selection of the desired conversion oscillator frequency is effected using the parameter adjust knob, UP/DOWN arrow keys, or numeric keypad. IFO can only be adjusted when the IFT detection mode is selected.

2-7.3 Memory Operations. The MEMORY menu, which is functionally summarized in Figure 2-9, allows the operator to access the receiver memory channels, and may be entered regardless of current receiver operating mode. While in this menu, memory channels of the receiver may be examined or changed, since all functions are done off-line of the current receiver operation. Also, memory parameters related to sweep and step operations can be selected from the MEMORY menu.

The receiver controller recalls a channel from the receiver under the following conditions:

a. When entering the MEMORY menu.

b. When the mchl parameter is changed.

c. When clr_a is activated.

d. When the undo command is used.

The receiver controller stores a channel when the mchl is changed, or when exiting the MEMORY menu if the data in the channel has changed. While in the MEMORY menu, the receiver mode and status in the upper right corner of the display are updated.

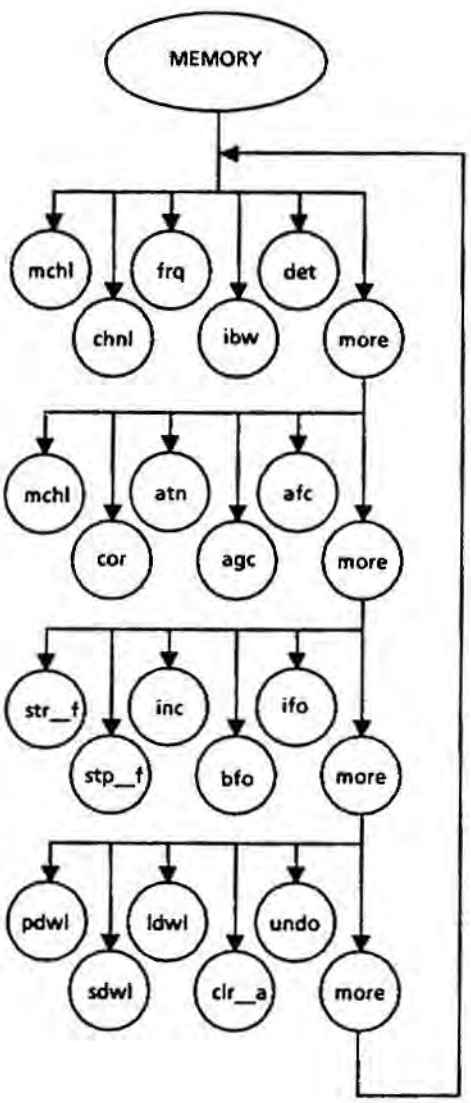


FIGURE 2-9. The MEMORY Menu

Functions available in the MEMORY menu are described in the following paragraphs. However, there is no <tw_rt> subfunction available in MEMORY mode.

2-7.3.1 Selecting, Examining, and Editing Memory Channels (mchl). Pressing the mchl function key on the MEMORY menu allows selection of memory channels (1 to 100) in the receiver for examination and/or editing. When a new channel is selected, a previously selected channel is stored again (if any subfunctions have been changed) and the new channel is displayed. Channel selection is accomplished by numeric entry, use of the parameter adjust knob, or use of the UP/DOWN arrow keys. Memory parameters [such as tuned frequency (frq - refer to paragraph 2-7.2.1), IF bandwidth (ibw - refer to paragraph 2-7.2.3), detection mode (det - refer to paragraph 2-7.2.4), automatic frequency control (afc - refer to paragraph 2-7.2.2), automatic gain control (agc - refer to paragraph 2-7.2.5), manual gain (atn - refer to paragraph 2-7.2.7), COR threshold (cor - refer to paragraph 2-7.2.6), and Beat Frequency Oscillator limits (bfo - refer to paragraph 2-7.2.10)] are set through function keys in a manner identical to setting active front panel parameters. Additional step and sweep parameters (such as channel disable/enable, sweep start and stop frequencies, sweep frequency increments, and sweep and scan dwell times can be set using the functions described in the following paragraphs. Memory channels may be used for manual, step, or sweep operations.

a. Enabling or Disabling a Memory Channel (chnl). This function is used to disable or to enable a memory channel from "SWEEP MEMORY" or "STEP" operation. Pressing the chnl function key in the MEMORY menu toggles this function on or off. If the channel is off, the sweep or step operations will skip over it.

b. Setting Sweep Start and Stop Frequencies in Memory (str_f and stp_f). The str_f and stp_f functions on the MEMORY menu allow the operator to control the sweep mode start and stop frequencies. The limits of these values are based on the receiver frequency range limits. Subfunction keys and entry methods are the same as used in the frq function; refer to paragraph 2-7.2.1. However, the start frequency must be a value less than the stop frequency.

c. Setting Sweep Frequency Increments (inc). The inc function on the MEMORY menu allows control of the sweep mode increment frequency. Subfunction keys and entry methods are the same as used in the frq function with the exception that + and - keys may be used to indicate the direction of sweep. A + indicates start to stop (positive) sweep, while a - indicates stop to start (negative) sweep. Refer to paragraph 2-7.2.1 for use of subfunction keys.

d. Setting Sweep or Step Pre-dwell Timer (pdwl). The pdwl function on the MEMORY menu sets the length of time that the receiver waits on each sweep or step point for a signal to appear. Fixed values may be selected from the designated subfunction keys, or the value may be adjusted with the UP/DOWN arrow keys on the keypad or the ADJ. knob. The range of this timer is from 0 to 996 ms, in 4 ms steps or infinity (inf).

e. Setting Sweep or Step Signal Dwell Timer (sdwl). The sdwl function on the MEMORY menu sets the length of time that the receiver dwells on a sweep point or step channel which has a signal present, before continuing to the next channel. Fixed values may be selected from the designated subfunction keys, or the value may be adjusted with the UP/DOWN arrow keys on the keypad or the ADJ. knob. The range of this timer is from 0 to 600 seconds, in 1 second steps or infinity (inf). Unless a parameter other than infinity (inf) is selected, the receiver sweep/step functions will step at the first active frequency and remain at this frequency.

f. Setting Sweep or Step Post-dwell Timer (ldwl). The ldwl function on the MEMORY menu sets the length of time that the receiver dwells on a sweep or step channel after a signal is lost, before continuing. Fixed values may be selected from the designated subfunction keys, or the value may be adjusted with the UP/DOWN arrow keys on the keypad or the ADJ. knob. The range of this timer is from 0 to 60 seconds, in 1 second steps or infinity (inf).

g. Clearing Memory Channels (clr_a). The clr_a function on the MEMORY menu allows the operator to clear all receiver sweep, step, and storage memory channels on the selected device only. An operator prompt is provided to avoid accidental activation.

h. Undoing Memory Changes (undo). The undo function on the MEMORY menu causes the currently-selected memory channel to be recalled from receiver memory, thereby undoing any changes which may have been entered since the last recall. It provides a convenient means of restoring parameters to their original stored value without having to change them individually. An operator prompt is provided prior to performing this operation.

2-7.4 Initiating Sweep Operations Via the SWP IM (Sweep Immediate) Menu. The SWP IM menu, which is functionally summarized in Figure 2-10, initiates sweep operations of the receiver while still allowing access to various receiver functions. The initiation of a sweep does not require the operator to preset any receiver parameters; the receiver sweeps using the last parameters entered. During sweep operations, any of the functions available in the SWP IM menu may be altered without stopping the sweep.

Sweep operations are initiated by selecting the swp im menu key. With the exception of str_f (start frequency), stp_f (stop frequency), inc (increment), and dwell timers, the receiver responds immediately to an altered parameter such as detection mode (det) COR level (cor), AGC mode (agc), etc. For the excepted parameters, the receiver responds to the new settings after the end of the current sweep. The following paragraphs further describe the cntrl (sweep control), str_f (start frequency), stp_f (stop frequency), and inc (increment) functions in the swp im menu.

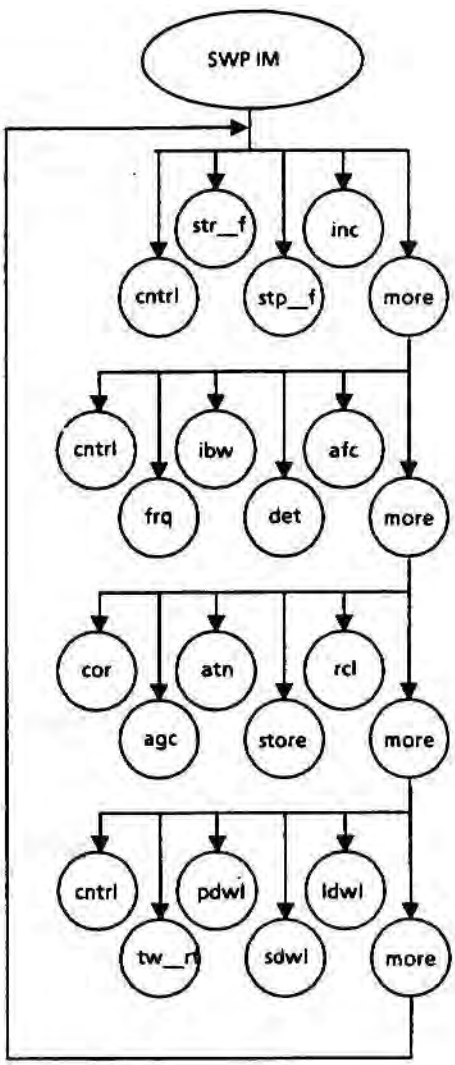


FIGURE 2-10. The SWP IM Menu

2-7.4.1 Sweep Control Functions (cntrl). The cntrl function allows the receiver operating mode to be selected based on the current menu. The following subfunctions are available when the cntrl function key is pressed:

a. suspd. When selected, suspends an active SWEEP IMMEDIATE operation.

b. advnc. When selected, enables a suspended operation or advances an active operation which is currently stopped on a signal.

c. manul. When selected, forces receiver operations into the manual mode.

d. swpim. When selected, starts the sweep if in manual or suspended operations or restarts an active sweep.

All subfunction keys listed above have an immediate action when pressed.

2-7.4.2 Setting Sweep Start and Stop Frequencies (str_f and stp_f). The str_f and stp_f functions on the SWEEP IMMEDIATE menu allow the operator to control the sweep mode start and stop frequencies. The limits of these value are based on the receiver frequency range limits. Subfunction keys and entry methods are the same as used in the frq function; refer to paragraph 2-7.2.1. However, the start frequency must be a value less than or equal to the stop frequency.

2-7.4.3 Setting Sweep Increment Frequencies (inc). The inc function on the SWEEP IMMEDIATE menu allows control of the sweep mode increment frequency. Subfunction keys and entry methods are the same as used in the frq function with the exception that + and - keys may be used to indicate the direction of sweep. A + indicates start to stop (positive) sweep, while a - indicates stop to start (negative) sweep. Refer to paragraph 2-7.2.1 for use of subfunction keys.

2-7.5 Initiating Sweep Operations Via the swp me (sweep memory) Menu. The SWP ME menu, which is functionally summarized in Figure 2-11, allows the operator to sweep frequencies stored in memory channels. Before the sweep memory function is initialized, a memory channel is assigned to a sector (sectr). Ten sectors are available for the assignment of memory channels for sweep memory operations. Otherwise, the initiation of a sweep does not require the operator to preset any receiver parameters; the receiver sweeps using the last parameters entered.

NOTE

The WJ-9207-1 RF Panoramic Display traces will not be activated unless a sector is assigned and selected (refer to paragraph 2-7.5.4).

Sweep memory operations are initiated by selecting the swp me menu key. When the SWP ME menu is in use, the signal strength, signal status, and frq parameter data are only displayed when the receiver is in signal dwell, suspend, or manual operation. The operating mode and status are continually updated, and the tuning wheel is only operational in the frq function.

2-7.5.1 Sweep Memory Control Functions (cntrl). The following subfunctions are available when the cntrl function key is pressed while in the SWP ME menu:

a. suspd. When selected, suspends an active SWEEP MEMORY operation.

b. advnc. When selected, enables a suspended operation or advances an active operation which is currently stopped on a signal.

c. manul. When selected, forces receiver operations into the manual mode.

d. swpme. When selected, starts the sweep if in manual or suspended operations, or restarts an active SWEEP MEMORY operation.

All subfunction keys listed above have an immediate action when pressed.

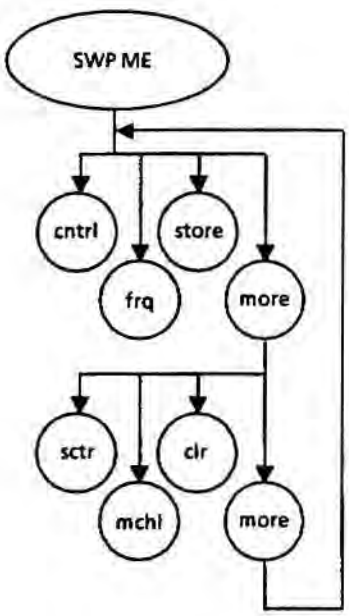


FIGURE 2-11. The SWP ME Menu

2-7.5.2 Sweep Memory Frequency (frq). The frq function allows the operator to tune the receiver if it is suspended. If it is actively sweeping a "SUSPEND DEV OPERATION" (with two associated subfunctions - sus abort) message will appear. If abort is pressed, no action is taken and the receiver controller returns to its previous state. If sus is pressed, the operation is suspended and the operator may now select and control the frequency.

2-7.5.3 Sweep Memory Store (store). The store function allows the current signal frequency and setup to be saved in a memory channel.

2-7.5.4 Sweep Memory Sectors (sctr). The sctr key allows selection of any one of up to ten sectors for memory sweep operations. When a sector is selected, the memory channel number that is assigned to it, including its start and stop frequencies, is displayed. The sector may be selected by the ADJ. knob, UP/DOWN arrow keys, numeric keypad, or by one of the labeled subfunction softkeys. The selected sector may be displayed on the WJ-9207-1 RF Panoramic Display (refer to SE460-BK-OMP-010 for operational procedures).

2-7.5.5 Memory Channel Edit (mchl). The mchl key allows the operator to select and examine memory channels stored for the sweep memory function. Once a sector is selected, the memory channel assigned to it may be changed by first pressing the mchl key, then using the ADJ. knob, UP/DOWN arrow keys, the numeric keypad, or one of the labeled subfunction keys. When a memory channel is selected, its start and stop frequencies are also displayed.

2-7.5.6 Sweep Memory Clear (clr). The clr key causes the sweep list to be cleared.

2-7.6 Initiating Step Operations Via the Step Menu. The STEP menu, which is functionally summarized in Figure 2-12, initiates the receiver to step through frequencies stored in memory channels. The receiver steps through the selected memory channels as determined by the operator's entered channel sequence.

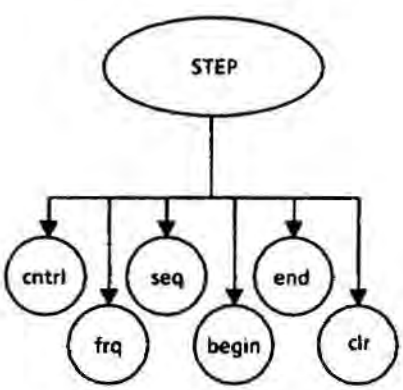


FIGURE 2-12. The STEP Menu

When the STEP menu is in use, the signal strength, signal status, and frq parameter data are only displayed when the receiver is in signal dwell, suspend, or manual operation. The operating mode and status are continually updated, and the tuning wheel is only operational in the frq function.

2-7.6.1 Step Control Functions (cntrl). The following subfunctions are available when the cntrl function key is pressed while in the STEP menu:

a. suspd. When selected, suspends an active STEP operation.

b. advnc. When selected, enables a suspended operation or advances an active operation which is currently stopped on a signal.

c. manul. When selected, forces receiver operations into the manual mode.

d. step. Starts the step if in manual or suspended operations, or restarts an active STEP MEMORY operation.

2-7.6.2 Setting Up the Step Operation Sequence. The seq key allows selection of a begin channel/end channel step sequence. A sequence may consist of either a single channel or a begin and end channel and all inclusive channels between. When a new sequence is selected, the BEG and END displayed parameters are updated with the values of the current sequence channel. Valid sequence numbers are 1 to 20, and may be selected using the numeric keypad, softkeys, UP/DOWN arrow keys, or the ADJ. knob. The begin must be less than the end.

The first and last softkeys provide an easier means of selecting a sequence number, since the operator can "jump" to the beginning or end. The del softkey removes the channels of the current sequence.

a. Entering the Step Operation Start Channel (begin). The begin key allows selection of the start channel of a particular step sequence. Selection of start channel may be made using the subfunction softkeys, numeric keypad, UP/DOWN arrow keys, or the ADJ. knob. A sngl subfunction softkey is available which allows the END channel to be deleted, making a step sequence consisting of a single channel.

b. Entering the Last Channel for a Step Operation (end). The end function allows selection of the last channel of a particular step sequence. Selection of the last channel may be made using the subfunction softkeys, numeric keypad, UP/DOWN arrow keys, or the ADJ. knob. A sngl subfunction softkey is available which allows the END channel to be deleted, making a step sequence consisting of a single channel.

c. Clr. The clr key clears the entire step list.

2-7.7 Sweep Lockout Operations (lckout menu). The LCKOUT menu, which is functionally summarized in Figure 2-13, provides a means for the operator to skip certain stored channels when engaging in sweep operations. This function is particularly valuable when certain channels are known to be inactive or contain unwanted signals. This allows the sweep operation to cycle faster through the active channels.

When the LCKOUT menu is in use the signal strength, signal status, and frq parameter data is only displayed when the receiver is in signal dwell, suspend, or manual operation. The operating mode and status are continually updated, and the tuning wheel is only operational in the frq function.

2-7.7.1 Selecting and Editing a Lockout Channel (chnl). The chnl key on the LCKOUT menu allows selection of a lockout channel for edit operations. As the channel number is varied with the ADJ. knob or the UP/DOWN arrow keys on the keypad, data contained in the channel is shown. Any modifications made to a channel are stored upon exit from the channel. The numeric keypad and designated subfunction softkeys may also be used to select the channel number.

a. Using the Current Receiver Frequency for a Lockout Start or Stop Frequency. The f>str function transfers the current receiver frequency to the current displayed lockout start frequency. The f>stp function transfers the current receiver frequency to the current displayed lockout stop frequency. These functions may only be used when the receiver sweep is suspended or stopped on a signal.

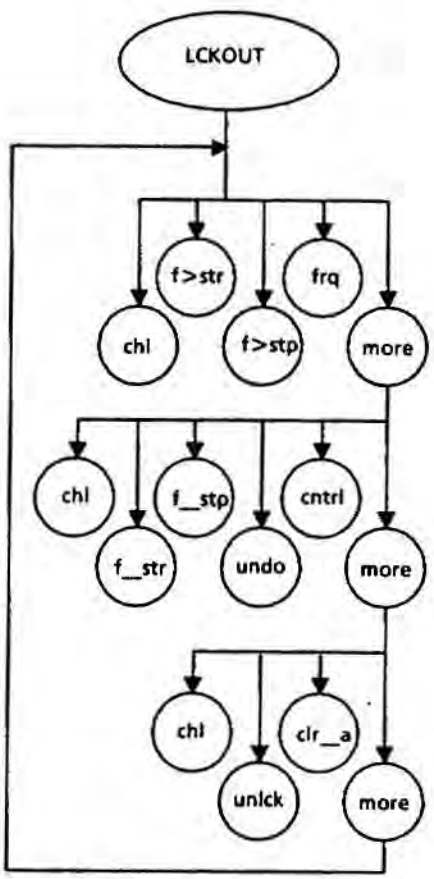


FIGURE 2-13. The Lockout Menu

b. Setting Lockout Start and Stop Frequencies (f_str and f_stp). The f_str and f_stp functions on the LCKOUT menu allow the operator to enter lock out start and stop frequencies. The limits of these values are based on the receiver frequency range limits. Subfunction keys and entry methods are the same as used in the frq function; refer to paragraph 2-7.2.1. However, the start frequency must be a value less than the stop frequency. The selected start and stop frequencies are not sent to the receiver until either the channel number is changed, or the menu is exited.

c. Undoing Lockout Changes (undo). The undo function on the LCKOUT menu causes the currently-selected memory channel to be recalled from receiver memory, thereby undoing any changes which may have been entered since the last recall. The undo function provides a convenient means of restoring parameters to their original stored value without having to change them individually. An operator prompt is provided as follow:

UNDO CHANGES TO LOCKOUT? yes no

NOTE

Activating a new menu or selecting a different memory channel will prevent the operator from undoing the most recent change using the undo function.

d. Clearing All Lockout Channels (clr_a). The clr_a function on the LCKOUT menu allows the operator to clear all receiver lockout memory channels. The sweep operation must be suspended prior to using the cir__a function. An operator prompt is provided as follows:

CLEAR ALL LOCKOUT MEMORY? yes no

e. Unlocking Memory Channels (unlck). The unlck function in the LCKOUT menu allows the selected memory channel to be become unlocked (not a lockout channel). The sweep operation must be suspended prior to using the unlck function.

2-7.7.2 Lockout Control Functions (cntrl). The following subfunctions are available when the cntrl function key is pressed while in the LCKOUT menu:

a. suspd. When selected, suspends an active step or sweep operation.

b. advnc. When selected, enables a suspended operation or advances an active operation which is currently stopped on a signal.

c. manul. When selected, forces receiver operations into the manual mode.

d. swpim and swpme. Starts the operation if in manual or suspended operations, or restarts an active operation.

2-7.8 Signal Queue Operation. The QUEUE menu, which is functionally summarized in Figure 2-14, allows the operator to monitor the signal activity present in a sweep or step operation. The menu displays the four most recent signals encountered. The operating mode and status are continually updated as the sweep or step operation progresses and the frequency shown at the top of the display is the most recent queue entry. The following paragraphs describe the functions available from this menu.

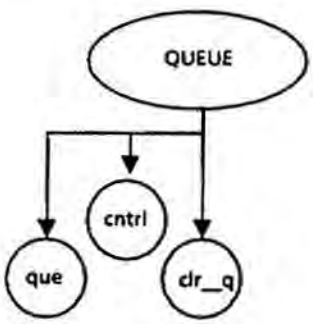


FIGURE 2-14. The QUEUE Menu

2-7.8.1 Turning the Queue Function On and Off (que). The que function turns the que on and off, thereby allowing a displayed signal frequency to be held for analysis.

2-7.8.2 Queue Control Functions (cntrl). The cntrl function is utilized in exactly the same manner as in the LCKOUT menu. Refer to paragraph 2-7.7.2.

2-7.8.3 Clearing the Receiver Queue (clr_q). The clr_q function in the QUEUE menu clears the receiver queue and the displayed channels.

2-7.9 Handing Off Current Parameters to Another Device (HNDOFF Menu). The HNDOFF menu, which is functionally summarized in Figure 2-15, allows the operator to transfer (i.e., hand off) the current operating parameters of the selected device to another device, or conversely, to load the selected device with the operating parameters of another device. In the HNDOFF menu, the operating mode and status are continually updated. The following paragraphs describe the available functions.

2-7.9.1 Defining the Parameters to be Handed Off (oper). The oper function allows the operator to define what parameters are to be transferred. The subfunctions available in this function are as follows:

a. frq. Frequency data transferred to selected device and accessible by manual menu key.

b. (manswpi). MANUAL and SWEEP IMMEDIATE data transferred.

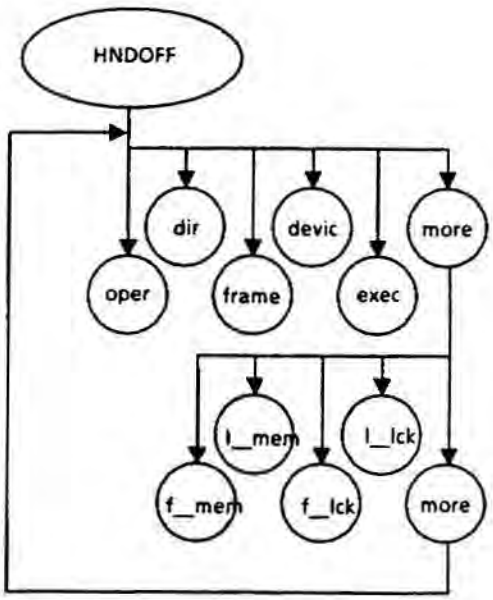


FIGURE 2-15. The HNDOFF Menu

c. mem. Specified memory channels transferred (enter channel numbers using f_mem, l_mem parameters on the second page of the softkeys). The f_mem (first memory channel) parameter key allows entry of the beginning channel to be handed off. The l_mem (last memory channel) parameter key allows entry of the ending channel to be handed off. Transferring memory channels replaces all existing programming on the destination memory channel.

d. lckot. Specified lockout channels transferred (enter channel numbers using f_lck, l_lck parameters on the second page of the softkeys). The f_lck (first lockout channel) parameter key allows entry of the beginning channel to be locked out. The l_lck (last lockout channel) parameter key allows entry of the ending channel to be locked out.

2-7.9.2 Specifying the Direction of the Transfer (dir). The dir function specifies the direction of the transfer, either to or from. Press the appropriate subfunction softkey to make the selection.

2-7.9.3 Selecting the Address of the Targeted Device's Frame (frame). The frame is used to select the address (local, or 0 to 30) of the frame which houses the device to be used in the handoff operation. Selection may be via softkeys, the numeric keypad, the UP and DOWN keys, or the ADJ. knob. This feature does not apply to the WJ-8907 Receiving System, since only the local address is available.

2-7.9.4 Selecting the Device's Address (devic). The devic function is used to select the address of the particular device to be used in the handoff operation. Selection may be via softkeys, the numeric keypad, the UP and DOWN keys, or the ADJ. knob.

2-7.9.5 Executing the Handoff (exec). The exec function causes the handoff to take place. After this key is pressed, the following sequence of events occur:

a. The Receiver Controller verifies that a communications path can be established to the handoff unit. If the NET is required, it is taken.

b. If the NET is busy, a NET NOT AVAILABLE error message is displayed.

c. After communications are established, a "token" is requested from the handoff device (if the transfer direction is "to").

d. If the device does not answer, the HANDOFF NO DEVICE error message is displayed.

e. If a token is requested and is unavailable, a HANDOFF NO TOKEN error message is displayed.

f. Once a token has been either granted ("to" transfer) the handoff takes place.

g. The error status of the "to" unit is read both before and after the handoff. If an execution error is not generated, the handoff was successful. If the handoff was unsuccessful, a "BAD HANDOFF" error is generated.

2-7.10 Setting Device Configuration Parameters (dv cfg menu). The DV CFG menu, which is functionally shown in Figure 2-16, allows the operator to examine and alter various device configuration parameters. When operating from the DV CFG menu, operating mode and status are continually updated. The following paragraphs describe the available functions.

2-7.10.1 Defining the Class of Signals to be Reported in Sweep and Step Operations (reprt). The reprt function in the DV CFG menu allows the operator to define what class of signals is reported in sweep and step modes of operation. Any combination of choices is permissible, and only subfunction softkey entries are valid. The subfunction choices available are as follows:

a. new_s. New signals

b. old_s. Old signals

c. s_lck. Skip lockout channels

d. s_adj. Skip adjacent sweep points

e. all_s. All signals (Clears all other choices).

All subfunction softkeys except all_s are toggle operations.

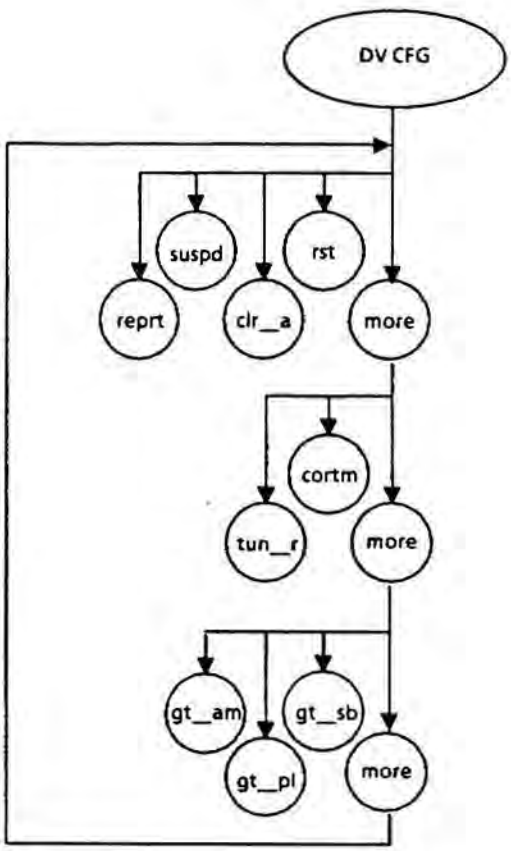


FIGURE 2-16. The Device Configuration Menu

2-7.10.2 Defining Actions to Cause Automatic Suspend Operation (suspd). The suspd function in the DV CFG menu allows the operator to define what sweep or step actions cause an automatic suspension of operation. Any combination of choices is permissible, and only subfunction softkey entries are valid. The subfunction choices available are as follows:

a. endsi. Suspend on end of SWEEP IM

b. endsm. Suspend on end of SWEEP ME

c. endst. Suspend on end of STEP sequence

d. ful_q. Suspend on full queue

e. onsig. Suspend on signal acquisition

f. off. Turns all suspends off.

All subfunction softkeys except off are toggle operations.

2-7.10.3 Resetting the Receiver (rst). The rst function in the DV CFG menu allows the operator to reset all current device parameters except for storage memory and lockout memory. The rst function includes an operator prompt to avoid accidental activation.

2-7.10.4 Clearing the Receiver (clr_a). The clr_a function in the DV CFG menu allows the operator to clear all device memory including lockouts and current parameters. The clr_a function includes an operator prompt to avoid accidental activation.

2-7.10.5 Selecting the Receiver's Manual Tuning Resolution (tun_r). The tun_r function in the DV CFG menu allows the operator to select either 100 Hz or 500 Hz tuning resolution while tuning in the manual or suspended operations. The receiver default is 100 Hz except when operating in sweep or step modes. In these modes, only 500 Hz tuning resolution is allowed. This function has no effect on the displayed frequency resolution. It only alters the internal receiver hardware operations.

2-7.10.6 Setting the Value of the COR Release Timer (cortm). The cortm function in the DV CFG menu allows the operator to set the COR release timer; that is, the length of time a signal must be absent before it is reported as such. Time may be entered using the subfunction softkeys, the numeric keypad, the UP/DOWN arrow keys, or the ADJ. knob. The permissible range of values is from 0 milliseconds (ms) to 2 seconds (s), in 20 ms increments.

2-7.10.7 Setting the Value of the AM/FM Gate Timer (gt_am). The gt_am function in the DV CFG menu allows the operator to set the length of time that a signal must remain below the AGC threshold before the receiver increases its gain in the AM or FM detection modes. The range of this timer is from 4 ms to 100 ms in 4 ms increments.

2-7.10.8 Setting the Value of the Pulse Gate Timer (gt_pl). The gt_pl function in the DV CFG menu allows the operator to set the length of time that a signal must remain below the AGC threshold before the receiver increases its gain in the Pulse detection mode. The range of this timer is from 4 ms to 252 ms in 4 ms increments.

2-7.10.9 Setting the Value of the CW/SSB Gate Timer (gt_sb). The gt_sb function in the DV CFG menu allows the operator to set the length of time that a signal must remain below the AGC threshold before the receiver increases its gain in the CW or SSB detection modes. The range of this timer is from 4 ms to 252 ms in 4 ms increments.

2-7.11 Error Checking (ERR CK MENU). The ERR CK menu, which is functionally summarized in Figure 2-17, allows the operator to monitor the device for error conditions. Two types of errors can be checked for: current or latched. These error types are based on the response to the CDE? (request current device-dependent error (DDE) register contents) and DDE? (request latched DDE register contents) remote queries, respectively.

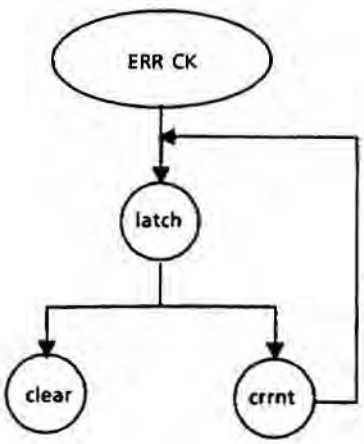


FIGURE 2-17. The ERR CK Menu

Upon entering the ERR CK menu, the Current Error display is shown. This display is updated via constant querying and decoding of the contents of the device-dependent error register of the device. Pressing the latch softkey while in the Current Error display causes the Latched Error display to be shown. This display is updated based on a single query and decode of the contents of the register which occurs upon entry into the display. The Latched Error display shows any errors that have occurred since power-up or since the last viewing of the Latched Error display. Pressing the clear softkey while in this display causes the contents of device-dependent error register to be cleared then queried and decoded for any new errors. The error display is cleared and updated simultaneously.

Error conditions that may be shown in either the Current or Latched Error display match those that may be returned with the CDE? and DDE? queries. Table 2-3 lists the bit-mapping of the CDE? and DDE? queries, the error types label and error code that is shown on the display corresponding to the bit, and the description of the error condition. There are four error types that can be displayed: power, Syn err (synthesizer error), micro (microprocessor error), and mem def (memory default). The error codes are displayed on the same line as the label for their error type.

2-7.12 Receiver Controller System Errors. All receiver controller system errors are displayed on the bottom line of the LCD display in the area normally used for function softkeys. The error message is bracketed with two blocks (▮error message▮). To the right of the error message the user options are placed. When the receiver controller shows an error, one of the options must be selected to perform any other receiver controller operations. Table 2-4 summarizes system error messages, related cause, and recovery actions.

TABLE 2-3. Error Code Definitions

CDE/DDE Bit	Displayed Error Type	Displayed Error Code	Error Description
0	power	fail	Power supply fault
1	power	+12	+12 Vdc fault
2	power	+7.5	+7.5 Vdc fault
3	power	-7.5	-7.5 Vdc fault
4	power	+30	+30 Vdc fault
5	syn err	1st	1st LO unlocked
6	syn err	2nd	2nd LO unlocked
7	syn err	trn	3rd LO unlocked
11	syn err	fe	Freq. Extender LO unlocked
13	syn err	mWcom	Microwave downconverter communications fault (not applicable)
14	syn err	mW	Microwave downconverter synthesizer fault (not applicable)
8	micro	ad err	A/D error
12	micro	eeprom	EEPROM failure to be written
9	mem def	eeprom	EEPROM has been defaulted. If this error has occurred, the receiver must be reconfigured and the receiver is unusable. Return receiver to depot for repair. This only applies to latched errors.
10	mem def	ram	RAM has been defaulted. All storage memory has been defaulted. This only applies to latched errors.
15			Not used

TABLE 2-4. Receiver Controller Error Messages

Error Message	Cause	Action
INVALID ENTRY	Attempt to access an invalid or inactive function.	CLEAR — Restores FPU to normal operation.
ENTRY OUT OF RANGE	Attempt to enter a value beyond the FPU limit.	CLEAR — Restores FPU to normal operation.
HANDOFF NET NOT AVAILABLE	Attempt to execute a handoff when the NET is busy.	CLEAR — Restores FPU to normal operation. Handoff may be re-attempted after the net is no longer busy.
HANDOFF NO DEVICE	Attempt to handoff to a device that is not present.	CLEAR — Restores FPU to normal operation. Verify handoff frame and device selection as well as NET connection.
BAD HANDOFF	Attempt to handoff a parameter to a device that does not support that operation. (i.e., frequency out of range).	CLEAR — Restores FPU to normal operation.
HANDOFF NO TOKEN	Attempt to handoff to a unit that is controlled by another FPU or host.	CLEAR — Restores FPU to normal operation.
DEVICE TIMEOUT ERROR	Device did not answer a front panel query. Possible NET failure, or device communications failure.	RETRY — Attempts to re-establish device communications. ABORT — Returns FPU to SELECT menu.
DEVICE HARDWARE ERROR	Device detected an internal hardware error.	CLEAR — Restores FPU to normal operation. Access the ERR CK menu to see actual error.
IOC NOT RESPONDING	IOC card did not answer power-up clear configuration.	CLEAR — Error is ignored and front panel continues operation.

2-7.13 Receiver Controller Operator Prompts. Operator prompts are displayed along the bottom line of the LCD display. They must be acted upon by pressing one of the softkeys displayed before other operations can occur. Table 2-5 summarizes operator prompts, related cause, and action required.

TABLE 2-5. Receiver Controller Operator Prompts

Operator Prompt	Cause	Action
DEV CONTROLLED BY: XX	Attempt to control a device that is controlled by FPU or host "XX". Device does not have its token.	MNTR — Enter monitor mode on the FPU. TAKE — Take control of the device. ABORT — Return to SELECT menu.
INCOMPATIBLE MENU	Attempt to select a menu that is not compatible with current device operations.	MAN — Force device to manual and to enter menu. SUS — Suspend device operation and enter menu. ABORT — Return to original menu.
SUSPEND DEV. OPERATION	Attempt to control frequency while the device was sweeping or stepping.	SUS — Suspend operation and allow frequency control. ABORT — Restore normal operation.
MONITOR, CONTROL BY: XX	Device is controlled by FPU or host "XX".	MORE — Allows access to other displays of current menu.

2-8 OPERATION IN DEGRADED MODE.

Details on WJ-9902-2 degraded mode operation may be found by referring to manual #SE460-BH-OMP-010.

2-9 SHUTDOWN PROCEDURE.

The following operating procedure removes power from the WJ-9902-2 Receiver Controller:

a. Move the LIGHT switch to the OFF (down) position.

b. De-energize the receiver controller by moving the PWR switch to the OFF (down) position.

2-10 EMERGENCY SHUTDOWN PROCEDURE.

The WJ-9902-2 does not require an emergency shutdown procedure.

CHAPTER 3

CIRCUITS DESCRIPTION

3-1 INTRODUCTION.

The following paragraphs describe the theory of operation of the WJ-9902-2 Receiver Controller to support the level of maintenance contained in this manual. Simplified functional block diagrams describe the signal, control, and power supply functions of each Lowest Replaceable Assembly (LRA) within the Receiver Controller. Schematic diagrams to support the depot level of maintenance may be found at the end of this document.

3-2 SIMPLIFIED FUNCTIONAL DESCRIPTION.

Functionally, the WJ-9902-2 Receiver Controller contains three sections. These are the equipment frame, the WJ-9902/FPU Front Panel Unit, and the WJ-9902/488 Host Interface. Internal cabling supplies control signaling and data transfer between sections.

The equipment frame section accommodates two WJ-8607-88-4 receivers. The equipment frame section provides operating power to the receivers and permits rack mounting in a standard 19-inch equipment rack. Except for the HPIL IN and HPIL OUT connectors and the power connector, all receiver connections are routed directly to the rear panel of the WJ-9902-2 for system interfacing. The equipment frame section contains an integral AC power supply that operates on 115 or 230 VAC, 44-400 Hz power, and provides +12 VDC power for receiver operation.

Refer to Figure 3-1 and FO-2. The WJ-9902/FPU Front Panel Unit Section provides full FPU operation for the receivers installed in the frame. The FPU provides a back-lit LCD display and a group of control keys that permit a local operator to exercise all of the capabilities of the installed receivers. The FPU provides a phone jack for receiver audio to be heard by the operator.

The WJ-9902-2 IEEE-488 (WJ-9902/488) Remote Interface section converts the FPU's RS-232C protocol into HPIL format for use by the receiver. Although the host interface section allows a host computer capable of communicating over an IEEE-488 bus to control the integral WJ-8607-88-4 receivers, and also includes a WJ-NET Interface that allows the receivers in the Equipment Frame to be accessed by WJ-Receiver Net controllers, these capabilities are not used in the R-2541/B Receiver configuration. Only the FPU Section provides control in the R-2541/B Receiver.

3-3 WJ-9902 EQUIPMENT FRAME SECTION, DETAILED FUNCTIONAL DESCRIPTION

The WJ-9902 Equipment Frame contains a switching power supply to provide the necessary power conversion from the ac source power to +12 volts required by the FPU, the IOC card, and the Miniceptor Receivers.

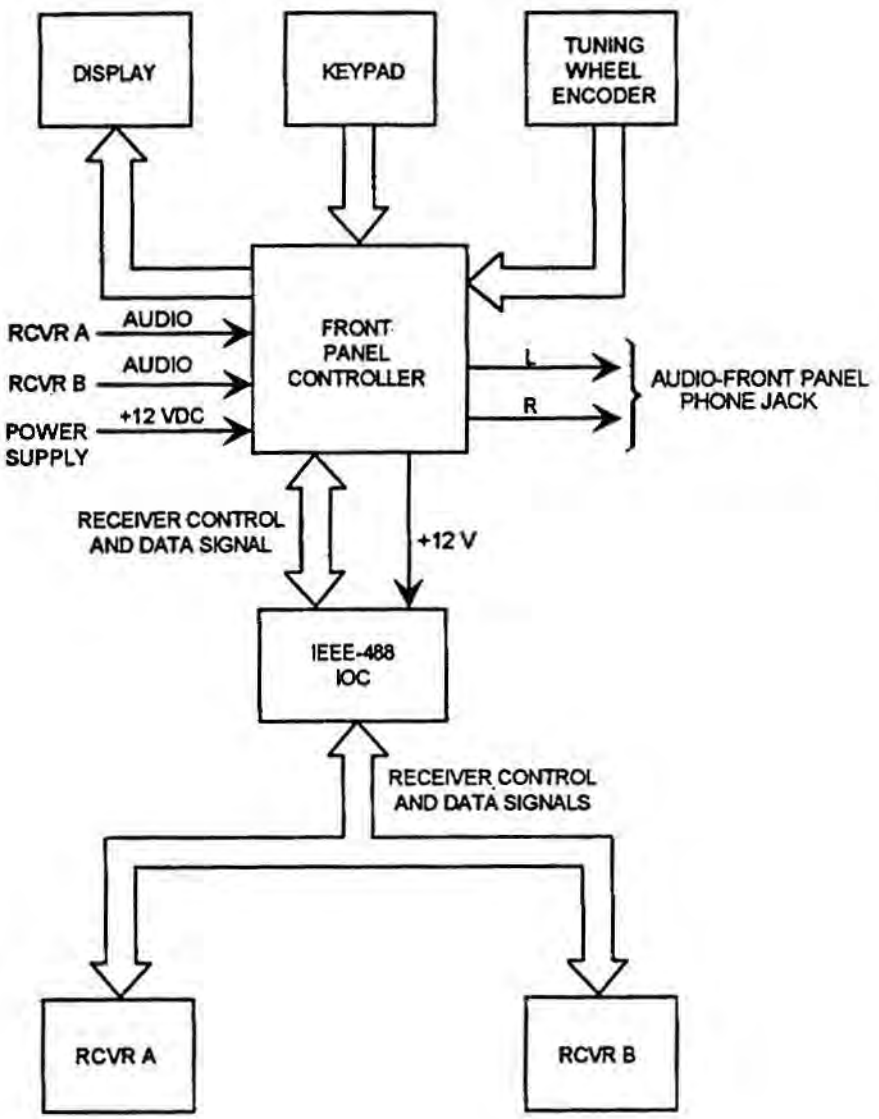


FIGURE 3-1. WJ-9902-2 Receiver Controller Functional Block Diagram

3-3.1 Power Supply. Power supplied to the WJ-9902-2 (see Figure FO-2) enters the unit at the Input Filter input jack, FL1J1, passes through the Line Filter, FL2, and enters the power converter (PS1). The power converter (PS1) is a complete unit sealed at the factory and cannot be repaired. FL1J1 takes a 115 volts ac input and PS1J2 outputs 12 volts dc to the FPU, the WJ-8607-88-4 Receivers and the fan.

3-4 WJ-9902/FPU FRONT PANEL UNIT (A1), DETAILED FUNCTIONAL DESCRIPTION

When combined with the WJ-9902/488 IEEE-488 Host Interface Section, the WJ-9902/FPU Front Panel Unit provides the means for the operator to control the receivers over the HPIL bus. Refer to Figure 3-2 for a block diagram of the WJ-9902/Front Panel Unit. Through its LCD Display and Keypad, the WJ-9902/FPU Front Panel Unit provides the interface between the operator and the WJ-9902/488 IEEE-488 Host Interface Section (IOC). Communications between the FPU and the IOC uses RS-232 protocol. A phone jack on the FPU provides an output for receiver audio.

Components of the FPU comprise the Operating Software (A1A1A1U28 and A1A1A1U29) and the Front Panel Assembly (A1A1).

3-4.1 Front Panel Operating Software. The Front Panel Operating Software resides on the two EPROMs, A1A1A1U28 and A1A1A1U29, programmed for use in the WJ-9902-2 Receiver Controller.

3-4.2 Front Panel Assembly (A1A1). Components of the Front Panel Assembly comprise the Front Panel Controller (A1A1A1), the Left and Right Volume controls (A1A1R1/R2), the LCD Display (A1A1U1), the Keyboard (A1A1U2), and the Tuning Wheel Encoder (A1A1U3). The following paragraphs explain the interrelationship of these components and describe in detail their circuits.

3-4.2.1 Front Panel Controller-Type 796856-2 (A1A1A1). The Front Panel Controller Assembly contains circuitry (FO-3) that accepts inputs from the keyboard and the IOC board, provides a response to the IOC board, and sends receiver information and control signals to the LCD for display. In addition, it selects and amplifies audio signals from the receiver. This assembly can be divided into five major sections: the Remote Interface section, the Key Interface section, the Microprocessor and Memory section, the Display Interface, and the Audio Amplifier section.

3.4.2.1.1 Remote Interface Section. The remote interface section consists of the two dual-asynchronous receiver/transmitters, U32 and U44; the RS-232 driver circuits, U45; the WJ-Net (RS-485) driver circuits, U47; and miscellaneous associated components. In the Barracuda configuration, U32 is used only for transmitting an alarm signal when an error condition has occurred. Since the WJ-Net is not used in the Barracuda system, U47 is present, but not used.

U44 indicates to the microprocessor, U31, that it is ready to accept a character for transmission by raising an interrupt. This active-low interrupt (SIO1TX) is prioritized by U11, which sets its pin 7 output high and its pin 6 and 9 outputs low when this interrupt becomes the highest priority. (Refer to paragraph 3-4.2.1.3d for a U11 description.)

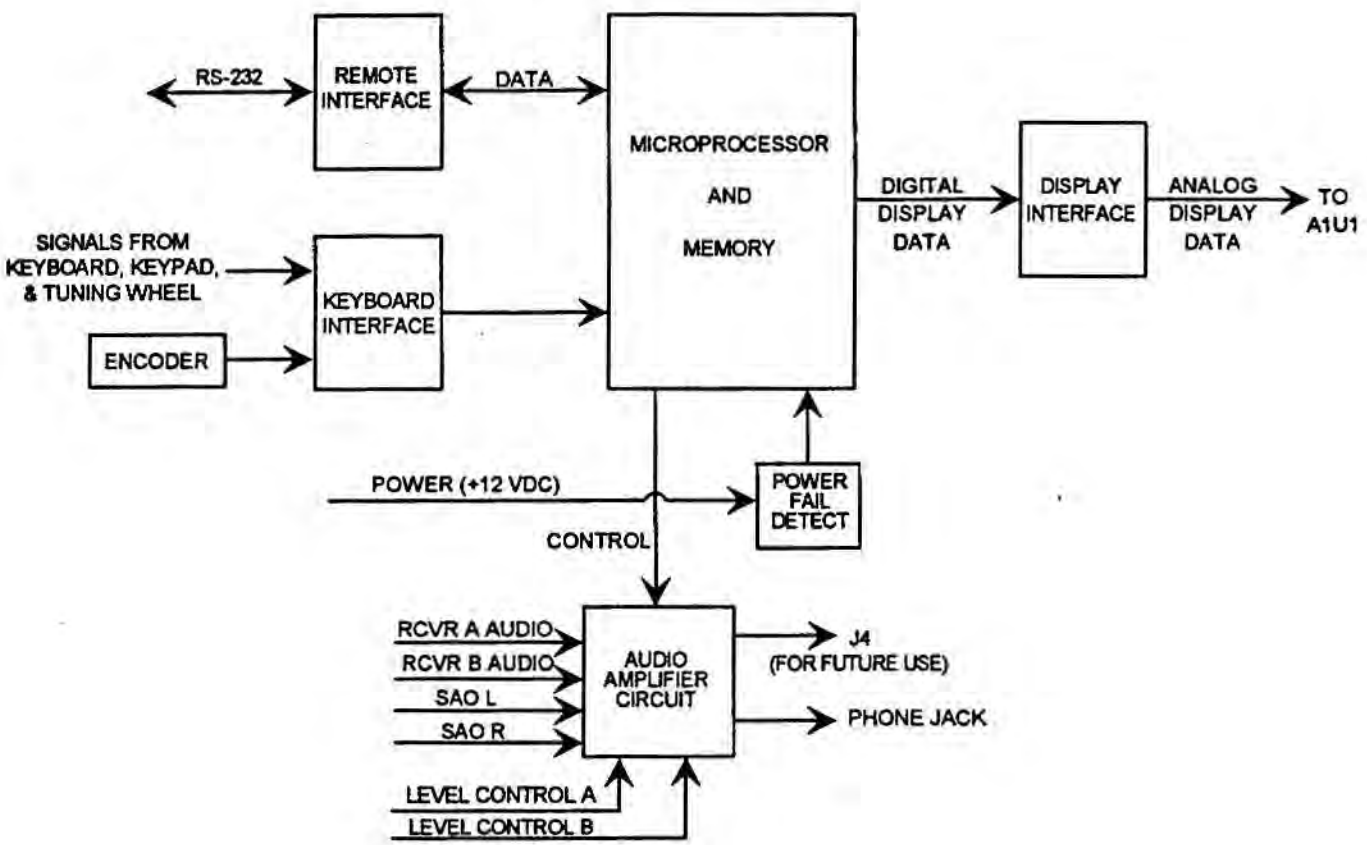


FIGURE 3-2. WJ-9902-2/FPU Functional Block Diagram

Microprocessor, U31, services the interrupt in three steps. First, it enables U44 (via its pin 39 input) by causing 3-to-8 decoder U9 to send its active-low SIO1/NET* output at pin 12. (Refer to paragraph 3-4.2.1.3f for a U9 description.) Next, microprocessor U31 sets its address lines A1 thru A4 to address the U44 transmit register associated with its TxDA output. Next U31 writes eight bits of character data on the data bus to this register by setting it R/W* output at pin 9 low. The R/W* signal is then ORed via U5D with the active low AS* signal from U31, pin 6, creating the active low WR* signal. On the falling edge of the WR* signal data is serially transmitted from the TxDA output at pin 33. The clock rate of the data transmission is determined by 3.6864-MHz oscillator, Y2. Transmit data is amplified by U45 and output at A1A1J1, pin 5 to the IOC board (A2). U44's TxDB output at pin 13 is used for network communications. This feature is not used in the R-2541/B Barracuda Receiver Set.

When receiving, U44 looks for a high-to-low transition of the start bit on pin 35 (RxDA). If a transition is detected, the start bit is tested for validity. If a valid start bit is detected, the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits have been assembled and one stop bit has been detected. The least significant data bit is received first. The data is then transferred into the U44 receive register associated with the RXDA pin 35 input and the active-low SIO1RX* line is asserted. U11 accords the SIO1RX* interrupt the highest priority of all interrupts including the SIO1TX* interrupt discussed above. When the SIO1RX* interrupt is received, U11's pin 9 output goes high and its pin 6 and 7 outputs go low. Microprocessor U31 services the interrupt by setting its R/W* output at pin 9 high. This logic is inverted by U8C and ORed with the AS* signal from U31 via U4B. U4B generates the active low RD* signal received at U44, pin 10. U31 also sets its address bus lines A1 thru A4 to address the receive register associated with the RxDA input. On the falling edge of the RD* signal, U44 places eight bits of buffered data on the data bus.

3-4.2.1.2 Keyboard Interface Section. The Keyboard Interface section (Figure FO-3) encodes the front panel's 26 push button keys, the Tuning Wheel, and the Parameter Adjust knob.

The 26 push button keys, whose interface to the Front Panel Controller is schematically depicted in Figure 3-3, is organized as a matrix of rows and columns. Each push button represents an intersection in the matrix. Switch closure is sensed and encoded by Key Encoder U22 and three-input AND gate U17B. Table 3-1 represents the truth table associated with the keyboard encoding process.

U22 continually scans the 26 keys at a nominal 500 Hz rate. This scan rate is determined by the value of C24. When no key is pressed, U22's row inputs (X1 thru X4) are high and its column outputs (Y1 thru Y4) are sequentially output as a logic "0" so that any given column output is active 25 percent of the time. AND gate U17B sees three logic highs at its inputs due to the presence of +5 Vdc through pull-down resistors R122, R130, and R121. This voltage also acts to reverse-bias diodes CR8 thru CR10, allowing the AY1-AY3 inputs to be isolated from the Y1 thru Y4 column outputs.

When a keypad key is pressed, the up arrow key (Δ), for example, the X1 output goes low, but nothing happens until it is scanned by the Y1 column output going low. The low X1/Y1 combination disables the internal scan counter, initiates an internal key bounce timer (whose nominal duration of 50 ms is determined by the value of C25), and locks out other Y inputs. Once the bounce clock times out without switch bounce, U22 latches out the key encode data at pins 14 thru 17 and sets its Data Available (DA) output at pin 12 high. During keypad closure, logic highs are seen at all three inputs of AND gate U17B, placing a logic high on the D

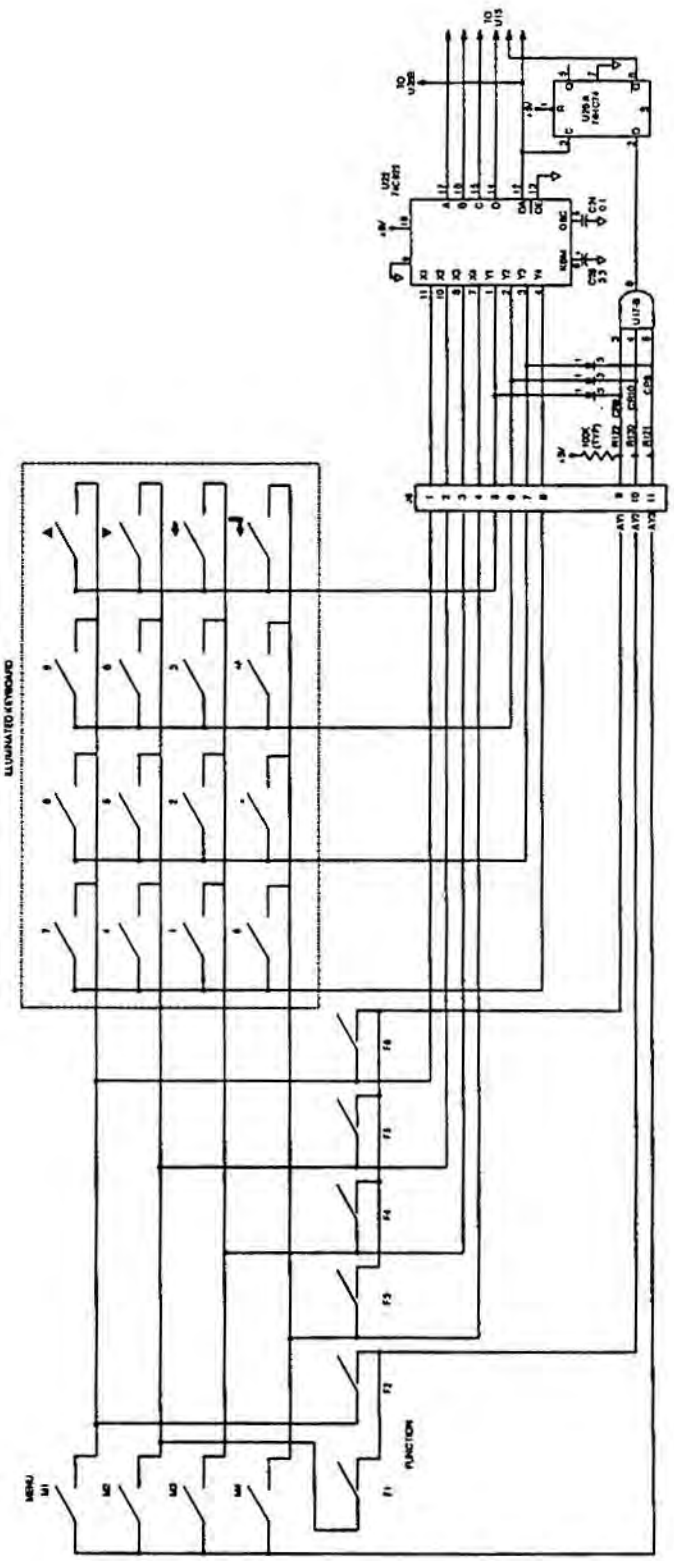


Figure 3-3. Keyboard Encoding Schematic Diagram

input of flip-flop, U26A. The DA output is fed to data latch U15 with the encode data, but it also serves two additional functions. First it clocks D-type flip flop U26A, allowing the data at its D input to be latched. U26A's Q-not output is fed to U15 along with other encode data. The DA output also feeds the clock input of U26B, which is used to raise an interrupt to the microprocessor.

When one of the MENU or FUNCTION keys is pressed, key encoding varies slightly. For example, if the F6 key is pressed, the +5 Vdc associated with R122 is pulled low, eliminating the reverse bias on CR9. This allows a low impedance path to the Y1 column output, which senses the switch closure in the X1 row. Key encoding is identical to that described above except that AND gate U17B now outputs a logic low, allowing a means to differentiate the up arrow key closure from the F6 key closure.

When U22 raises the DA line, this line clocks U26B, placing a low at AND gate U17C, pin 10. The low output at U17C, pin 8, raises an interrupt to the microprocessor through U11. Refer to paragraph 3-4.2.1.3d for a U11 description. When the microprocessor services the interrupt, it asserts U10's active-low KEYS* pin 10 output which enables U15 to put the data available on the data bus. Refer to paragraph 3-4.2.1.3f for a U10 description.

Similarly, inputs from the Tuning Wheel Encoder and the Parameter ADJ switch, S2, cause interrupts to be generated. As the ADJ. control is rotated, S2-pins 1 and 3 momentarily pulse low, with these signals being routed through the de-bounce correction IC U13. The output at U13-pin 15, is the data input to D-Type flip-flop U25B. The clock signal for U25B is supplied by the de-bounce IC U13-pin 2, via inverter U8B. This output at U8B-pin 4 also supplies the clock input for D-Type flip-flop U24B. The toggling of U24B-pin 8 from a high to low state produces the interrupt at U11-pin 11 via AND gate U17C. Additionally, as the tuning wheel is adjusted, the high to low transition at J7-pin 2 supplies the clock signal to U24A. The toggling of U24A-pin 6 from a high to low state also produces an interrupt signal at U11-pin 11 via AND gate U17C.

U24A, U24B, and U26B are used with U16 to provide the microprocessor with the respective ability to mask interrupts from the Tuning Wheel Encoder, the Parameter ADJ switch, and the Keyboard. U24A, U24B, and U26B receive a clocking signal that indicates a request for interrupt. If the microprocessor wants to mask the interrupt from a specific area of the keyboard/ tuning wheel/ADJ switch, it can write a zero into U16 at the location that corresponds to the interrupt; otherwise, it writes a logic high to the U16D input. For example, if the microprocessor doesn't want to service interrupts from the keyboard, it can write a zero in Data Bit 0 in U16, clock it in by writing to address 7 (111 on A1-A3) to 3-to-8 address decoder U23. Thus, when the DA line clocks U26B, the Not-Q output will remain high and U17C will output a high to U11, not generating an interrupt. For a discussion of U11 or U10 operations, see paragraphs 3-4.2.1.3d or f, respectively.

TABLE 3-1. Keypad Encoding

Key	U22-17	U22-16	U22-15	U22-14	U17B
▲	0	0	0	0	1
▼	1	0	0	0	1
←	0	1	0	0	1
↵	1	1	0	0	1
9	0	0	1	0	1
6	1	0	1	0	1
3	0	1	1	0	1
+/-	1	1	1	0	1
8	0	0	0	1	1
5	1	0	0	1	1
2	0	1	0	1	1
•	1	1	0	1	1
7	0	0	1	1	1
4	1	0	1	1	1
1	0	1	1	1	1
0	1	1	1	1	1
F6	0	0	0	0	0
F5	1	0	0	0	0
F4	0	1	0	0	0
F3	1	1	0	0	0
F2	0	0	1	0	0
F1	1	0	1	0	0
M1	0	0	0	1	0
M2	1	0	0	1	0
M3	0	1	0	1	0
M4	1	1	0	1	0

3-4.2.1.3 Microprocessor and Memory Section. The Microprocessor and Memory section of the Front Panel Controller Assembly performs the task of monitoring and controlling the circuits of the Front Panel. See Figures 3-2 and FO-3. The Microprocessor and Memory section consists of the microprocessor, U31; EPROMs U28 and U29; Static RAMs, U36 and U37; the Power Fail circuit, U34, Q1, Q2, and Q3; the Interrupt Control circuit, U11; and the Data Transfer Control Circuit, U3.

a. Microprocessor. A Motorola MC68HC000 Microprocessing Unit (U31) communicates with other circuits in the assembly via a 23-bit address bus and a 16-bit bidirectional data bus. The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals that it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the peripheral device. During a read cycle, the processor receives data from either the memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both upper and lower bytes simultaneously by asserting both upper and lower data strobes (UDS*, AND LDS*). When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when A0 equals zero, UDS* is issued. When A0 is one, LDS* is issued. When the data is received, the processor correctly positions it internally.

During a write cycle, the processor sends data to either the memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe for that byte. For byte operations, when A0 equals zero, UDS* is issued. When A0 is one, LDS* is issued.

The microprocessor uses five signals for asynchronous bus control, i.e., AS*, R/W*, UDS*, LDS*, and DTACK*. The Address Strobe, AS*, indicates a valid address present on the address bus. The Read/Write signal, R/W*, defines the data bus transfer as a read or write cycle. The Data Transfer Acknowledge, DTACK*, is an input signal that indicates that a data transfer is complete. When the microprocessor recognizes the DTACK* signal during a read cycle, data is latched and the bus cycle is terminated. When DTACK* is recognized during a write cycle, the bus cycle is terminated.

Three inputs to the microprocessor (IPL0*, IPL1*, and IPL2*) indicate the encoded priority level of the device requesting an interrupt. Level 7 is the highest priority; whereas level 0 indicates that no interrupts are requested. Level 7 cannot be masked. The least significant bit is IPL0*, and the most significant is IPL2*. These lines must remain stable until the processor signals interrupt acknowledge (FC0-FC2 are all high) to ensure the interrupt is recognized.

Reset (RESET*) is a bidirectional signal that resets (starts a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (RESET instruction) causes all external devices to be reset, but the internal state of the microprocessor is not affected. A total system reset is the result of external HALT* and RESET* signals applied simultaneously.

HALT* is a bidirectional signal that, when driven by a external device, causes the processor to stop at the completion of the current bus cycle. When the processor is halted using this input, all control signals are inactive and all tri-state lines are put in their high impedance state. When the processor stops executing instructions (as in a double bus fault), the processor drives the HALT* line to indicate to external devices that the processor has stopped.

The processor status lines (FC0, FC1, and FC2) indicate the state (user or supervisor) and the cycle type currently being executed. The information indicated by the function code outputs is valid whenever AS* is active. In the WJ-9902-2 configuration, only the presence of the interrupt acknowledge (FC0-FC2 all ones) is of any significance.

b. Memory Section. The EPROMs U28 and U29 provide the system software for the operation of the receiver controller. For the microprocessor to read data from the EPROMS, the R/W* line at U31-pin 9 is toggled high. This high is buffered and inverted by U8C, supplying a logic low to the pin 24 Output Enable (OE) inputs of U28 and U29. A logic level low Chip Enable (CE) is supplied to the EPROMS via AND gate U7C. The static RAMs, U36 and U37, store current parameters for use during operation. The OE signal supplied to the EPROMS is also routed to the static RAMS. U36's Write Enable (WE*) input is the ORed combination of the microprocessor's R/W* and UDS*/LDS* signals via U4A. Similarly, U37's WE* input is derived from the ORed comvbination (via U4C) of the mircoprocessor's R/W* and LDS* signals. The Chip Enable signal for the static RAMS (RAM*) is provided by 3-to-8 line decoder U9-pin 13 via tansistor Q1. (See paragraph 3-4.2.1.3 for a U9 description.)

c. Power Fail Circuit. The Power Supply monitor circuit, U34, monitors the +5 volt supply and when the supply voltage falls below a nominal +4.3 volts, it asserts the RES* signal which resets the microprocessor. Included in this section is the memory protect circuit composed of Q1, Q2, and Q3. Q1 protects the RAM circuits during power up by preventing a spurious RAM select signal, RAM*, attempting to select either U36 or U37. The presence of CR13 prevents Q1 from conducting until the +5 volt supply is at full voltage and the microprocessor is up and running. Additionally, when the RESET* goes low, CR7 ensures that Q1 is turned off as quickly as possible. Zener diode VR1, Q2 and Q3 ensure that if the Vcc voltage of the RAM circuits is not present that the memory is held intact by the battery BT1. Under normal operations the +5 Vdc is applied to the cathode of zener diode VR1, producing a voltage of 3.3 Vdc. This 3.3 Vdc turns on transistor Q2, allowing Q3 to provide Vcc to the static RAMs U36 and U37. If the +5 Vdc becomes too low for VR1 to provide the required 3.3 volts, Q2 is turned off along with Q3, applying the +2.8 Vdc from battery BT1 and associated circuitry to the static RAMs for memory retention.

d. Interrupt Control Circuit. The 10-4 decoder, U11, decodes the active-low interrupts from the peripheral devices and prioritizes the interrupts being requested. For example, a receive interrupt (SIO1RX*) from the DUART U44 has the highest priority (six). Similarly, a transmit interrupt has a priority of five, and a keyboard interrupt has a priority of one. Other interrupts are not used. TP13 provides a means to test U11 operations. Placing an active low on TP13 results in an active high output at U11, pin 14, and active low outputs at U11, pins 6, 7, and 9. These logic levels will be present regardless of other active interrupts. Table 3-2 depicts the functional operation of U11.

TABLE 3-2. U11 Interrupt Processor Output Functions

Interrupt	Priority	Input	A U11-9	B U11-7	C U11-6	D U11-14
TP13	7th (Highest)	U11-4	0	0	0	1
SIO1RX*	6th	U11-3	1	0	0	1
SIO1TX*	5th	U11-2	0	1	0	1
Front Panel	1st (Lowest)	U11-11	0	1	1	1

e. Data Transfer Control. Some peripherals such as memory devices can transfer data in a much shorter time than other peripherals such as the display and the DUART. U3 controls the rate at which data transfer takes place. When the processor asserts the Address line A23 high, then the counter, U3, starts the count at 14 and one clock cycle later (15), U3 asserts the Carry output (pin 15). This disables the counter and asserts the active-low DTACK* signal via inverter U2B. If the peripheral being accessed is a slow transfer type, then the processor puts A23 low and U3 starts counting at four. Eleven clock cycles later, the counter reaches 15 and asserts the DTACK* signal. An interrupt acknowledge clears U3.

f. Address Decoders (U9, U10, and U23). Address Decoders U9, U10, and U23 are identical 3-to-8 decoders that provide a single active-low output in accordance with the inputs received at its pin 1 thru pin 3 (A0-A2) inputs, where A0 represents the least significant bit and A2 is the most significant bit. For example, when the input logic is all zeroes, then the address decoder's Y0 output at pin 15 goes low. All other outputs are set to a logic high. Each address decoder is enabled by the combination of high logic at its pin 6 input and low gating logic at its pin 4 and 5 inputs.

The Real-time Clock, U1, is not used in the WJ-9902-2 configuration.

3-4.2.1.4 Display Interface Section. The Display Interface section consists of a HD61830 Dot Matrix Liquid Crystal Graphic Display Controller (U27) and an 8K by 8-bit RAM (U35). The display operates only in the alphanumeric mode. The characters are displayed by storing character codes in the RAM and developing them into dot patterns with the internal character generator ROM.

The microprocessor enables U27 through U9 with the active-low LCD* signal. When the microprocessor needs to write a character for display, it asserts the R/W* low at U27-Pin 17, and puts the character code on the parallel data bus. U27 writes the character code into U35 and when the microprocessor asserts the ELCD signal, transmits the dot pattern for the character to the display through J5. The signal outputs at J5, pins 1 through 5, are identified as follows:

J5-pin 1 (D) is the display data serial output for the LCD display.

J5-pin 2 (FLM) provides the frame signal for display synchronization.

J5-pin 3 (M) converts liquid crystal driving signals into AC when the display driver is in the alphanumeric display mode.

J5-pin 4 (CL1) provides the display data latch signal for the LCD drivers.

J5-pin 5 (CL2) provides the display data shift clock for the LCD drivers.

U27's input and output signals can be grouped into four categories. The first group consists of control inputs and outputs. They include one output, WE*, and five inputs, RES*, CS*, E, R/W*, and RS, see **Table 3-3.** (Note that an asterisk indicates an active-low condition.) the inputs and outputs of U27 are all at CMOS logic levels.

The second group, DB0 thru DB7, is the 8-bit data word from the system DATA bus, DATA00 thru DATA07.

The third group, MA0 thru MA11 is display memory address data to and from the external RAM, U35.

The final group MD0 thru MD7 is the 8-bit RAM data from U35. The external character generator ROM, U14, is not used in this application. Thus, data lines RD0 thru RD7 and address lines MA12 thru MA15 are also not used.

TABLE 3-3. U27 Control Inputs and Outputs

Pin Desig./No.	I/O	Function
WE*/13	O	Write Enable - Allows data to be written to U35.
RES*/14	I	Reset - Low sets display to OFF.
CS*/15	I	Chip Select - Enabled when low.
E/16	I	Enable - Data is written on the falling edge. Data can be read when E is high.
R/W*/17	I	Read/Write - Data is written to the system DATA bus when high, read from the DATA bus when low.
RS/18	I	Register Select - Instruction Register selected when high. Data register when low.

U35 is configured for memory read unless the /WE line from U27 is low. In the read mode, wheever a memory address is passed to U35 from U27, MA0 thru MA11, the 8-bit data word at that address is placed on the data bus and passed to U27, MD0 thru MD7. When /WE is low, the data at U35, pins 11 thru 19 (D0-D7) is written to the memory location indicated through pins 10 thru 3 and 25, 24, 21, and 23 (A0-A11).

3-4.2.1.5 Audio Amplifier Section. The Audio Amplifier section enables the microprocessor to select an audio input from a receiver and direct it through a series of amplifiers to a specific output. In the Barracuda Receiver Set, audio from Receiver A is input to pin 2 of J2 and Receiver B audio is input to J2-pin 8. Once selected, these audio signals are amplified, routed through the front panel Level Control knob, amplified again and output to the phone jack, J10.

Receiver A audio is input to pin 2 of U41, a quad single-pole single-throw switch, that connects Receiver A audio to the Front Panel Controller audio amplifier circuitry whenever the Receiver A (Device 1) audio output is selected for monitoring at the WJ-9902-2 headphone jack. All control lines for U41 are supplied by octal D-Type flip-flop U43. For front panel audio of Receiver A, a high is applied to U41-pin 1 by U43 closing the switch between U41-pins 2 and 3. The audio signal is then routed to amplifier U40A (a J-FET input operational amplifier). The output of U40A at pin 1 is approximately 4.5 Vpp for an AM modulated signal (modulation frequency 1 kHz/50%) with the receiver AGC set to normal. The audio output of U40A is then routed to the WJ-9902-2 front panel LEVEL control potentiometer R2 via J9-pin 1 (left channel audio level control) and returned to the Front Panel Controller via J9-pin 2. Refer to Figure FO-2 for a schematic detail of audio leveling by R2.

The audio signal at J9-pin 2 is supplied to amplifier U46 via R45 and C41. U46 provides a fixed gain of approximately 22, as determined by resistors R115 and R116. The audio output at U46-pin 1 is capacitively coupled to the left channel headphone jack J10 via capacitors C45, C46, and C66.

Audio outputs for Receiver B are supplied by an identical circuit as described above via quad switch U42, amplifier U40B, the front panel LEVEL control potentiometer R2, and amplifier U39. Receiver B audio is supplied to the right channel headphone jack J10 via capacitors C52, C53, and C69

The +12 Vdc, required by U39 thru U42 and U46, is provided by J2-pin 1. The DC-DC Converter U21 accepts the +12 Vdc from J2-pin 1 and creates the -12 Vdc required by U40, U41, and U42. The +5 Vdc voltage regulator U6 receives +12 Vdc via rectifier diodes CR1 through CR3 and filter capacitor C4. The +5 Vdc output of U6 is then filtered by capacitor C75 and supplied to U43.

3-4.2.2 LCD Assembly-Type 282524-1 (A1A1U1). The Liquid Crystal Display (LCD) Assembly is a 240 by 64 dot graphic and alphanumeric display with back lighting.

3-4.2.3 Keyboard-Type 481657 (A1A1U2). The keyboard consists of a shielded, backlit panel with embossed keys for softkeys, and an illuminated 16-key keypad. The Keyboard plugs into A1A1J6 on the Front Panel Controller Assembly. Refer to paragraph 3-4.2.1.2 for further details.

3-4.2.4 Tuning Wheel Encoder Assembly-Type 282520-1 (A1A1U3). The Tuning Wheel Encoder Assembly plugs into A1A1J7 of the Front Panel Controller Assembly and can be turned continuously in either direction to control frequency subfunctions on the display. See paragraph 3-4.2.1.2 for further details.

3-5 WJ-9902/488 IEEE-488 Remote Interface Section (A2), DETAILED FUNCTIONAL DESCRIPTION.

The WJ-9902/488 Host Interface Section (IOC) provides the interface between the FPU Section (FPU) and the WJ-8607-88-4 Receivers. The IOC converts the RS-232C output from the FPU into HPIL format for transmittal to the receivers, and converts status information and data from the receivers from HPIL to RS-232 for use and display by the FPU. Although the IOC enables the FPU to communicate over the IEEE-488 bus and to control receivers over the WJ-Net, these options are not used in the WJ-8907 Receiver Set. The IOC comprises a Microprocessor and Memory section, a Front Panel Interface section, a HPIL Interface section, an IEEE-488 Interface section, and a WJ-Net Interface section (refer to Figure 3-4 and FO-4).

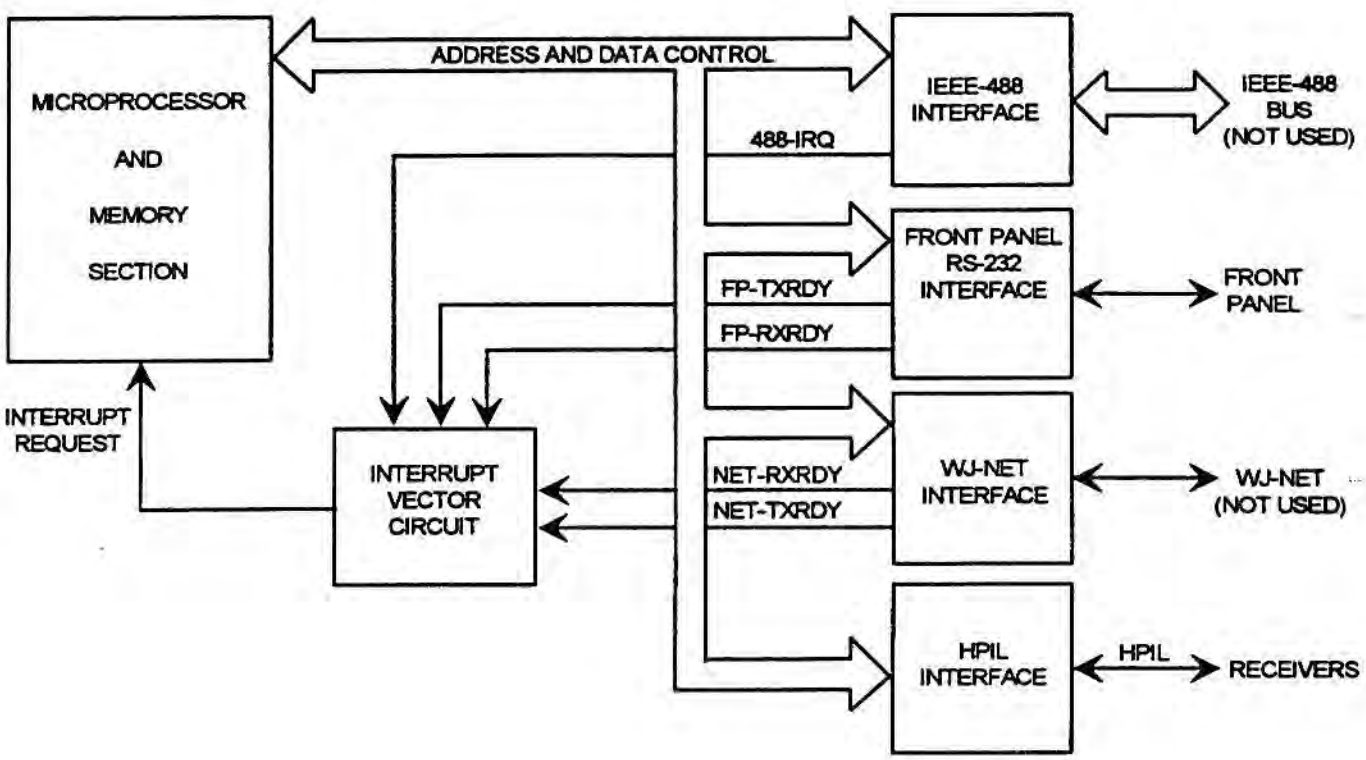


FIGURE 3-4. WJ-9902-2/488 Host Interface Functional Block Diagram

3-5.1 Microprocessor and Memory Section. The Microprocessor and Memory section controls the communications through the IOC by servicing interrupts from each of the communications interfaces. When an interrupt occurs, the interrupt control circuit provides an interrupt vector address in memory to the microprocessor. The microprocessor accesses memory at that address to service the interrupt. Typically, the FPU sends a byte of serial data to the IOC preceded by a start bit, and followed by a predetermined number of stop bits. The Front Panel Interface stores the data and raises the FP-RXRDY interrupt. The Microprocessor then tells the Front Panel Interface to put the data on the data bus. The Microprocessor enables the HPIL Interface and the data is stored by the HPIL Interface for transmission to the receivers. In the opposite direction, the Microprocessor enables the HPIL interface for receiving, and when the receiver sends status or data to the FPU, the HPIL interface converts the serial data to parallel, stores it, and puts it on the parallel data bus for transmit to the FPU interface. When the transmit buffer of the FPU interface is empty, the FPU interface raises the FP-TXRDY interrupt to the microprocessor and the microprocessor directs the FPU interface to store the data to be transmitted to the FPU. The FPU interface then converts the parallel data to serial data by transmitting one bit at a time to the FPU, least significant bit first.

The Microprocessor and Memory Section consists of the Microprocessor, U1, the EPROM, U18, and the RAM, U23. Also included in this section is the interrupt control circuitry of U6, U7, U8, U19, U20, U9, U10, U11, U12, U13, U14, U15, U16, and U17.

The microprocessor's 16-bit address bus and 3-to-8 line decoder U26 generate the active-low, Computer Operating Properly (COP*) signal on a regular timely basis to provide a means of error detection in the event of malfunction. The high-to-low transition of the COP* signal puts a positive square-wave pulse on the Q output of U2B, pin 5, with a pulse width of 6.8 seconds. If the microprocessor does not send this signal within 6.8 seconds, pin 5 goes to ground and the error LED, DS1, lights. The COP* signal is also used to feed the Watchdog Input, WDI, of the Power Supply Monitor Circuit, U3. If the microprocessor fails to generate the COP* signal within the proper time limit, U3 will generate a P-FAIL* signal and reset the microprocessor, even though there has been no failure of the +5 volt supply.

Should the +5 volt supply fall below +2.3 volts, U3 generates the P-FAIL signal which resets the microprocessor, the communications DUART, U27, the octal D-Type Flip-Flop U33, and the HPIL Interface IC U34.

Some of the peripherals of the microprocessor require more time to process an interrupt than others, so the microprocessor generates the SLOW-I/O* or the FAST-I/O* signal depending on which type of interrupt requires servicing. The microprocessor puts an address on the upper eight bits of the address bus of 01100000, which is decoded by comparator U4 as P=Q*. Depending on which type of interrupt is being serviced, fast or slow, bit 07 is set or clear, respectively.

Generating the SLOW-I/O* signal causes the one-shot, U2A, to hold the MRDY of the microprocessor low which allows stretching the E and Q signals to extend data-access time. When MRDY is low, E and Q may be stretched in integral multiples of one-half bus cycles, thus allowing slower processing of interrupts.

When an interrupt occurs, an interrupt line is asserted (e.g., FP-RXRDY) and the address associated with the interrupt is decoded by the combination of quad OR gates U9, U10, U13, U14, and 8-to-3 line encoders U15 and U16. U16 asserts the active-low IRQ* signal via inverter U5D to the microprocessor U1-pin 3. The microprocessor responds with the VECTOR-LATCH* signal which is sent to the pin 1 Output Enable (OE) input of octal latch, U21. The interrupt vector address is then available on the ADDRESS-MUX bus. This interrupt vector address is a location in RAM which holds the address of the program counter, a location in ROM, which will service the interrupt.

The DUART, U27, produces a programmable counter signal which is used by the software in the microprocessor as a software clock. This signal is accessed through the Fast Interrupt Request input, FIRQ* U1-pin 4, and is enabled when the COUNT-FIRQMASK signal is low at OR gate U8D-pin 13.

3-5.2 FPU Interface Section. The FPU Interface section consists of a receiver/driver module (U30) and an asynchronous receiver/transmitter (half of a Dual Asynchronous Receiver Transmitter - DUART) (U27). As a driver, U30 takes the nominal +5 volt TTL of U27 and converts it to the ±10 volts of the RS-232 standard. As a receiver, it takes the ±5 to ±15 volt input from the RS-232 FPU input and converts it to the +5 volt TTL used by the circuitry of the IOC.

When acting as a receiver, U27 looks for a high-to-low transition of the start bit on pin 35 (RxDA). If a transition is detected, the start bit is tested for validity. If a valid start bit is detected, the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits have been assembled and one stop bit has been detected. The least significant data bit is received first. The data is then transferred into the Receive Holding Register (RHR) and the active-low FP-RXRDY* line is asserted. When the microprocessor services the interrupt, it asserts the active-low E.RD* line and puts the address of the RHR on the address bus. U27 responds by putting the one character from the RHR on the data bus.

When acting as a transmitter, U27 indicates to the microprocessor that it is ready to accept a character for transmission by raising an interrupt on the active-low FP-TXRDY* line (U27-pin 29). Upon servicing the interrupt, the microprocessor loads eight bits on the data bus, enables U27 by raising the FP/NET* line and asserting the active-low E.WR* line, sets the address lines to that of the Transmit Holding Register (THR), and U27 loads the character. Data is transmitted from the THR to the transmit shift register when the transmitter has completed transmission of the previous character. The transmitter converts the parallel data from the microprocessor to a serial bit stream that it outputs on the TxDA output (U27-pin 33). This output is amplified by U30 for output to the front panel.

3-5.3 HPIL Interface Section. The HPIL Interface Section, under control of the microprocessor, converts the parallel data on the internal data bus to serial data for transmittal on the HP Interface Loop (HPIL). The HPIL Interface also converts the serial data input from the HPIL to parallel data for the internal data bus. If the transmit buffer on U34 (the HPIL interface IC) is empty, U34 raises an interrupt to the microprocessor (HPIL-IRQ*, U34-pin 2). When enabled by the microprocessor asserting an active-low E.WR* signal at U34-pin 27, U34

buffers the parallel data from the data bus and then transmits the data to the HPIL by passing it through the hybrid transformer, T1, to the HPIL. T1, in conjunction with capacitors C41 through C44, resistors R51 and R54 through R56, and zener diodes VR1 thru VR4, provide the necessary isolation and voltage conversion from HPIL levels to integrated circuit logic levels. When data is input from the HPIL, U34 buffers the data received via transformer T1, and raises the HPIL interrupt. When enabled by the microprocessor (E.RD*), U34 outputs the data in parallel to the data bus. Additionally, capacitor C58 and inductor L1 provide external frequency control for U34's internal oscillator.

3-5.4 IEEE-488 Interface Section. (Not used in the R-2541/B.) The IEEE-488 Interface provides both talk and listen capabilities between the WJ-9902-2 and an external controller, transferring data in a bit-parallel, byte-serial form. Sixteen interconnecting lines plus eight ground and shield lines form the interface. The sixteen interconnecting lines consist of eight bi-directional data bus lines, three data byte transfer lines, and five bus management lines. The IEEE-488 Interface section translates the +5 volt TTL data on the parallel data bus into the negative logic (>+2 volts = logic 0; < 0.8 volts = logic 1) of the IEEE-488 standard bus. Transceiver U43 transfers data or address (command) information between the WJ-9902-2 and the external controller using the eight data bus lines (DI01-DIO8). The three data byte transfer lines (DAV, NRFD, and NDAC) indicate the availability and validity of the information on the data bus lines, the readiness of the listening device to accept data, and whether the data has been accepted. Four of the five interface management lines (ATN, SRQ, IFC, and EOI) indicate whether the data bus is carrying data or address information, to request service, to clear the interface, and to indicate the end of a transfer sequence. The fifth line (REN) is not used. Transceiver U44 drives or receives these eight data transfer and management lines.

This interface permits the WJ-9902-2 to talk or to listen when commanded by a controller. The WJ-9902-2 can also initiate a SRQ to the controller and reply to the controller's serial poll, and can respond to SDC (Selected Device Clear) and DCL (Universal Device Clear). Also, the WJ-9902-2 can pass information to and from the Miniceptor via the extended talk and listen capabilities.

3-5.5 WJ-Net Interface Section. (Not used in the R-2541/B.) The WJ-Net Interface section consists of a receiver/driver module (U29) and an asynchronous receiver/transmitter (U27). As a driver, the receiver/driver receives the active-high 485-TALK signal at U29-pin 3 and converts the nominal +5 volt TTL of the receiver/transmitter it to the -10 to +15 volts of the RS-485 standard. As a receiver U29-pin 2 is held low by the 485-LISTEN* signal; it then takes the -10 to +15 volt input from the RS-485 input and converts it to the +5 volt TTL used by the circuitry of the IOC. When acting as a receiver Dual Asynchronous Receiver Transmitter (DUART) U27, which is shared with the FPU interface, converts the serial data from the WJ-Net into parallel data and stores it in the DUART buffer. The DUART then raises the NET-RXRDY interrupt and, when appropriate, the microprocessor causes the DUART to put the data on the parallel bus.

When acting as a transmitter, if its transmit buffer is empty, the DUART generates the NET-TXRDY interrupt and, when appropriate, the microprocessor enables the DUART to store the data that is on the parallel bus in the DUART's transmit buffer. The DUART then transmits the data to the WJ-NET in serial fashion, placing a start bit first, then transmitting the data one bit at time, and closing with a predetermined number of stop bits.

CHAPTER 4

MAINTENANCE

4-1 GENERAL.

Depot level maintenance of the WJ-9902-2 Receiver Controller comprises troubleshooting and fault isolation of an individual assembly or printed circuit board down to the component level and subsequent repair by replacing the faulty component. Figure 4-1 details the sequence of events that should take place during corrective maintenance. Hence, organization of this section consists of paragraphs detailing performance tests that determine whether the suspect assembly is performing properly, removal and replacement procedures as an aid to troubleshooting, followed by a troubleshooting table with subparagraphs on fault isolation procedures. For WJ-9902-2 performance tests, refer to the WJ-9902-2 Organizational Maintenance Manual.

4-2 REQUIRED TEST EQUIPMENT AND TOOLS.

The test equipment and tools listed in Table 4-1, or equivalent equipment, is required to perform the following performance tests and troubleshooting procedures.

TABLE 4-1. Test Equipment Required

SCAT No.	Equipment	NSN/NICN CAGE/P/N
4207	Oscilloscope Tektronix Model 2465B	6625-01-213-9354 80009-2465B-11
N/A	Flat Blade Screwdriver	N/A
N/A	#2 Phillips Screwdriver	N/A
N/A	6" Adjustable Open end Wrench	N/A
N/A	ESM Maintenance Kit	N/A
N/A	Test Bed - "Known-good" WJ-9902-2 with a "known-good" WJ-8607-88-4 Receiver	N/A
N/A	Test Cable A	See Figure 4-2
N/A	Test Cable B	See Figure 4-2

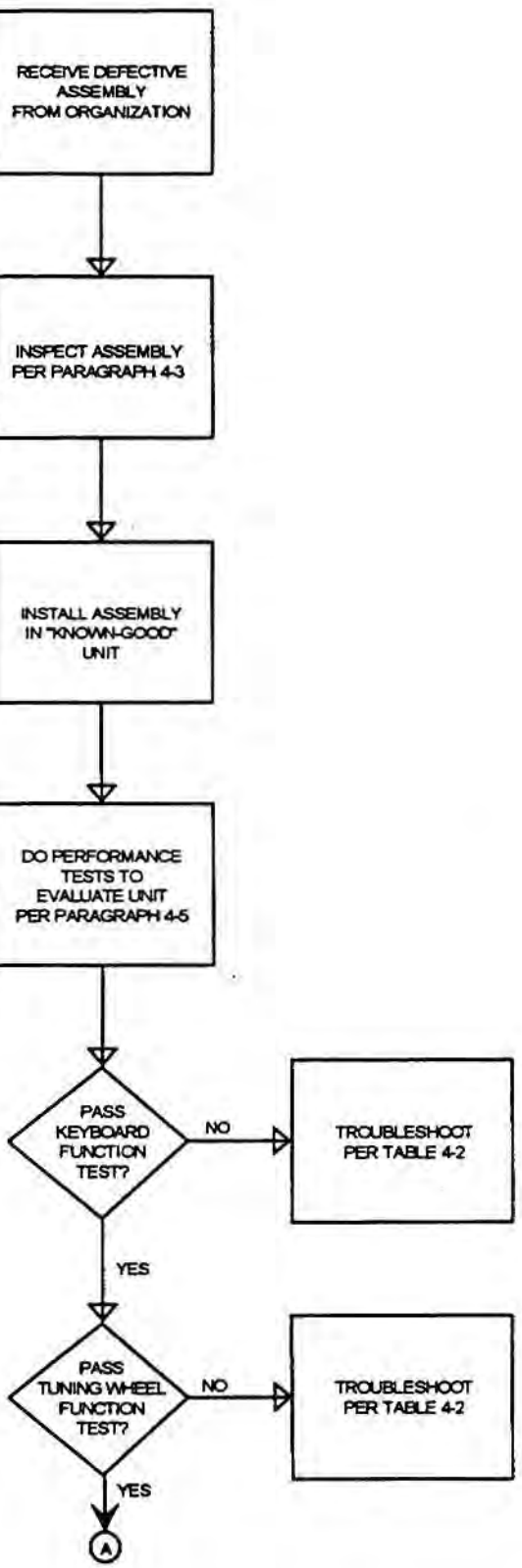


FIGURE 4-1. Corrective Maintenance Flow Chart

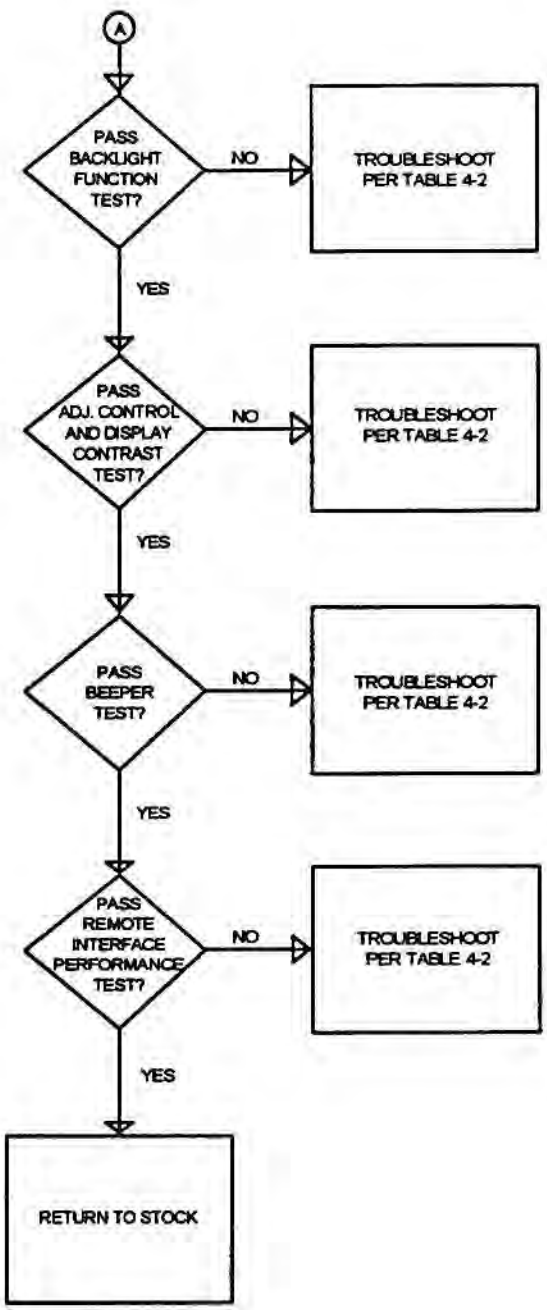


FIGURE 4-1. Corrective Maintenance Flow Chart-CONT

4-2.1 Use of Test Fixtures. The procedures detailed below presume the use of a "known-good" WJ-9902-2 Receiver Controller with at least one "known-good" WJ-8607-88-4 VHF/UHF Receiver as a test fixture. The only parts designated to be repaired at the depot are the LCD Display (282524-1), the Front Panel Controller PC Assembly (796856-2), and the Remote Interface PC Assembly (796896-1). If one of these assemblies is returned to the depot for repair, it should be installed into the "known-good" Receiver Controller, performance tests run to establish the area of malfunction, and then troubleshooting procedures performed to localize the defective component.

4-2.1.1 Test Cables A and B. The Test Cables A and B, shown in Figure 4-2, are not commercially available products and must be built by the service technician to perform the troubleshooting and fault isolation procedures described below.

4-3. VISUAL INSPECTIONS.

A visual inspection must be performed to check the overall appearance of the returned assembly (unit under test (UUT)) before any electrical tests are performed. Perform a complete visual inspection and correct all discrepancies before proceeding to any electrical test. A complete visual inspection includes the following:

a. Check for broken or damaged components.

b. Check that all conductors, cables, and terminals are soldered.

c. Check for loose or broken hardware, such as screws, rivets, and connectors.

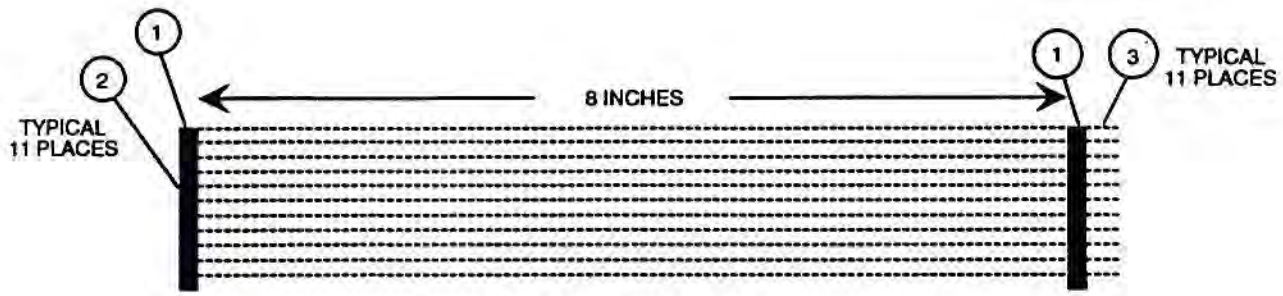
d. Check for charred or burnt printed circuit runs.

4-4. ASSEMBLY REMOVAL AND REPLACEMENT PROCEDURES.

After inspecting the returned assembly, and determining that the assembly should be tested electrically, perform the procedures in the following paragraphs for installation of the assembly in the "known-good" unit.

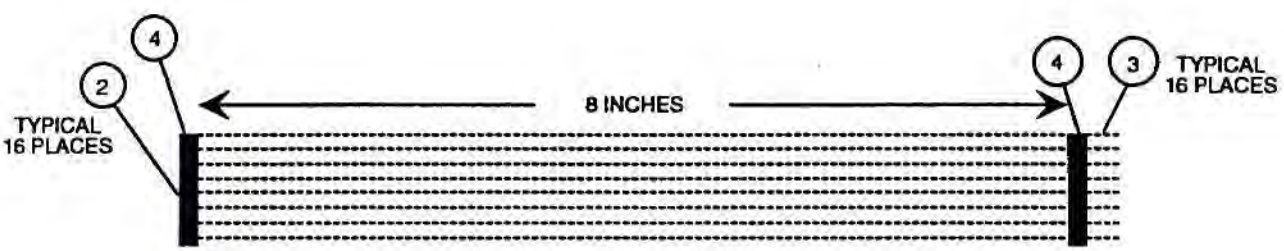
WARNING

Electrical shock hazard to personnel exists when the receiver controller is opened while powered-up. Ensure that the controller is turned off and external power is disconnected from the rear panel's 120/230 VAC connector, prior to opening the controller.



TEST CABLE A SIDE VIEW

TEST CABLE A TOP VIEW



TEST CABLE B SIDE VIEW

TEST CABLE B TOP VIEW

PARTS LIST

ITEMNO.	DESCRIPTION	PART NUMBER
1	Housing, 11 Position, Single Row, 0.100 Ctr	2-87499-0
2	Contact, Crimp, Female	87046-1
3	Contact, Crimp,Male	102107-1
4	Housing, 16 Position, Double Row, 0.100 Ctr	3-87499-3

Manufacturer is AMP Inc. (CAGEC-00779)
2800 Fulling Mill RD.
P.O. Box 3608
Middletown, PA 17105-3608

FIGURE 4-2. Test Cable Construction

WARNING

This unit contains a lithium battery as backup power for memory retention. Extreme care should be used in storage, handling, and disposal of lithium batteries. Improper handling may present an explosion hazard.

- Always wear eye protection when handling batteries.
- Do not puncture, compact, incinerate, short circuit, or expose to temperatures above 160°F (71°C).
- Do not expose batteries to charging currents.
- Do not store loose batteries in bins. Always store in original containers.
- Dispose of batteries properly. Discharged cells should be handled with care, as they retain significant energy. They should be electrically isolated and packaged for disposal. Dispose in accordance with local regulations for hazardous material disposal. DO NOT INCINERATE OR COMPACT.

CAUTION

This equipment contains assemblies subject to damage by static electricity. Use approved grounding procedures before touching, removing, or replacing assemblies or components.

4-4.1 Installation of Assembly in "Known-Good" Unit. Install returned assembly (UUT) in known-good unit as follows:

a. Ensure that power is removed from the WJ-9902-2 Receiver Controller.

b. Remove the two captive screws at the back of the WJ-9902-2 top cover.

c. Slide the cover towards rear of unit. Pull the cover up and off.

d. Repeat procedure b and c to remove the bottom cover.

e. Verify that the fuseholder contains a 1.0 amp slow-blow fuse. If not, remove and replace with proper fuse.

f. If defective assembly (UUT) is Front Panel Controller PC Assembly, install in "known-good" test unit per paragraph 4-4.2. If UUT is LCD Display, install in "known-good" test unit per paragraph 4-4.3. If UUT is Remote Interface PC Assembly, install in "known-good" test unit per paragraph 4-4.4.

g. Perform the troubleshooting procedures found in Table 4-2.

4-4.2 Front Panel Controller, A1A1A1. Refer to Figure 4-3.

4-4.2.1 Removal Procedure.

a. Perform the procedure in paragraph 4-4.1 to open the WJ-9902-2 for maintenance.

b. Remove four screws (number 1) securing handle to front panel.

c. Remove four screws (number 2) securing the center support to the front panel.

d. Remove four screws (number 3) holding front panel to side panels of WJ-9902-2.

e. Remove connector FPU-W1P1 from Front Panel Controller connector A1J1.

f. Remove connector FPU-P1 from Front Panel Controller connector A1J2.

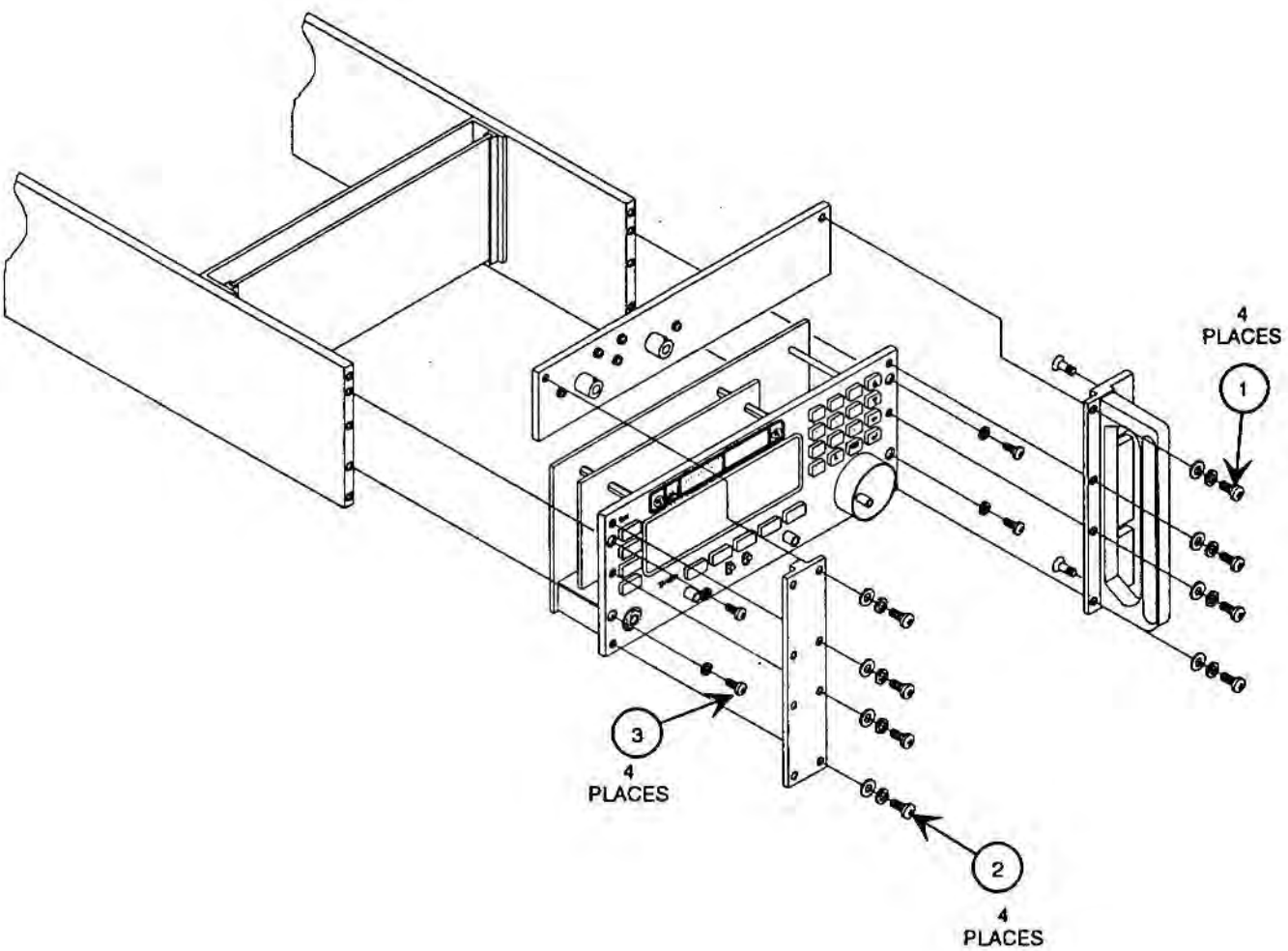


FIGURE 4-3. Removal of the Front Panel and Front Panel Controller

CAUTION

The LCD panel is made of plate glass. Do not apply mechanical shocks or press hard on the LCD display. The polarizer on the display is easily scratched. Handle with care. Do not remove the panel or frame from the LCD.

g. Lay the front panel on a soft cloth to avoid scratching the LCD panel.

h. Remove control knob from front of ADJ (A1S2) switch.

i. Remove nut from PHONE jack.

CAUTION

Exercise extreme care when separating controller board from LCD Display to prevent bending or breaking pins in the connectors plugging into A1J5 and A1J6.

j. Remove two screws, one nut, and associated washers attaching Front Panel Controller assembly to Keyboard.

k. Separate Front Panel Controller board A1A1A1 from LCD Display A1A1U1 by gently pulling apart.

l. Disconnect Tuning Wheel Encoder from board at A1A1J7.

m. Disconnect level control from board at A1A1J9.

n. Disconnect light switch from board at A1A1J8. Board is free of attaching hardware and may be replaced.

4-4.2.2 Replacement Procedure.

a. Reconnect light switch to board at A1A1J8.

b. Reconnect level control to board at A1A1J9.

c. Reconnect Tuning Wheel Encoder to board at A1A1J7.

d. Ensure that DIP switch A1A1A1S1 is configured correctly (Refer to Appendix A).

CAUTION

Exercise extreme care when reconnecting controller board to LCD Display to prevent bending or breaking pins in the connectors plugging into A1A1J5 and A1A1J6.

e. Reconnect LCD Display and Keyboard to board by carefully aligning pins from LCD Display into A1A1J5 and pins from Keyboard into A1A1J6. This step also includes aligning the phone jack and ADJ control with their respective holes in the front panel.

f. Reinstall nut on PHONE jack.

g. Reinstall two screws, one nut, and associated washers securing Front Panel Controller to Keyboard.

h. Replace control knob on ADJ (A1A1S2) switch.

i. Reconnect FPU-P1 to A1A1J2.

j. Reconnect FPU-W1P1 to A1A1J1.

k. Reinstall front panel on receiver controller using four screws.

4-4.3 LCD Display, A1A1U1.

4-4.3.1 Removal Procedure.

a. Perform the procedure in paragraph 4-4.1 to open the WJ-9902-2 for maintenance.

b. Perform removal steps a through n of paragraph 4-4.2.1 to remove Front Panel Controller A1A1A1.

c. Remove standoff nut, three hex nuts, and associated washers to remove LCD Display from the front panel.

4-4.3.2 Replacement Procedure.

a. Attach LCD Display to front panel using standoff nut, three hex nuts and associated washers.

b. Perform steps a through k of paragraph 4-4.2.2 to reinstall Front Panel Controller A1A1A1.

4-4.4 Remote Interface Board, A2.

4-4.4.1 Removal Procedure.

a. Perform the procedure in paragraph 4-4.1 to open the WJ-9902-2 for maintenance.

b. Remove connector FPU-W1P2 from Remote Interface Board connector A2J2.

c. Remove connector IOC-P2 from Remote Interface Board connector A2J3.

d. Remove connector IOC-W1P1 from Remote Interface Board connector A2J1.

e. Remove Remote Interface Board (A2) from receiver controller by sliding up.

4-4.4.2 Replacement Procedure.

a. Ensure replacement Remote Interface board is configured correctly (Refer to Appendix A).

b. Replace Remote Interface board (A2) by sliding into slots on frame.

c. Reconnect FPU-W1P2 to A2J2.

d. Reconnect IOC-P2 to A2J3.

e. Reconnect IOC-W1P1 to A2J1.

4-5 PERFORMANCE TESTS.

This paragraph provides performance tests as an aid in troubleshooting or as verification procedures after repairs have been made. These procedures should be performed by skilled technicians who are thoroughly familiar with proper operation of the test equipment listed in Table 4-1. Should a unit or assembly fail a performance test, proceed to the troubleshooting instructions in paragraph 4-6.

4-5.1 Front Panel Unit Performance Test. The procedures in the following paragraphs verify the correct performance of the Front Panel Unit. Before performing the following tests, replace the "known-good" Front Panel Controller PC Assembly (A1A1A1) with the suspect assembly (UUT) in accordance with paragraph 4-4.2.

4-5.1.1 Keyboard Function Test. Press each of the keys on the front panel keypad, verifying that each key functions as intended. This includes the MENU and FUNCTION keys. Proper functioning can be determined by the microprocessor of the front panel controller correctly commanding the front panel display. Refer to paragraph 2-4 for a complete listing of the available front panel keys and their intended function/response. If the UUT fails the Keyboard Function Test, perform the Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.

4-5.1.2 Tuning Wheel Function Test. Refer to paragraph 2-7.2 for front panel and tuned frequency operating procedures/indications. Setup the front panel so that the tuned frequency of the receiver is displayed, and that the tuning wheel is capable of command. Select a tuning resolution of 100 kHz or less. While viewing the UUT frequency display, slowly rotate the tuning wheel at least one revolution in each direction pausing at least once to verify that a new tuned frequency is displayed by the receiver. At the same time, confirm that counter-clockwise rotation tunes "downwards". If the UUT fails the Tuning Wheel Function Test, perform the Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.

4-5.1.3 Backlight Function Test. Turn the backlight on and off with the LIGHT switch. Verify that the display backlighting is uniform in illumination with no dead spots. Roll up a sheet of paper to form a tube and place one end against 16-key keypad such that room light is blocked and view keypad from other end of tube. Verify that the keypad is backlit. If the UUT fails the Backlight Function Test, perform the Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.

4-5.1.4 ADJ. Control and LCD Display Contrast Test. Using the front panel, select the CONTRAST mode (see paragraph 2-7.1.3). Rotate the ADJ. control counterclockwise; the contrast indication should decrement toward zero. Verify that the display fades until no characters can be detected. Rotate the ADJ. control clockwise until the contrast indication reads "20" (it will be difficult to read). Any pixel in the display that is not correctly driven will be lighter that the others. Verify that all pixels are driven to a very dark level. If the UUT fails the ADJ. Control and LCD Display Contrast Test, perform the Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.

4-5.1.5 Beeper Test. Using the CONFIG Menu (refer to paragraph 2-7.1.3), turn on the beeper function and verify pushing the keys causes the beeper to sound. If the UUT fails the Beeper Test, perform the Front Panel Controller PC Assembly Fault Isolation Test per paragraphs 4-6.1.2.

4-5.2 Remote Interface PC Assembly (A2) Performance Test. The procedures in the following paragraph verify the performance of the Remote Interface PC Assembly. Before performing this test, replace the "known-good" assembly with the suspect assembly in accordance with paragraph 4-4.4.

4-5.2.1 Front Panel-to-Receiver Communications Test. Perform the Tuning Wheel Function Test of paragraph 4-5.1.2, above. If the receiver accepts the assigned frequency with no error messages (see Chapter 2, paragraph 2-7.12 and Table 2-4), then the communications path between the front panel and the receiver through the Remote Interface PC Assembly is intact and the UUT passes. If the UUT fails the Front Panel-to-Receiver Communications Test,

first perform the Front Panel Controller Communications Interface Test per paragraph 4-6.1.2.d and if the problem is still not solved, perform the Remote Interface PC Assembly Fault Isolation procedures per paragraph 4-6.1.3.

4-6. TROUBLESHOOTING AND FAULT ISOLATION PROCEDURES.

The following troubleshooting table (Table 4-2) and the fault isolation procedures (paragraph 4-6.1 and following) are provided as an aid in localizing the cause of a malfunction to a particular component or group of components on an assembly within the receiver controller. During troubleshooting and fault isolation, references to the circuit descriptions in Chapter 3 and to the schematic diagrams at the rear of this manual should be made.

The procedures in this manual presume that the faulty unit has been repaired at the Organizational Repair Facility and that only those repairs that cannot be performed at the organizational level remain. The LRAs that are repaired at the depot level are as follows: the LCD Display (A1A1U1), the Front Panel Controller PC Assembly (A1A1A1), and the Remote Interface (IOC) PC Assembly (A2). For organizational maintenance repair procedures, refer to the Operation and Organizational Maintenance Manual with Parts List for the R-2541/B Receiver, Barracuda, WJ-9902-2 Receiver Controller (SE460-BM-OMP-010).

WARNING

Electrical shock hazard to personnel exists when the receiver controller is opened while powered-up. Ensure that the controller is turned off and external power is disconnected from the rear panel's 120/230 VAC connector, prior to opening the controller.

4-6.1 Fault Isolation Tests. The following fault isolation test procedures may be used as directed by the results of the troubleshooting procedures of Table 4-2. These procedures should be performed only by skilled technicians familiar with the test equipment of Table 4-1.

4-6.1.1 LCD Display Fault Isolation Test. The only repair authorized for the LCD Display Assembly is to replace the connector. The LCD Display itself is not repairable. Perform LCD Display Fault Isolation Test as follows:

a. Perform LCD Display Performance Test per paragraph 4-5.1.4.

b. Remove defective LCD Display Assembly from Front Panel Assembly per paragraph 4-4.3.

c. Perform visual inspection of LCD Display Assembly. If the connector A1-J5 is broken, replace connector.

d. If no obvious visual defect is present, check continuity of connector A1-J5 between input and entrance onto LCD PC assembly. If connector fails continuity check, replace connector. If connector passes continuity check, scrap LCD Display Assembly.

TABLE 4-2. Troubleshooting Procedures

Failure Indication	Probable Cause	Maintenance Action
LCD Display erroneous.	Failed LCD Display, (A1A1U1).	Perform LCD Display Fault Isolation Test per paragraph 4-6.1.1.
Display does not reflect keypress.	Failed Front Panel Controller PC Assembly (A1A1A1).	Perform Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.
Display does not respond to tuning wheel.	Failed Front Panel Controller PC Assembly (A1A1A1).	Perform Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.
Back lighting does not come on for front panel.	Failed Front Panel Controller PC Assembly (A1A1A1).	Perform Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.
Audio not present in either or both earphones.	Failed Front Panel Controller PC Assembly (A1A1A1).	Perform Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.
Display shows message "IOC NOT RESPONDING".	Failed Front Panel Controller PC Assembly (A1A1A1).	Perform Front Panel Controller PC Assembly Fault Isolation Test per paragraph 4-6.1.2.
	Failed Remote Interface PC Assembly (A2).	Perform Remote Interface PC Assembly Fault Isolation Test per paragraph 4-6.1.3
Display shows message "DEVICE TIMEOUT ERROR"	Failed Remote Interface PC Assembly (A2).	Perform Remote Interface PC Assembly Fault Isolation Test per paragraph 4-6.1.3.

4-6.1.2 Front Panel Controller PC Assembly Fault Isolation Test. Fault isolation of the Front Panel Controller PC Assembly consists of a thorough visual inspection in accordance with paragraph 4-3. If no visual defects are found then the UUT should be installed in a "known-good" WJ-9902-2 unit as shown in Figure 4-4 and the performance test of paragraph 4-5 performed. Following the performance test, the microprocessor (MPU) should be checked for proper operation, as described in step (a) below, using the existing performance test setup. If the MPU is operating properly, then depending on the improper operation of the Front Panel Unit, check either the Keyboard Interface Circuits, the Display Interface Circuits, or the Communications Interface Circuits. As an aid to fault isolation, refer to the detailed functional/circuit descriptions contained in paragraph 3-4.2.1.3 and schematic diagram Figure FO-3 for additional circuit level information as required. Refer to the assembly drawing Figure 5-4 for Front Panel Controller Assembly components location diagrams. Perform fault isolation as follows:

a. Microprocessor and Memory Section Fault Isolation. Isolate faults in this section as follows:

1. Check TP19, the /RESET line and TP18, the /HALT line for the MPU. Voltage should be at a logic high. If at a logic high, go to step 3. If /RESET and/or /HALT is low, verify +5 Vdc ±0.5 volts at TP16, +5 volt regulator output. If +5 volts is present, go to step 2. If +5 volts is missing at TP16 verify +12 Vdc at J1-Pin 1. If +12 volts is present, troubleshoot/replace voltage regulator U6, capacitors C4 and C75, and diodes CR1 through CR3. If +12 volts is missing, troubleshoot/replace power supply PS1 and associated cabling.

2. Verify +3.3 Vdc ±0.5 volts at the anode of VR1. If +3.3 volts is not present, troubleshoot/replace VR1, R140, and R141. If +3.3 Vdc is present at VR1 anode, verify +5 Vdc at TP22. IF +5 volts is missing at TP22, troubleshot/replace transistors Q2 and Q3, and resistor R142. If +5 volts is present at TP22, replace U34.

3. If TP19 is at +5 Vdc, use an oscilloscope to check the 12 MHz clock at TP17 (CLK). This signal should be a +5 Vp-p approximate square wave, oscillating at 12 MHz. If the clock signal is not correct, check for 12 MHz signal at U8-9. If signal is present replace U8. If signal is not present replace Y1 and associated capacitors.

4. If the clock is correct, check the address lines A1-A23, U31-32 through U31-51, and U31-53 through U31-55. Signals should be as shown in Figure 4-5. They should vary between a logic high and a logic low. If any address line is a constant high or low, or is varying to a voltage level less than +5 volts, replace U31.

5. If replacing U31 does not cure the problem, any component connected to the parallel address bus that receives the faulty data line could be the cause of the problem. The following list

of components should be removed individually (if it receives the faulty data line) and U31 retested after the removal of each component.

ADDR 01 thru ADDR 04 = U1, U32, U44
ADDR 01 thru ADDR 15 = U36, U37
ADDR 01 thru ADDR 20 = U28, U29

6. If the address lines are correct, check the data lines, D0-D15, U31-1 through U31-5 and U31-58 through U31-68. Signals should be as shown in Figure 4-6. They should vary between 0 and +5 volts. If any data line is a constant 0 or +5 volts, or is varying to a voltage level less than +5 volts, replace U31.

7. If replacing U31 does not cure the problem, any component connected to the parallel data bus that receives the faulty data line could be the cause of the problem. The following list of components should be removed individually (if it receives the faulty data line) and U31 retested after the removal of each component.

D00 thru D03 = U1, U18
D00 thru D05 = U16
D00 thru D07 = U28, U37, U43, U20, U27, U33, U32, U44
D08 thru D15 = U29, U36, U38

After retest, if the failed data line is now correct, replace the component removed. If the failed data line is still not correct, remove the next component from the list above. If the failed data line is still not correct with all required components removed from the data bus, replace the Front Panel Controller PC Assembly.

8. If data lines are correct, check TP12 for the EPROMs (U28 and U29) chip select. This should be a signal as shown in Figure 4-7. If chip select is not correct, troubleshoot through U7C and U9 back to U31 and replace as necessary.

9. If EPROMs chip select is correct, check TP21 for RAMs (U36 and U37) chip select. Signal should be as shown in Figure 4-8. If chip select is not correct, troubleshoot Q1 and U9. Replace as necessary.

10. If RAMs Chip Select is correct, measure the dc voltage at the junction of BT1 and R111. BT1 is the battery for memory backup and should be at +2.8 Vdc ±0.5 volts. If voltage is not correct replace BT1.

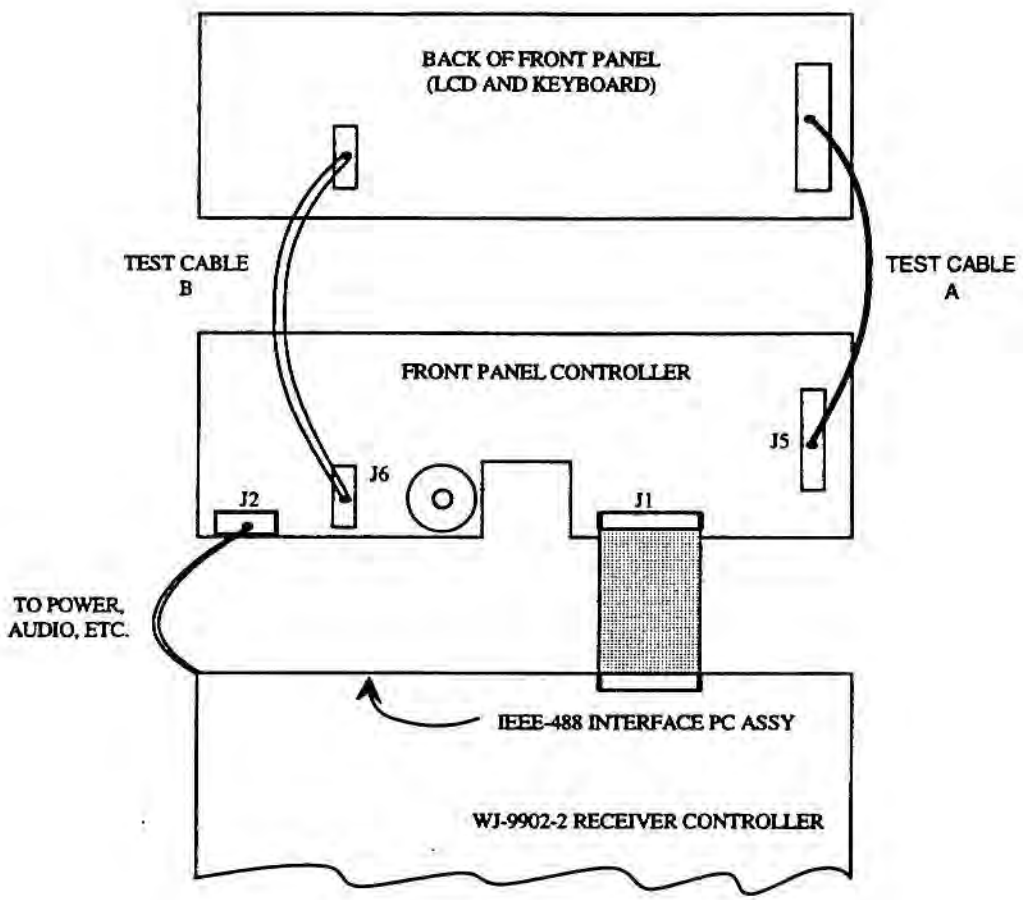


FIGURE 4-4. Test Setup for Front Panel Controller Fault Isolation

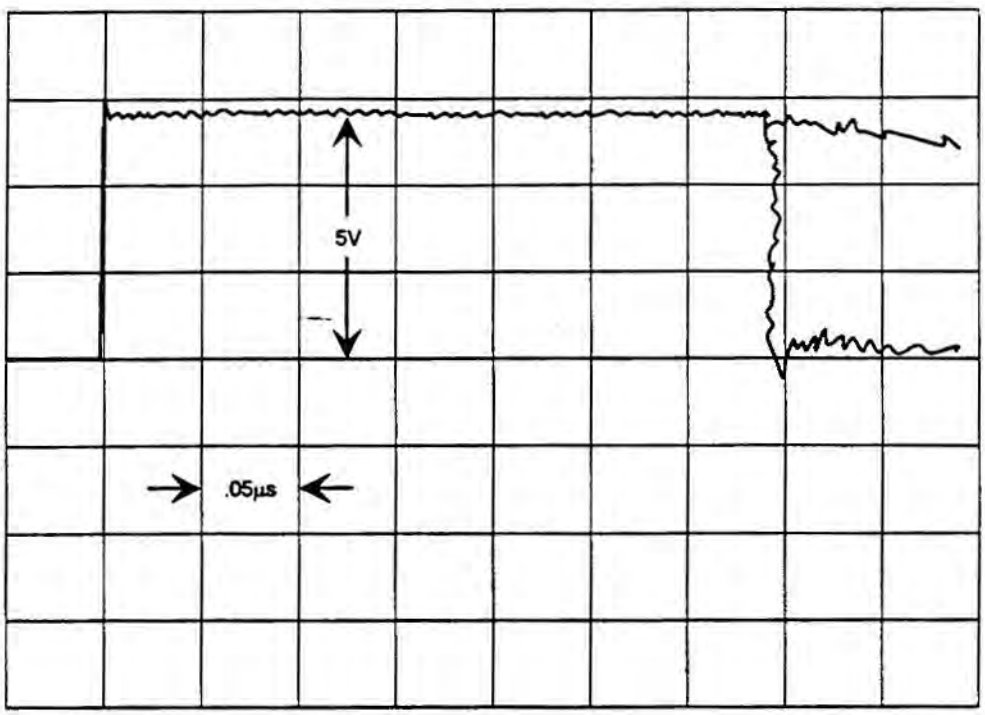


FIGURE 4-5. Typical Signal Trace for Address Lines (A1-A23)

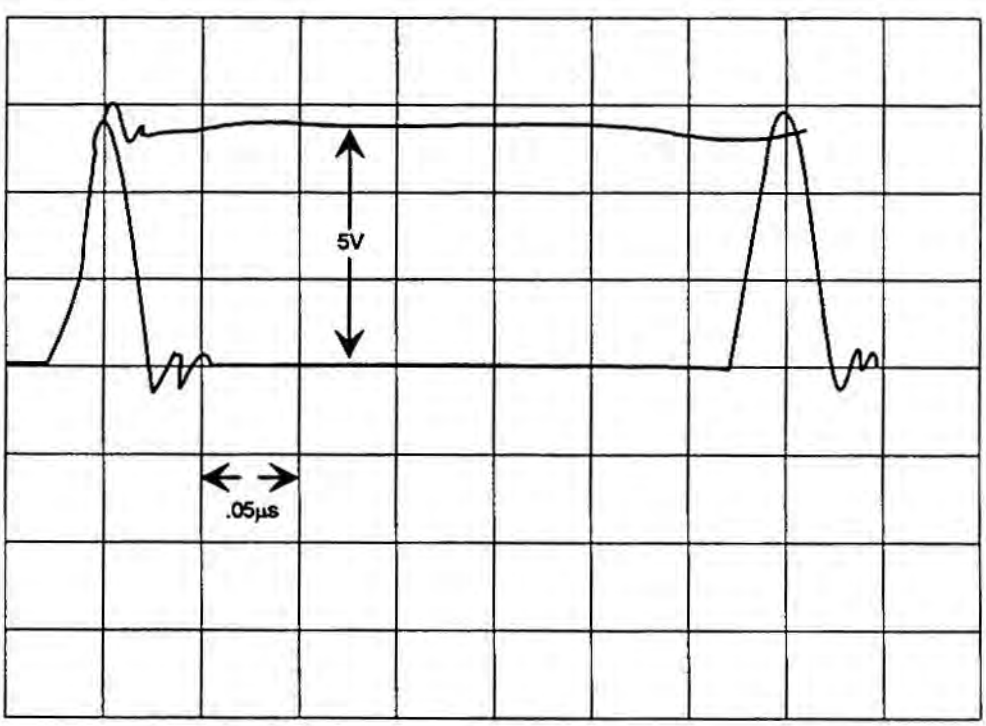


FIGURE 4-6. Typical Signal Trace for Data Lines (D0-D15)

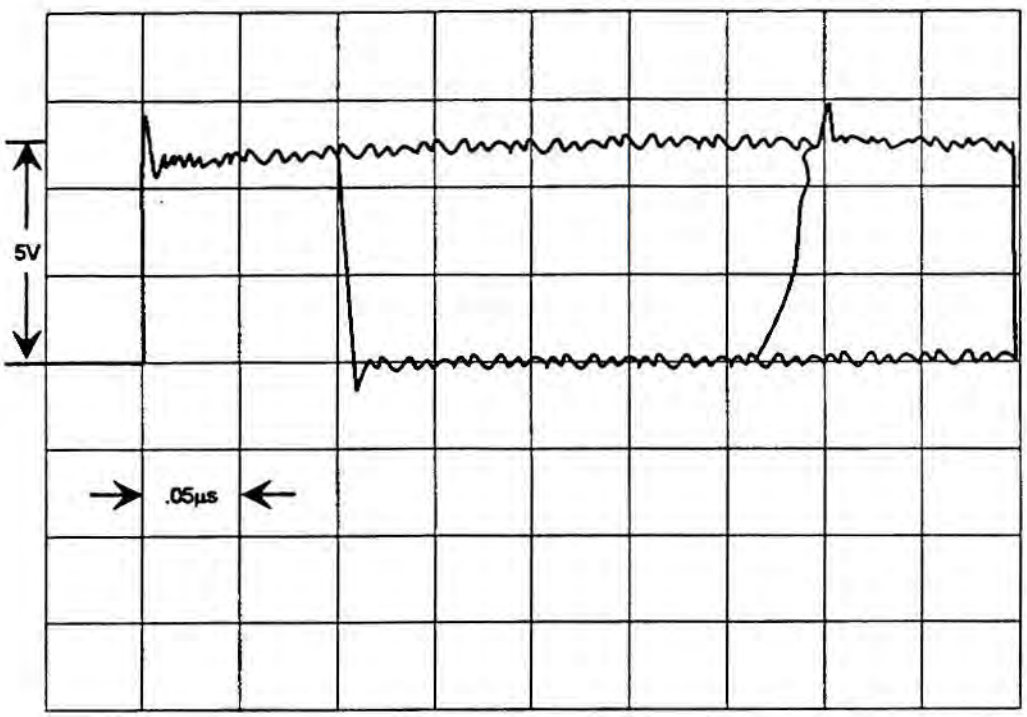


FIGURE 4-7. Typical Signal Trace for TP12

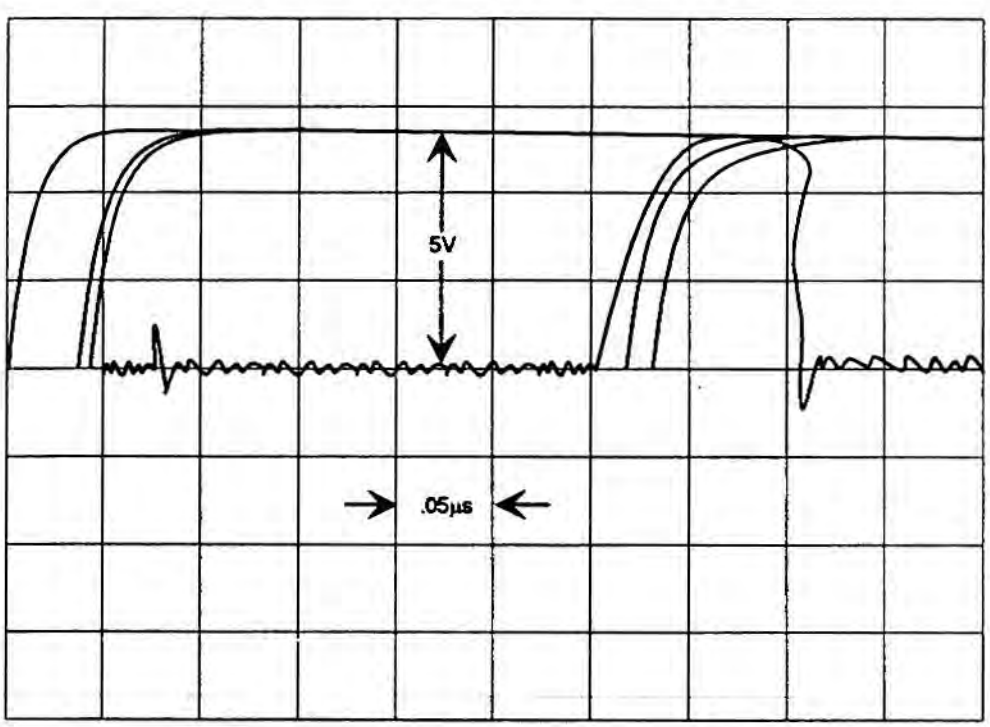


FIGURE 4-8. Typical Signal Trace for TP21

b. Keyboard Interface Circuits Fault Isolation. As an aid to fault isolation, refer to the detailed functional/circuit descriptions contained in paragraph 3-4.2.1.2 and schematic diagram Figure FO-3 for additional circuit level information as required. Refer to the assembly drawing Figure 5-4 for Front Panel Controller Assembly components location diagrams. Isolate faults in this section as follows:

1. If the display does not reflect the correct keypress (see paragraph 2-4), the problem may lie in the keyboard interface circuits, U22 and U15. Isolate faults as follows:

   (a) Using an oscilloscope, observe the signal at U22-12. Signal should vary from 0 to +5 Vdc as a key is pressed. If signal is not correct, replace U22.

   (b) If signal is correct, check output of U15. These are data lines and should be as shown in Figure 4-9. If data lines are not correct an open connection exist between U15 and the microprocessor U31. Repair trace or scrape board.

2. If the display does not respond to the tuning wheel, then the problem may lie in the interrupt control circuits, U17C and U11. Isolate faults as follows:

   (a) Using an oscilloscope, check signal at U17-8 as tuning wheel is turned. Signal should fluctuate between +5 and 0 Vdc as shown in Figure 4-10. If signal is correct, replace U11.

   (b) If signal is correct, check inputs to U17, pins 9, 10, and 11. Pin 9 should be a logic high that pulses low as the tuning wheel is rotated, while pins 10 and 11 should be at a logic high. If pin 9 is not pulsing low or if pin 11 is low, replace U24. If pin 10 is low, replace U26.

3. If the display does not respond to movement of the ADJ. control, then the problem lies either in the ADJ. control, S2, or the Hex Debounce circuit, U13. Using an oscilloscope, measure the signal at TP15. The signal should be constant +5Vdc. When S2 is rotated, the oscilloscope should show a momentary negative pulse. (An inversion of the signal at TP15 should appear at TP14.) If the signal does not appear correct, check the signal at the terminals of S2. S2-pins 1 and 3 should indicate +5 Vdc, pulsing low as the ADJ. control is rotated. If the signal is correct at S2, replace U13. If the signal is still not correct, replace S2. If the signal was correct at TP15 and TP14, monitor the signal at U18-14. As the ADJ. control is adjusted, U18-14 should vary between 0 and +5 Vdc. If this signal is incorrect, replace U25. If this signal is correct, but there is still no response at the display, replace U18.

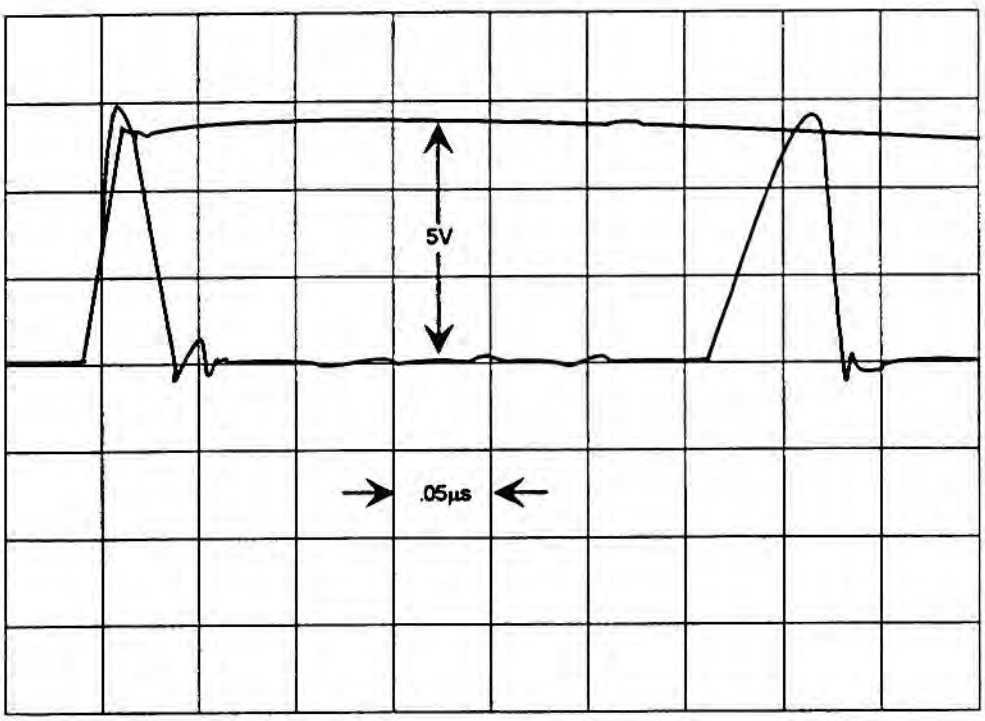


FIGURE 4-9. Typical Signal Trace at U15-Pins 3, 5, 7, 9, 11, 13

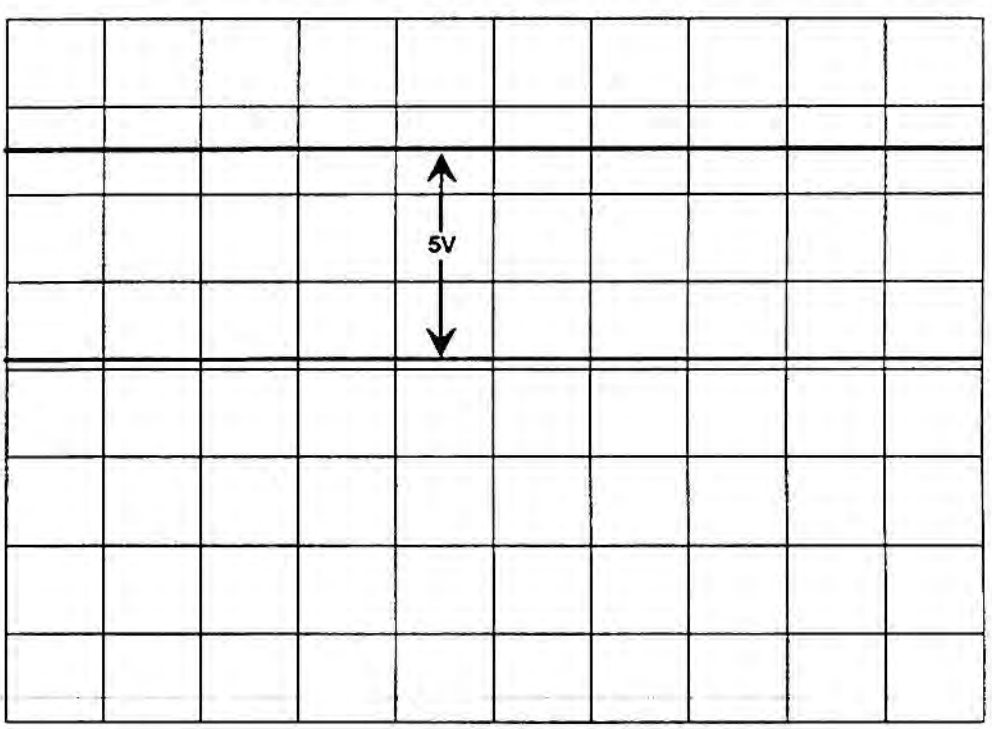


FIGURE 4-10. Typical Signal Trace at U17-8

c. Display Interface Circuits Fault Isolation. As an aid to fault isolation, refer to the detailed functional/circuit descriptions contained in paragraph 3-4.2.1.4 and schematic diagram Figure FO-3 for additional circuit level information as required. Refer to the assembly drawing Figure 5-4 for Front Panel Controller Assembly components location diagrams. Isolate faults in this section as follows:

1. If the LCD display does not show any characters and the LCD is known to be good, the fault probably lies in U27, the LCD Display Controller. Check the enable (ELCD) signal at TP1. Signal should be as shown in Figure 4-11. If signal is not correct, monitor the Address Select (AS*) line at TP4. This signal should appear as shown in Figure 4-11. Ensure this signal is inverted at U2D-8. If incorrect, replace U2. If U2D is functioning properly, troubleshoot/replace U3 and/or U7.

2. If the ELCD signal is correct, check output to LCD on J5-1. Signal should be as shown in Figure 4-12. If the output signal is not correct, check display data inputs to U27 at U27-21 through U27-28. Signals should be present as shown in Figure 4-6.

3. If data inputs are correct,troubleshoot/replace U27 and U35. Refer to paragraph 3-4.2.1.4 for circuit description information.

d. Communications Interface Circuits Fault Isolation. As an aid to fault isolation, refer to the detailed functional/circuit descriptions contained in paragraph 3-4.2.1.1 and schematic diagram Figure FO-3 for additional circuit level information as required. Refer to the assembly drawing Figure 5-4 for Front Panel Controller Assembly components location diagrams. Isolate faults in this section as follows:

1. If the front panel displays the message "IOC NOT RESPONDING" (refer to paragraph 2-7.12 and Table 2-4) and the IEEE-488 Interface PC Assembly is known to be operational, then the fault lies in the front panel controller's communications interface circuits, U44 or U45. Verify the presence of Front Panel Transmit Data (FPTXD) at J1-5. A good data signal toggles between +10 Vdc and -10 Vdc continuously, with each positive and negative transition lasting approximately 100 μs. If FPTXD is not present at J1, check for the presence of the signal at U45-7. If present there, scrap board. If not present there, check U45-10. If present, replace U45.

2. If FPTXD is not present at U45-10, check TP2 for clock signal. The clock signal should be a square wave oscillating at approximately 3.6864 MHz. If clock signal is present, replace U44. If clock signal is not correct, replace Y2 and/or inverter U2.

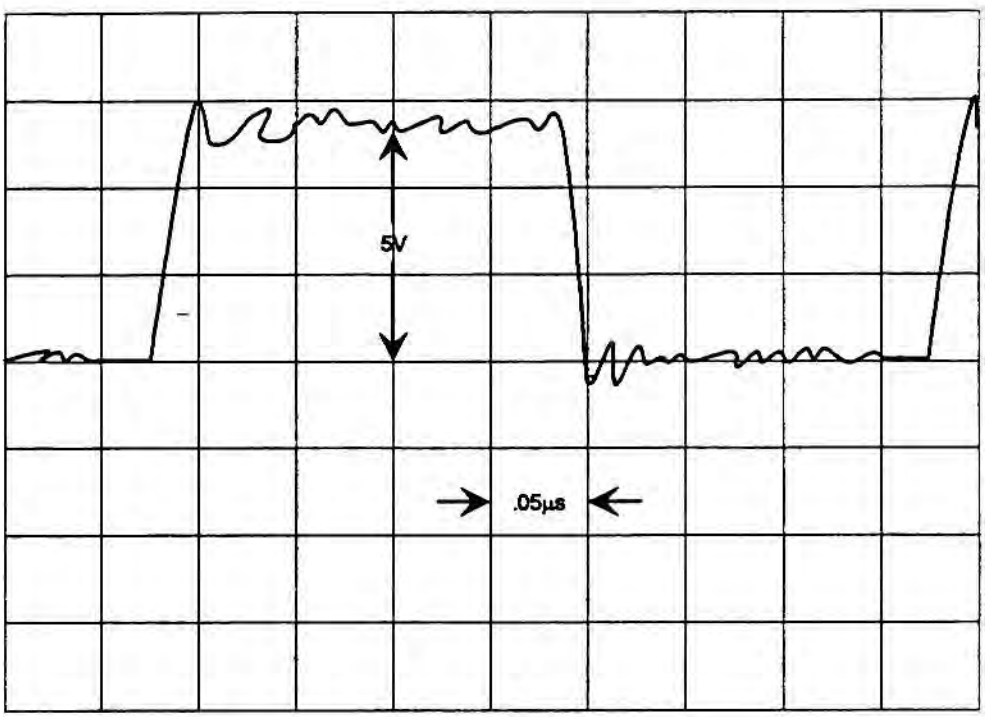


FIGURE 4-11. Signal Trace of Enable LCD Signal (ELCD)

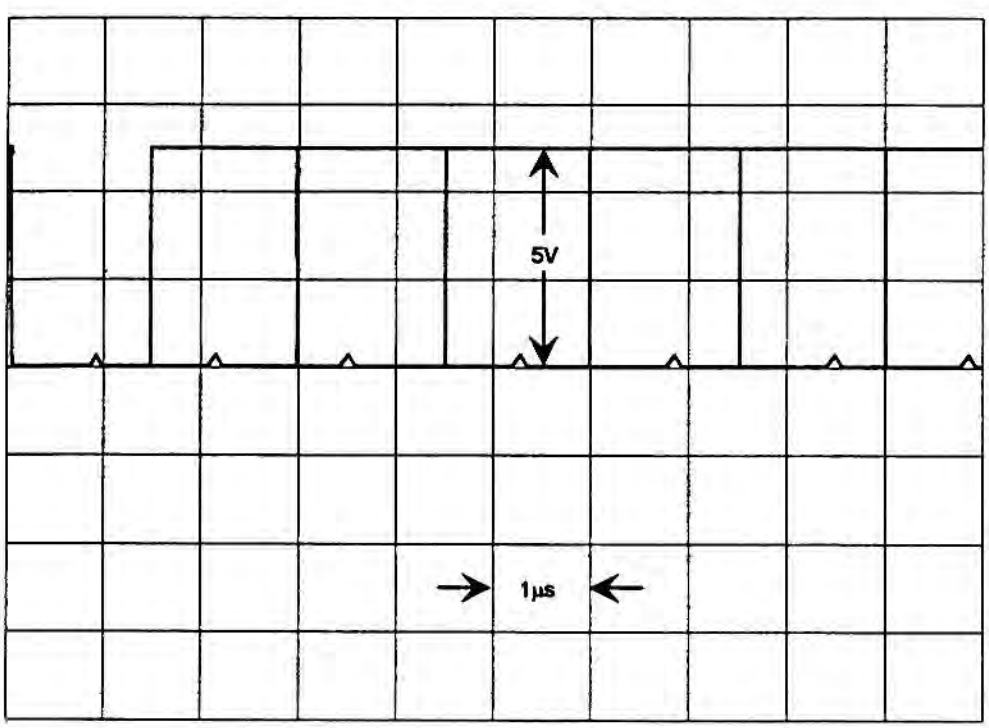


FIGURE 4-12. Signal Trace of LCD Output Signal (D)

4-6.1.3 Remote Interface PC Assembly Fault Isolation Test. Fault isolation of the Remote Interface PC Assembly consists of checking the microprocessor Error Lamp, DS1. If the microprocessor is running properly, then depending on the front panel error, check either the Front Panel Interface or the HPIL Loop Interface. As an aid to to fault isolation, refer to the detailed functional/circuit descriptions contained in paragraph 3-5 and schematic diagram Figure FO-4 for additional circuit level information as required. Refer to the assembly drawing Figure 5-6 for Remote Interface PC Assembly components location diagrams. Perform fault isolation as follows:

a. Microprocessor and Memory Section Fault Isolation. If DS1 is lit (see Figure 5-6 item 29 for location), it means that the Microprocessor (MPU) cannot run the software. Isolate faults in this section as follows:

1. Check TP4, the P-FAIL* line for the MPU. Voltage should be at a logic high. If P-FAIL* is high, go to step 3. If P-FAIL* is low, verify +5 Vdc at U3-3 and the COP* signal at U3-11 (as described in paragraph 3-5). If +5 Vdc and COP* are present, replace U3. If +5 Vdc is not present, go to step 2. If COP* is not present, go to step 3.

2. Verify +5 Vdc ±0.5 volts at U35-3. If +5 volts is present, an open circuit exist between U35-3 and U3-3. Repair or scrap Remote Interface PC Assembly. If +5 volts is not present at U35-3, check for a +12.0 Vdc input at U35-1. If +12 volts is present, troubleshoot/replace voltage regulator U35 and filter capacitor C49. If +12 volts is missing at U35-1, troubleshoot/replace power supply PS1 and associated cabling.

3. Using an oscilloscope, check the 12 MHz clock at U1-38. This signal should be a +5 Vp-p sine wave, oscillating at 12 MHz. If the clock signal is not correct, replace Y1 and associated capacitors.

4. If the clock is correct, observe the E (TP6) and Q (TP7) lines. These should be 3 MHz square waves, +5 Vp-p. If these lines are not correct, replace U1.

5. If E and Q are correct, check TP13 for the EPROM (U18) chip select. This should be a +5 Vdc signal going to ground sometime every machine cycle. If this signal is correct, go to step 6. If TP13 is not correct, check for a 3 MHz square wave (+5 Vp-p) at U8C-8. If signal is not present at U8C-8 replace U8. If signal is present at U8C-8, troubleshoot/ replace U19 and U20.

6. If the chip select is correct, check the data lines out of the EPROM, U18, pins 13-15 and 18-22. They should vary between 0 and +5 volts as shown in Figure 4-13. If data lines are incorrect, check the address lines, U18, pins 2-11, 24, and 27-31. They should vary between 0 and +5 volts. Since each address lines transition from 0 to +5 Vdc is different, any 0 to +5 Vdc transition is considered correct. If the address lines are correct, replace U18. If the address lines are incorrect, check address outputs of MPU, U1, pins 8-23. If the address lines are not correct, replace U1. If the address lines are correct an open circuit exist between U1 and U18. Repair PC board or scrap board as required.

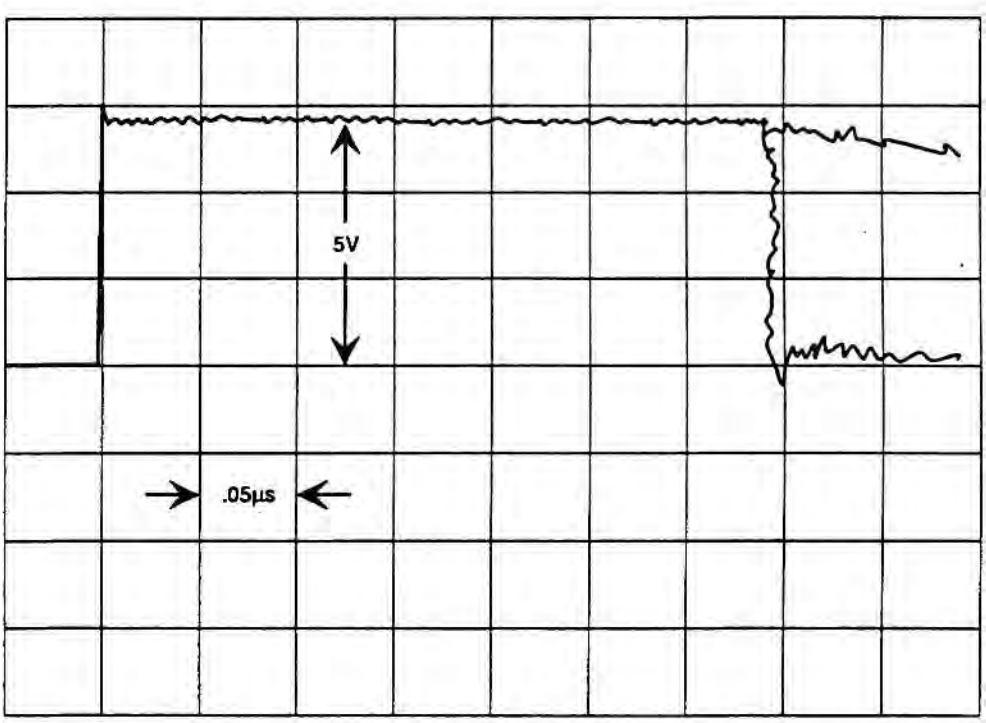


FIGURE 4-13. Typical Signal Trace for Data Lines (D0-D7)

b. Front Panel Interface Fault Isolation. If the front panel has the error message, "IOC NOT RESPONDING" (see paragraph 2-7.12 and Table 2-4), and repeated attempts to access a receiver are not successful, then the Front Panel Interface section, U27, U30, and associated components are probably defective. As an aid to fault isolation, refer to the detailed functional/circuit descriptions contained in paragraph 3-5.2 and schematic diagram Figure FO-4 for additional circuit level information as required. Refer to the assembly drawing Figure 5-6 for Remote Interface PC Assembly components location diagrams. Isolate faults as follows:

1. Verify the presence of FPTXD at U30-13. A good data signal toggles between +10 Vdc and -10 Vdc continuously, with each positive and negative transition lasting approximately 100 µs. If this signal is missing, check for a short circuit to ground at U30-13 or an open circuit from U30-13 to J2-5. Repair or replace the Remote Interface Assembly as required.

2. Check signal at U30-12. Signal should toggle between 0 and +5 Vdc but have the same appearance and timing as the FPTXD signal in step 1 above. If signal is incorrect, replace U30.

3. If incoming signal is reaching U27 correctly, check U27-38 (RST) for a logic high. If RST is high, check U28-3 for a logic high. If high, replace U28. If U28-3 is low (0 Vdc) perform fault isolation test in paragraph 4-6.1.3(a).

4. Check clock signal from Y2 at U27-36. Signal should be 5 Vp-p sine wave, oscillating at 3.686 MHz. If clock signal is not correct, replace Y2 and associated capacitors.

5. Check chip enable signal FP/NET* at U27-39. This signal should be a logic high with a negative-going pulse. If there is no pulse and the module under test passed the Microprocessor/Memory test in paragraph 4-6.1.3(a), replace U24. If the test in paragraph 4-6.1.3(a) have not been performed, do so now.

6. Check the read enable (E.RD*: U27-10) and write enable (E.WR*: U27-9) inputs to U27. The two signals should be pulse trains of opposite TTL logic levels. If the read enable and write enable inputs are not correct, troubleshoot through U6-pins 8 and 11 back to MPU. Replace U6 as necessary. If enable inputs are correct, replace U27. Note that the read cycle begins on the falling edge of the read enable and the transfer occurs when the enable is at a low. The write cycle begins when the write enable is at a low and the transfer occurs on the rising edge of the enable.

c. HPIL Loop Interface Fault Isolation. A fault in the HPIL Loop Interface shows up with a front panel message: "NO DEVICE" for the selected receiver. As an aid to fault isolation, refer to the detailed functional/circuit descriptions contained in paragraph 3-5.3 and schematic diagram Figure FO-4 for additional circuit level information as required. Refer to the assembly drawing Figure 5-6 for Remote Interface PC Assembly components location diagrams. Isolate faults in the HPIL Loop Interface as follows:

1. Check U34-25 (P-FAIL*) and verify that pin is at a logic high. If P-FAIL* is low, check TP4. If TP4 is low, perform the fault isolation procedures in paragraph 4-6.1.3. If TP4 is not low, an open circuit exist betwen TP4 and U34-25. Repair or replace board as required.

2. Check U34-28 (HPIL*) and verify that signal is a negative-going logic pulse. If pulse is not correct, and the module under test passed the Microprocessor/Memory test in paragraph 4-6.1.3(a), replace U24. If the test in 4-6.1.3(a) have not been performed, do so now.

3. Check U34-26 (E.RD*) and U34-27 (E.WR*) and verify that signals are pulse trains of opposite TTL logic levels. If the signal at U34-26 is not correct, replace U6. If the signal at U34-27 is not correct, check the R/W* line at U1-32. This signal should be a logic high with a negative-going pulse occuring approximately every 2 mS. If the signal at U1-32 is incorrect, replace U1. If the R/W* signal is good, verify an inverted signal at U5E-10. If the signal at U5E-10 is good, replace U6. If the signal at U5E-10 is incorrect, replace U5.

4. Check U34-2 (IRQ*) and verify that signal is a negative-going pulse. If pulse is not correct, replace U34.

5. If U34 appears to be operating correctly, then the fault lies in T1. Replace T1.

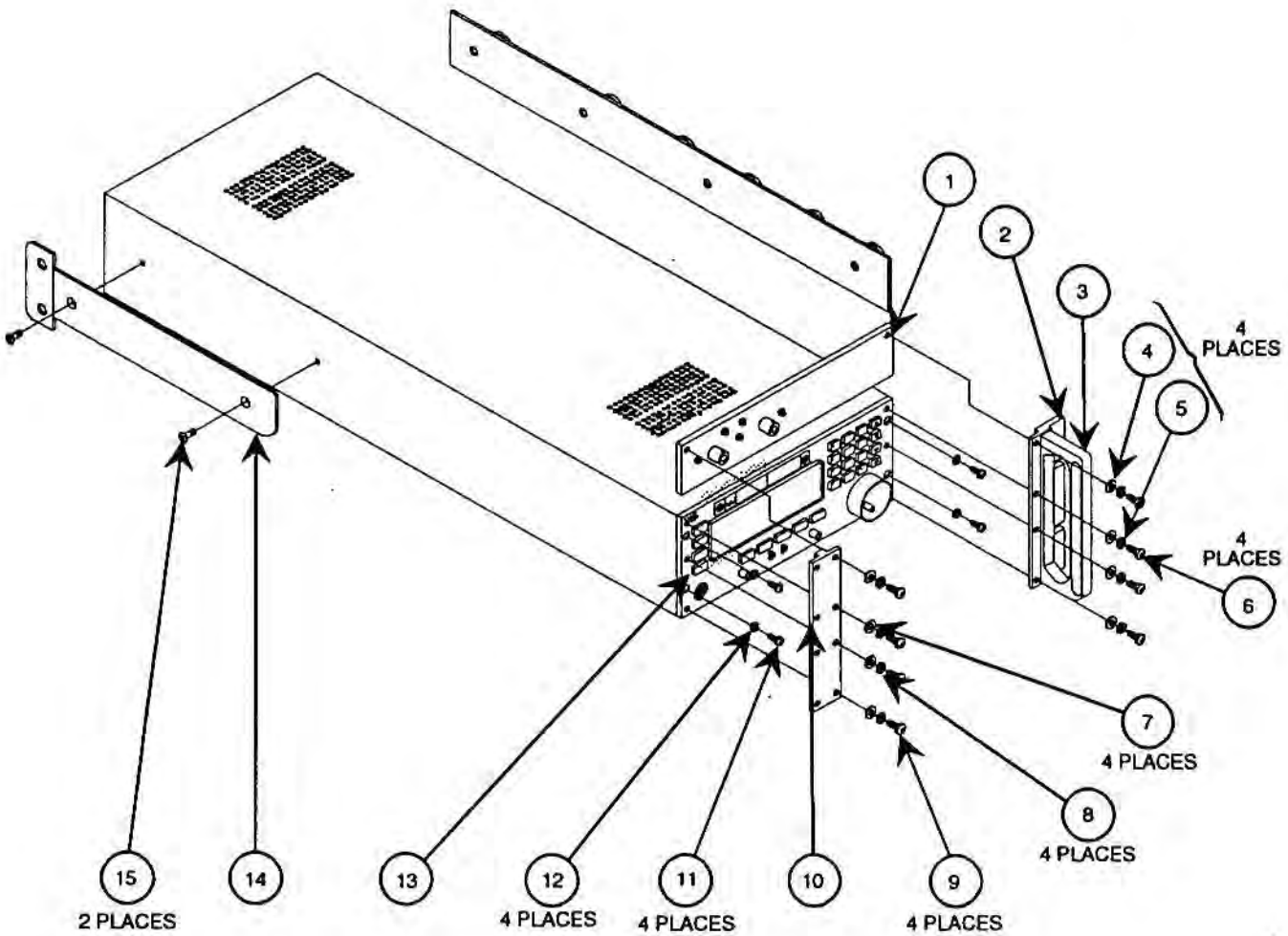


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location (Sheet 1 of 10)

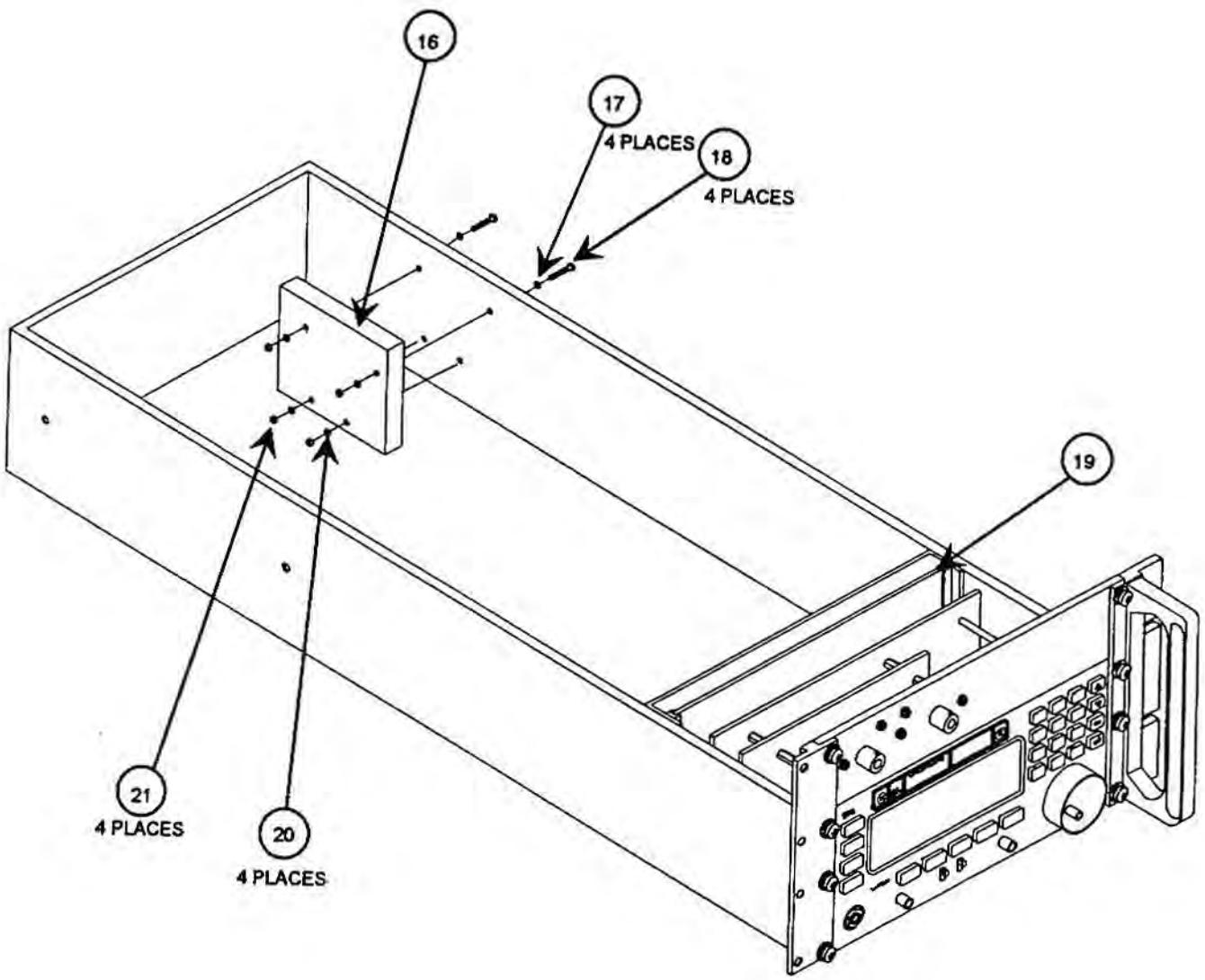


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location
(Sheet 2 of 10)

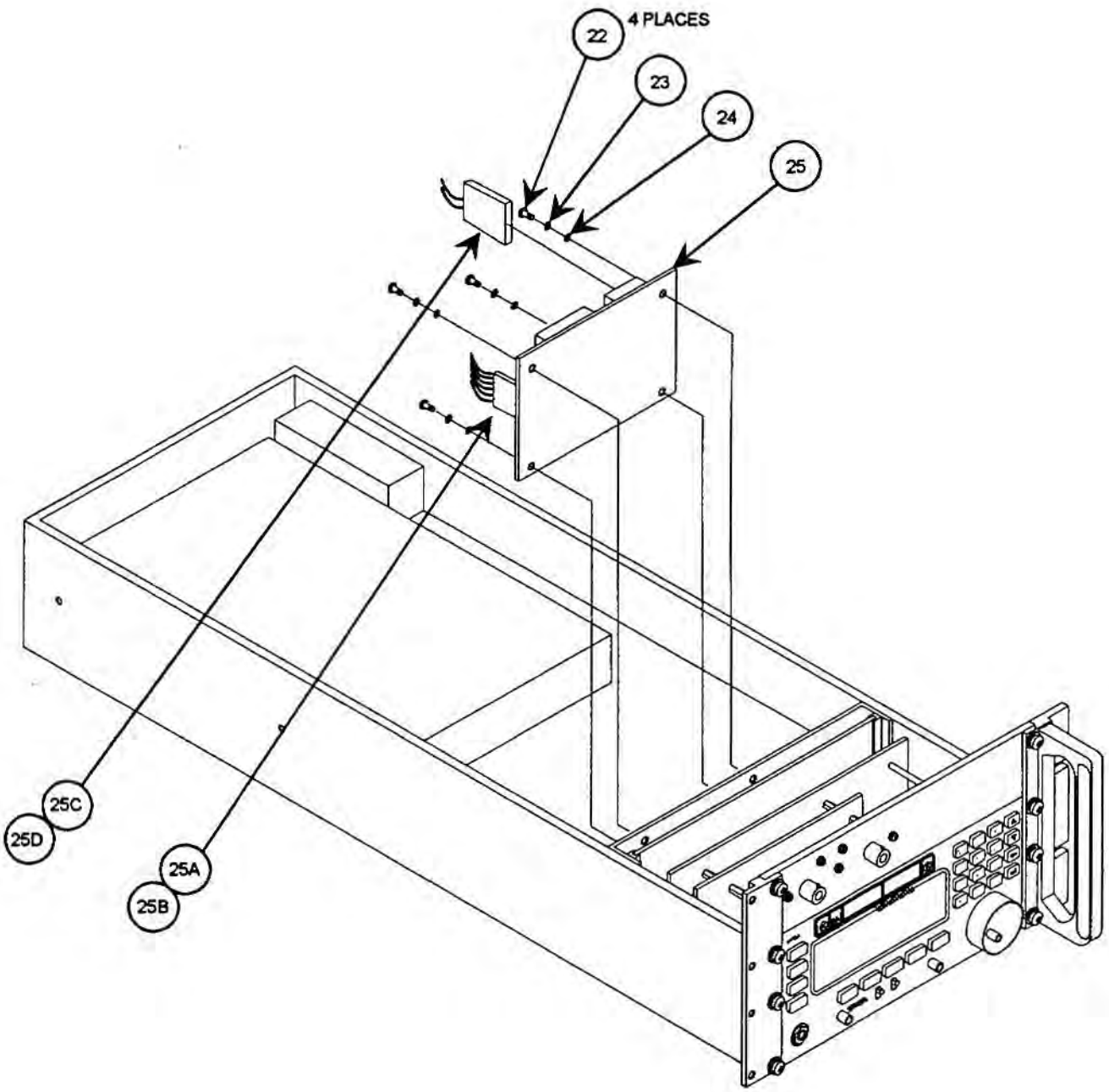


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location
(Sheet 3 of 10)

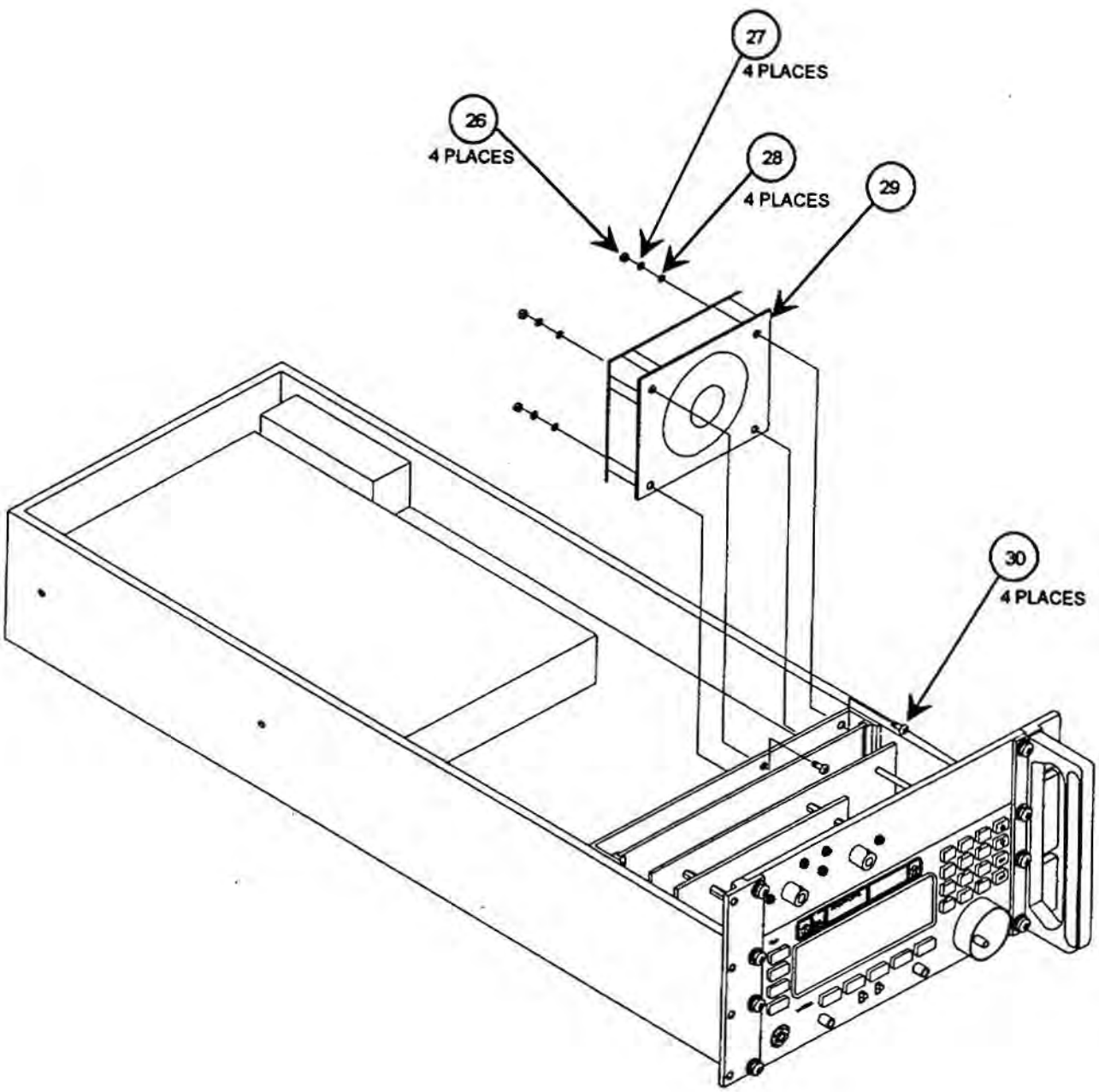


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location
(Sheet 4 of 10)

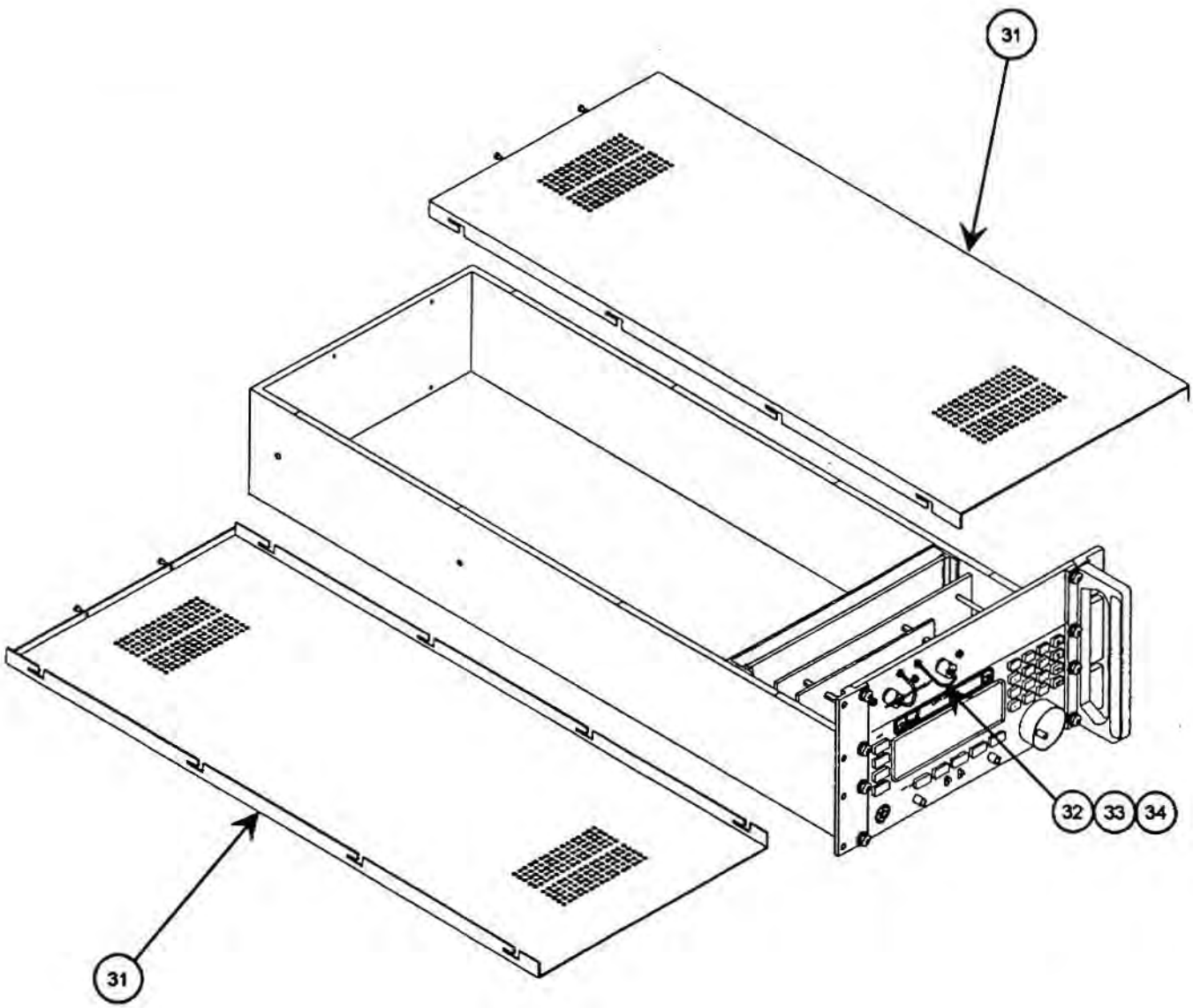


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location
(Sheet 5 of 10)

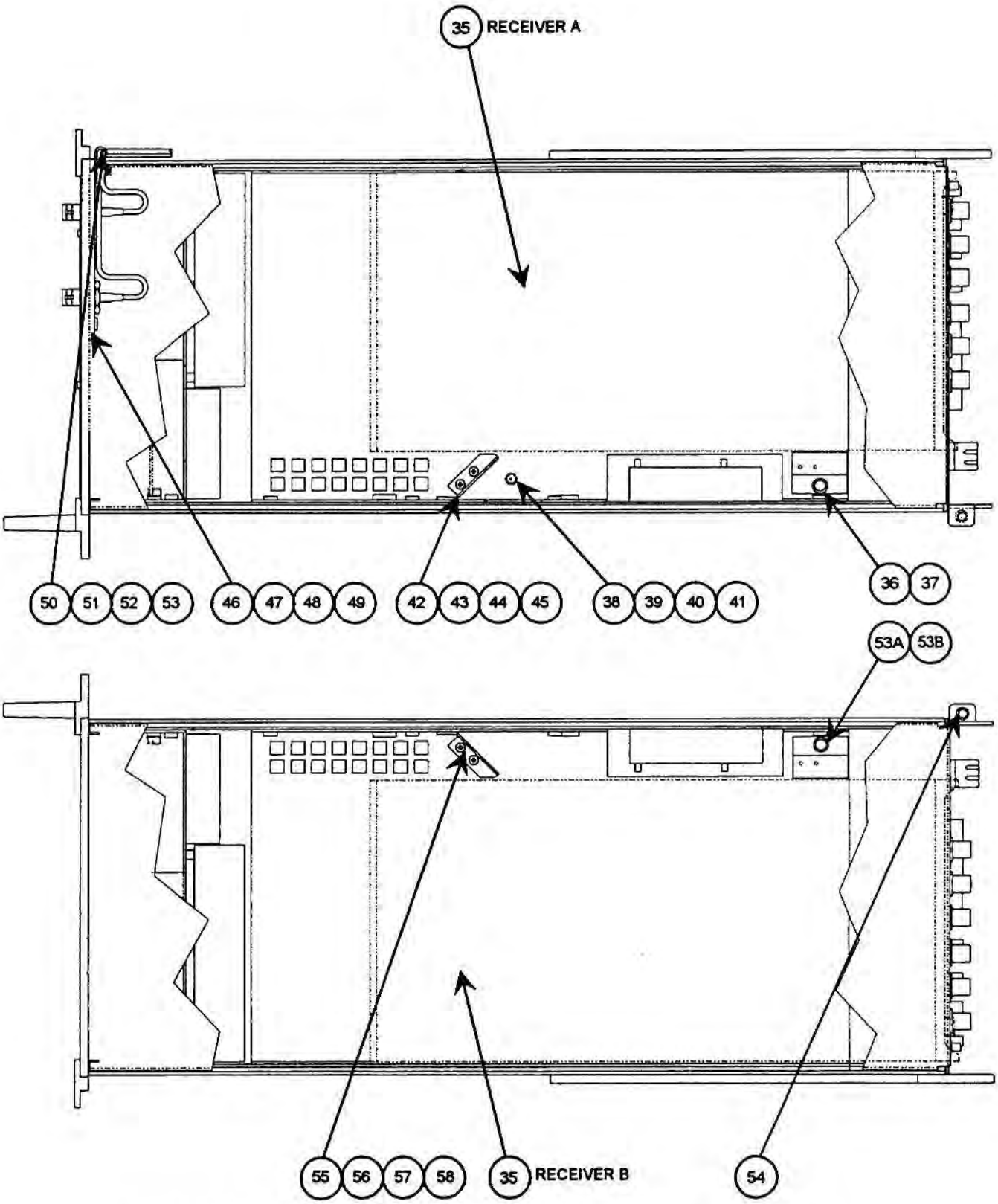


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location
(Sheet 6 of 10)

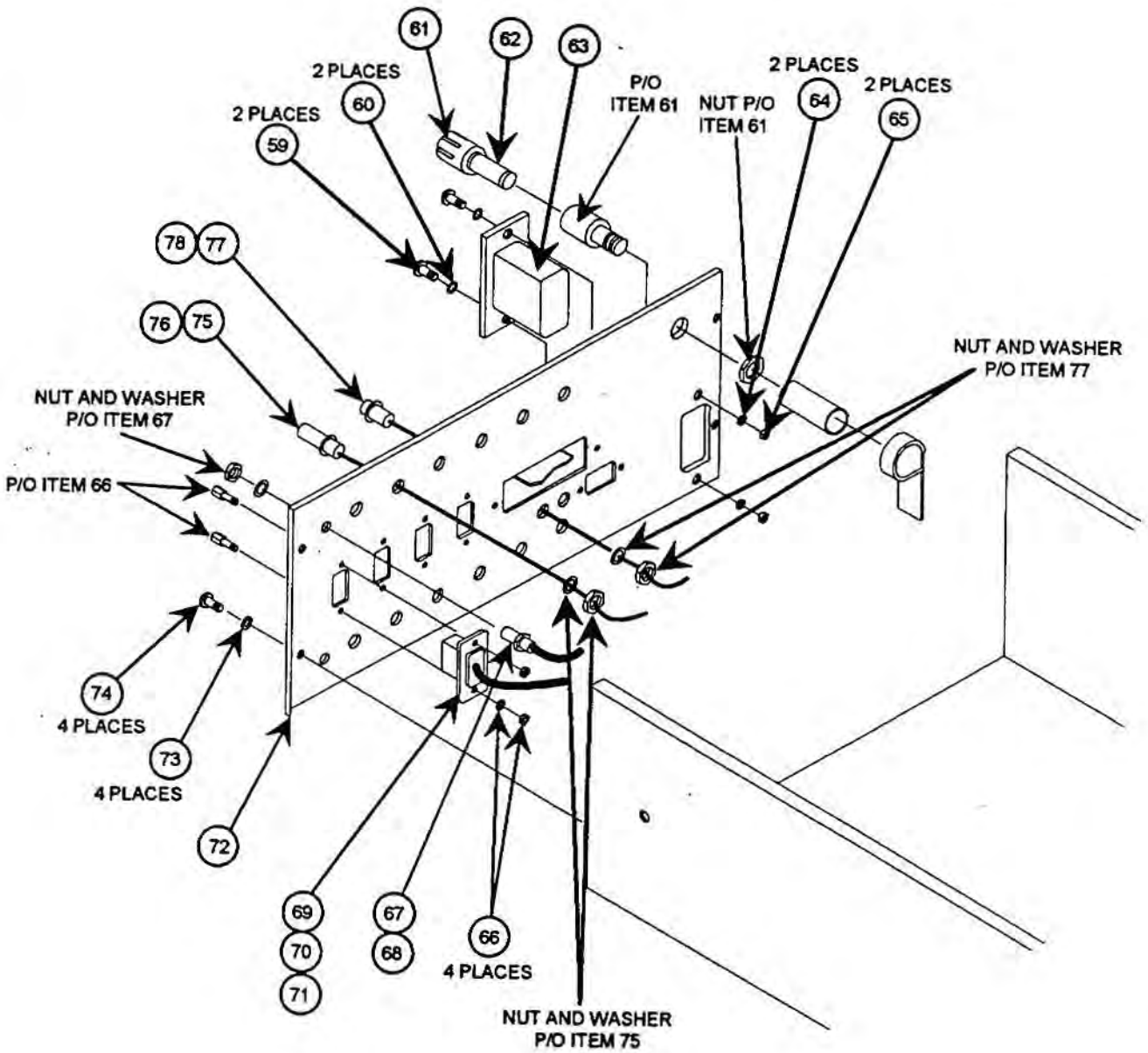


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location
(Sheet 7 of 10)

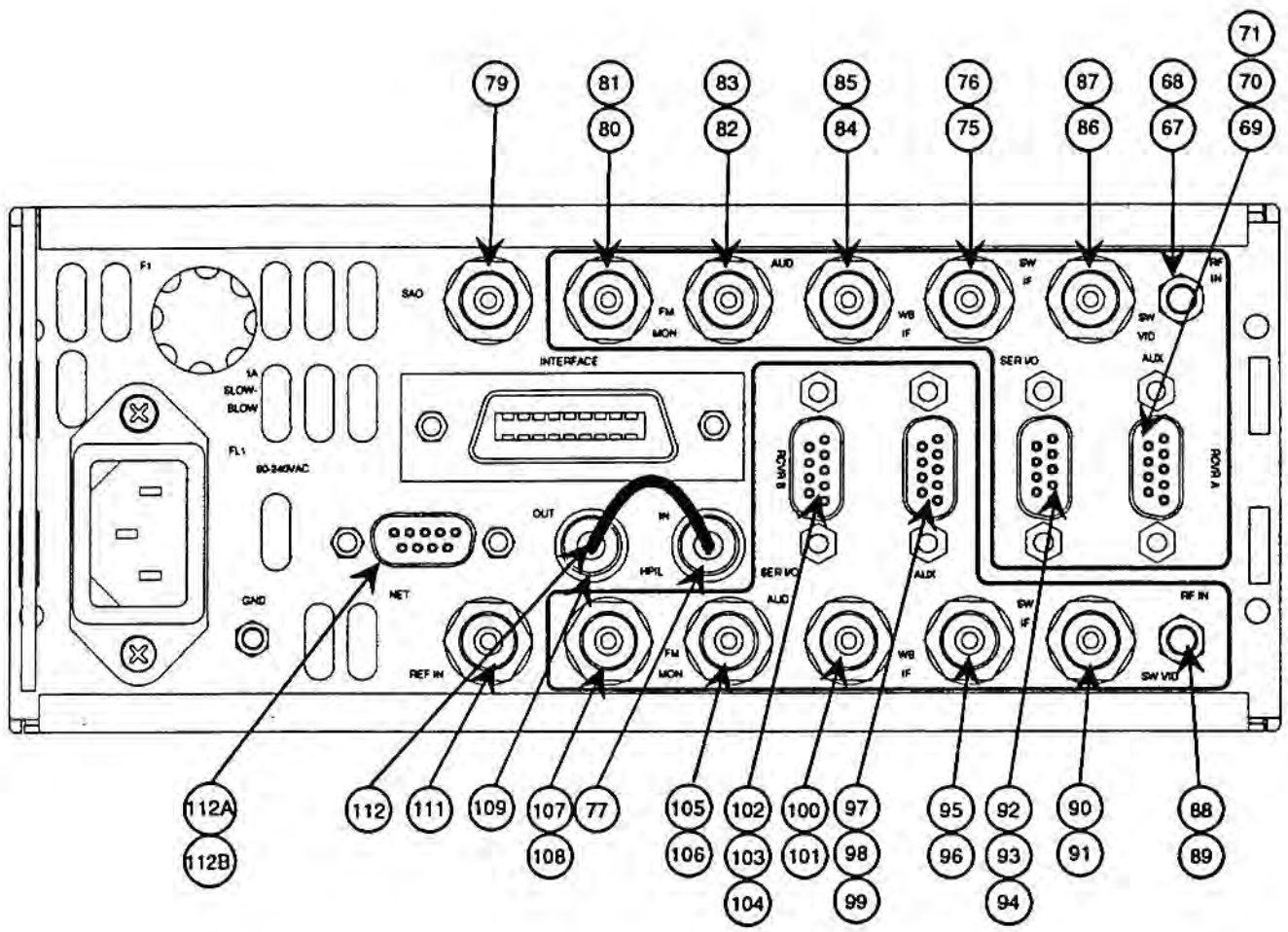


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location (Sheet 8 of 10)

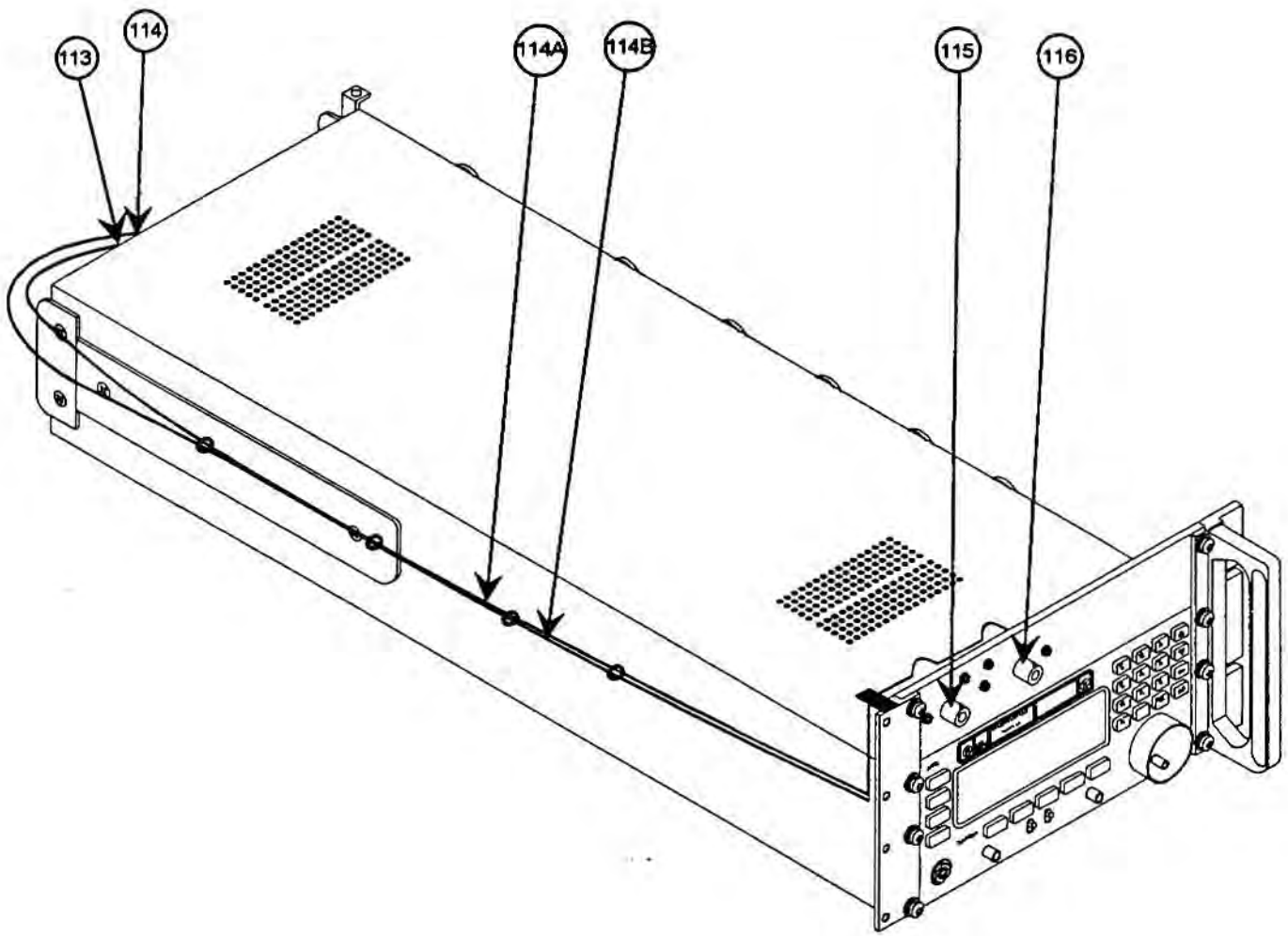


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location
(Sheet 9 of 10)

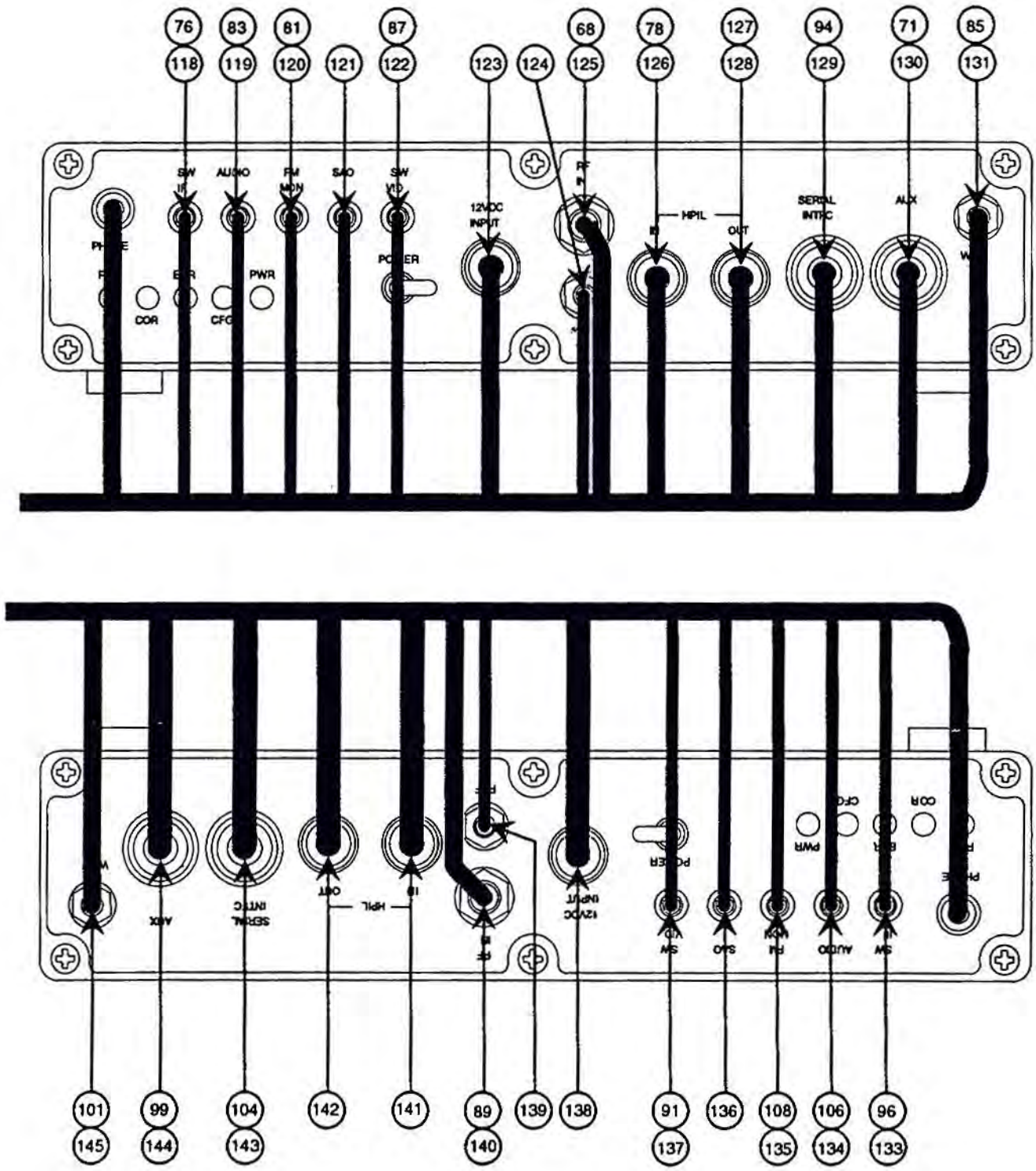


FIGURE 5-1. WJ-9902-2 Receiver Controller Assembly Parts Location
(Sheet 10 of 10)

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX A10

R76	Same as R7			
R77 Thru R79	Same as R1			
R80	Same as R7			
R81	Same as R7			
R82	Resistor, Fixed: 6.8 M, 5%, 1/10 W	1	841414-165	14632
R83	Same as R6			
R84	Same as R7			
R85	Same as R1			
R86	Same as R1			
R87	Same as R34			
R88	Same as R34			
S1	Switch, 8-position DIP	2	ADP-08S	95146
S2	Same as S1			
T1	Transformer	1	9100-4226	28480
U1	Microprocessor Unit, 3.0 MHz	1	HD63C09P	62786
U2	Multivibrator	1	8674HC123SO16N	14632
U3	Microprocessor Supervisory Circuit	1	MAX691CWE	9AA13
U4	Magnitude Comparator	1	8674HC682SO20W	14632
U5	Hex Inverter	2	8674HC04SO14U	14632
U6	Quad 2-Input NAND Gate	2	8674HC00SO14U	14632
U7	Quad 2-Input OR Gate	6	8674HC32SO14U	14632
U8 Thru U10	Same as U7			
U11	Octal D-type Flip-flop	3	8674HC273SO20W	14632
U12	Same as U11			
U13	Same as U7			
U14	Same as U7			
U15	Encoder	2	8674HC148SO16U	14632
U16	Same as U15			
U17	Quad 2-Input Data Selector	1	8674HC157SO16U	14632
U18	EPROM, Unprogrammed	1	8627C512-15U	14632
U19	Same as U6			
U20	Quad 2-Input AND Gate	1	8674HC08SO14U	14632
U21	Tri-State Octal D-Type Latch	2	8674HC373SO20W	14632
U22	Same as U21			
U23	RAM	1	8662256LFP-12SLT	14632
U24	Decoder	3	8674HC138SO16U	14632
U25	Same as U24			
U26	Same as U24			
U27	DUART	2	SCC2692AC1A44	18324
U28	Same as U5			

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX A10

U29	Bus Transceiver	3	8675176SO8N	14632
U30	Interface	2	MAX232CWE	9AA13
U31	Octal Tri-State Buffer	2	8674HC244SO20W	14632
U32	Same as U31			
U33	Same as U11			
U34	HPIL Interface	1	ILB3-0002	28480
U35	Voltage Regulator	1	MC78M05CDT	04713
U36	Same as U27			
U37	Same as U29			
U38	Same as U29			
U39	Same as U30			
U40	Switch, SPST	1	DG412DY	17856
VR1	Diode, Zener	4	MMBZ5236BLT1	04713
VR2				
Thru	Same as VR1			
VR4				
XU1	Socket, 40 Pin	1	40-6518-00	51167
XU18	Socket	1	IC61-0324-033	NEPEN
Y1	Crystal, Quartz: 12 MHz	1	NMS120	61441
Y2	Crystal, Quartz: 3.6864 MHz	1	NMS037-20	61441

FOLDOUTS

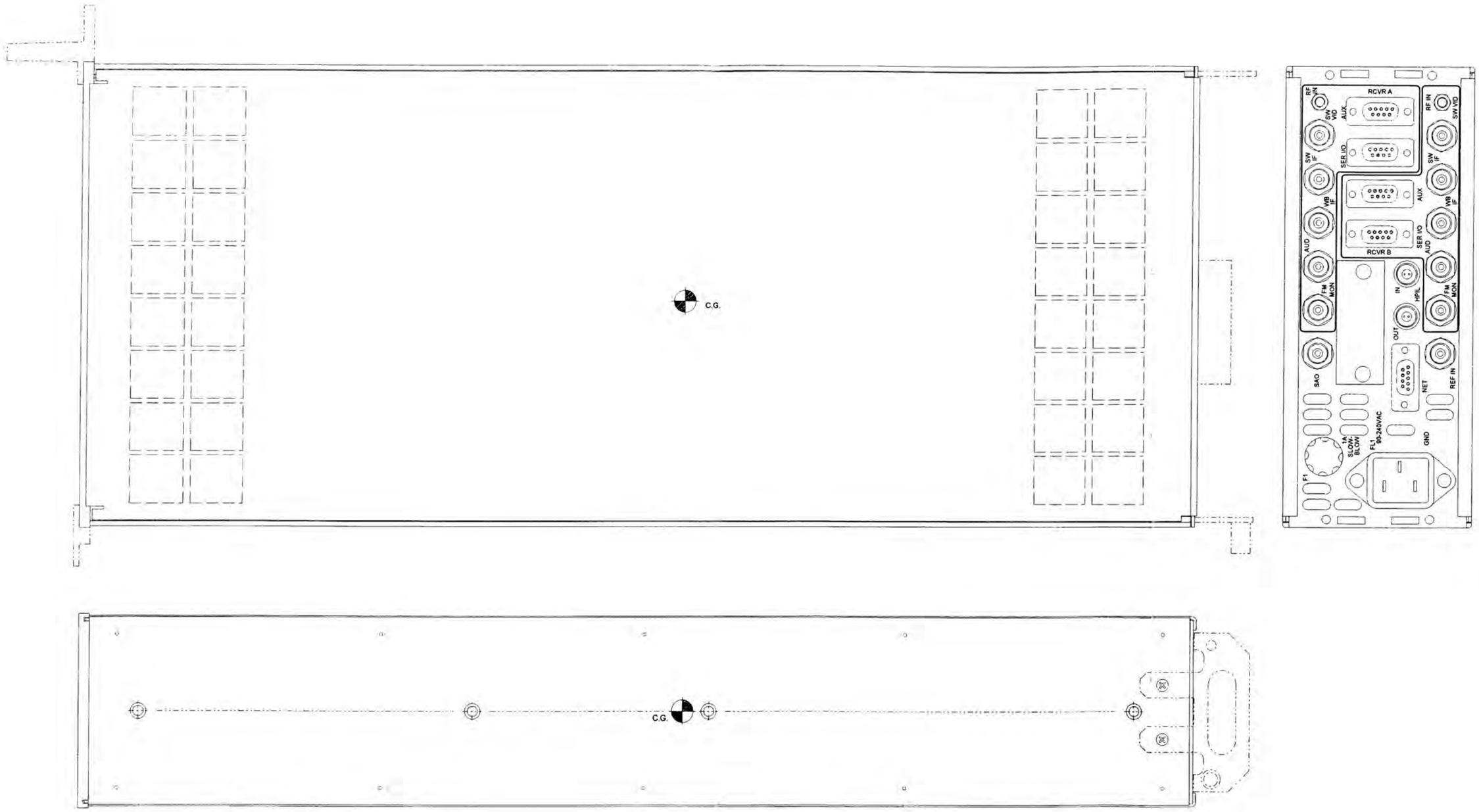
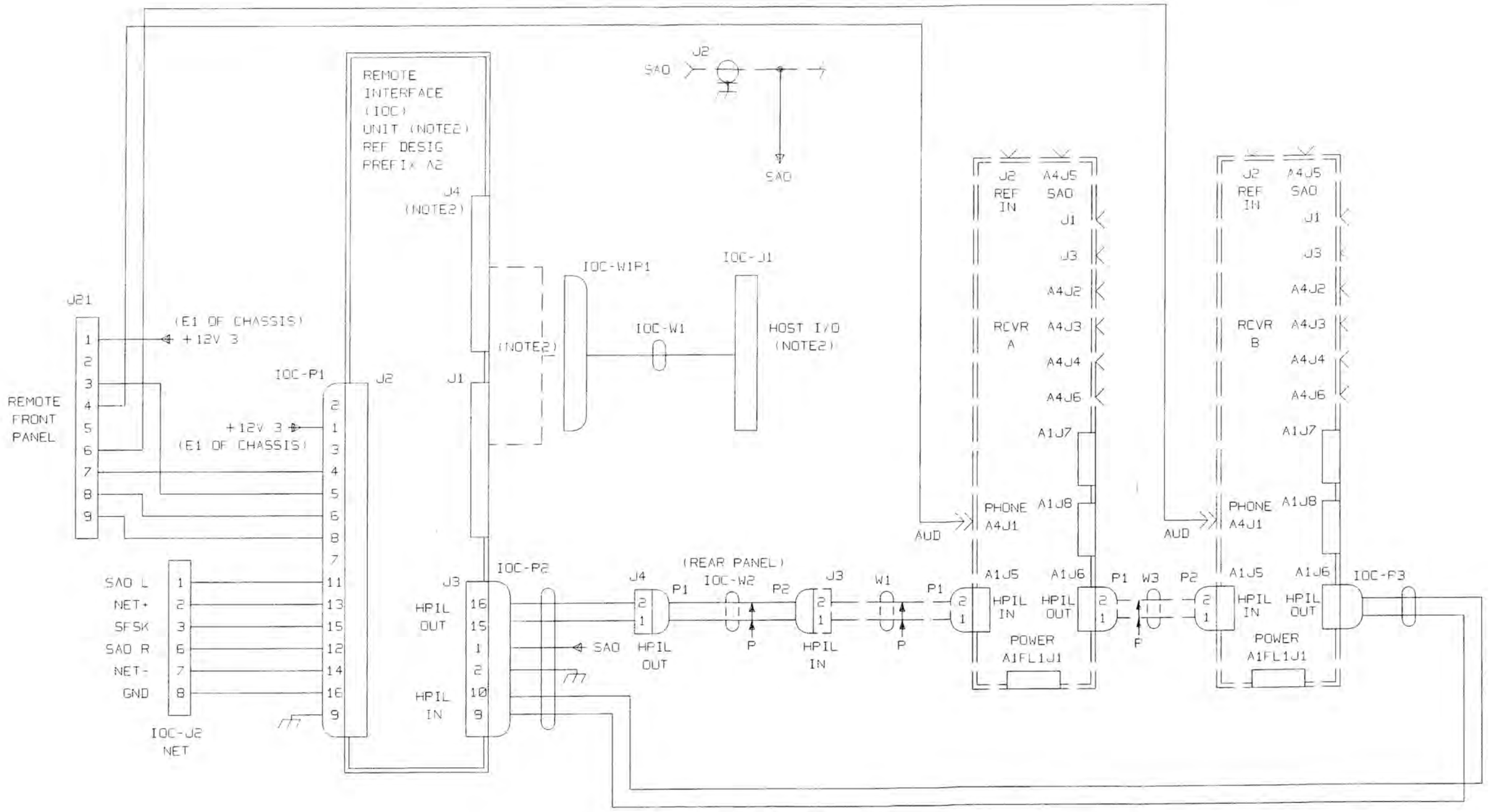


Figure FO-1. Type WJ-9902A Equipment Frame Outline Drawing 483038 (A) FP-1/(FP-2 blank)



NOTES:

1. DOTTED LINES INDICATE EXISTING MODULES/ASSY.
2. SEE TABLE FOR UNIT NUMBER ASSIGNMENT.

UNIT	HOST I/O	TYPE NO.	SCHEM	IOC-W1P1	A2J4
WJ9902/488	IEEE-488	796896-1	581103	TO A2J1	N/A
WJ9902/232	RS-232	796902-1	581108	TO A2J1	INSTALLED
WJ9902/422	RS-422	796902-1	581108	TO A2J4	INSTALLED

Figure FO-2. Type WJ-9902A Remote Interface Diagram Schematic Diagram 481830 (D)

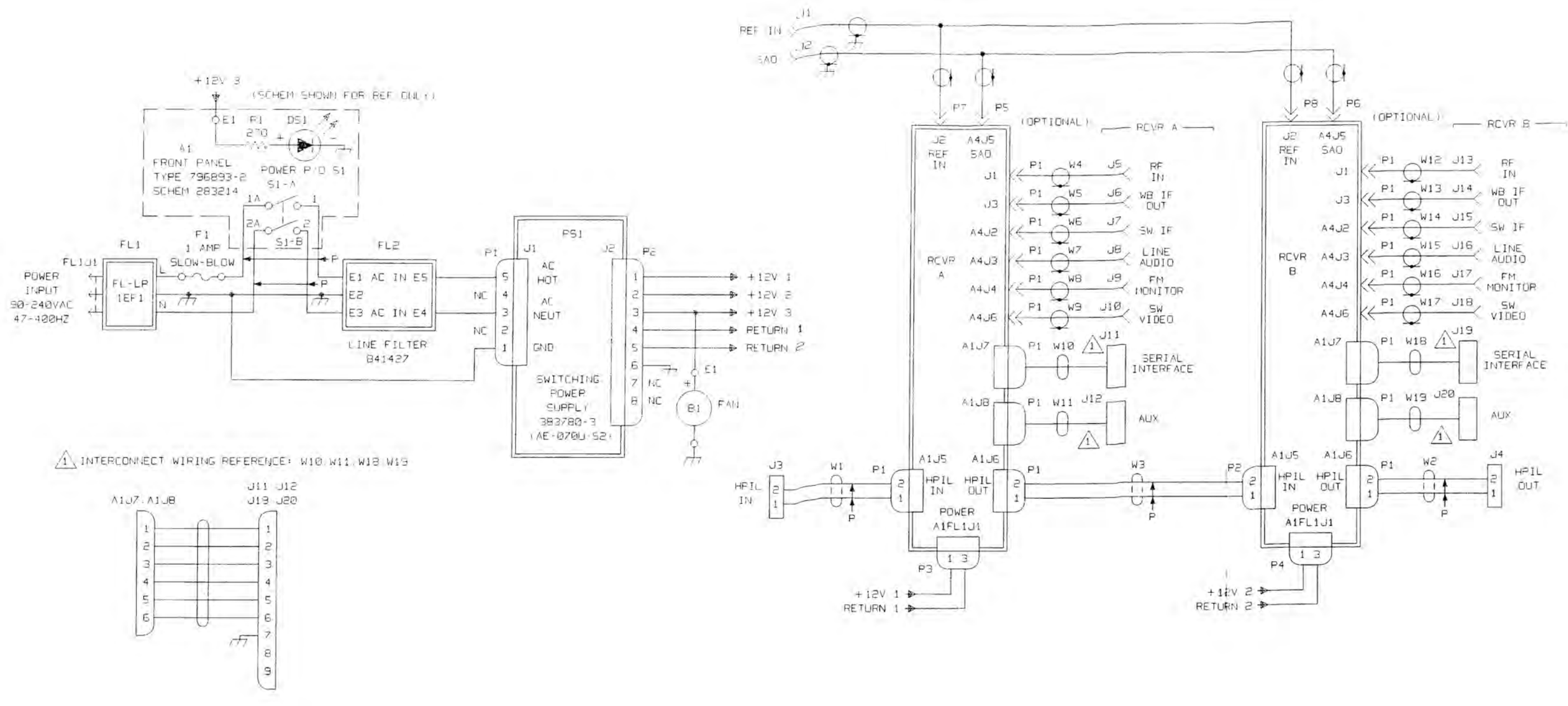


Figure FO-3. Type WJ-9902A Equipment Frame Interconnection Diagram Schematic Diagram 483039 (A)

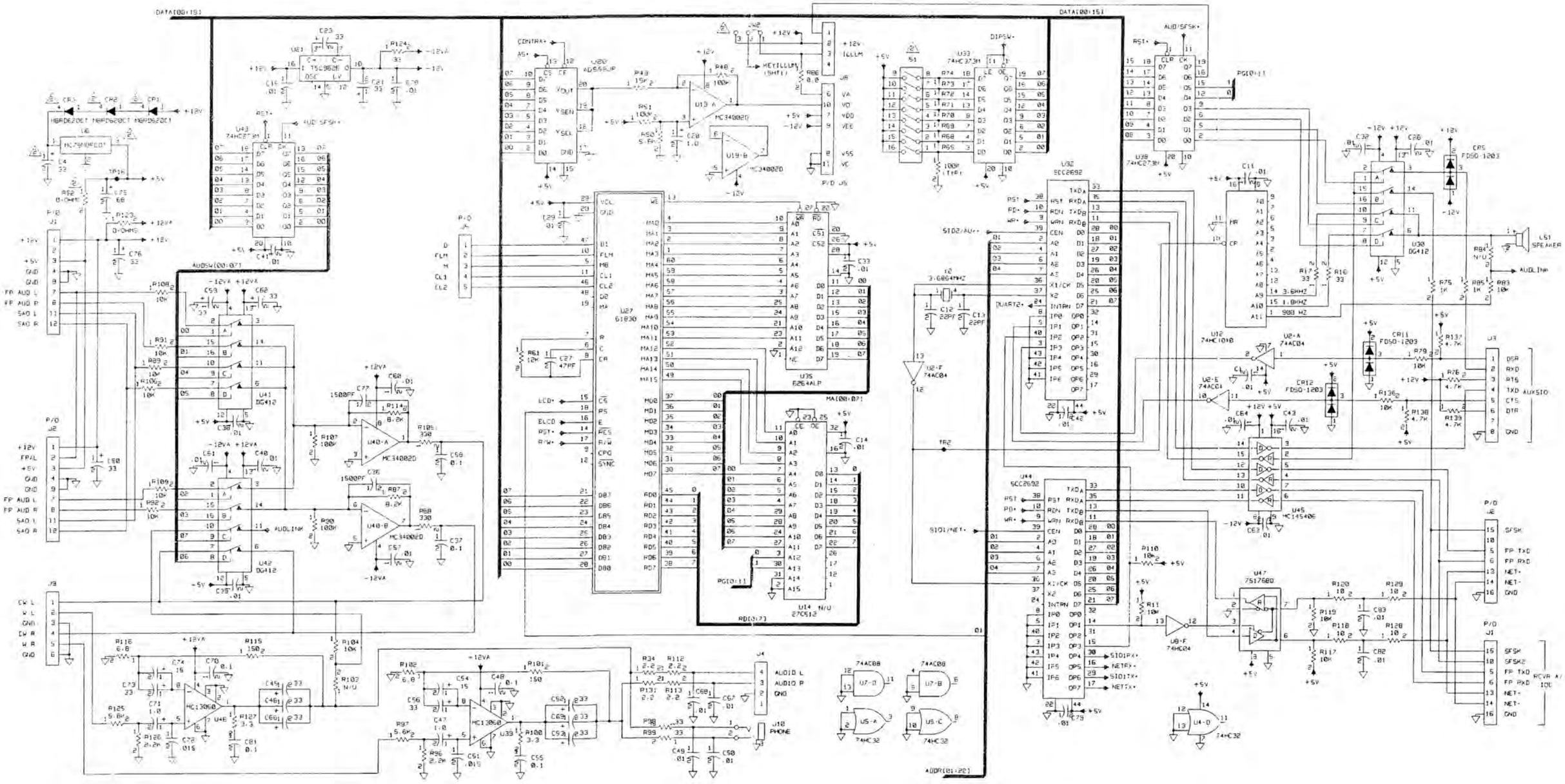
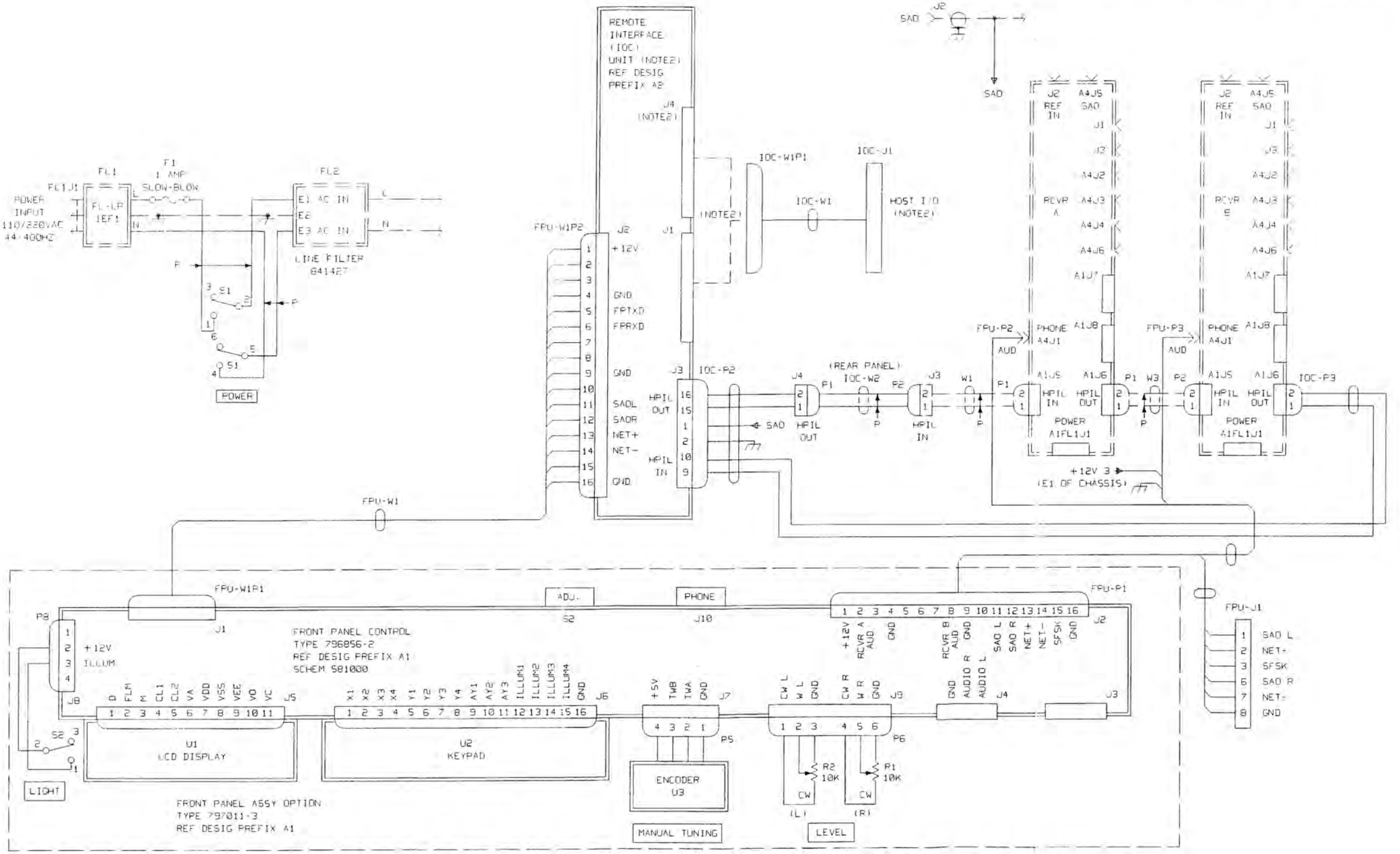


Figure FO-A-1. Type 796856-2 Front Panel Controller Assembly (A1A1) Schematic Diagram 581000 (Sheet 2 of 2) (E)

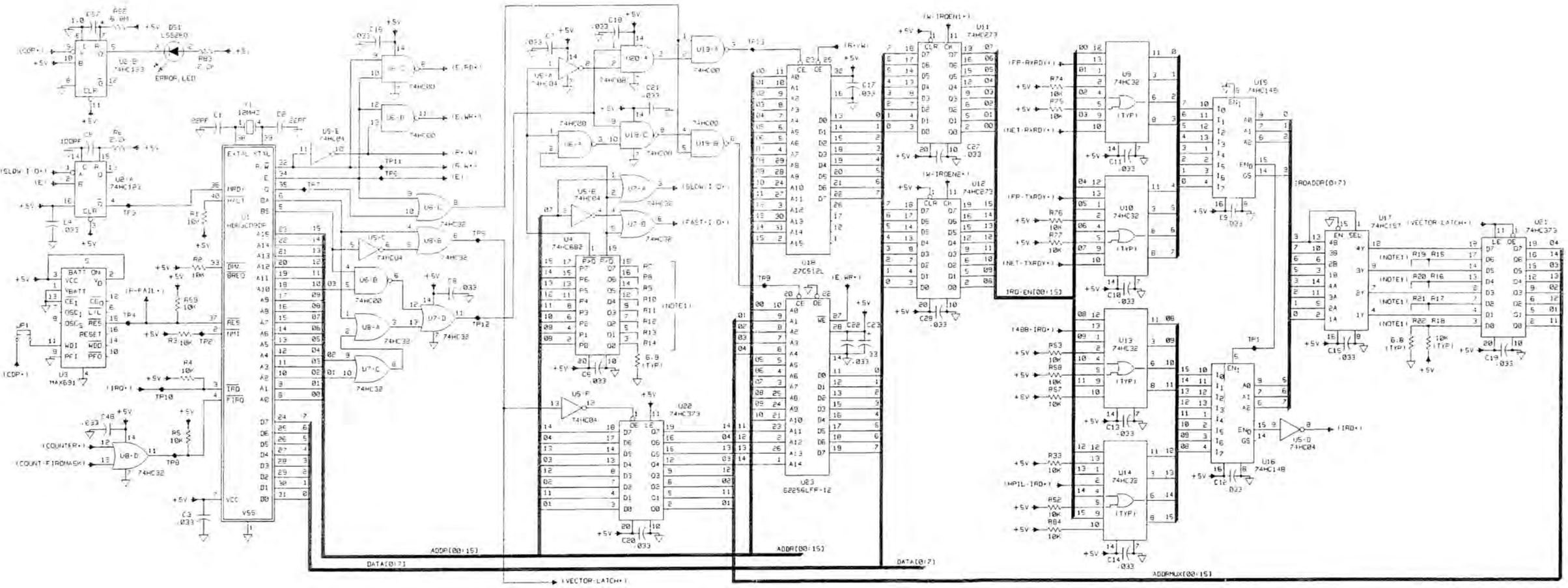


NOTES:

1. EXCEPT FOR ASSY A1, DOTTED LINE INDICATES EXISTING MODULES/ASSY.
2. SEE TABLE FOR UNIT NUMBER ASSIGNMENT.

UNIT	HOST I/O	TYPE NO.	SCHEM	IOC-W1P1	A2J4
WJ9902/488	IEEE-488	796896-1	581103	TO A2J1	N/A
WJ9902/232	RS-232	796902-1	581108	TO A2J1	INSTALLED
WJ9902/422	RS-422	796902-1	581108	TO A2J4	INSTALLED

Figure FO-A-2. Type WJ-9902/FPU Interconnection Diagram Schematic Diagram 481831 (H)



TYPE	796896-1
R7	USED
R8	NOT USED
R9	NOT USED
R10	USED
R11	USED
R12	USED
R13	USED
R14	USED
R19	NOT USED
R20	USED
R21	NOT USED
R22	NOT USED

Figure FO-B-1. Type 796896-1 IOC 488 Remote Interface PC Assembly (A2) Schematic Diagram 581103 (Sheet 1 of 2) (D1)

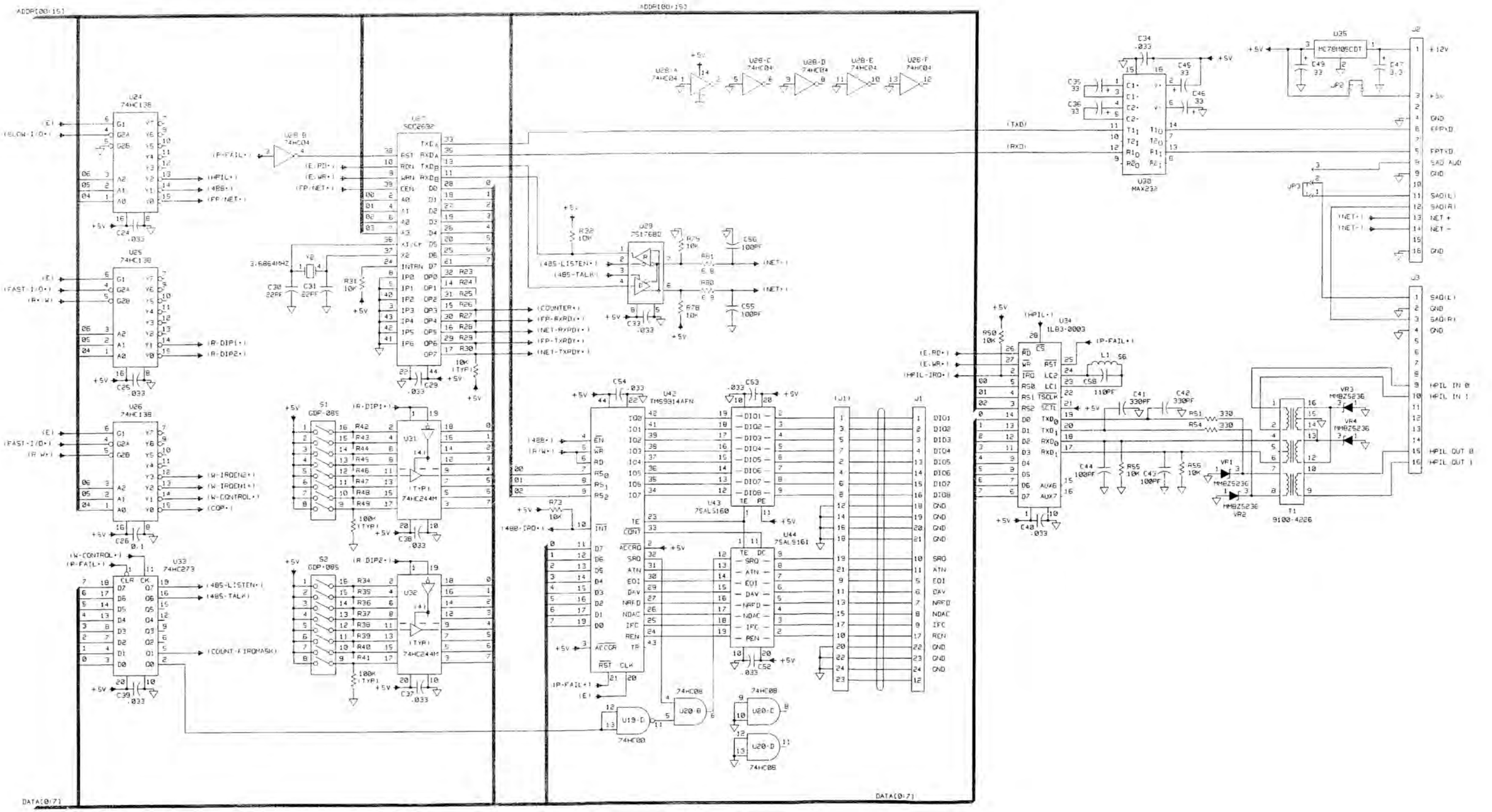
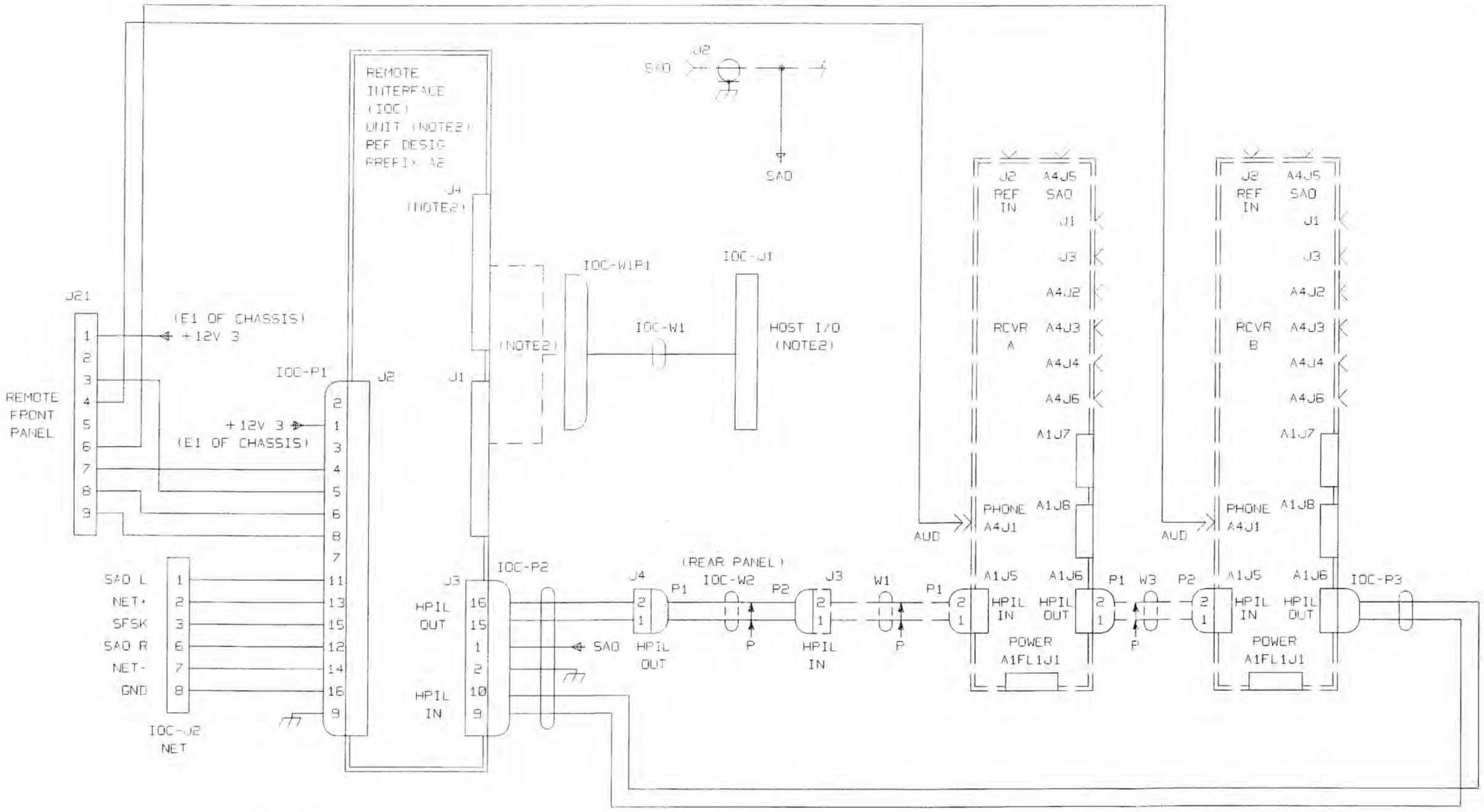


Figure FO-B-1. Type 796896-1 IOC 488 Remote Interface PC Assembly (A2) Schematic Diagram 581103 (Sheet 2 of 2) (D1)

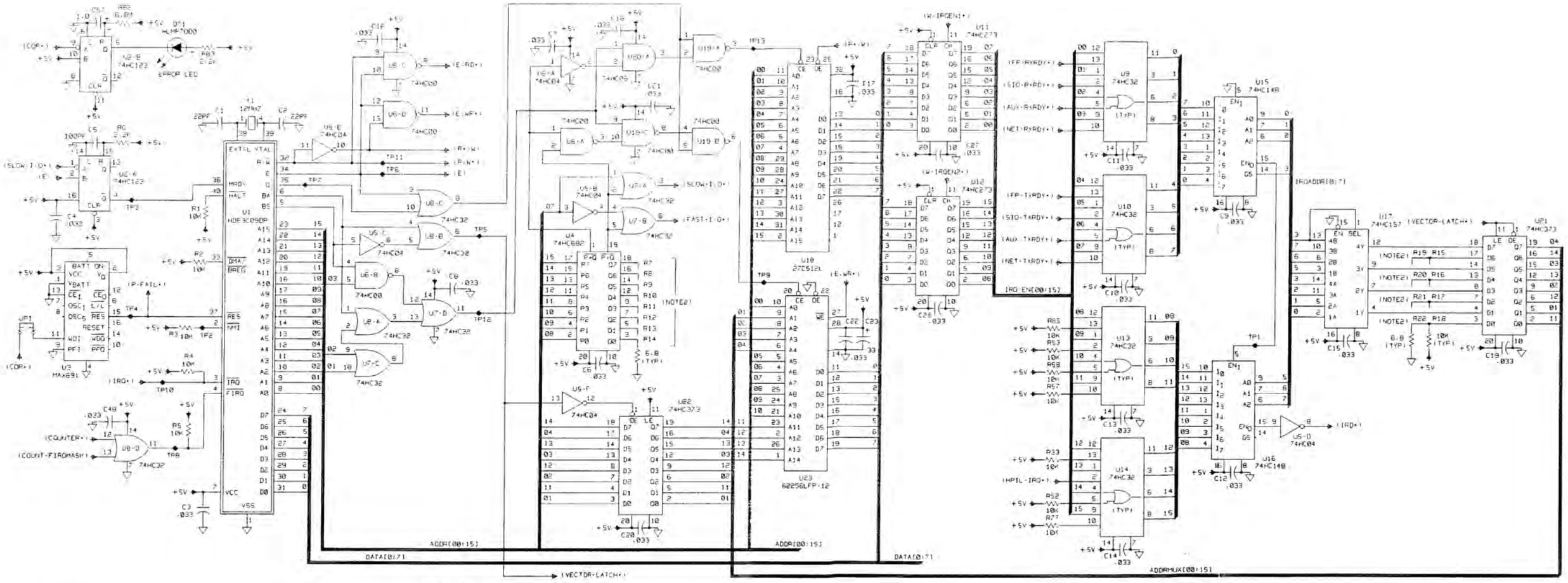


NOTES:

1. DOTTED LINES INDICATE EXISTING MODULES/ASSY.
2. SEE TABLE FOR UNIT NUMBER ASSIGNMENT.

UNIT	HOST I/O	TYPE NO.	SCHEM	IOC-W1P1	A2J4
WJ9902/488	IEEE-488	796896-1	581103	TO A2J1	N/A
WJ9902/232	RS-232	796902-1	581108	TO A2J1	INSTALLED
WJ9902/422	RS-422	796902-1	581108	TO A2J4	INSTALLED

Figure FO-B-2. Type WJ-9902/488 Host Interface Option Schematic Diagram 481830 (D)



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A) RESISTANCE IS IN OHMS ±5%, 1/8W.
   B) CAPACITANCE IS IN µF.
2. SEE TABLE A FOR USAGE.

TABLE A

TYPE	796902-1
R7	USED
R8	NOT USED
R9	NOT USED
R10	USED
R11	USED
R12	USED
R13	USED
R14	USED
R19	NOT USED
R20	USED
R21	NOT USED
R22	NOT USED

Figure FO-C-1. Type 796902-1 IOC-SIO Remote Interface PC Assembly (A10) Schematic Diagram 581108 (Sheet 1 of 2) (A)

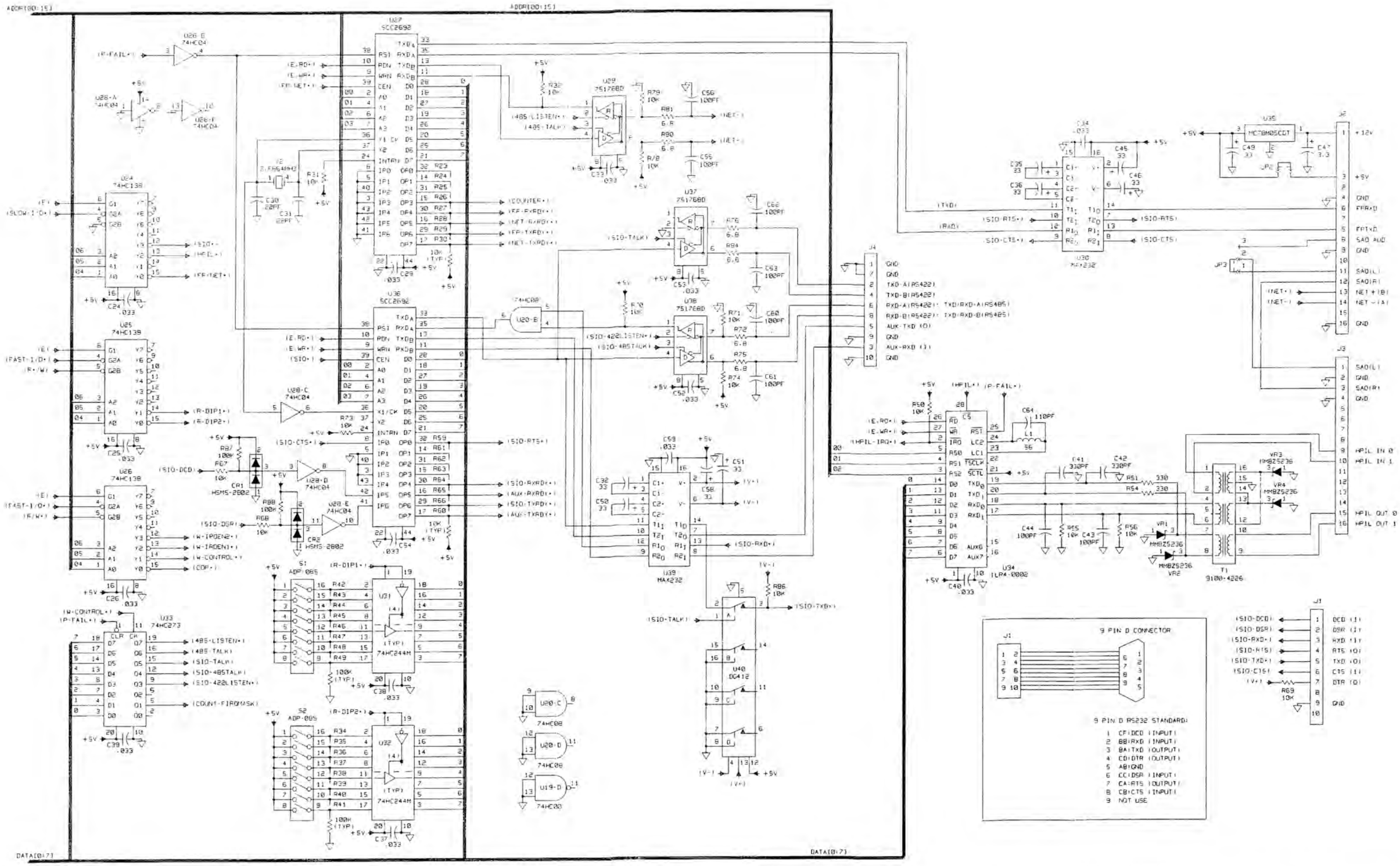


Figure FO-C-1. Type 796902-1 IOC-SIO Remote Interface PC Assembly (A10) Schematic Diagram 581108 (Sheet 2 of 2) (A)

NOTES:

1. DOTTED LINES INDICATE EXISTING MODULES/ASSY.
2. SEE TABLE FOR UNIT NUMBER ASSIGNMENT.

UNIT	HOST I/O	TYPE NO.	SCHEM	IOC-W1P1	A2J10
9908/488	IEEE-488	796896-1	581103	TO A10J1	N/A
9908/232	RS-232	796902-1	581108	TO A10J1	INSTALLED
9908/422	RS-422	796902-1	581108	TO A10J4	INSTALLED

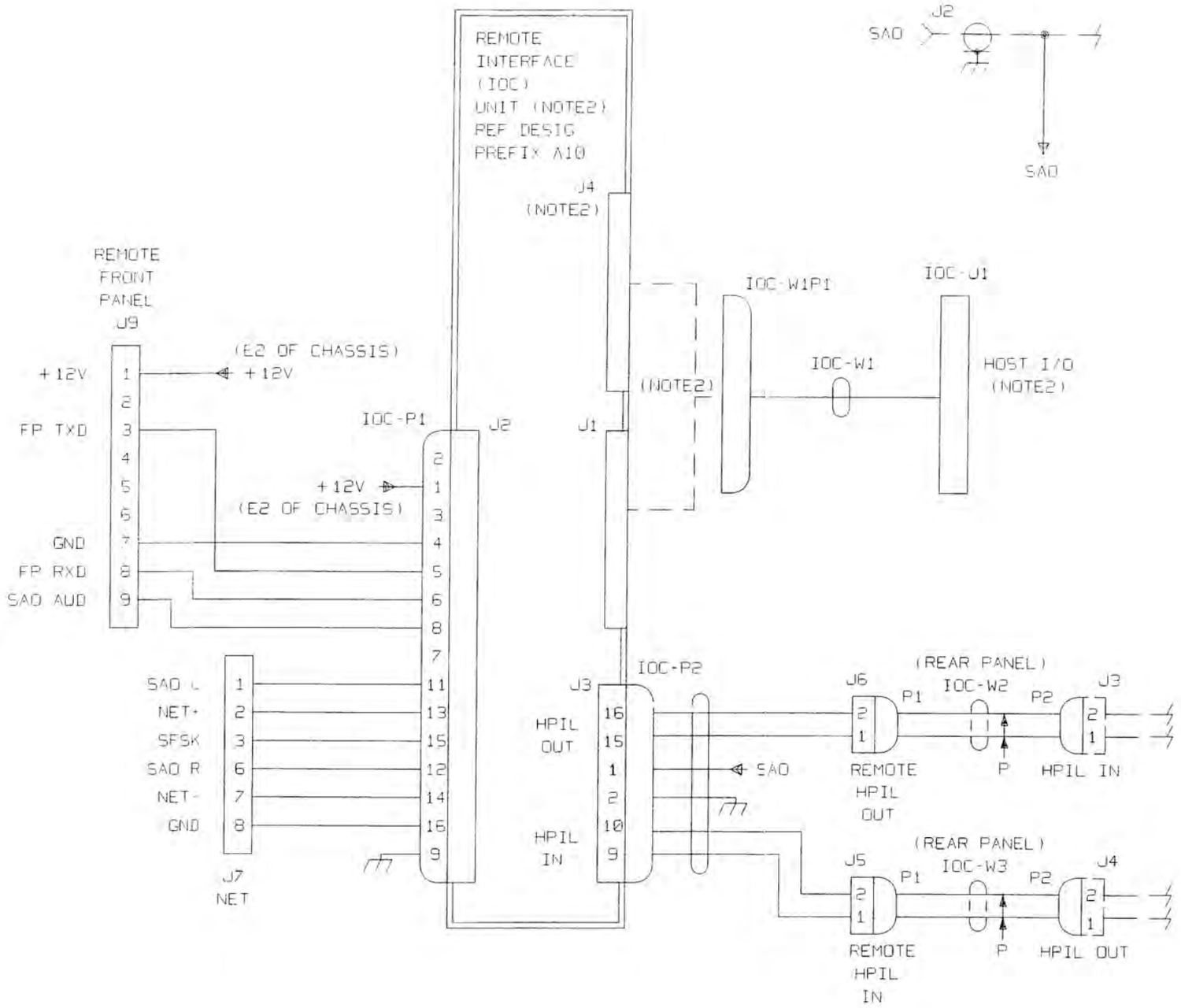


Figure FO-C-2. Type WJ-9902A Remote Interface Interconnection Schematic Diagram 481836 (E)