INSTRUCTION MANUAL

FOR

WJ-9040 SYSTEM COMMON EQUIPMENT

WATKINS-JOHNSON COMPANY
700 QUINCE ORCHARD ROAD
GAITHERSBURG, MARYLAND 20878-1794

October 1990

PROPRIETARY STATEMENT

WARNING

This equipment employs dangerous voltages which may be fatal if contacted. Exercise extreme caution in working with this equipment with any of the protective covers removed.

WARNING

Ensure the EPS Power Supply is set up properly for the correct 115 or 230 VAC setting prior to connecting power to the WJ-9040 System. Set the EPS100A's line voltage selector switch S2 to the 115 V position (left) or the 230 V position (right) in accordance with the line voltage being used.

EQUIPMENT MALFUNCTIONS

This unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. If an apparent malfunction is encountered after installation, verify that the correct input signals are present at the proper connectors. Prior to taking any corrective maintenance action or breaking any seals, contact your Watkins-Johnson representative, or the Watkins-Johnson Company Service Department to prevent the possibility of voiding the terms of the warranty. Contact the Watkins-Johnson Company via mail, telephone, wire, or cable at:

Watkins-Johnson Company
Company Service Department
700 Quince Orchard Road
Gaithersburg, Maryland 20878-1794

Toll Call: (301) 948-7550 Ext. 7201
TELEX: 89-8402
TWX: 710-828-0546
TELEFAX: (301) 921-9479
EASYLINK: 62928185

If reshipment is necessary, follow the instructions in the following paragraph (Preparation for Reshipment or Storage). Do not return the equipment until a Return for Maintenance Authorization (RMA) number has been obtained from the Watkins-Johnson Company's Customer Service Department. See Item 10 in the **General Terms and Conditions of Sale** paper (WJ Form # WJ-151-X) for more information on equipment returns.

PREPARATION FOR RESHIPMENT OR STORAGE

If the unit must be prepared for reshipment, the packaging method should follow the pattern established in the original shipment. Use the best packaging materials available to protect the unit during reshipment or storage. When possible, use the original packing container and cushioning materials. If the original packing materials are not available, use the following procedure:

1. Wrap the unit in sturdy paper or plastic.

2. Place the wrapped unit in a strong shipping container and place a layer of shock-absorbing material (3/4-inch minimum thickness) around all sides of the unit to provide a firm cushion and to prevent movement inside the container.

3. If shipping the unit for service, fill out all information on the 5x6 PRODUCT DISCREPANCY REPORT card (WJ Form # WJC-QA55-0) that was provided with the original shipment. Also ensure that the Return for Maintenance Authorization (RMA) number is recorded on the card. If this card is not available, attach a tag to the unit containing the following information:

   a. Return for Maintenance Authorization (RMA) number.
   b. The Watkins-Johnson Type/Model number of the equipment.
   c. Serial number.
   d. Date received.
   e. Date placed in service.
   f. Date of failure.
   g. Warranty adjustment requested, yes or no.
   h. A brief description of the discrepant conditions.
   i. Customer name and return address.
   j. Original Purchase Order/Contract number.

4. Thoroughly seal the shipping container and mark it **FRAGILE.**

5. Ship to:

   Watkins-Johnson Company
   700 Quince Orchard Road
   Gaithersburg, Maryland 20878-1794
   U.S.A

When storing the equipment for extended periods, follow the above packing instructions to prevent damage to the equipment. The safe limits for storage environment are:

Temperature: -40 to +70°C
Humidity: less than 95%

INSTRUCTION MANUAL FOR WJ-9040 COMMON EQUIPMENT

REVISION RECORD

REVISION	DATE	DESCRIPTION
A	4/86	Initial Revision Level Assigned
B	3/89	Incorporated changes to the system configuration (EPS100A) and to the WJ-9040 IOM108's CPU (A5) and System I/O (A3)
C	8/89	Corrected errata in the Replacement Parts List. Reflected addition of 10 MHz external reference input to the SRM105A
D	3/90	Corrected errata concerning proper procedure for selecting AC line voltage in the EPS100A.
E	10/90	Add SRQ information

WJ-9040 SYSTEM COMMON EQUIPMENT
REVISION A CHANGE 1

TITLE: INSTRUCTION MANUAL FOR THE WJ-9040 SYSTEM COMMON EQUIPMENT

MANUAL DATE: October 1990

CHANGE 1 DATE: May 1991

APPLICABILITY: All units.

CHANGES/ERRATA INFORMATION: Changes refer to updates of the instruction manual to cover design modifications. Errata refer to corrections to and clarifications of information in the manual.

CHANGE 1 SUMMARY: This change corrects adds information on the serial I/O Switch settings.

ERRATA: Add this table to **paragraph 2.4.4.1.**

Table 2-8A. Serial I/O Setup Procedures

Switch	Settings	
S1	CLOSED = 0;	OPEN = 1
S2	CLOSED = 0;	OPEN = 2
S3	CLOSED = 0;	OPEN = 4
S4	CLOSED = 0;	OPEN = 8
S5	X	
S6	X	
S7	X	
S8	CLOSED = 0;	TERMINATION ON
	OPEN = 0;	NO TERMINATION
X = DON'T CARE		

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SECTION I

GENERAL DESCRIPTION

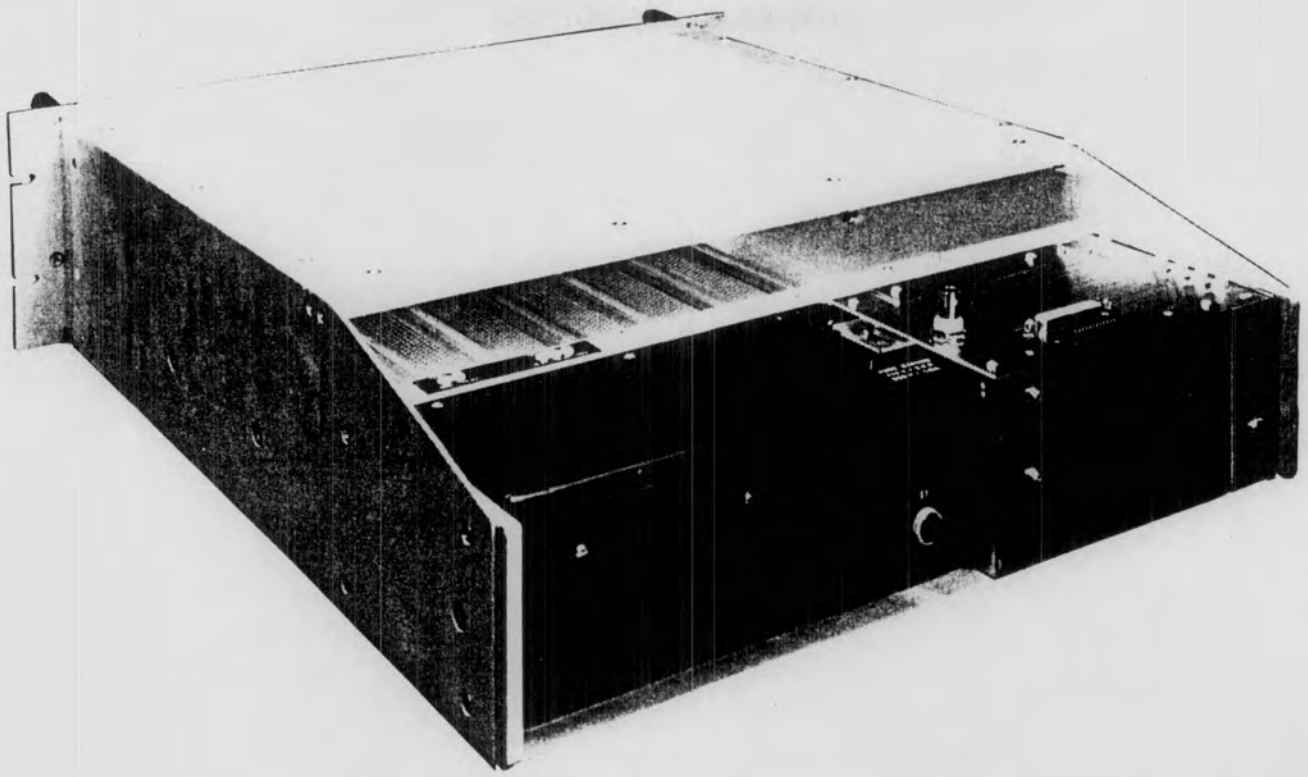


Figure 1-1. WJ-9040 System Common Equipment (3/4 Rear View)

SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The WJ-9040 System Common Equipment (**Figure 1-1**) is the basic building block of the WJ-9040 System. The WJ-9040 System hardware is a compatible family of functional units in modular form. These modules are supported by the EFR100 Equipment Frame to effect the necessary control, interface, power and signal routing. Common module size, power and control along with unique module identifier codes allow for the addition, removal or change of any module in any position in the frame.

The unit consists of a frame in which the system modules are mounted and a backplane which provides the modules with power and control signals. At the rear of the frame the EPS100A Power Supply, the IOM108 I/O Control Module and the SRM105A Site Reference Module are mounted. All wiring within the frame is accomplished by the use of a flexible printed circuit board.

The IOM108 I/O Control Module is the central point of interface within the equipment frame. It serves as an input/output port for both control signals and module output signals. In addition, the IOM108 performs all "housekeeping" functions within the frame. All programs required for interface to any WJ-9040 module are stored in ROM within the IOM108. The IOM108 implements system control via a high speed serial I/O port or through optional IEEE-488/RS-232 ports. In addition, a 25 pin D-series connector provides polled module outputs to the user and has audio selection and distribution capabilities.

The EPS100A Power Supply Module supplies +8.2 Vdc, ±18.3 Vdc and +29 Vdc to all WJ-9040 modules through the equipment frame. The EPS100A utilizes a high efficiency switching mode design and employs a power line filter and short circuit protection. A pushbutton power switch/indicator is located at the rear of the units AC input receptacle.

The SRM105A Frequency Reference Module provides four highly stable, 50 MHz signals to any WJ-9040 module requiring a frequency reference for proper operation. The unit receives power from the EPS100A Power Supply and uses a stable, temperature compensated crystal oscillator to provide the four outputs. An output splitter and buffer amplifier provide high isolation. In addition, the SRM105A is capable of locking to a 1, 5, or 10 MHz site reference for applications requiring accuracy beyond that provided by the basic SRM105A.

1.2 MECHANICAL CHARACTERISTICS

The WJ-9040 System Common Equipment mounts in a standard 19-inch rack cabinet and occupies a maximum of 20 inches of depth. The frame accepts up to eight eighth-rack, four quarter-rack, or two half-rack modules. The frame is equipped with mounting modules for slides or brackets, thus allowing easy rack mounting. Handles are supplied at the front of the frame to improve transportability.

The IOM108 I/O Control Module is mounted in the rear of the equipment frame. The main chassis and top cover are constructed of brass and plated with nickel. The front panel mounts a 37 pin D-series connector that interfaces the IOM108 with the equipment frame. The WJ-9040 serial interface is a BNC connector accessible through the top cover. The user polled I/O connector and optional IEEE-488 or RS-232 connector are also accessible through the top cover.

The EPS100A Power Supply is mounted on the rear of the equipment frame. The unit is fabricated from extruded 16 gauge aluminum. The front panel mounts a 25 pin D-series connector that distributes DC power to the equipment frame. Ventilating holes punched in the top and bottom covers provide convection cooling for the power supply, eliminating the need for blowers.

The SRM105A Site Reference Module is mounted on the rear of the equipment frame. The main chassis and side cover area is constructed of brass and plated with nickel. The front panel mounts a 25 pin D-series connector that supplies DC power to the SRM105A. The top panel mounts four SMA series female coaxial connectors that provide the 50 MHz reference outputs.

1.3 OPERATIONAL OVERVIEW

The WJ-9040 System Common Equipment is the major WJ-9040 interface unit designed to provide multiple control of system modules or equipment frames. **Figure 1-2** is a simplified block diagram showing the relationship between the major elements of the WJ-9040 System. All data transfer between system modules and equipment frames is provided by the IOM108 I/O Control Module and is accomplished through program controlled I/O. The IOM108 implements data transfer by two primary sources:

- Data transfer between system modules, within an equipment frame, is accomplished by five signal lines comprising the EFR100 backplane control/data bus. Data is transferred serially via the data in and data out lines. Addressed Enable B is used to enable one of the eight slots in the frame for communication.

- Data transfer between equipment frames, in the WJ-9040 System, is accomplished by the IOM108 high speed serial I/O port. Data is transferred bidirectionally via the serial I/O port. The first frame functions as an initiator while the second frame functions as a responder.

1.4 EQUIPMENT SUPPLIED

The following items are supplied with the unit:

- EFR100 Equipment Frame
- IOM108 I/O Control Module
- EPS100A Power Supply
- SRM105A Site Reference Module
- WJ-9040 System Common Equipment Instruction Manual

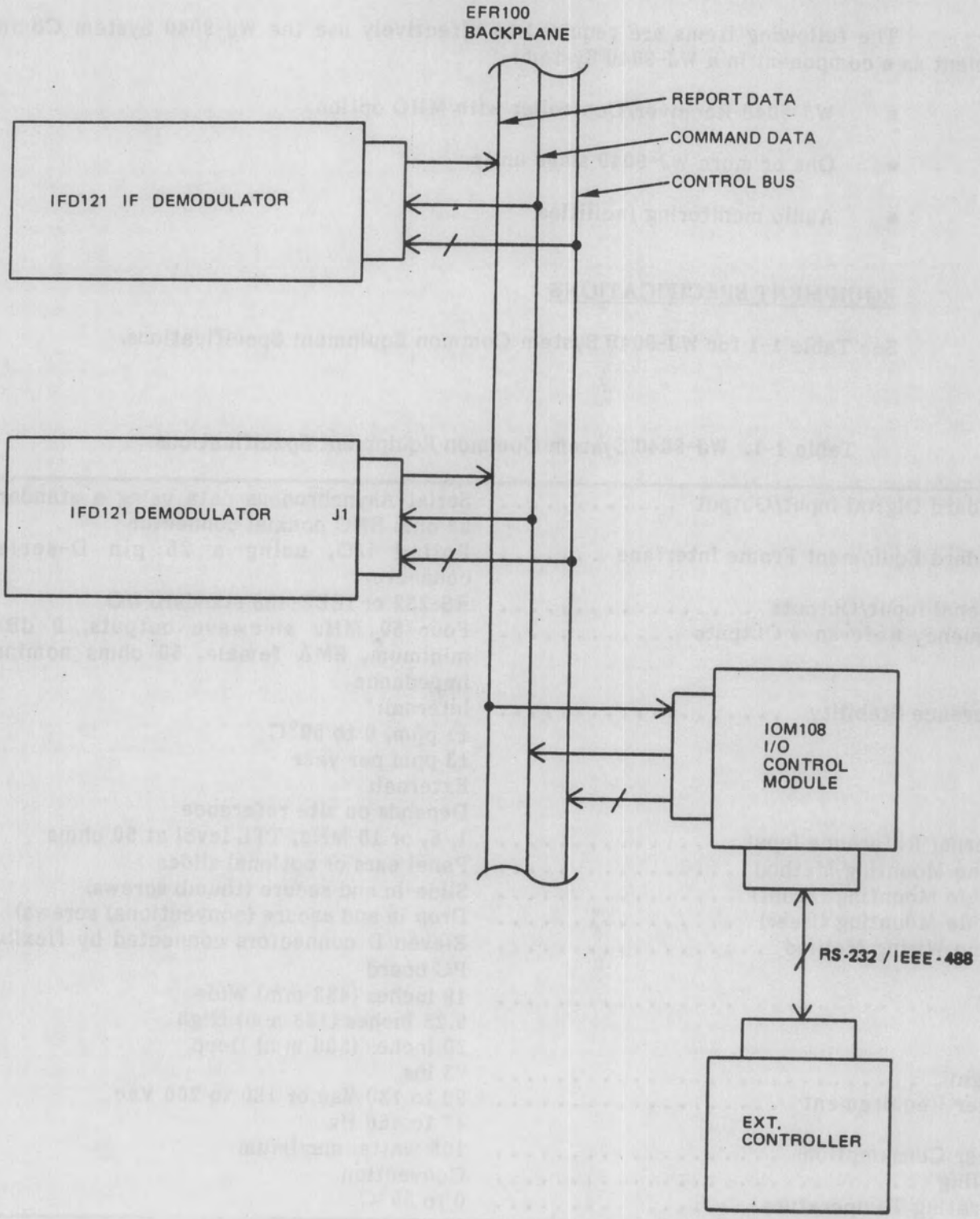


Figure 1-2. WJ-9040 System Configuration

1.5 EQUIPMENT REQUIRED BUT NOT SUPPLIED

The following items are required to effectively use the WJ-9040 System Common Equipment as a component in a WJ-9040 System:

- WJ-9040 Receiver/Controller with MHO option
- One or more WJ-9040 slave units
- Audio monitoring facilities

1.6 EQUIPMENT SPECIFICATIONS

See **Table 1-1** for WJ-9040 System Common Equipment Specifications.

Table 1-1. WJ-9040 System Common Equipment Specifications

Standard Digital Input/Output	Serial Asynchronous data using a standard 50 ohm BNC coaxial connector
Standard Equipment Frame Interface	Polled I/O, using a 25 pin D-series connector
Optional Input/Outputs	RS-232 or IEEE-488 standard I/O
Frequency Reference Outputs	Four 50 MHz sinewave outputs, 0 dBm minimum, SMA female, 50 ohms nominal impedance
Reference Stability	Internal: ±1 ppm, 0 to 50°C ±3 ppm per year External: Depends on site reference
External Reference Input	1, 5, or 10 MHz, TTL level at 50 ohms
Frame Mounting Method	Panel ears or optional slides
Module Mounting (Front)	Slide-in and secure (thumb screws)
Module Mounting (Rear)	Drop in and secure (conventional screws)
Frame Wiring Method	Eleven D connectors connected by flexible PC board
Size	19 inches (483 mm) Wide 5.25 inches (133 mm) High 20 inches (508 mm) Deep
Weight	23 lbs.
Power Requirement	90 to 130 Vac or 180 to 260 Vac 47 to 450 Hz
Power Consumption	105 watts, maximum
Cooling	Convection
Operating Temperature	0 to 50°C

SECTION II

INSTALLATION AND OPERATION

SECTION II

INSTALLATION AND OPERATION

2.1 UNPACKING AND INSPECTION

Examine the shipping carton for damage prior to unpacking the equipment. If the carton appears to be damaged, have the carrier's agent present when the equipment is unpacked. If this is not possible, retain all packaging material and shipping containers for the carrier's inspection to verify damage to the equipment after unpacking. Also ensure that the equipment shipped corresponds to the packing slip. Contact the Watkins-Johnson Company, CET Division, or your Watkins-Johnson representative for any discrepancies or shortages.

The unit was thoroughly inspected and factory-adjusted for optimum performance prior to shipment. It is therefore ready for use upon receipt. After uncrating and checking the contents against the packing slip, inspect all exterior surfaces for dents and scratches. If external damage is visible, remove the dust covers and inspect the internal components for apparent damage. Then check the internal cables for loose connections, and plug-in items such as printed wiring boards, which may have been loosened from their receptacles.

2.2 PREPARATION FOR RESHIPMENT AND STORAGE

If the equipment must be prepared for reshipment, follow the packing methods of the original shipment. Retain the original materials for the repackaging effort. Conditions during storage and shipment should be limited as follows:

- Maximum Humidity: 95% (no condensation)
- Temperature Range: -40°C to +85°C

2.3 INSTALLATION PROCEDURES

Watkins-Johnson equipment is designed for use when the operational temperature is between 0 and +50°C. Equipment installation should provide for free-flowing air circulation around and through ventilated units. Multiple stacking of electronic equipment in a standard console can produce an appreciable increase in operating temperature for all equipment contained within the console. Forced-air ventilation may be necessary to maintain proper air circulation and temperature for efficient operation of the equipment. The following paragraphs detail the procedures for installing the four units comprising the WJ-9040 System Common Equipment.

2.3.1 EQUIPMENT FRAME INSTALLATION

The WJ-9040 EFR100 Equipment Frame is designed for installation in 19-inch racks in accordance with MIL-STD-189 or E.I.A. Standard RS-310. It is recommended that chassis slides be added to the racks for ease of assembly, access to the unit and to provide adequate support for general installations. Mobile installation of the frame should be evaluated on an individual basis.

Rear panel access is essential for making or changing input and output connections and installing or removing interface unit modules. **Table 2-1** lists the connectors associated with the equipment frame.

Table 2-1. EFR100 Frame Connectors

Reference Designator	Description	Connection
J1-J8	PWR, CONT/COMM	Plug in Module
J9	DC POWER IN	EPS100A
J10	I/O INTERFACE	IOM108
J11	PWR, AUX I/O	SRM105A

2.3.2 IOM108 INSTALLATION

Perform the following steps to install a single IOM108 on the EFR100 Equipment Frame.

1. Position the IOM108 near its mounting location at the rear of the EFR100.
2. Align the IOM108 connector, A1J1, with the EFR100 mate connector.
3. Slowly slide the IOM108 until contact is made with the EFR100 connector. At this point, apply extra pressure and seat the IOM108 in the EFR100 connector.
4. Secure the IOMI08 with four mounting screws installed at the bottom of the EFR100.

Rear panel access to the EFR100 Equipment Frame is essential for making or changing connections to the IOM108. **Table 2-2** lists the connectors associated with the IOM108.

Table 2-2. IOM108 I/O Interface Connectors

Reference Designator	Description	Connection
A1A1J1	RS-232/IEEE-488	Computer Controller
A1A2J1	Bidirectional Polled I/O	User Selected Interface Device
A1A3J1	Coax Serial I/O	WJ-9040 Controller
A1J1	PWR	A1J10 Equipment Frame

2.3.3 EPS100A INSTALLATION

WARNING

Ensure the correct line voltage on the EPS100A is selected prior to connecting the EPS100A to the AC power source. Set the EPS100A's line voltage selector switch S2 to the 115 V position (left) or the 230 V position (right) in accordance with the line voltage being used.

Perform the following steps to install a single EPS100A on the EFR100 Equipment Frame:

1. Position the EPS100A near its mounting location at the rear of the EFR100.
2. Align the EPS100A connector, J1, with the EFR100 mating connector.
3. Slowly slide the EPS100A forward until physical contact is made with the EFR100 connector. At this point, apply extra pressure and seat the EPS100A in the EFR100 connector.
4. Secure the EPS100A with six mounting screws installed at the bottom of the EFR100.

Access to the EFR100 Equipment Frame rear panel is essential for making or changing input and output connections to the EPS100A. The EPS100A Power Supply is equipped with two connectors, J1 and P1. Line cord connector, J1, plugs into an AC outlet and connector, P1, mates with the DC OUT connector, J9, on the equipment frame.

2.3.4 SRM105A INSTALLATION

Perform the following steps to install a single SRM105A on the EFR100 Equipment Frame.

1. Configure the SRM105A to use either the internal reference or an external 1 MHz, 5 MHz, or 10 MHz reference by setting DIP switch S1 in accordance with **Table 2-3** and **Figure 2-1.** The SRM105A is configured for use with the internal reference at the factory.
2. Position the SRM105A near its mounting location at the rear of the EFR100.
3. Align the SRM105A connector, A1J1, with the EFR100 mate connector.
4. Slowly slide the SRM105A until contact is made with the EFR100 connector. At this point, apply extra pressure and seat the SRM105A in the EFR100 connector.
5. Secure the SRM105A with two mounting screws installed at the bottom of the EFR100.

Table 2-3. Reference Generator Switch S1 Configuration

Reference Selection	S1A	S1B	S1C
External 1 MHz	UP	UP	DOWN
External 5 MHz	UP	DOWN	DOWN
External 10 MHz	DOWN	DOWN	DOWN
Internal 50 MHz	X	X	UP

X = Does Not Matter

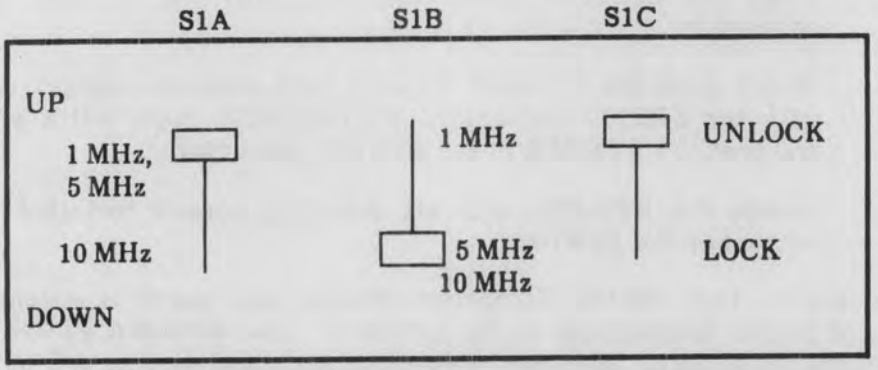


Figure 2-1. S1 DIP Switch Configuration

Access to the rear panel of the EFR100 Equipment Frame is essential for making or changing input and output connections. **Table 2-4** lists the connectors associated with the SRM105A.

Table 2-4. SRM105A Site Reference Module Connectors

Reference Designator	Description	Connection
J1-J4	50 MHz Reference Out	50 MHz Ref. Input Connector on WJ-9040 Receiver
A1J1	PWR IN	A1J11 on EFR100 Equipment Frame
J5	1, 5, 10 MHz Reference IN	Input from Optional External Reference

2.3.5 WJ-9040 MODULE INSTALLATION

The WJ-9040 System Common Equipment accepts up to eight eighth-rack, four quarter-rack, or two half-rack WJ-9040 type processing modules. Specific procedures for installing WJ-9040 modules are covered in the individual instruction manuals for those modules.

2.4 OPERATION

The following paragraphs are an operator's guide to the function and operation of the WJ-9040 System Common Equipment within the WJ-9040 System. It is recommended that **paragraph 1.3**, Operational Overview, be reviewed before reading the information in this paragraph.

2.4.1 INTRODUCTION

The WJ-9040 System Common Equipment is a major WJ-9040 interface unit designed to provide multiple control of system modules or equipment frames without requiring direct operator attention. The major active component of the Common Equipment is the IOM108 which provides software-controlled bidirectional data transfer between all remotely controllable units within the WJ-9040 System. **Figure 2-2** shows a basic WJ-9040 System configuration. System control may be effected by three different methods, described as follows:

- A WJ-9040 System Receiver/Controller may be installed in the EFR100. This unit can control its internal receiver and any other WJ-9040 System receivers within its equipment frame. The IOM108 provides the required handshaking and data transfer between modules.

- A computer terminal equipped for RS-232/IEEE-488 may be used. Using the WJ-9040 System commands, the terminal communicates with the equipment frame in ASCII format via the IOM108. The IOM108 provides the required handshaking and data exchange with the terminal, translates the data and controls the operation of the modules within an equipment frame. Command protocol and data format is provided in **paragraph 2.4.3.**

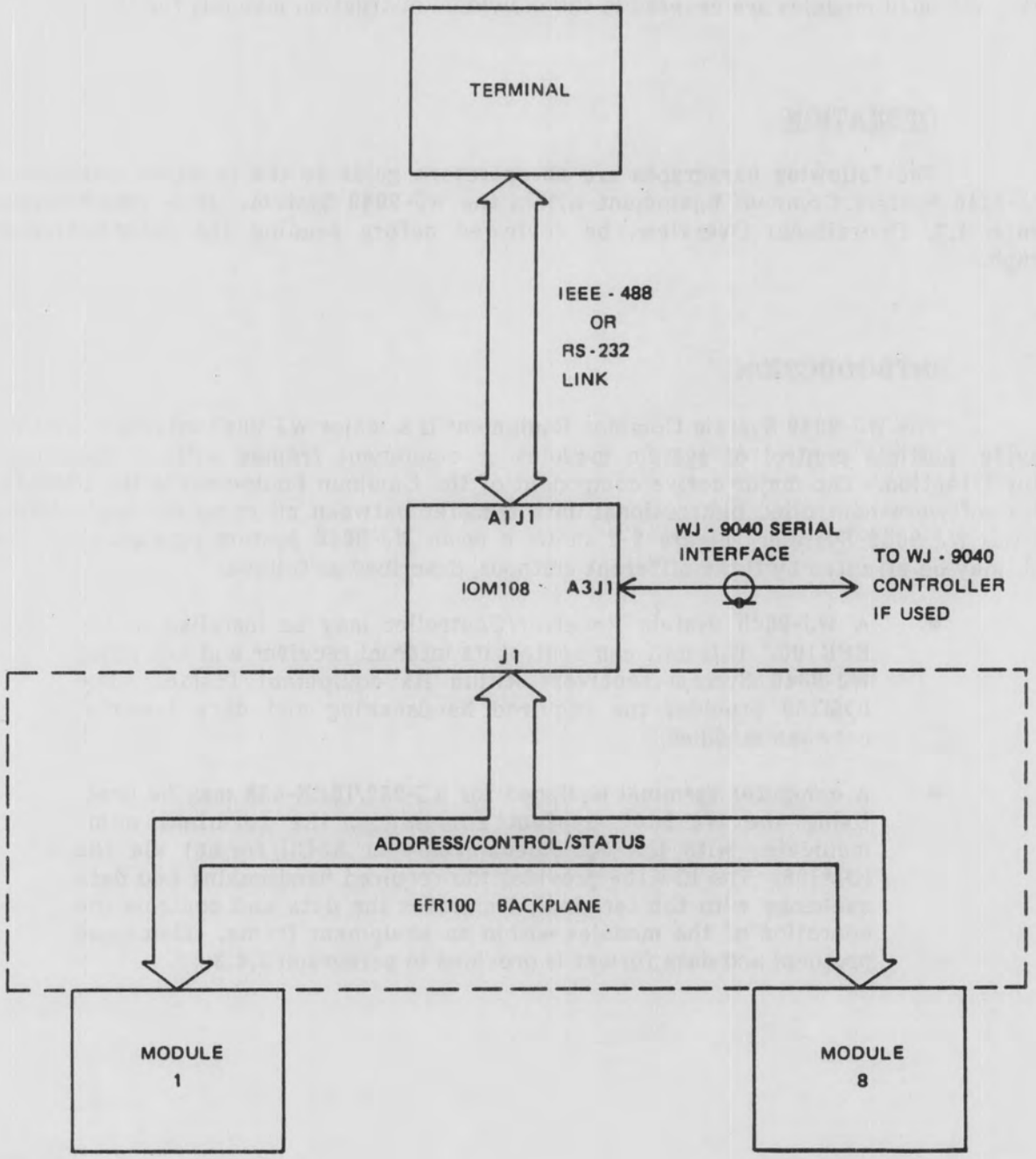


Figure 2-2. Basic WJ-9040 System Configuration

- A system controller (WJ-862X-4 with Master/Handoff Option (MHO)) may be connected to the WJ-9040 Serial I/O, A3J1. Using the W-J defined system software, the system controller can control one or more equipment frames via the high speed serial I/O jack on the IOM108. Typically, communication would be via an external interface unit which would translate system software to the command and data format used by the IOM108. System software descriptions are provided in **paragraph 2.4.4.**

2.4.2 RECEIVER/CONTROLLER OPERATION

Figure 2-3 shows the minimum hardware configuration required for receiver/controller operation using the WJ-9040 System Common Equipment. As shown, one receiver/controller (typically a WJ-8626A-4 or WJ-8628-4) and at least one slave (or handoff) module are required. The receiver/controller must be configured for the Master/Handoff Option (MHO). All communication is contained within the EFR100 frame and is handled by the IOM108. Specific instructions for operating the receiver/controller in this configuration are contained in the WJ-8626A-4 and the WJ-8628A-4 Instruction Manuals.

2.4.3 EXTERNAL COMPUTER TERMINAL OPERATION VIA IOM108

Figure 2-4 shows the minimum hardware requirements needed to implement the operation of a single equipment frame connected to an external computer terminal.

2.4.3.1 General Requirements

The EFR100 Equipment Frame must be minimally equipped with at least one remotely controllable WJ-9040 Module, an EPS100A Power Supply and an IOM108 Module. The IOM108 will be configured with either a DIO488 or a DIO232 Module. If a DIO232 is used, refer to **paragraph 2.4.3.2** for RS-232 setup procedures. For DIO488 operation, refer to **paragraph 2.4.3.3** for hardware setup.

The computer terminal chosen by the user must be configured with either an IEEE-488 or RS-232 port. The choice of either the IEEE-488 or RS-232 port is dictated by the specific IOM108 configuration. If RS-232 is used, the user terminal must be configured for eight bits per character, one stop bit, and no parity. The IOM108 automatically echoes the ASCII data back to the terminal for the RS-232 option; therefore, only half duplex mode is needed. Also, the terminal baud rate must match the DIO232 baud rate in the IOM108 (see **paragraph 2.4.3.2**). In both cases, the user is responsible for ensuring that the terminal can transmit and display ASCII characters via the external I/O port.

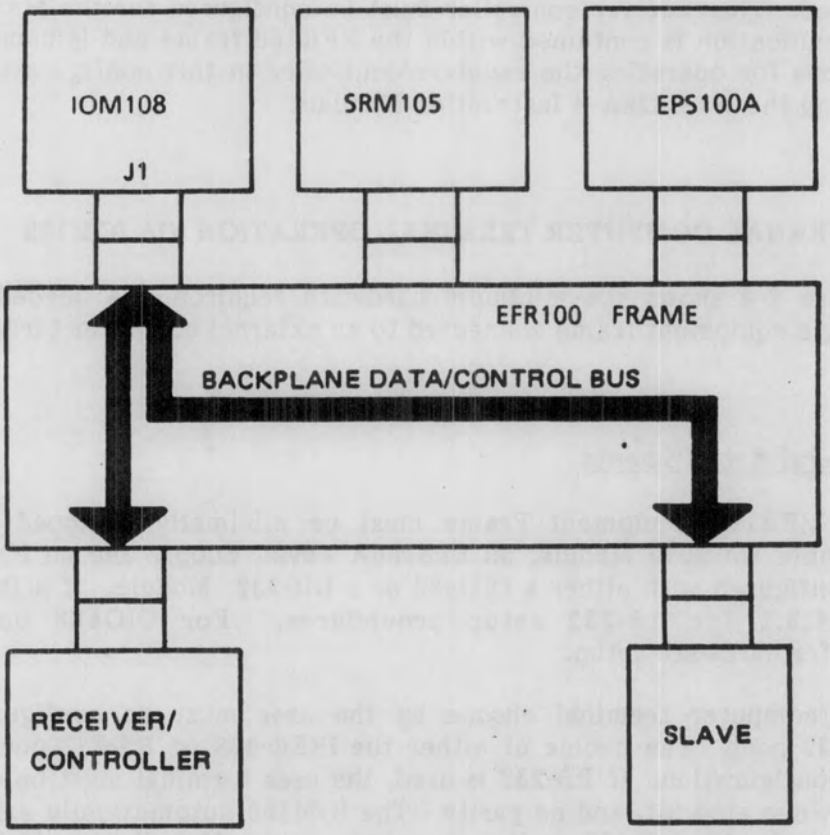


Figure 2-3. Receiver/Controller Operation Via IOM108

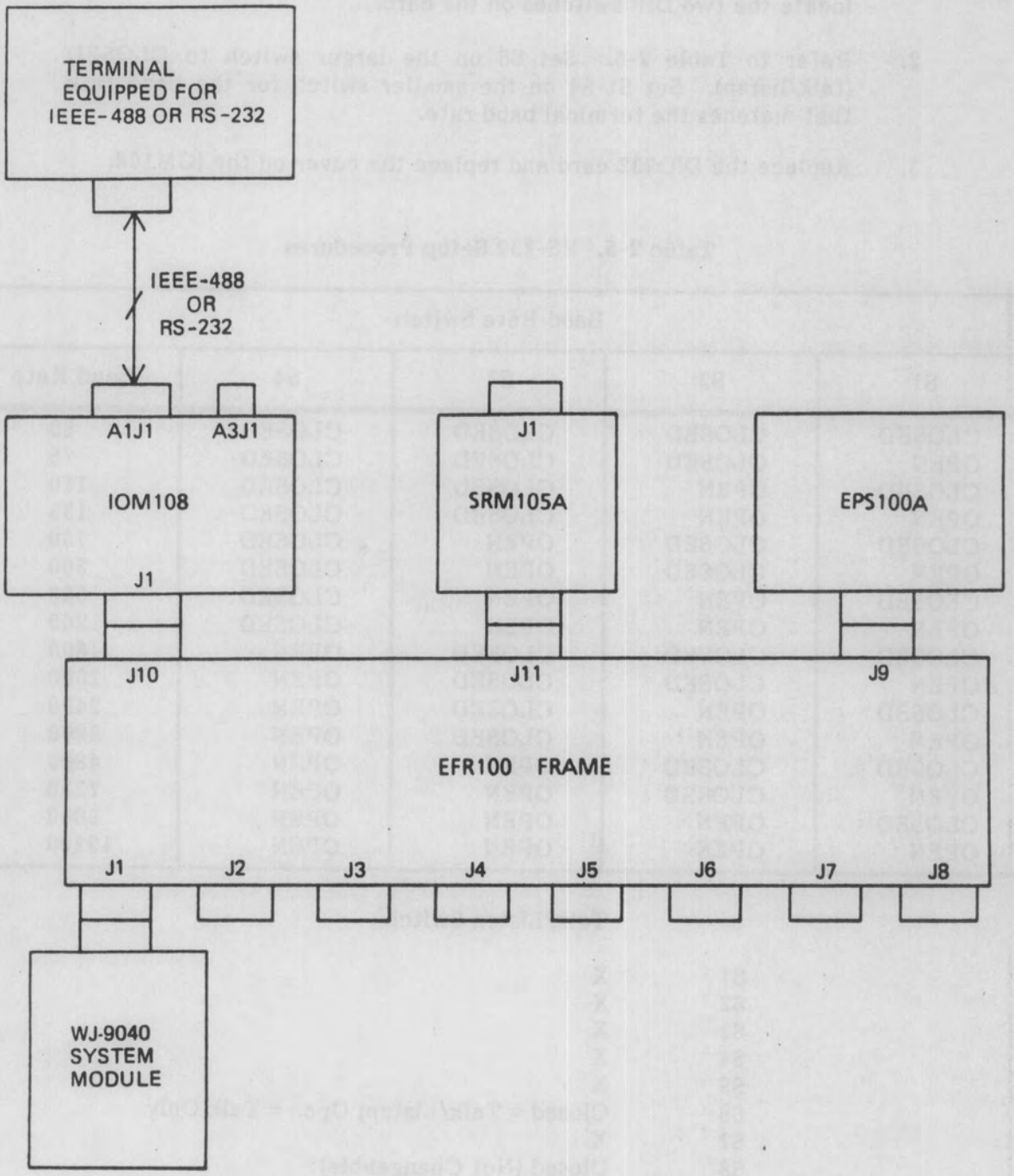


Figure 2-4. Computer Terminal Operation

2.4.3.2 RS-232 Setup Procedures

If RS-232 operation via the DIO232 interface is desired, the two DIP switches on the card must be properly set. To set the switches, proceed as follows:

1. Remove the IOM108 cover, remove the DIO232 card, A1A1, and locate the two DIP switches on the card.
2. Refer to **Table 2-5.** Set S6 on the larger switch to CLOSED (talk/listen). Set S1-S4 on the smaller switch for the baud rate that matches the terminal baud rate.
3. Replace the DIO232 card and replace the cover on the IOM108.

Table 2-5. RS-232 Setup Procedures

Baud Rate Switch				
S1	S2	S3	S4	Baud Rate
CLOSED	CLOSED	CLOSED	CLOSED	50
OPEN	CLOSED	CLOSED	CLOSED	75
CLOSED	OPEN	CLOSED	CLOSED	110
OPEN	OPEN	CLOSED	CLOSED	135
CLOSED	CLOSED	OPEN	CLOSED	150
OPEN	CLOSED	OPEN	CLOSED	300
CLOSED	OPEN	OPEN	CLOSED	600
OPEN	OPEN	OPEN	CLOSED	1200
CLOSED	CLOSED	CLOSED	OPEN	1800
OPEN	CLOSED	CLOSED	OPEN	2000
CLOSED	OPEN	CLOSED	OPEN	2400
OPEN	OPEN	CLOSED	OPEN	3600
CLOSED	CLOSED	OPEN	OPEN	4800
OPEN	CLOSED	OPEN	OPEN	7200
CLOSED	OPEN	OPEN	OPEN	9600
OPEN	OPEN	OPEN	OPEN	19200

Talk/Listen Switch

S1	X
S2	X
S3	X
S4	X
S5	X
S6	Closed = Talk/Listen; Open = Talk Only
S7	X
S8	Closed (Not Changeable)

Note: X = Don't Care

2.4.3.3 IEEE-488 Setup Procedures

If IEEE-488 operation via the DIO488 interface is desired, the DIP switch on the card must be properly set. To set the switch, proceed as follows:

1. Loosen the screws on the switch cover on the rear of the IOM108 and locate the DIP switch.
2. Refer to **Table 2-6.** Switch positions S1-S5 control the IEEE-488 address. The T-address is factory set to 6 and should match the address on the back panel. The user may define the address to 0-31 by setting the switches off/on.
3. Switch S6 equips the IOM108 for either a listen only or a talker/listener.
4. Switches 7 and 8 are not connected and can be disregarded.
5. Replace the switch cover on the IOM108 and tighten the screws.

Table 2-6. IEEE-488 Setup Procedures

Switch	Settings
S1	CLOSED = 0; OPEN = 1 488 Address
S2	CLOSED = 0; OPEN = 2 Selection
S3	CLOSED = 0; OPEN = 4
S4	CLOSED = 0; OPEN = 8 (Binary 0-31)
S5	CLOSED = 0; OPEN = 16
S6	CLOSED = Listen only; 1 = Talk/Listen
S7	Not Used
S8	Not Used

Example:

S1 = CLOSED, S2 = OPEN, S3 = OPEN, S4 = CLOSED, S5 = CLOSED

Address = 0 + 2+ 4 + 0 + 0 = 6

2.4.3.4 Terminal Operation

Terminal operation consists of operator-entered character strings in ASCII format. These English mnemonic strings permit the operator to control the WJ-9040 Modules in the equipment frame. Specific control features include the following:

- Activation/deactivation of modules
- Programming of modules, such as frequency or gain of receivers
- Monitoring status of modules

Table 2-7 lists the commands which may be used to operate the terminal for control of WJ-9040 Modules. When using these commands, the following general considerations must be observed:

1. Commands transmitted to the WJ-9040 are in ASCII format. The user must be familiar with his own specific terminal requirements necessary to transmit the commands listed in **Table 2-7** to the WJ-9040.
2. Spaces entered by the operator will be ignored by the WJ-9040. Backspaces and deletions may be used within the string entry to correct an error.
3. More than one command may be entered on one line. Spaces are recognized by the WJ-9040.
4. A command entry error will cause termination of command execution beginning where the error occurred.
5. Execution of entered commands does not begin until the WJ-9040 receives a line feed (LF) ASCII character. It will be necessary to consult the user terminal documentation to determine the necessary keystrokes required to transmit the ASCII LF character.

Table 2-7. WJ-9040 System Operation Via IEEE-488/RS-232 Interface

Command	Operation	Explanation	Example
AFC	Turns on AFC	Automatic frequency control is turned on	AFC
AUD n	Turns on Audio	Polled Audio to that slot is enabled	AUD 5
AUD?	Interrogates Audio	Returns the slot number of active unit	AUD?
AFC/	Turns off AFC	Automatic frequency control is turned off	AFC/
AFC?	Asks for state of AFC	Returns with a response of ON or OFF	AFC?
********AFC is only used with VHF and UHF receivers ********			
AGC	Turns on AGC	Automatic gain control is turned on	AGC
AGC/	Turns off AGC	Manual gain control is selected	AGC/
AGC?	Asks for the state of AGC	Returns a response of FAST, SLOW, or OFF	AGC?
AGCF	Sets AGC to FAST	Automatic gain control is switched to FAST	AGCF
AGCS	Sets AGC to SLOW	Automatic gain control is switched to SLOW	AGCS
*****AGCF and AGCS are valid only for WJ-8626A-1 and WJ-8626A-4*****			
AM	Selects AM	Sets receiver in AM detection mode	AM
BFO (+/-)f	Sets the BFO frequency	Sets BFO to frequency f kHz	BFO-3.2
BFO?	Asks for BFO frequency	Returns the BFO frequency in kHz	BFO?
BWn	Sets the bandwidth	Sets the bandwidth to number n, where 0 =n =7	BW2

The character n is not a bandwidth, it is a number that represents the specific bandwidth slot the receiver looks at. The actual bandwidth that is selected is determined by which bandwidth card is in the slot.

Table 2-7. WJ-9040 System Operation Via IEEE-488/RS-232 Interface (Continued)

Command	Operation	Explanation	Example
BW?	Asks what BW# has been selected	Returns the number of the BW selected	BW?
BWC?	Asks what the BW is	Returns with the BW in kHz	BWC?
BD n	Sets the baud rate #	Sets the baud rate to number n, where 0≤n≤8	BD2
The command BDn is valid only with WJ-862X-4 receivers which have the FSK option installed in them. The number n is associated with an actual rate. The corresponding rates can be found in the FSK option manual.			
BD?	Asks what baud rate was selected	Returns with the number and actual rate	BD?
CLR	Resets a unit	The addressed module's status is reset to zeros	CLR
COS n	Sets COS level	Sets Carrier Operated Squelch to a level of n, where 0≤n≤63	COS 7
COS?	Asks for level of COS	Returns the COS level	COS?
CST?	Asks for the state of COS	Returns a response of ON if signal is ≤COS and OFF otherwise	CST?
CW	Selects CW detection mode	Puts receiver in the CW detection mode	CW
DET?	Asks for the detection mode	Returns the selected detection mode	DET?
DWL, n,m	Sets sector and channel dwell times	Sector dwell is set to n, channel dwell is set to m, 0≤n,m≤9	DWL 2,3
DWL* n,m	Sets WJ-8626A-4 dwell times	Sets on hit time to n and off hit time to m for an WJ-8626-A scan, 0≤n,m≤9	DWL* 4,2
DWL?	Asks for the IOM dwell times	Returns the sector and channel scan dwell times	DWL?
EXAM n	Asks for slot status	Returns the type of module in slot n, where 0≤n≤8	EXAM 3

Table 2-7. WJ-9040 System Operation Via IEEE-488/RS-232 Interface (Continued)

Command	Operation	Explanation	Example
FASTSS	Sets SS to fast mode	Sets a WJ-8626A-1 or WJ-8626A-4 into a fast SS mode	FASTSS
FM	Sets FM detection	Puts the receiver in FM detection mode	FM
FRQ f	Sets the tuned frequency	Receiver is tuned to frequency f MHz	FRQ 21.876
FRQ?	Asks for the tuned frequency	Returns the tuned frequency of the receiver	FRQ?
FSK (+/-)	Sets FSK detection mode	Puts a WJ-862X-4 with FSK option into FSK mode	FSK
INL n,m,-p	Enables specified memory channels to be included in a channel scan	Sets memory channels 1-99 so they will be included in a channel scan	INL 4-7, 9
INL* n,m-p	Enables specified memory channels for a WJ-862X-4 internal scan	Tells the WJ-862X-4 to include memory channels in its scan	INL*3-10
LCK n,m-p	Locks specified channels out of a channel scan	Locks out memory channels from a channel scan	LCK 1-4, 99
LCK* n-m	Locks specified memory channels from a WJ-862X-4 channel scan	Locks out WJ-862X-4 memory channels from IF scan	LCK*5-88
LSB	Sets LSB detection mode	Sets receiver in the LSB detection mode	LSB
MAN n	Stops specified scan	n=0 stops channel scan, $1 \leq n \leq 8$ stops sector n scan	MANO
MAN*	Stops a WJ-862X-4 scan	Tells a WJ-862X-4 to stop scanning	MAN*
NORMSS	Sets SS to normal mode	Puts WJ-8626A-1, A-4 into signal strength mode	NORMSS

Table 2-7. WJ-9040 System Operation Via IEEE-488/RS-232 Interface (Continued)

Command	Operation	Explanation	Example
RCL n	Recalls specified memory channel	Recalls and executes specified channel status to the receiver it was assigned to, 1≤n≤99	RCL 54
RCL* n	Recalls specified WJ-862X-4 memory channel	Recalls and executes WJ-862X-4 memory channel, 1≤n≤99	RCL* 75
RFG n	Sets RF gain	Sets the level of RF gain, 0≤n≤63	RFG 28
RFG?	Asks for the RF gain level	Returns the RF gain level from 0 to 63	RFG?
SCN	Starts channel scan	Begins IOM channel scan at the first allocated channel that has been included	SCN
SCN*	Starts a WJ-862X-4 channel scan	Begins WJ-862X-4 internal channel scan	SCN*
SLOT n	Addresses the specified slot	Addresses specified slot so that following commands will be executed on that slot, 0≤n≤8	SLOT 1
RMT	Sets unit to remote	Puts smart unit into remote	RMT
RMT?	Asks the remote status	Returns either remote or local for a smart unit	RMT?
SS?	Asks for signal strength	Returns the signal strength in a range from 0 to 99	SS?
STO n	Allocates a memory channel	Puts present status of active receiver into IOM memory channel n	STO 5
STO* n	Allocates WJ-862X-4 memory channel	Puts the present status of WJ-862X-4 in memory channel n	STO* 91
SLOT	Asks for slot	Returns slot number of unit currently being controlled	SLOT?

Table 2-7. WJ-9040 System Operation Via IEEE-488/RS-232 Interface (Continued)

Command	Operation	Explanation	Example
SH n	Sets the shift rate for FSK option	Puts the WJ-862X-4 into shift rate n for the FSK mode option, $1 \leq n \leq 8$	SLOT?
SH?	Asks for the shift rate	Returns with the shift rate number and actual rate	SH?
VER?	Requests software revision	Returns a string indicating the IOM108 software version and revision	VER?
USB	Sets USB detection mode	Sets receiver in the USB detection mode	USB
VIEW n	Display memory channel n	Returns with value of memory channel n complete status	VIEW 43
VIEW* n	Displays WJ-862X-4 memory channel	Returns with value of WJ-862X-4 memory channel n complete status	VIEW* 21

2.4.3.5 **IOM108 Scan Setup and Operation**

IOM108 internal software permits the use of the commands listed in **Table 2-8** to perform a memory channel scan on an addressable receiver in the EFR100 Equipment Frame being controlled. To setup and perform the scan, use the following procedure:

1. Select the receiver with the slot "n" command. Enter information that is to be stored in a memory channel. This includes the following:
   - Frequency
   - Detection Mode
   - Bandwidth
   - COS Level
   - AGC
   - BFO (IF Detection Mode is CW)
   - RF Gain (IF Manual Gain is selected)
2. Store selected status data into memory channel n with the command:

   STO n 0 n100

   Continue with steps 1 and 2 until all the desired information has been stored.

NOTE

Memory channels can be stored in any order. Each memory channel is associated with only one receiver.

3. Include memory channels that are to be scanned with the command:

   INL n,m-p m<p

   The following are valid include statements:

   INL 2 INL 1-8
   INL 3,4 INL 5,6,9
   INL 10, 1-7

4. Lock out memory channels not wanted in the scan with the command:

   LCK n, m-p m<p

5. Set up a dwell time for the memory scan:

   DWL n,m

   m = Is the time in seconds that the scan remains on a hit after the signal has dropped away.

   n = Is the time in seconds that the scan remains on a hit when the signal is present.

NOTE

Steps 3, 4, and 5 may be executed in any order previous to the start of the scan. Steps 1-5 must be executed at least once before the scan has started.

6. Start memory channel scan with the command:

   SCN

7. Stop memory scan with the command:

   MAN 0

Table 2-8. Sample Terminal Operation Scenario

Command	Response
SLOT 1	Active light on slot 1 receiver turns on
EXAM 1	RECV 5 kHz - 30 MHz (CR/LF)
EXAM 2	NO ADDRESSABLE UNIT (CR/LF), nothing is in slot 2
EXAM 3	RECV 5 kHz - 30 MHz (CR/LF)
EXAM 4	NO ADDRESSABLE UNIT (CR/LF)
EXAM 5	RECV 5 kHz - 30 MHz (CR/LF)
EXAM 6	NO ADDRESSABLE UNIT (CR/LF)
EXAM 7	RECV 5 kHz - 30 MHz (CR/LF)
EXAM 8	NO ADDRESSABLE UNIT (CR/LF)
FRQ 23.45	Sets slot 1 (previously activated) at 23.45 MHz
AGC COS20 AM	Sets slot 1 to AGC fast, sets COS level to 20 and Detection Mode AM
SLOT 3	Active light on slot 3 receiver turns on
FRQ?	12.000 MHz (CR/LF)
AGC? DET?	FAST (CR/LF) FM (CR/LF)
AGC/RFG15	Turns AGC off and sets RF gain level to 15
COS?	10 (CR/LF)
SLOT 5	Active light on slot 5 receiver turns on
FRQ? AGC? DET?	9.8760 MHz (CR/LF) OFF (CR/LF) CW (CR/LF)
COS? RFG? BFO?	0 (CR/LF) 63 (CR/LF) 0.00 kHz
BW 2	Selects bandwidth number 2 inside receiver
BW? BWC?	2 (CR/LF) 6 kHz (CR/LF)

Table 2-8. Sample Terminal Operation Scenario (Continued)

Command	Response
SLOT 7	Active light on slot 7 receiver turns on
AM AGCS BW3 FRQ20	Sets AM detection mode, Selects AGC slow, bandwidth number 3 and 20 MHz.

2.4.3.6 **Reporting the Carrier-Operated Squelch Status of Receivers**

When a receiver, which is installed in a WJ-9040 EFR100, receives a signal that exceeds the preset squelch threshold level during a scan, it communicates the presence of this "hit" to the IOM108 by resetting the logic of a hardware line that is monitored by the IOM108. This action causes the IOM108 to set a bit in its Slot Summary Register that pertains to the slot installation of the signaling receiver. **Figure 2-5** depicts the architecture of the IOM108's status register. It is composed of the Slot Summary Register and three other eight-bit registers, whose logic gating allow programmers the flexibility to mask scan hits. The four registers can be split into two pairs.

The first pair is composed of the Slot Summary Register and the Slot Summary Enable Register. Each bit in the Slot Summary Register is logically ANDed to a bit in the Slot Summary Enable Register. The ANDED combination of these two registers is logically ORed to set the Slot Summary Bit in the Status Byte Register.

The second pair of registers is the Status Byte Register and the Service Request (SRQ) Enable Register. The IOM108 only uses one bit in each of these registers. The Slot Summary bit (bit 7) of the Status Byte Register is logically ANDed to the Slot Summary Enable bit (bit 7) of the SRQ Enable Register. If both bits are a logic high, then a service request is generated.

There are six remote control commands associated with the SRQ byte. These are described below:

*SRE n - This command defines the enable bits in the Service Request Enable Register where n is a number from 0 to 255.

Bit	Function
0	Not Used
1	Not Used
2	Not Used
3	Not Used
4	Reserved
5	Reserved
6	Not Used
7	Enable SSB

*SRE? - This command returns the value of the Service Request Enable Register in decimal.

*STB? - This command returns the value of the Status Byte Register in decimal.

Bit	Function
0	Not Used
1	Not Used
2	Not Used
3	Not Used
4	Reserved
5	Reserved
6	SRQ
7	SSB

SSE n - This command defines the enable bits in the Slot Summary Enable Register where n is a number from 0 to 255.

Bit	Function
0	Enable SL1
1	Enable SL2
2	Enable SL3
3	Enable SL4
4	Enable SL5
5	Enable SL6
6	Enable SL7
7	Enable SL8

SSE? - This command returns the value of the Slot Summary Enable Register in decimal.

SSR? - This command returns the value of the Slot Summary Register in decimal. This is a destructive read; once the command is executed the register is cleared.

Bit	Function
0	SL1
1	SL2
2	SL3
3	SL4
4	SL5
5	SL6
6	SL7
7	SL8

In response to the service request, the system controller can query the IOM108 as to which slot has signaled the scan hit via the SSR? query. It can then query the individual receiver for further information about the signal activity via the HIT*? query. The receiver returns information concerning the scan band, the signal strength, and the frequency of the signal. Because this information is overwritten by successive "hits", it is recommended that the scanning receiver be set for infinite on-hit and after-hit dwells.

2.4.4 SYSTEM CONTROLLER OPERATION

This paragraph will describe the operation of a single equipment frame connected to a master system controller such as the WJ-862X-4 with option MHO. **Figure 2-2** shows the hardware interconnections necessary to implement master system controller operation.

2.4.4.1 WJ-9040 Serial I/O Definition

As shown in **Figure 2-2,** the master system controller communicates with the IOM108 via the high speed serial I/O jack. The high speed serial I/O uses the industry standard 6502 interface to implement a data communication link with the following characteristics:

- 50 ohm impedance
- Shielded, coaxial BNC connectors
- Logic levels are 0 Vdc (low) and +1 Vdc (high)

Communication between the controller and IOM is only initiated by the controller, with the IOM functioning as responder. Information interchange between the two units has a particular format called the W-J system protocol which is organized into groups of 8-bit blocks. These 8-bit blocks may represent a system command (two 4-bit hexadecimal digits) or data (one 8-bit binary digit). The W-J system protocol organizes the 8-bit blocks into a format. All communication between units will be structured according to the following format:

ADDRESS	Equipment Frame, Module No.	(two 4-bit digits)
INSTRUCTION	Specific system command	(two 4-bit digits)
DATA	Information	(one 8-bit digit)
CHECKSUM	Summation of all bytes	(one 8-bit digit)
TERMINATOR	All bits = 1, E.O.M.	(one 8-bit digit)

Table 2-9 lists all current specific commands used by the WJ-9040 system protocol. These commands are interpreted by the IOM108 software, which then directs the addressed module via the EFR100 backplane protocol. **Figure 2-6** is a communication timing diagram showing the sequence of events that occur during system level communication between the master receiver and IOM108. Note that communications always begin with a Request-to-Send (RTS) command from the master receiver. **Figure 2-7** shows the timing for the RTS command.

Table 2-8A. Serial I/O Setup Procedures

Switch	Settings	
S1	CLOSED = 0;	OPEN = 1
S2	CLOSED = 0;	OPEN = 2
S3	CLOSED = 0;	OPEN = 4
S4	CLOSED = 0;	OPEN = 8
S5	X	
S6	X	
S7	X	
S8	CLOSED = 0;	TERMINATION ON
	OPEN = 0;	NO TERMINATION
X = DON'T CARE		

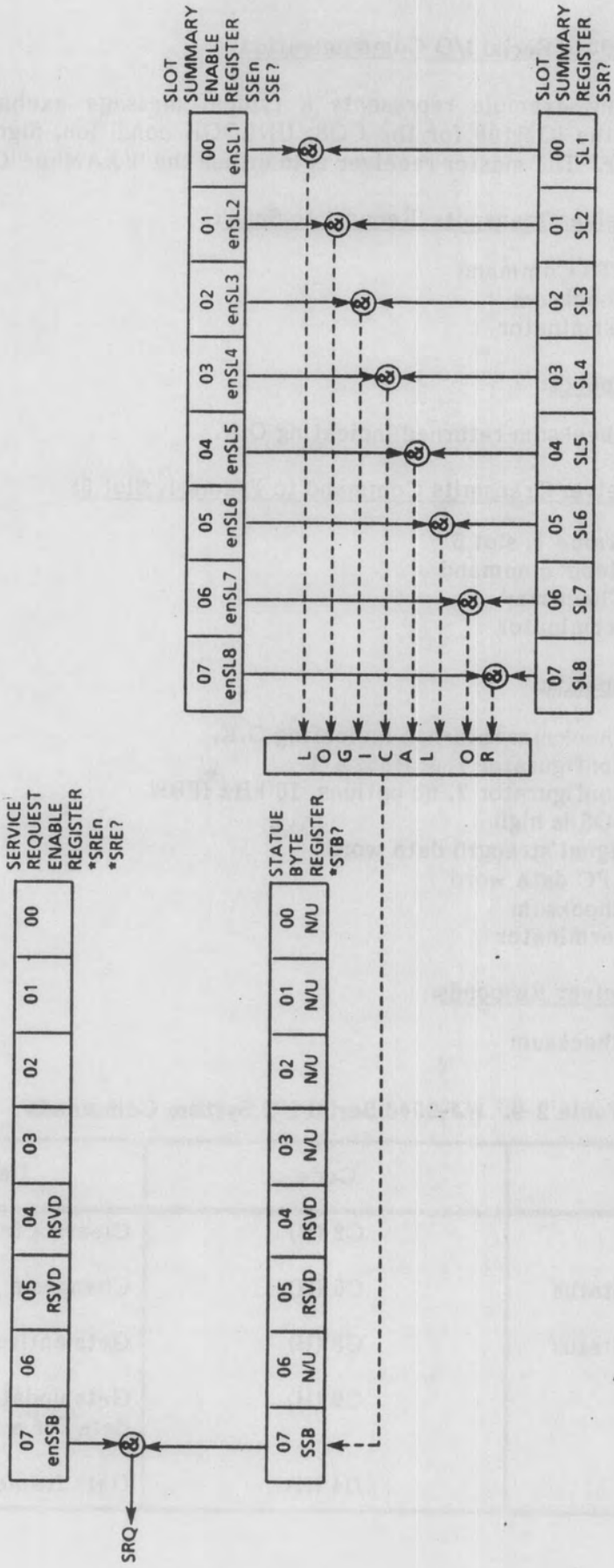


Figure 2-5. Hierarchy of the Service Request

2.4.4.2 **Typical WJ-9040 Serial I/O Communication**

The following example represents a typical message exchange when a master receiver is interrogating the IOM108 for the COS, UNLOCK condition, Signal Strength and AFC voltage of a slave receiver. The master receiver is in either the 'EXAM' or 'CTRL' mode.

Master Receiver Transmits 'Request to Send':

D4 (H) RTS Command
D4 (H) Checksum
FF (HH) Terminator

IOM108 Responds:

D4 (H) Checksum returned indicating O.K.

Master Receiver Transmits Command to Frame 1, Slot 5:

15 (H) Frame 1, slot 5
C9 (H) 'Read' command
DE (H) 'Checksum'
FF (H) Terminator

IOM108 Responds:

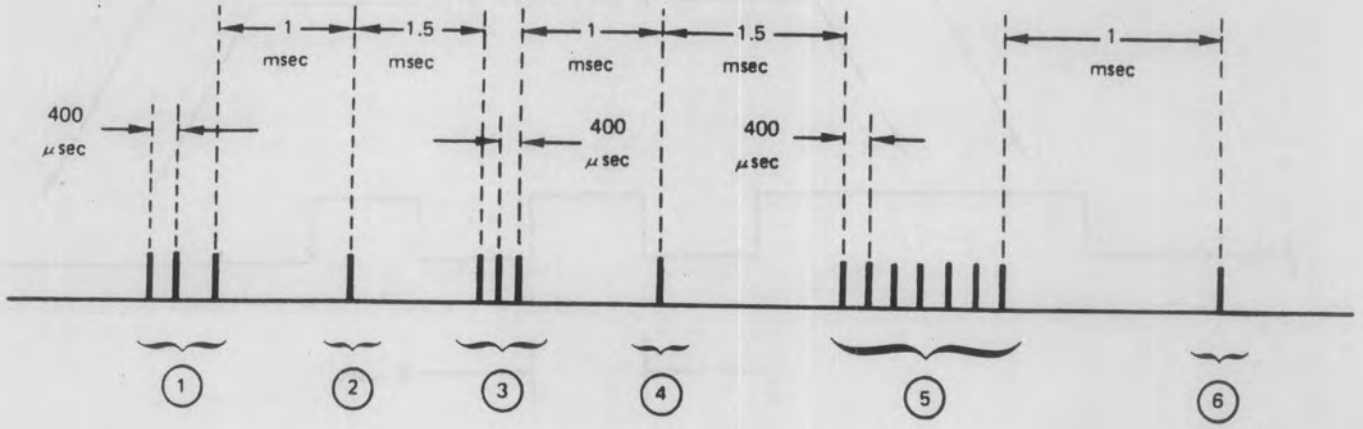
DE (H) Checksum returned indicating O.K.
14 (H) Configurator 1, WJ-862X-1
0A (H) Configurator 2, no options, 16 kHz IFBW
02 (H) COS is high
15 (H) Signal strength data word
89 (H) AFC data word
9C (H) Checksum
FF (H0) Terminator

Master Receiver Responds:

9C (H) Checksum

Table 2-9. WJ-9040 Serial I/O System Commands

Command	Code	Description
Clear Frame	C2 (H)	Clears a frame's status
Change Complete Status	C5 (H)	Changes a module's status
Equipment Frame Status	C8 (H)	Gets entire frame status
Read	C9 (H)	Gets update on pertinent data for a module
Request-to-Send	D4 (H)	Gets frame's attention



1 Request to send from master receiver

2 Checksum acknowledgement from IOM108

3 Address, command checksum from master receiver

4 Checksum acknowledgement from IOM108

5 Data message from IOM108, with checksum

6 Checksum acknowledgement from master receiver

Figure 2-6. Master Receiver/IOM108 Communication Timing Diagram

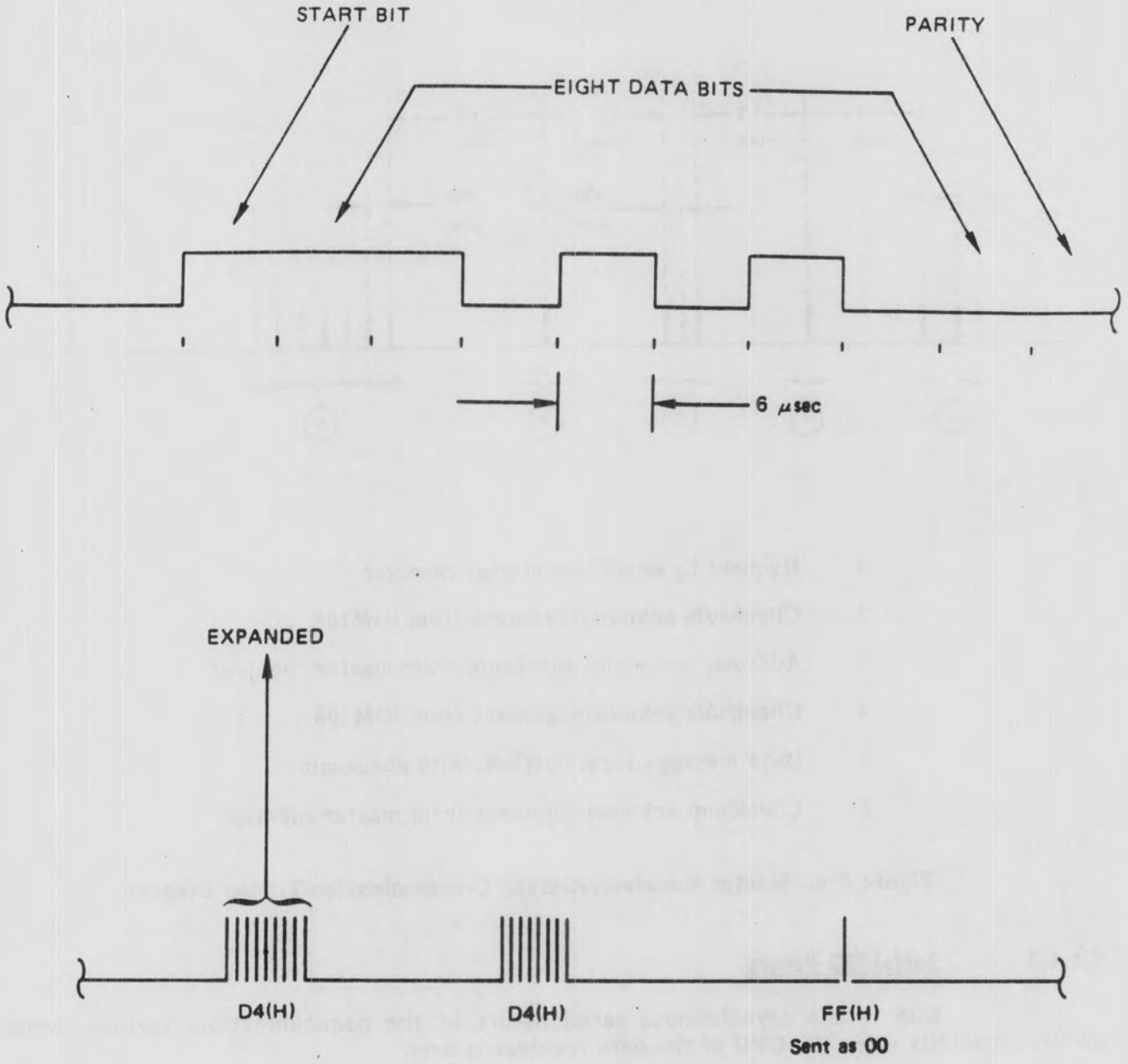
2.4.4.3 **Serial I/O Errors**

Due to the asynchronous serial nature of the communication, various errors can occur, especially when the CPU of the data receiver is busy.

The sending unit (transmitter) will repeatedly attempt to send the RTS (request-to-send) message (up to 125 times) until a valid checksum acknowledgement is returned from the data receiver. During this series of attempts, the data receiver might return data of 00 H or return nothing at all, in which case the transmitting device times out and tries again.

When the RTS exchange is complete, the command message is transmitted. Another checksum acknowledgement is expected from the data receiver. If no valid acknowledgement is returned, the command is repeated up to 10 times.

A similar acknowledgement protocol is used when the IOM108 becomes the transmitter for the data requested by the master receiver.



Request - to - send command from Master Receiver

Figure 2-7. Typical Timing for One Character Frame

SECTION III

CIRCUIT DESCRIPTION

SECTION III

CIRCUIT DESCRIPTION

3.1 INTRODUCTION

This section describes the theory of operation of the WJ-9040 System Common Equipment. A simplified block diagram is provided to show the overall organization of the unit. A functional description is provided using individual block diagrams for each module in the unit. The functional description is followed by individual circuit level descriptions of each module.

3.2 GENERAL DESCRIPTION

Figure 3-1 is a simplified block diagram of the WJ-9040 System Common Equipment. The unit consists of the following major modules:

- EFR100 Equipment Frame
- IOM108 I/O and Interface Module
- EPS100A Power Supply Module
- SRM105A Frequency Reference Module

A general discussion of the function and technical characteristics of each major module follows.

3.2.1 EFR100 EQUIPMENT FRAME

A general discussion of the EFR100 Equipment Frame functions and signal interfaces is provided in the following paragraphs.

3.2.1.1 EFR100 Equipment Frame Function

The EFR100 performs the following functions:

- Provides mechanical mounting for WJ-9040 modules.
- Distributes DC power and command/control data to the various WJ-9040 modules.

3.2.1.2 EFR100 Equipment Frame Signal Interfaces

The following input/output signals interface with the EFR100:

- DC power (+29 V, +18.2 V, -18.2 V, +8.2 V) inputs from the EPS100A via A1J9 and is routed to system modules via A1J1-A1J8, A1J10 and A1J11.

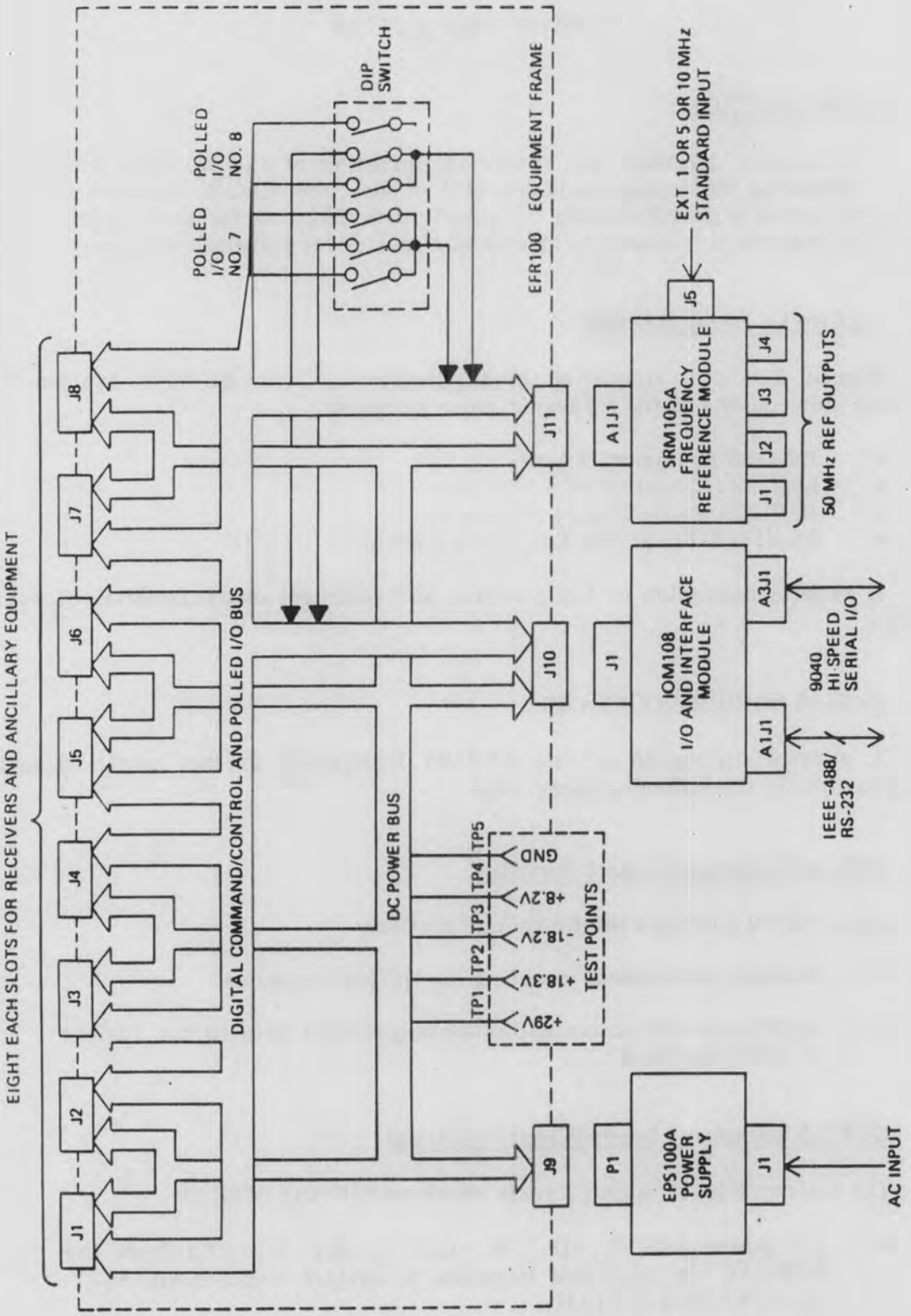


Figure 3-1. WJ-9040 System Common Equipment Interface Unit Block Diagram

- Digital command/control data interfaces with the IOM108 via A1J10 and is routed to system modules via A1J1-A1J8 and A1J11.
- Polled I/O data inputs from system modules via A1J1-A1J8 and is routed to the IOM108 via A1J10 or to an auxiliary system module via A1J11.

3.2.2 IOM108 I/O CONTROL MODULE

A general discussion of the IOM108 I/O Control Module functions and signal interfaces is provided in the following paragraphs.

3.2.2.1 IOM108 Module Function

The IOM108 Module performs the following functions:

- Provides a central interface point for system modules.
- Contains system operating software.
- Monitors the status of modules in the equipment frame.

3.2.2.2 IOM108 Module Signal Interface

The following input/output signals interface with the IOM108:

- Digital command/control data, polled I/O and DC power are input from the equipment frame via A1J1.
- IEEE-488 or RS-232 command/control data interfaces with an external controller via A1A1J1.
- High-speed serial I/O command/control interfaces with a system controller or another equipment frame via A1A3J1.

3.2.3 EPS100A POWER SUPPLY

A general discussion of the EPS100A Power Supply function and signal interfaces is provided in the following paragraphs.

3.2.3.1 EPS100A Power Supply Function

The EPS100A Power Supply performs the following functions:

- Provides AC to DC power conversion and supplies correct DC operating voltages to the system modules.

- Provides AC input selection to accommodate a wide range of AC line voltages.

3.2.3.2 **EPS100A Power Supply Signal Interfaces**

The following input/output signals interface with the EPS100A:

- AC input voltage, 90 to 130 Vac or 180 to 260 Vac, inputs to the EPS100A via J1.
- DC operating voltages (+29 V, +18.2 V, -18.2 V and +8.2 V) are output to the equipment frame via P1.

3.2.4 SRM105A SITE REFERENCE MODULE

A general discussion of the SRM105A Site Reference Module function and signal interfaces is provided in the following paragraphs.

3.2.4.1 **SRM105A Module Function**

The SRM105A module performs the following functions:

- Generates a highly stable 50 MHz reference signal for use by WJ-9040 HF/VHF receiver synthesizers.
- Permits locking to an external master reference for high overall accuracy in multiple frame configurations.

3.2.4.2 **SRM105A Module Signal Interface**

The following input/output signals interface with the SRM105A:

- DC power is input to the SRM105A from the equipment frame via A1J1.
- External 1 5, or 10 MHz standard reference is input to the SRM105A via J5.
- 50 MHz reference signals are output from the SRM105 via J1-J4.

3.3 WJ-9040 SYSTEM COMMON EQUIPMENT FUNCTIONAL DESCRIPTION

3.3.1 EFR100 EQUIPMENT FRAME

Refer to **Figure 3-1**, WJ-9040 System Common Equipment Block Diagram. As shown in **Figure 3-1**, the EFR100 Equipment consists of three major functional areas:

- DC Power Bus
- Digital Command/Control and Polled I/O Bus
- Polled I/O Switch

3.3.1.1 DC Power Bus

DC supply voltages of +29 V, +18.2 V, -18.2 V and +8.2 V are generated by the EPS100A Power Supply and are input to the EFR100 via J9. The DC power bus distributes these four DC voltages to A1J1-A1J8 to power receivers and ancillary equipment, to A1J10 to power the IOM108 and to A1J11 to power the SRM105A.

3.3.1.2 Digital Command/Control and Polled I/O Bus

The digital command/control bus interfaces the receiver slots A1J1-A1J8 with the IOM108 via A1J10. This bus contains a bidirectional serial data line and timing/control lines to permit the exchange of command data between the receiver slots and the IOM108.

The polled I/O bus transfers receiver outputs such as audio, signal strength and COS status to the IOM108, thus permitting the IOM108 to monitor the status of any installed receiver. Additionally, this bus permits the selective routing of audio outputs between modules installed in the EFR100 Equipment Frame.

3.3.1.3 Polled I/O Switches

The polled I/O switches tap the polled I/O lines number 7 and 8 and permit the selective routing of these lines to the IOM108 via A1J10 or to the auxiliary connector A1J11.

3.3.2 IOM108 I/O INTERFACE MOTHERBOARD

Refer to **Figure 3-2**, IOM108 Block Diagram. As shown in **Figure 3-2**, the IOM108 I/O Interface Motherboard consists of the following major modules:

- Digital I/O (A1A1)
- Polled I/O (A1A2)
- System I/O (A1A3)
- Extended CPU (A1A5)

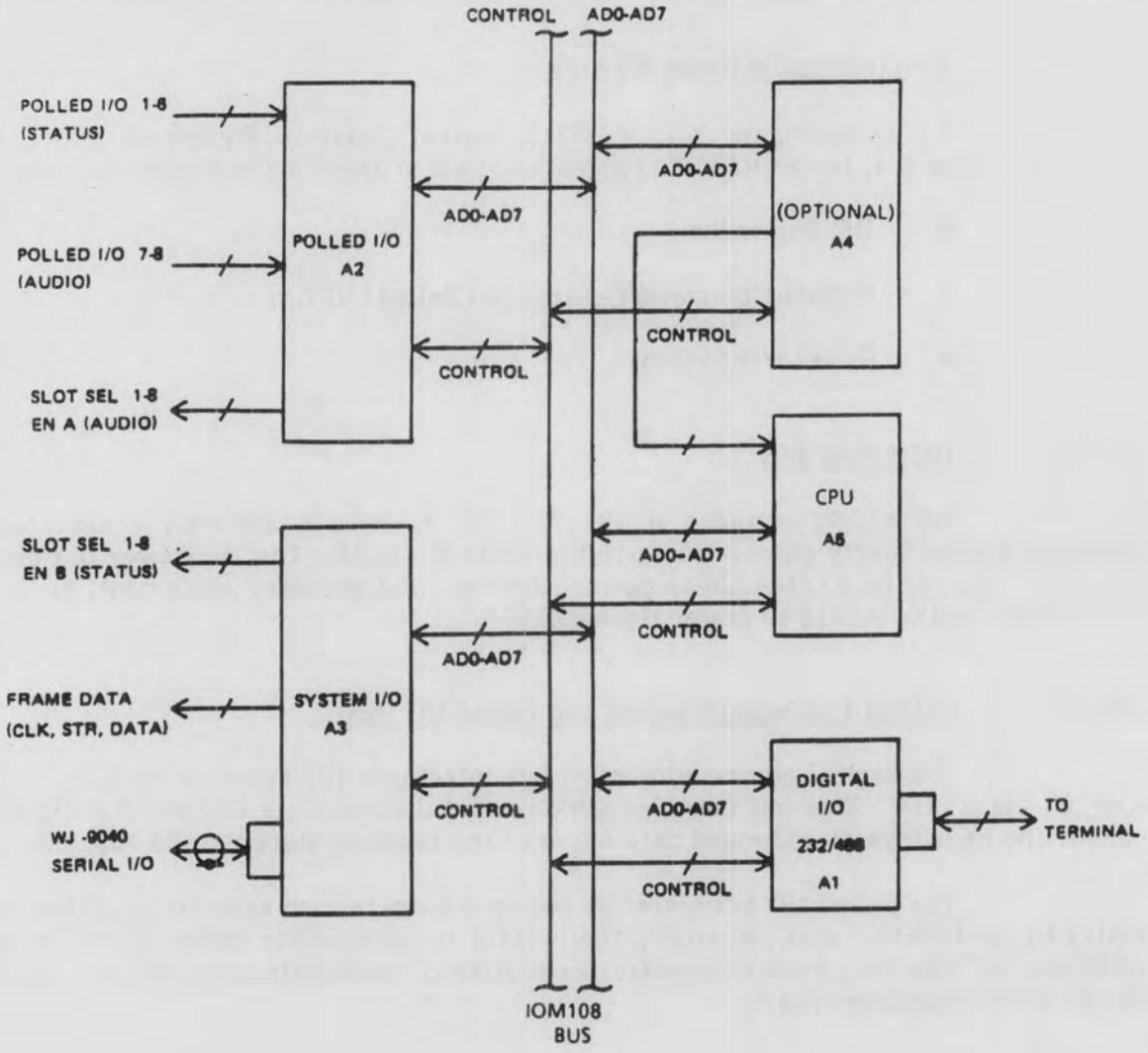


Figure 3-2. IOM108 I/O Interface Motherboard (A1) Block Diagram

NOTE

Early IOM108 Module configurations have the Extended Memory (A1A4) and the CPU (A1A5) as separate boards. Current IOM108 Modules have these two boards combined as the Extended CPU (A1A5).

3.3.2.1 Digital I/O (A1A1)

The digital I/O module will be structured for the IEEE-488 or RS-232 formats, as selected. The module communicates with an external computer terminal device using standard IEEE-488 or RS-232 bus structures. Data from the computer terminal is interfaced to the IOM108 address/data bus. The digital I/O module interrupts the CPU when the computer terminal transmits data and transmits data to the terminal when directed to do so by the CPU.

3.3.2.2 Bidirectional Polled I/O (A1A2)

The polled I/O module interfaces polled I/O lines 1-6 from each of the eight receiver slots to the IOM108 address/data bus. Lines 1-6 represent the status of the modules plugged into the receiver slots. The polled I/O module selectively polls each active slot by transmitting a slot select signal. Each active slot, when polled, transmits polled I/O lines 1-6 to the polled I/O module which then places the data on the IOM108 address/data bus. Polled I/O lines 7 and 8, which are typically audio outputs from the modules plugged into the receiver slots, are also selectively polled by the slot select signals. These lines are transmitted through the polled I/O switch to auxiliary connector, A1J11.

3.3.2.3 System I/O (A1A3)

The system I/O module interfaces the frame data (CLOCK, STROBE, DATA IN, DATA OUT) between the IOM108 address/data bus and the eight receiver slots on the equipment frame. The frame data is used to distribute command and control information to the various modules in the frame. Communication with the eight receiver slots is accomplished by Enable B slot select lines 1-8 generated by the system I/O module. The system I/O module also interfaces WJ-9040 serial I/O data from the system controller to the IOM108 address/data bus.

3.3.2.4 Extended CPU (A1A5)

The Extended CPU module controls overall IOM108 operation and coordinates all data transfer between IOM108 modules via the address/data bus. The Extended CPU executes system software by reading the program from its ROM. In normal operation, the Extended CPU stores parameters and commands by reading data into and out of RAM via the address/data bus. All communication between the IOM108 and the equipment frame is accomplished through modules A1A1, A1A2 and A1A3 and the address/data bus.

3.3.3 EPS100A POWER SUPPLY

Refer to **Figure 3-3**, EPS100A Power Supply Block Diagram. As shown in **Figure 3-3**, the AC line input voltage enters via J1. The voltage select sets the power supply to accept either 115 or 230 Vac. An in-line fuse is provided for supply protection and an in line power switch is used to energize or deenergize the supply. The line filter removes AC noise from the line. The AC line voltage enters the switching supply module which converts the AC voltage to four DC voltages: +29 V, +18.2 V, -18.2 V and +8.2 V. These voltages are routed to the equipment frame via P1.

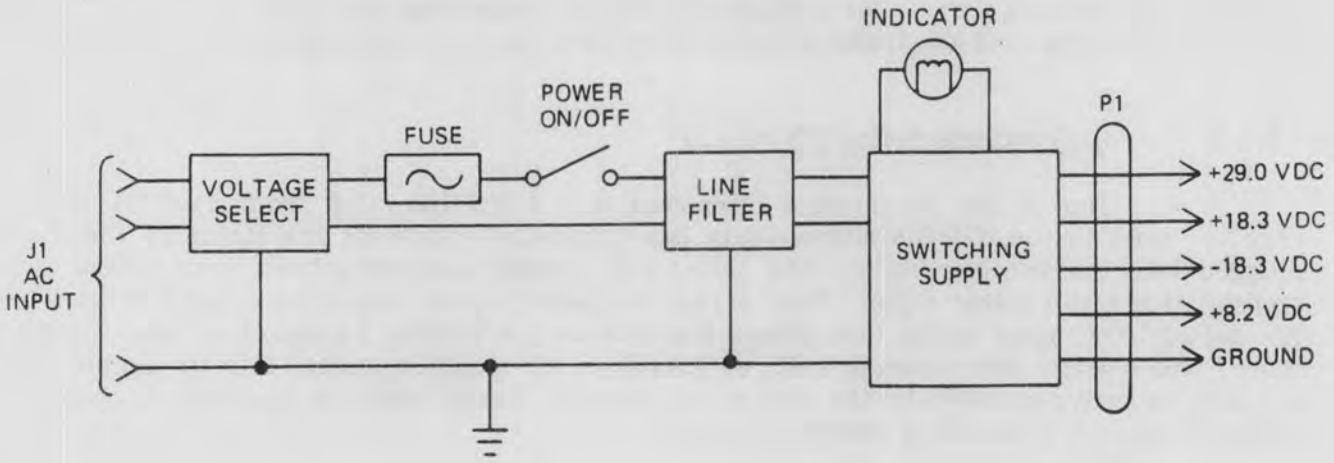


Figure 3-3. EPS100A Power Supply Block Diagram

3.3.4 SRM105 SITE REFERENCE MODULE

Refer to **Figure 3-4**, SRM105 Site Reference Module Block Diagram. As shown in **Figure 3-4**, the main element of the SRM105 is a 50 MHz temperature compensated variable crystal oscillator (TCVCXO). In the Free Run mode, the oscillator generates a stable 50 MHz signal which is amplified by a buffer amplifier and split four ways by a splitter to provide the four reference outputs at J1-J4. In the External Mode, the 50 MHz signal is compared with an external 1 or 5 or 10 MHz reference signal. The 50 MHz signal is divided by 200 (1 MHz external input) or by 40 (5 or 10 MHz external input). A phase detector and loop filter provide the frequency comparison and generate the necessary correction voltage to force the 50 MHz TCVCXO to lock with the external reference signal.

3.4 THEORY OF OPERATION

The following paragraphs provide a detailed circuit description of each of the WJ-9040 System Common Equipment modules. Simplified block diagrams are used throughout the text to clarify the description. These block diagrams should be used in conjunction with the schematic diagrams located in **Section VI.**

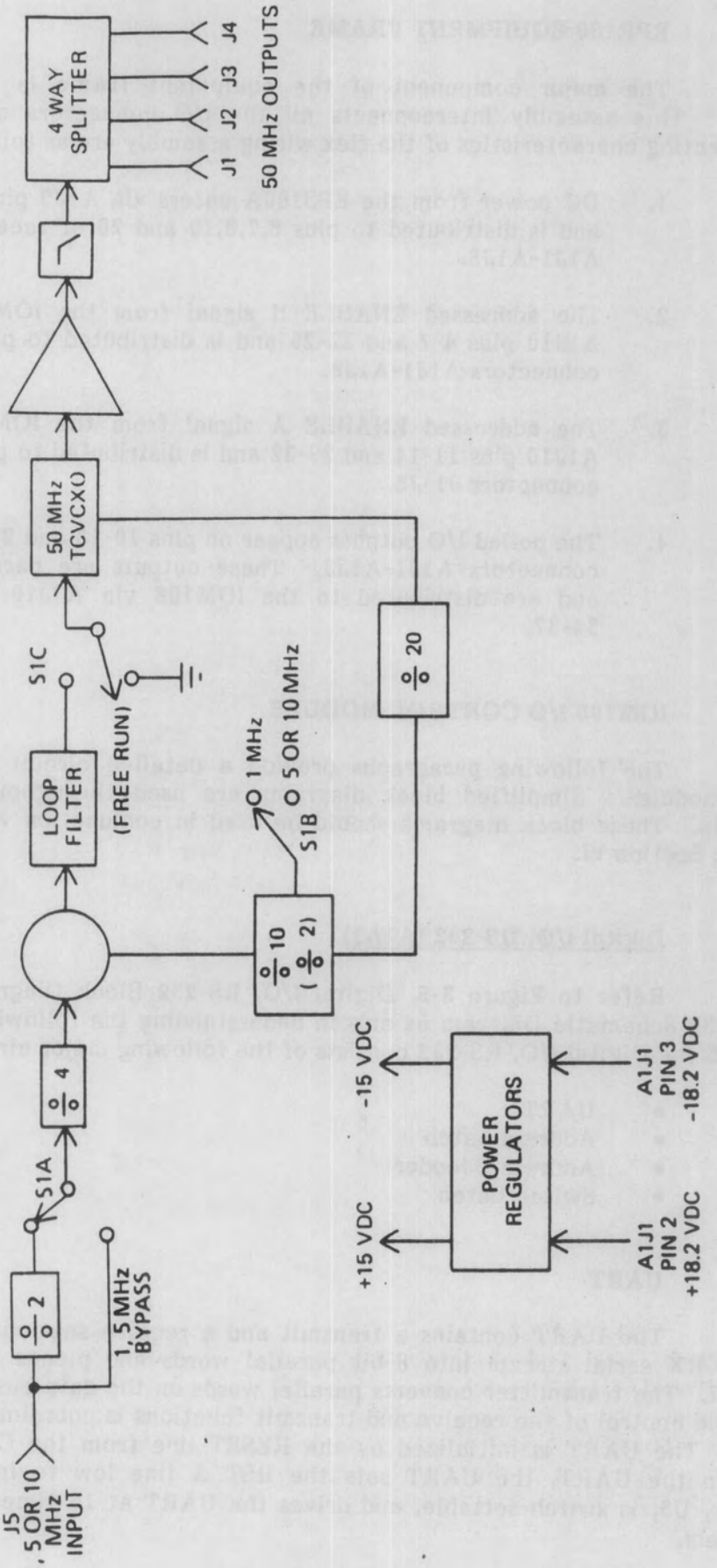


Figure 3-4. SRM105A Site Reference Module Block Diagram

3.4.1 EFR100 EQUIPMENT FRAME

The major component of the equipment frame is the backplane flex wiring assembly. This assembly interconnects all the I/O connectors on the frame. The major interconnecting characteristics of the flex wiring assembly are as follows:

1. DC power from the EPS100A enters via A1J9 pins 1-5 and 9-13, and is distributed to pins 6,7,8,19 and 20 of receiver connectors A1J1-A1J8.

2. The addressed ENABLE B signal from the IOM108 enters via A1J10 pins 4-7 and 22-25 and is distributed to pin 1 of receiver connectors A1J1-A1J8.

3. The addressed ENABLE A signal from the IOM108 enters via A1J10 pins 11-14 and 29-32 and is distributed to pin 9 of receiver connectors J1-J8.

4. The polled I/O outputs appear on pins 10-13 and 22-25 of receiver connectors A1J1-A1J8. These outputs are paralleled together and are distributed to the IOM108 via A1J10 pins 16-19 and 34-37.

3.4.2 IOM108 I/O CONTROL MODULE

The following paragraphs provide a detailed circuit description of each of the IOM108 modules. Simplified block diagrams are used throughout the text to clarify the description. These block diagrams should be used in conjunction with the schematic diagrams located in **Section VI.**

3.4.2.1 Digital I/O, RS-232 (A1A1)

Refer to **Figure 3-5,** Digital I/O, RS-232 Block Diagram, and **Figure 6-3,** Digital I/O, RS-232 Schematic Diagram as aids in understanding the following description. As shown in **Figure 3-5** the Digital I/O, RS-232 consists of the following major circuit areas:

- UART
- Address Latch
- Address Decoder
- Switch Latch

3.4.2.1.1 UART

The UART contains a transmit and a receive section. The receiver converts the incoming RX serial stream into 8-bit parallel words and places them on the IOM data bus, AD0-AD7. The transmitter converts parallel words on the data bus to a serial TX data stream. Timing and control of the receive and transmit functions is coordinated by the address latch and decoder. The UART is initialized by the RESET line from the CPU. When received data is present in the UART, the UART sets the RST A line low to interrupt the CPU. A clock generator, U5, is switch-settable, and drives the UART at 16 times the baud rate of the serial data stream.

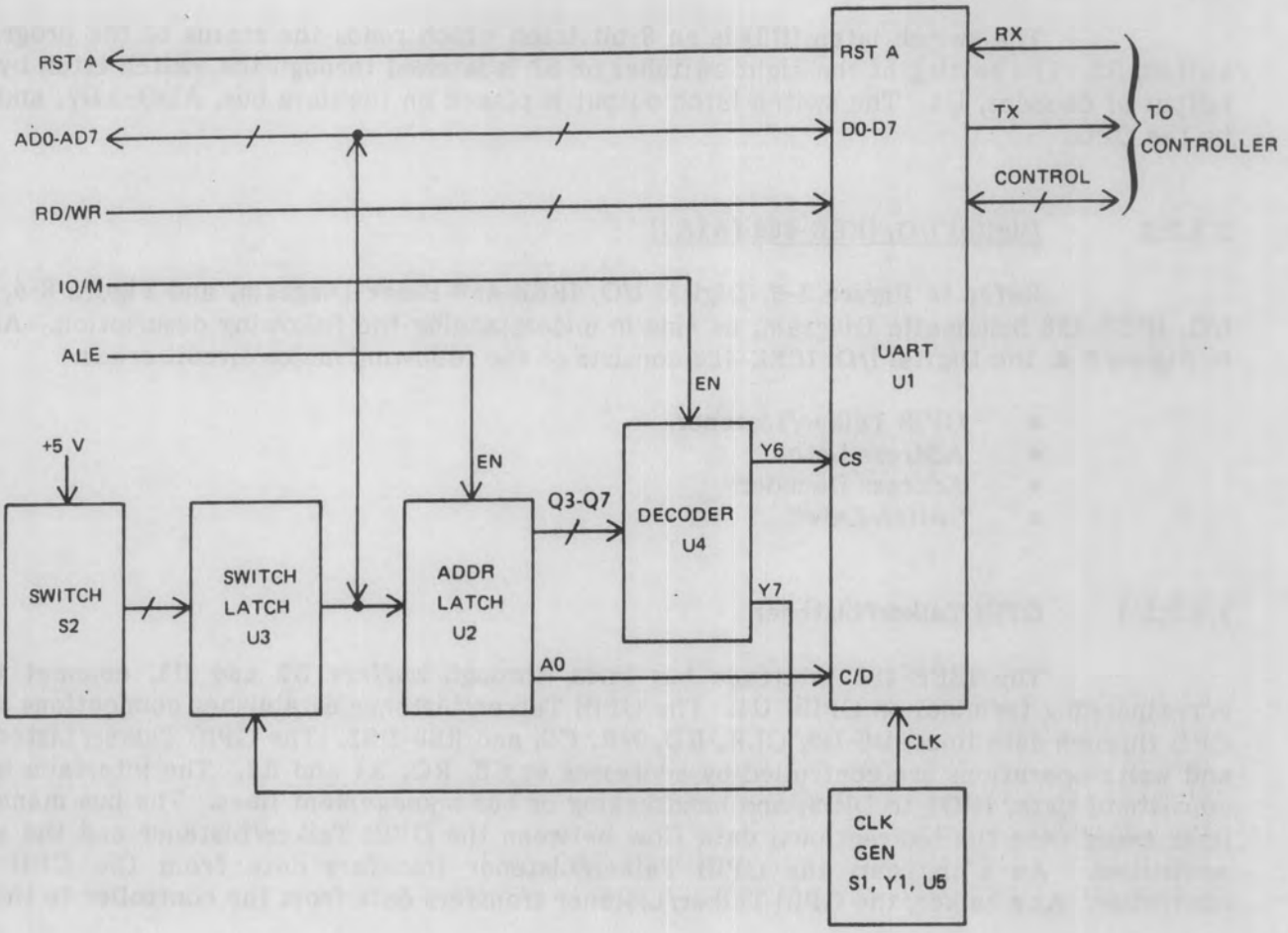


Figure 3-5. Digital I/O, RS-232, Block Diagram

3.4.2.1.2 Address Latch

The address latch is an 8-bit latch which captures and holds the address present on the AD0-AD7 bus. When a valid address is present at the input of the latch, the CPU brings the ALE line momentarily low, transferring the address to the Q outputs of the latch. The Q0 output selects the transmit or receive in the UART. Outputs Q3-Q7 drive the address and enable inputs to the decoder.

3.4.2.1.3 Address Decoder

The address decoder is a 3-to-8 line decoder. Its address bits are driven from the Q3-Q5 outputs of the address latch. Its enable inputs are driven from Q6 and Q7 of the latch and the IO/M* signal from the IOM control bus. The Y6 output enables the UART, while the Y7 output enables the switch latch.

*Indicates Active Low

3.4.2.1.4 Switch Latch

The switch latch (U3) is an 8-bit latch which reads the status of the programming switch, S2. The setting of the eight switches on S2 is latched through the switch latch by the Y7 output of decoder, U4. The switch latch output is placed on the data bus, AD0-AD7, and is read by the CPU.

3.4.2.2 Digital I/O, IEEE-488 (A1A1)

Refer to **Figure 3-6**, Digital I/O, IEEE-488 Block Diagram, and **Figure 6-4**, Digital I/O, IEEE-488 Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-6**, the Digital I/O, IEEE-488 consists of the following major circuit areas:

- GPIB Talker/Listener
- Address Latch
- Address Decoder
- Switch Latch

3.4.2.2.1 GPIB Talker/Listener

The IEEE-488 interface bus lines, through buffers U2 and U3, connect to their corresponding terminal on GPIB, U1. The GPIB Talker/Listener establishes connections with the CPU through data lines, D0-D7, CLK, RD, WR, CS, and RS0-RS2. The GPIB Talker/Listener read and write operations are controlled by addresses at CS, RO, R1 and R2. The interface bus lines consists of data, DIO1 to DIO8, and handshaking or bus management lines. The bus management lines coordinate the bidirectional data flow between the GPIB Talker/Listener and the external controller. As a listener, the GPIB Talker/Listener transfers data from the CPU to the controller. As a talker, the GPIB Talker/Listener transfers data from the controller to the CPU.

3.4.2.2.2 Address Latch

The address latch is an 8-bit latch which captures and holds an address present on the AD0-AD7 bus. When a valid address is present at the input of the latch, the CPU brings the ALE line momentarily low, transferring the address to the Q outputs of the latch. The Q0-Q2 outputs drive the RS0-RS2 inputs to the UART. Outputs Q3-Q7 drive the address and enable inputs of the decoder.

3.4.2.2.3 Address Decoder

The address decoder is a 3-to-8 line decoder. Its address bits are driven from the Q3-Q5 outputs of the address latch. Its enable inputs are driven from Q6 and Q7 of the latch and the IO/M signal from the IOM control bus. The Y6 output enables the Talker/Listener, and the Y7 output enables the switch latch.

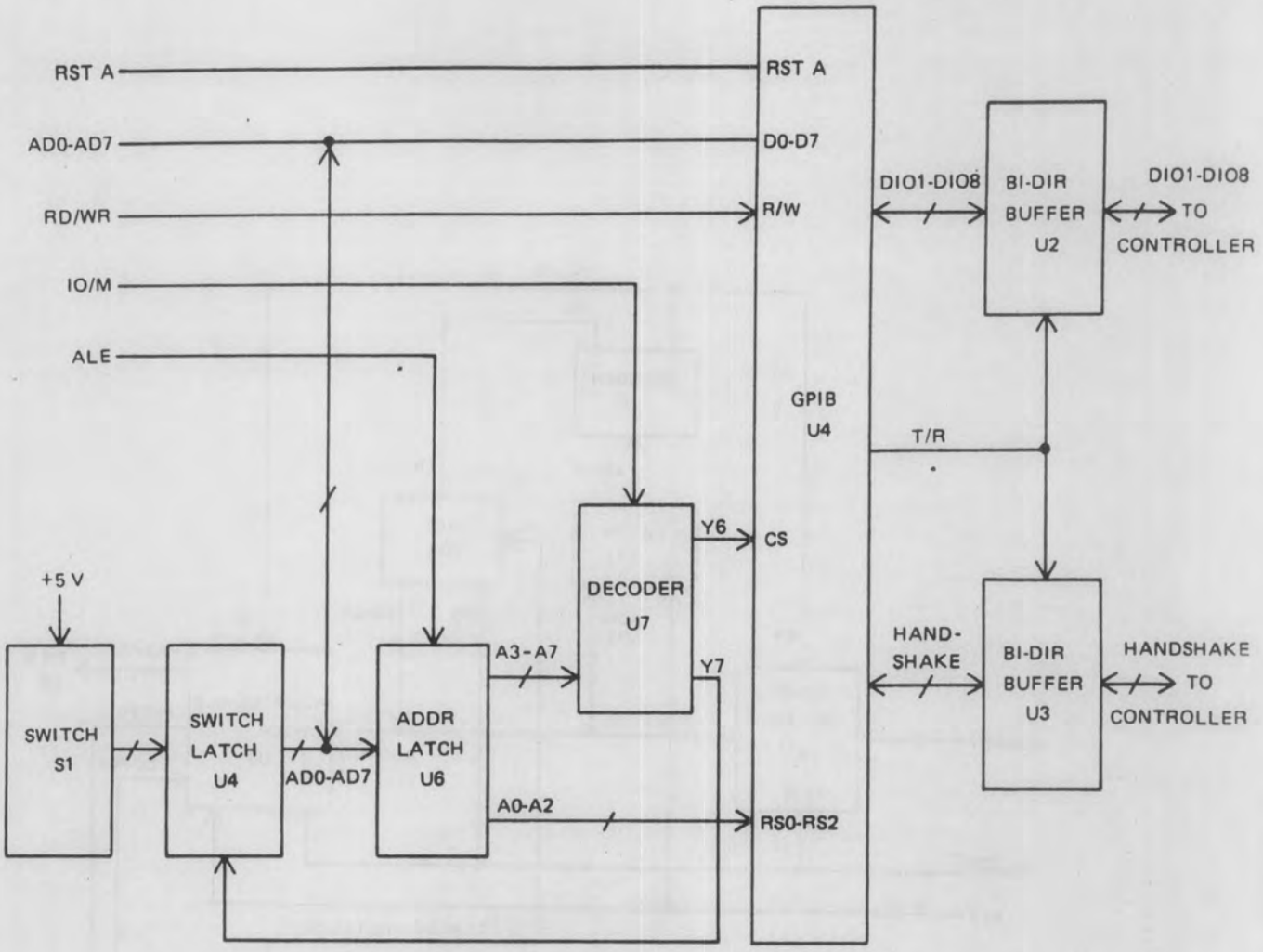


Figure 3-6. Digital I/O, IEEE-488, Block Diagram

3.4.2.2.4 Switch Latch

The switch latch is an 8-bit latch which reads the status of the programming switch, S1. The setting of the eight switches on S1 is latched through the switch latch by the Y7 decoder output. The switch latch output is placed on the data bus, AD0-AD7, and is read by the CPU.

3.4.2.3 Bidirectional Polled I/O Module (A1A2)

Refer to **Figure 3-7**, Polled I/O Block Diagram, and **Figure 6-5**, Bidirectional Polled I/O Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-7**, the bidirectional polled I/O consists of the following major circuit areas:

- Bidirectional Buffer
- Address Latch and Decoder
- Addressable Switch
- Polled I/O 3,4,5,6 Control
- Polled I/O 1,2,7,8 Control
- A/D Converter

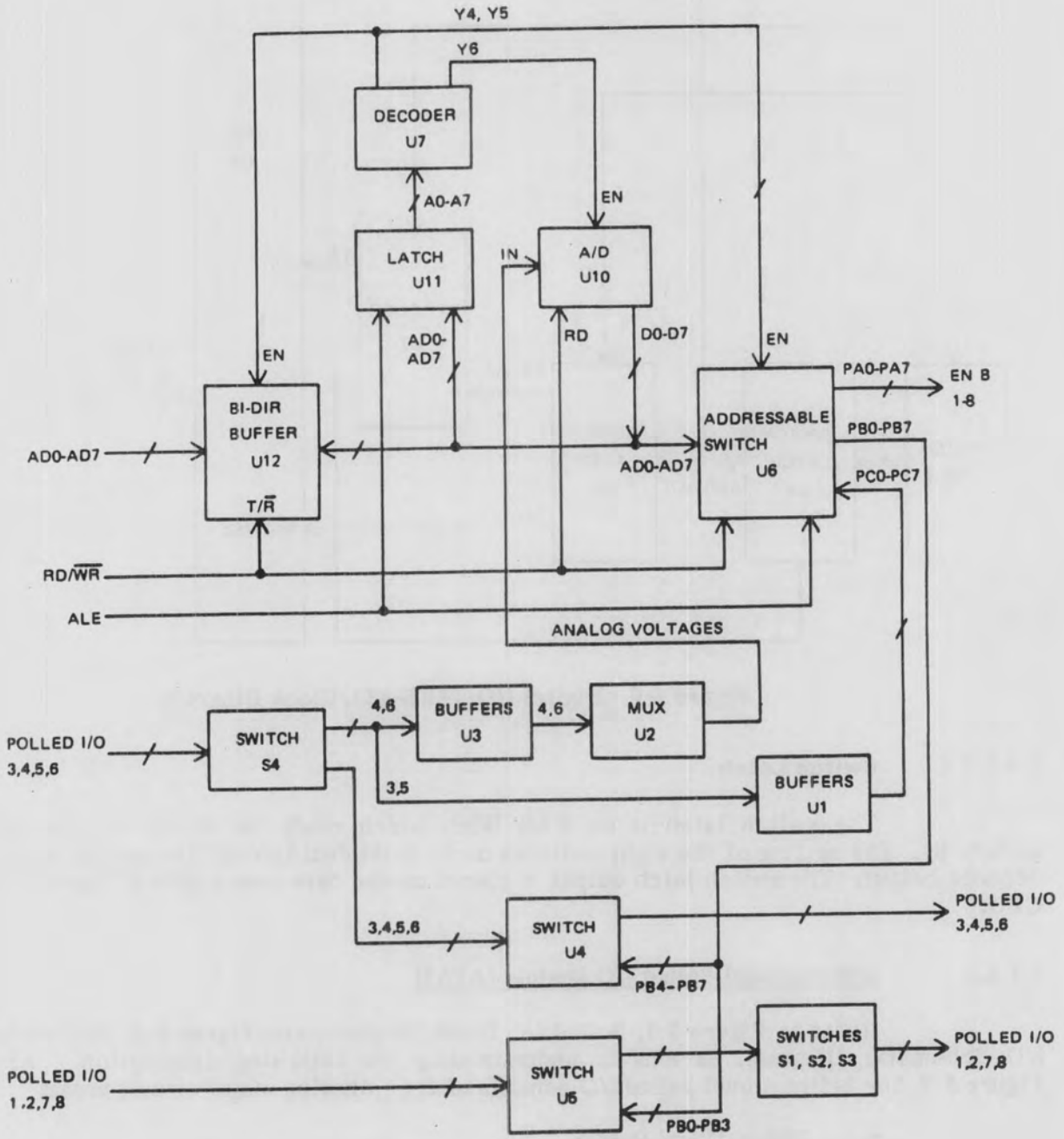


Figure 3-7. Bidirectional Polled I/O Block Diagram

3.4.2.3.1 Bidirectional Data Buffer

The data buffer is a bidirectional transceiver. The direction of data flow is controlled by the RD line from the CPU. The buffer is enabled by the address decoder output. When the RD line is high, the data buffer transfers data from the polled I/O module to the IOM data bus, AD0-AD7. When the RD line is low, the data buffer transfers data from the IOM data bus to the polled I/O module.

3.4.2.3.2 Address Latch and Decoder

The address latch is an 8-bit latch which captures and holds an address from the IOM data bus while a specific operation is performed. The CPU outputs an address on the IOM data bus and follows by bringing the ALE line momentarily low. This transfers the address on the D inputs of the latch to the Q outputs. The latched address output drives the address inputs of the address decoder. The address decoder is a 3-to-8 line decoder. It is enabled by the IO/M line from the IOM control bus. Only three outputs, Y4, Y5, and Y6 are used. The range of hex addresses used by the decoder are from 48 (U7-Y4) to 68 (U7-Y6). The following list shows the decoder outputs and their functions:

Y4, Y5 -- Select Addressable Switch
Y6 -- Select A/D Converter

NOTE

If Y4, Y5 and Y6 are not enabled, then the bidirectional buffer is enabled.

3.4.2.3.3 Addressable Switch

The addressable switch is a bidirectional I/O device which interfaces the IOM data bus to a number of other devices. The switch is configured by software to operate with seventeen outputs and three inputs. The direction of data transfer is controlled by the RD/WR lines from the IOM control bus. The A output ports are used to output the ENABLE A lines to the EFR100 Equipment Frame. In this operation, WR is low and the ENABLE A data word is transferred from the IOM data bus, AD0-AD7, to the A port outputs. The B and C ports are used for transferring data from the polled I/O inputs to the data bus and to the user connector J1. In this operation, RD is low, and the polled I/O data is transferred from the B and C ports to the IOM data bus, AD0-AD7 to be read by the CPU.

3.4.2.3.4 Polled I/O 3,4,5,6 Control

Polled I/O lines 3,4,5 and 6 from the EFR100 Equipment Frame slots pass through switch S4. Switch S4 can route the lines either through U3, U2 and U10 to the data bus, or through U1 and U6 to the data bus. Lines 4, 6 are varying analog voltages. Switch S4 is set to route these lines through buffer U3 and MUX U2 to the A/D converter, U10. The A/D is enabled by the address decoder and the RD line from the IOM bus. The A/D converts the analog voltages on lines 4 and 6 to 8-bit digital words and places them on the IOM data bus, AD0-AD7, to be read by the CPU. Switch S4 routes polled I/O lines 3,5 through buffer U1 to addressable switch U6. Lines 3,5 are digital lines, either high or low, and do not exceed analog-to-digital conversion.

The addressable switch transfers the data on the lines to the IOM data bus, AD0-AD7, to be read by the CPU.

3.4.2.3.5 Polled I/O 1,2,7,8 Control

Polled I/O 1,2,7,8 lines are normally audio signal lines, but may transfer other signals to the user or to other equipment. These four lines are first routed through addressable switch U5. This switch is addressed by the port B output of addressable switch U6. Switch U5 selects which of the four lines, 1,2,7 or 8, will be passed. The output of switch U5 goes through a matrix of switches composed of S1, S2 and S3. These switches permit selectable routing of the audio signal to different destinations.

3.4.2.3.6 A/D Converter

The A/D converter converts analog voltages from the polled I/O inputs to 8-bit data words. In typical operation, polled I/O 4 and 6 voltages are selectively routed by multiplexer U2 to the analog input of the A/D converter. The analog input voltage range is 0 to +3 Vdc, corresponding to a digital output of 0 to 255 binary. The converter continuously samples and converts analog input to digital words. The converted digital words are only placed on the IOM data bus when the A/D converter is enabled by the address decoder output, Y6.

3.4.2.4 System I/O (A1A3)

Refer to **Figure 3-8**, System I/O Block Diagram, and **Figure 6-6**, System I/O Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-8**, the System I/O consists of the following major circuit areas:

- UART
- Data Buffer
- I/O Data Latch
- Address Latch
- Address Decoder
- Enable B Data Latch
- Shift Register
- WJ-9040 I/O Buffer/Receiver
- Frame Select Buffer

3.4.2.4.1 UART

The UART (Universal Asynchronous Receiver Transmitter) is a bidirectional transmitter/receiver interfacing between the IOM data bus and the WJ-9040 serial interface data line. The UART has a parallel transmit input data port, TBR1-TBR8, and a parallel receive output data port, RB1-RB8. Transmit/receive select functions are controlled by the address decoder. In the transmit mode, parallel data input from the IOM bus drives the UART TBR port. The UART converts this to serial data and outputs the data via the TRO port. In the receive mode, serial data drives the RRI port of the UART. The UART converts this to parallel data and outputs the data via the RB port to the IOM data bus.

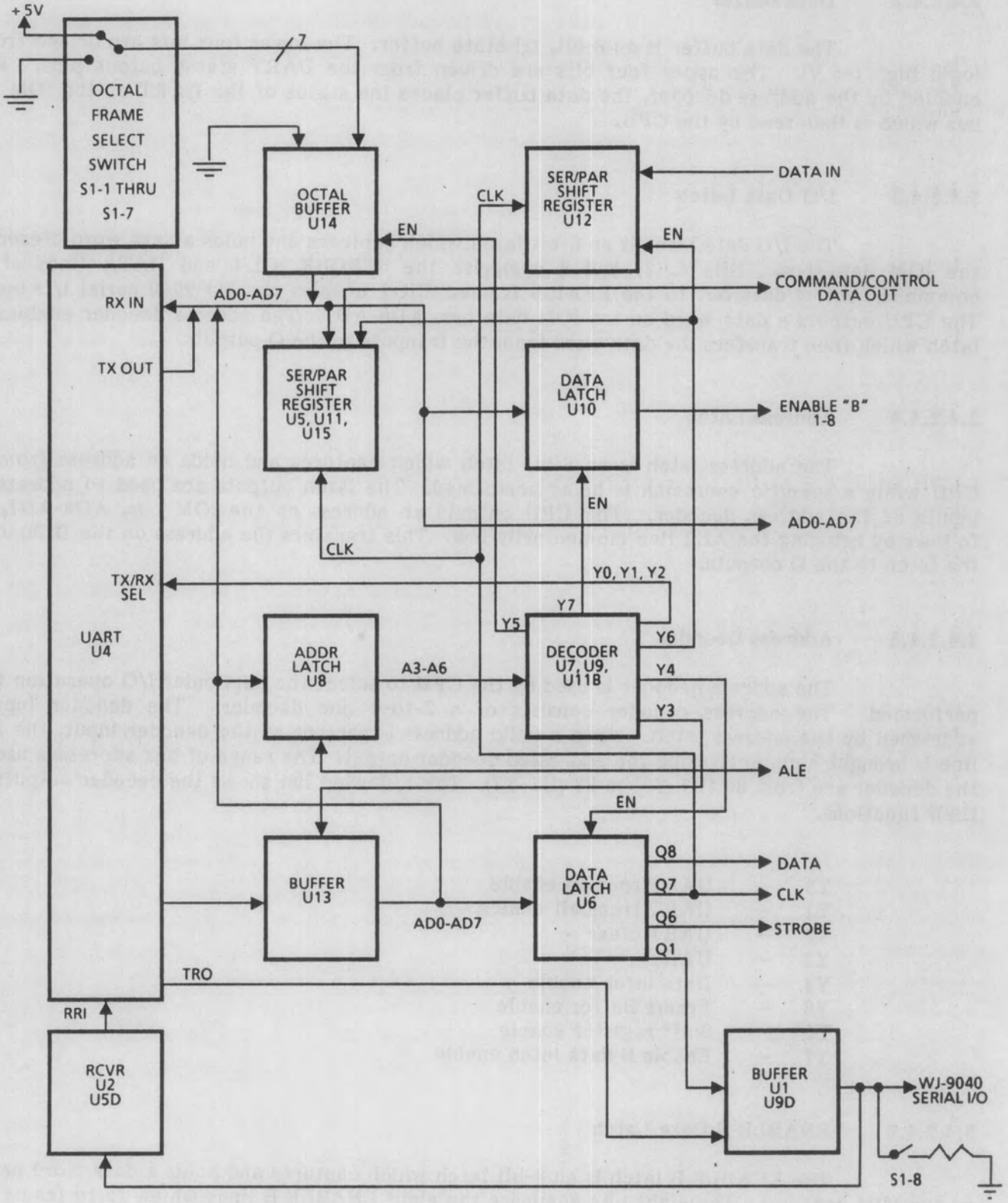


Figure 3-8. System I/O Block Diagram

3.4.2.4.2 Data Buffer

The data buffer is an 8-bit, tri-state buffer. The lower four bits are driven from a logic high (+5 V). The upper four bits are driven from the UART status output pins. When enabled by the address decoder, the data buffer places the status of the UART on the IOM data bus which is then read by the CPU.

3.4.2.4.3 I/O Data Latch

The I/O data latch is an 8-bit latch which captures and holds a data word present on the IOM data bus. Bits 6, 7, and 8 comprise the STROBE, CLK and DATA lines of the command/control data out to the EFR100 frame. Bit 1 enables the WJ-9040 serial I/O buffer. The CPU outputs a data word on the IOM data bus, AD0-AD7. The address decoder enables the latch which then transfers the data word from the D inputs to the Q outputs.

3.4.2.4.4 Address Latch

The address latch is an 8-bit latch which captures and holds an address from the CPU while a specific operation is being performed. The latch outputs are used to address the inputs of the address decoder. The CPU outputs an address on the IOM bus, AD0-AD7, and follows by bringing the ALE line momentarily low. This transfers the address on the D inputs of the latch to the Q outputs.

3.4.2.4.5 Address Decoder

The address decoder is used by the CPU to select the particular I/O operation to be performed. The address decoder consists of a 3-to-8 line decoder. The decoder input is addressed by the address latch. When a valid address is present at the decoder input, the IO/M line is brought high, activating the addressed decoder output. The range of hex addresses used by the decoder are from 80 (U7-Y0) to 88 (U7-Y7). The following list shows the decoder outputs and their functions.

Y0 — UART receive enable
Y1 — UART transmit enable
Y2 — UART clear
Y3 — UART
Y4 — Data latch enable
Y5 — Frame Buffer enable
Y6 — Shift register enable
Y7 — Enable B data latch enable

3.4.2.4.6 ENABLE B Data Latch

The ENABLE B latch is an 8-bit latch which captures and holds a data word present on the IOM data bus. The eight bits comprise the eight ENABLE B lines which go to frame slots in the EFR100. The CPU outputs a data word on the IOM bus which corresponds to the frame slot selected. Only one of the eight bits will be high, the other seven bits will be low. The

address decoder enables the latch which then transfers the ENABLE B data word from the D inputs of the latch to the Q outputs.

3.4.2.4.7 Shift Register

The shift register converts the serial report data coming in from the units in the EFR100 to parallel format and places it on the IOM data bus. Serial data drives the shift register data input and is clocked into the register via the CLOCK from U6-Q7. When all eight bits of serial data have been clocked in, the address decoder enables the shift register which then places the data directly on the IOM data bus, AD0-AD7.

3.4.2.4.8 WJ-9040 I/O Buffer Receiver

Unity gain buffer amplifier, U1, interfaces the WJ-9040 serial data output from the UART to the serial output line. U1 has a capability to drive a 50 ohm line. Line receiver, U2, converts the WJ-9040 serial input data to TTL level data and operates with hysteresis to sharpen noisy input data and provide a clean square data line to the UART input.

3.4.2.4.9 Frame Select Switch and Buffer

The Frame Select Switch S1 configures the WJ-9040 System by identifying the number of EFR100 equipment frames that are present in the system. When enabled by Address Decoder U7, octal buffer U14 writes this information to the address/data bus.

Seven inputs of buffer U14 are tied through resistor network RN1 to a +5 Vdc logic high. Closing one of seven S1 switch positions pulls the +5 Vdc logic to ground causing a logic low to be seen at the associated buffer input. Generally, switch positions 5 through 7 are not used. One input of U14 is always tied to ground. The eighth position of octal switch S1 is used to switch in R2, which provides a 56-ohm termination to the serial output stream. This termination path is only required in the IOM108 that is contained in the last EFR100 in a series of frames; otherwise, S1-8 remains open. This switch is configured at the factory according to system requirements. For multiple equipment frame operation, set S1 as follows:

# of EFR100s in system	S1-1	S1-2	S1-3	S1-4	S1-5	S1-6	S1-7	S1-8
1	C	O	O	O	N/U	N/U	N/U	C
2	O	C	O	O	N/U	N/U	N/U	X
3	C	C	O	O	N/U	N/U	N/U	X
4	O	O	C	O	N/U	N/U	N/U	X
5	C	O	C	O	N/U	N/U	N/U	X
6	O	C	C	O	N/U	N/U	N/U	X
7	C	C	C	O	N/U	N/U	N/U	X
8	O	O	O	C	N/U	N/U	N/U	X

C = Closed O = Open X = Open unless contained in last frame of series

3.4.2.5 Extended CPU (A1A5)

Refer to **Figure 3-9,** Extended CPU Block Diagram, and **Figure 6-7,** Extended Memory Schematic Diagram and **Figure 6-8,** CPU Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-9,** the Extended CPU consists of the following major circuit areas:

- CPU Chip
- Bidirectional Data Latch
- Address Latch
- Address Decoder
- ROM
- RAM

NOTE

Early IOM108 Module configurations have the Extended Memory (A1A4) and the CPU (A1A5) as separate boards. Current IOM108 Modules have these two boards combined as the Extended CPU (A1A5).

3.4.2.5.1 CPU Chip

The NSC-800 CPU chip controls a 16-bit address bus and an 8-bit data bus. The lower eight bits of address are in common with the data bus (AD0-AD7). A 4.9152 MHz crystal oscillator circuit, Y1, sets the clock rate for the CPU. The CPU chip also outputs the RD*, WR*, IO/M*, ALE and other control signals necessary for I/O control. It performs instructions which are obtained from the control program contained in the program memory (ROM). These instructions are routed to the instruction register of the CPU and then carried out during instruction cycles. Each instruction cycle specifies the functions to be performed by the rest of the IOM108.

The CPU addresses memory through the address latch U6 for the lower eight bits of address (AD0-AD7) and directly through the address bus for the upper eight bits of address (A8-A15). Data is transferred between the CPU chip and either a memory or the IOM data bus via the data latch.

3.4.2.5.2 Bidirectional Data Buffer U6

The data buffer is a bidirectional transceiver. The direction of data flow is controlled by the RD line from the CPU. When the RD* line is high, the data buffer transfers data from the CPU to the IOM data bus, AD0-AD7. When the RD* line is low, the data buffer transfers data from the IOM data bus to the CPU.

*Indicates Active Low

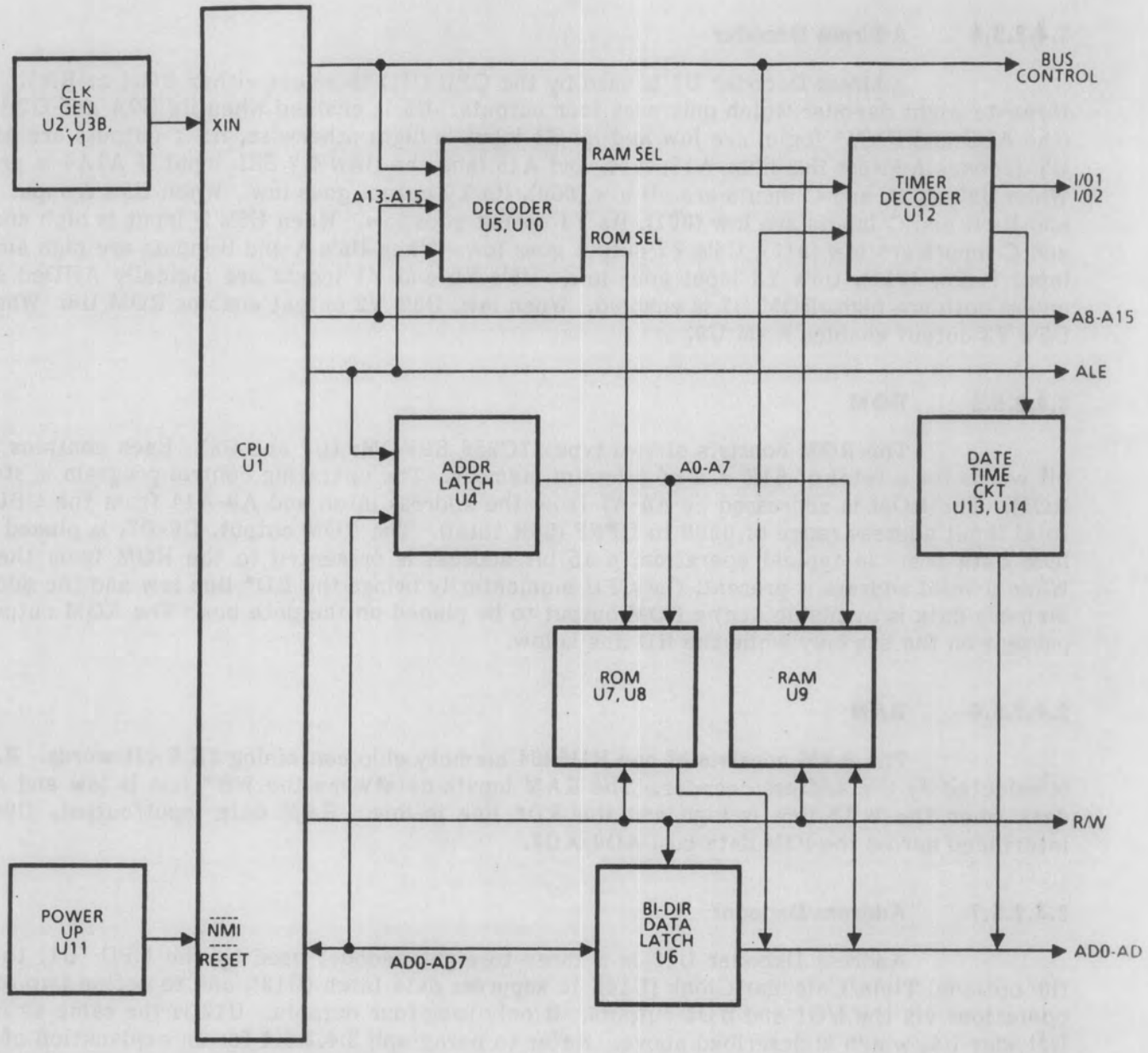


Figure 3-9. Extended CPU Block Diagram

3.4.2.5.3 Address Latch U4

The address latch is an 8-bit latch which captures and holds an address from the CPU while a specific operation is being performed. The latch outputs are used to address the lower eight bits of ROM and RAM. The CPU outputs an address on the AD0-AD7 bus and follows by bringing the ALE line momentarily high. This transfers the data on U4's D inputs to its Q outputs, to form the address bus A0-A7. The latched address output drives the address inputs of the ROM and RAM.

3.4.2.5.4 Address Decoder

Address Decoder U5 is used by the CPU (U1) to select either ROM or RAM. It is a three-to-eight decoder which only uses four outputs. U5 is enabled when its G2A and G2B inputs (the ALE and IO/M* logic) are low and its G1 input is high; otherwise, its Y outputs are all high. U5 decodes Address Bus lines A13, A14, and A15 (and the BANK 2 SEL input if A1A4 is present). When U5's A, B, and C inputs are all low (000), its Y0 output goes low. When U5's A input is high and its B and C inputs are low (001), its Y1 output goes low. When U5's B input is high and its A and C inputs are low (010), U5's Y2 output goes low. When U5's A and B inputs are high and its C input is low (011), U5's Y3 input goes low. U5's Y0 and Y1 inputs are logically ANDed so that unless both are high, ROM U7 is enabled. When low, U5's Y2 output enables ROM U8. When low, U5's Y3 output enables RAM U9.

3.4.2.5.5 ROM

The ROM consists of two type 27C256 EPROMs (U7 and U8). Each contains 32K 8-bit words for a total of 64K X 8 of program memory. The operating control program is stored in ROM. The ROM is addressed by A0-A7 from the address latch and A8-A14 from the CPU for a total input address range of 0000 to DFFF (56K total). The ROM output, D0-D7, is placed on the IOM data bus. In typical operation, a 15 bit address is presented to the ROM from the CPU. When a valid address is present, the CPU momentarily brings the RD* line low and the addressed memory data is available at the ROM output to be placed on the data bus. The ROM outputs are present on the bus only while the RD line is low.

3.4.2.5.6 RAM

The RAM consists of one HM6264 memory chip containing 8K 8-bit words. RAM U9 is selected by the address decoder. The RAM inputs data when the WR* line is low and outputs data when the WR* line is high and the RD* line is low. RAM data input/output, D0-D7, is interfaced across the IOM data bus, AD0-AD7.

3.4.2.5.7 Address Decoder

Address Decoder U12 is a three-to-eight decoder used by the CPU (U1) to select the optional Time/Calendar Clock (U14), to suppress data latch (U13), and to define two external operations via the I/O1 and I/O2 outputs. It only uses four outputs. U12 is the same as Address Decoder U5, which is described above. Refer to **paragraph 3.4.2.5.4** for an explanation of gating and decoding logic. U12's inputs are enabled by A2 and A4-A7 of the CPU Address Bus and the IO/M* line. U12 is addressed by A0, A1, and A3 of the CPU Address bus. When low, U12's Y0 output is used to suppress data latch U13 during write cycles. When low, U12's Y1 output is used to enable optional Time Calendar Clock (U14). When low, U12's Y2 and Y3 outputs are used to define operations on the optional A4A4 assembly via the I/O1 and I/O2 outputs.

3.4.2.5.8 Date/Time Circuitry (Option)

The Date/Time Circuitry is made up of U13, U14, Y2 and their associated parts. When clock pulses are received from the Timer Decoder, the hex D flip-flop (U13) provides Q1, Q2, Q3, and Q4 signals to U14, a real time clock. If a chip select signal is present at U14, these inputs determine the outputs to the CPU data bus. Timing for U14 is provided by Y2, a 32.768 MHz crystal. The Date/Time Circuitry is an option to the basic IOM108.

*Indicates Active Low

3.4.3 EPS100A POWER SUPPLY

Refer to **Figure 3-10,** EPS100A Power Supply Block Diagram, as an aid in understanding the following detailed circuit descriptions.

3.4.3.1 AC Input Circuitry

AC input power (115/230 Vac) passes through fuse F1 and the line voltage selector to the power transformer. The voltage selector configures the primary of the transformer to accept 115 or 230 Vac, as required. The power transformer provides AC outputs to two main circuit areas:

- 115 Vac to the switching regulator
- 24 Vac to the +8.2 V regulator

3.4.3.2 Switching Regulator

The primary of the power transformer sends 115 Vac to the switching regulator. This voltage passes through a line filter to a rectifier/filter, which provides approximately +150 Vdc output. This DC voltage drives the switching oscillator which operates at 20 kHz. The output of the switching oscillator drives the switching transformer. The switching transformer has three secondary outputs, each rectified by a single rectifier and filtered to provide DC outputs of +29 V, +18 V, and -18 V. The +29 V output is sampled and fed to the switching regulator circuit. This regulator varies the drives to the switching oscillator to maintain the +29 V output at its nominal rating. The +18 V and -18 V outputs are automatically compensated by the switching regulator.

3.4.3.3 +8.2 V Regulator

The 24 Vac secondary output of the power transformer is rectified and filtered to give approximately +12 Vdc. This voltage is dropped to +8.2 V by the +8.2 V regulator circuit.

3.4.4 SRM105A SITE REFERENCE MODULE

Refer to **Figure 6-10,** SRM105A 1 MHz, 5 MHz Site Reference Module Schematic Diagram, as an aid in understanding the following detailed circuit description. As shown in **Figure 6-10,** the SRM105A consists of the following major circuit areas:

- Temperature Compensated Crystal Oscillator
- Output Buffer and Splitter
- External Reference Input Conditioning
- Loop Divider
- Phase Detector

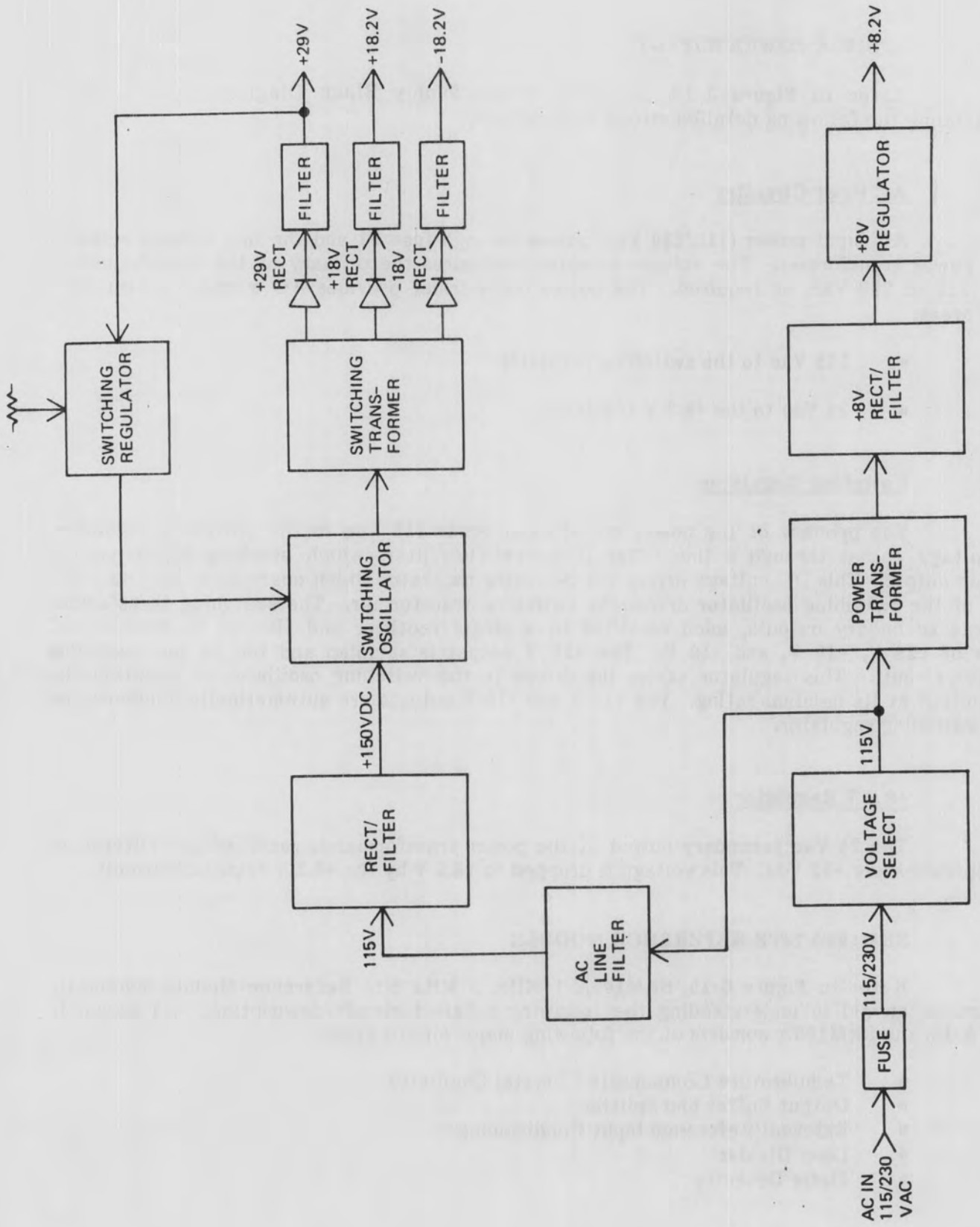


Figure 3-10. EPS100A Power Supply Block Diagram

3.4.4.1 Temperature Compensated Crystal Oscillator (U3)

The temperature compensated crystal oscillator, U3, generates stable 50 MHz sine wave signals at 0 dBm output level and operates in two modes, fixed and variable. With pin 4 grounded through S1, U3 is in fixed mode. The stability of oscillation, in the order of ±1 ppm, is determined by U3 internal components. With pin 4 connected to the phase locked loop output through S1, U3 is in the variable mode. The frequency of oscillation is determined by the voltage output of the loop. The voltage output of U3 is split by splitter U4 with one output driving loop divider, U5, and the other output driving the output buffer.

3.4.4.2 Output Buffer and Splitter (U4)

The 50 MHz output from splitter, U4, is amplified by buffer U6 to a level of +10 dBm. The signal is then split by splitter U7 to give four outputs at approximately 0 dBm each. These outputs appear at J1-J4 as the 50 MHz reference outputs.

3.4.4.3 External Reference Input Conditioning

The 1/5 MHz external reference input signal is conditioned by line receiver U10B and converted to TTL level square waves. The signal then passes through or around bypass divider U11, as selected by switch S1A. The signal is then further conditioned by U10A and drives the input of the phase detector. When a 10 MHz external reference is used, S1 is set so U11 is in the circuit, and the output of U10A is 5 MHz. When a 1 MHz external reference is used, S1 is set so U11 is out of the circuit, and the output of U10A is 1 MHz. When a 5 MHz external reference is used S1 is set so U11 is out of the circuit, and the output of U10 is 5 MHz.

3.4.4.4 Loop Divider (U5)

Loop divider U5 is driven from the 50 MHz reference output of splitter U4. Divider U5 provides a fixed divide ratio of 20. The U5 output, 2.5 MHz, drives the variable or "unknown" input of phase detector U1.

3.4.4.5 Phase Detector/Programmable Divider (U1)

The phase detector/programmable divider, U1, compares the 2.5 MHz signal from the loop divider with either a 1 or 5 MHz external reference input from the input conditioning circuit. If a 5 MHz input is used, switch S1B sets U1 to internally divide the loop divider output by 2. If a 1 MHz input is used, S1B sets U1 to internally divide the loop divider output by 10. The 1 or 5 MHz external reference signal is internally divided by 4 by U1. The output from U1 is the frequency error tuning voltage. This voltage is filtered by loop filter U2. When S1C is in the LOCKED position, the loop filter output forces the 50 MHz output of U3 to "lock" to the 1 or 5 MHz external reference input.

3.5 WJ-9040 SYSTEM COMMON EQUIPMENT SOFTWARE DESCRIPTION

The major control and interface element within the WJ-9040 System Common Equipment is the IOM108 module. This paragraph describes the major software routines used by the IOM108 in executing its normal functions. The IOM108 software is resident in the Extended CPU module, A1A5, and works in conjunction with other modules in the IOM108 to perform interfacing and control of the WJ-9040 modules installed in the equipment frame. Briefly, the IOM108 software performs the following functions:

- Initializes the memory, polled I/O, and digital I/O upon power up.
- Checks configuration of all connected hardware.
- Maintains an active memory list of active hardware slots and equipment types installed.
- Responds to polled I/O requests from the equipment frame.
- Responds to commands from the remote computer.
- Responds to WJ-9040 serial I/O commands.

These functions are performed by five main programming routines within the IOM108 software. **Figure 3-11** is a simplified flow diagram showing the software flow for the five routines. As shown, the five main routines are:

- Power Up Initialization
- Main Loop
- Serial I/O Interrupts
- IEEE-488/RS-232 Interrupts
- Service Requests

These routines will be explained in greater detail in the following paragraphs.

3.5.1 POWER UP INITIALIZATION

The power up initialization routine is activated immediately after application of power to the IOMI08. The routine accomplishes the following functions:

- Clears all flags and variables stored in memory.
- Checks the status of the equipment frame to get an updated configuration list.
- Sets the digital I/O hardware and polled I/O ports.
- Transfers software control to the main loop.

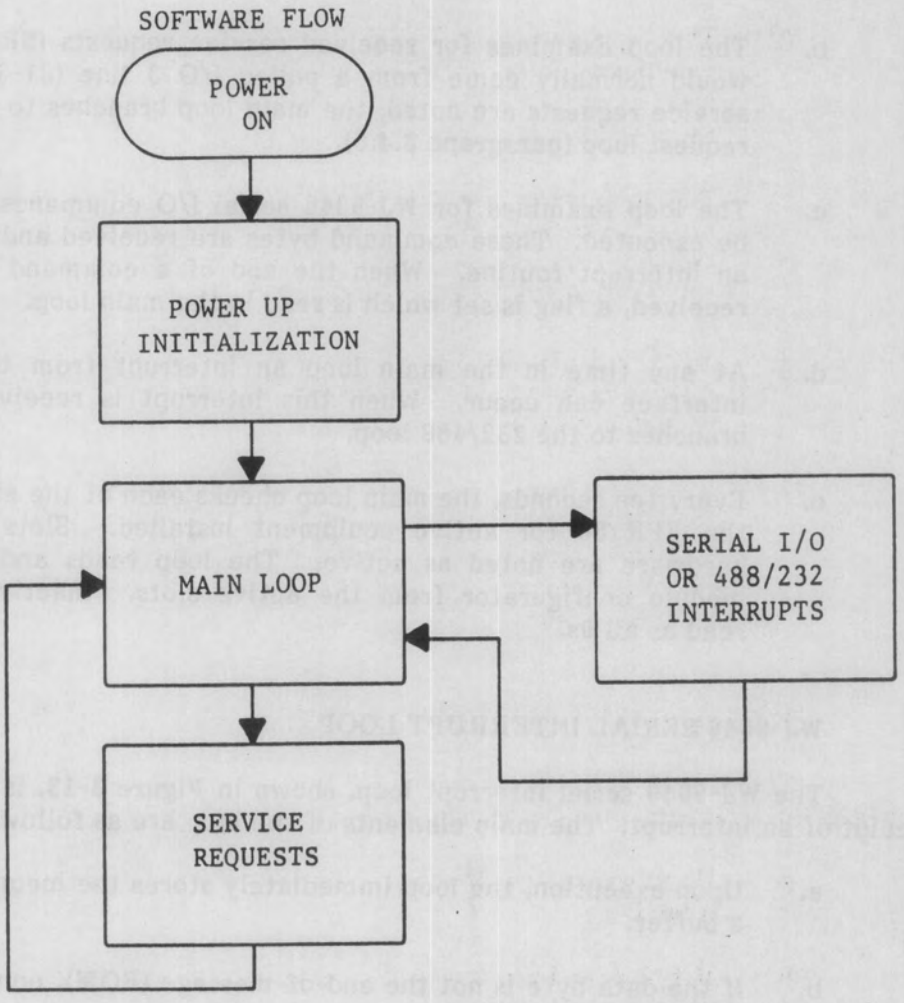


Figure 3-11. Simplified Software Flow Diagram

3.5.2 MAIN LOOP

The main loop, shown in **Figure 3-12,** is a series of routines that repeat continuously. In the absence of either a service request or an I/O request, the main loop runs a continuous cycle. The main elements of the loop are as follows:

a. The loop searches memory for the list of active slots in the EFR100 Equipment Frame. Active slots are then sequentially polled and the polled I/O parameters are transferred to the IOM108.

b. The loop examines for received service requests (SRQs). SRQs would normally come from a polled I/O 3 line (J1-35). If any service requests are noted, the main loop branches to the service request loop **(paragraph 3.4.5).**

c. The loop examines for WJ-9040 serial I/O commands waiting to be executed. These command bytes are received and handled by an interrupt routine. When the end of a command message is received, a flag is set which is read in the main loop.

d. At any time in the main loop an interrupt from the 232/488 interface can occur. When this interrupt is received, control branches to the 232/488 loop.

e. Every ten seconds, the main loop checks each of the eight slots in the EFR100 for active equipment installed. Slots containing hardware are noted as active. The loop reads and stores the module configurator from the active slots. Inactive slots are read as all 0s.

3.5.3 WJ-9040 SERIAL INTERRUPT LOOP

The WJ-9040 serial interrupt loop, shown in **Figure 3-13,** is automatically executed upon receipt of an interrupt. The main elements of the loop are as follows:

a. Upon execution, the loop immediately stores the incoming byte in a buffer.

b. If the data byte is not the end-of-message (EOM), control returns directly to the main loop.

c. Upon receipt of EOM, the loop generates and sends a checksum to the controller.

d. The loop then sets a command flag, and control returns to the main loop.

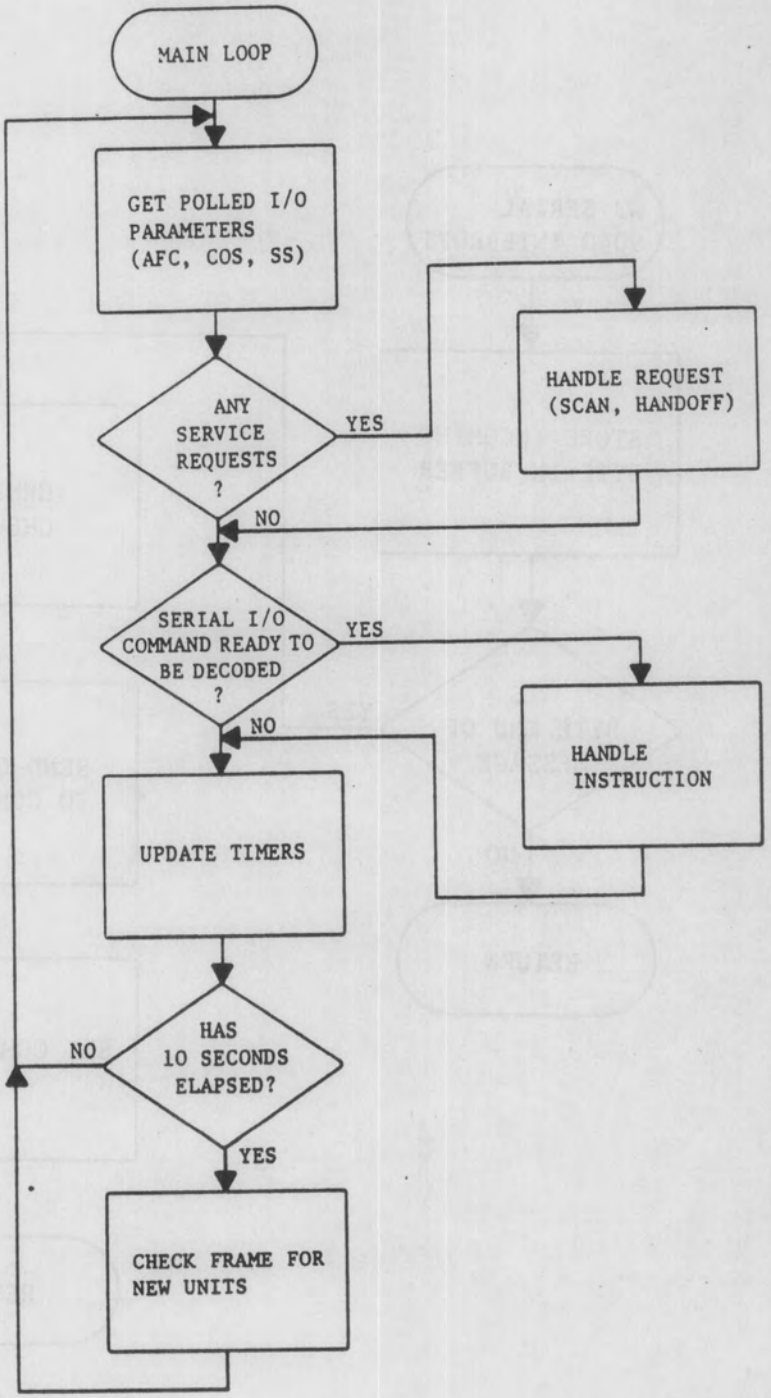


Figure 3-12. Main Loop Software Flow Diagram

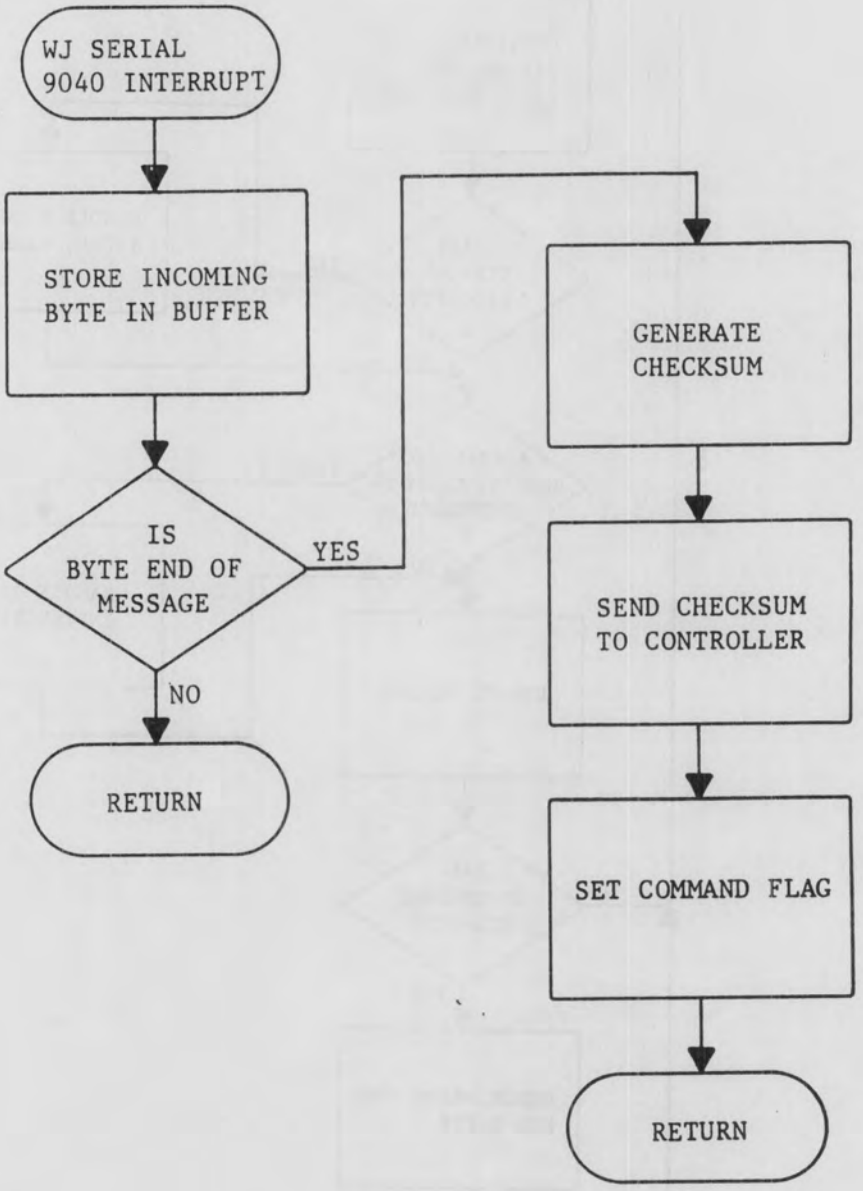


Figure 3-13. WJ-9040 Serial Interrupt Loop Software Flow Diagram

3.5.4 IEEE-488/RS-232 INTERRUPT LOOP

The IEEE-488/RS-232 interrupt loop, shown in **Figure 3-14**, is automatically executed upon receipt of an interrupt. The main elements of the loop are as follows:

a. Upon execution, the loop immediately transmits or receives the data string.

b. Upon receipt of the end-of-message (EOM), the current string is decoded and control returns to the main loop.

c. If no EOM is received at the end of the data string, control returns directly to the main loop.

d. Control returns to the main loop.

3.5.5 SERVICE REQUEST

The service request loop, shown in **Figure 3-15**, is automatically executed by the main loop upon receipt of a service request. The main elements of the loop are as follows:

a. Upon execution, the loop first verifies that a valid service request exists. If no pending requests are found, control returns to the main loop.

b. If a valid service request is found, the loop checks to see if it is an IOM scan request generated by the 232/488 or a HANDOFF/continuous control request generated by a WJ-862X-4 receiver. If either is found, the loop branches to an appropriate subroutine to handle the request.

c. If the service request is one defined by a user option, the loop branches to an appropriate subroutine to handle the specific task.

d. Control returns to the main loop.

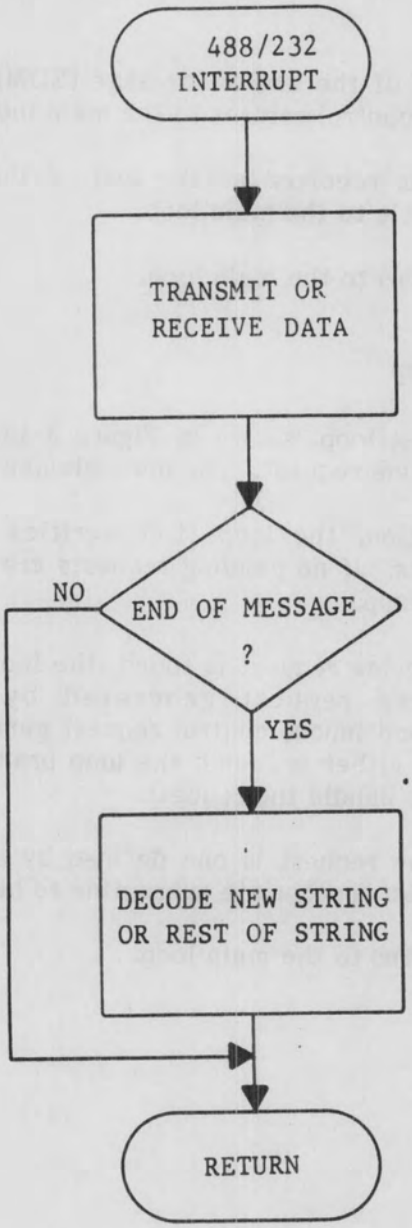


Figure 3-14. IEEE-488/RS-232 Interrupt Loop Software Flow Diagram

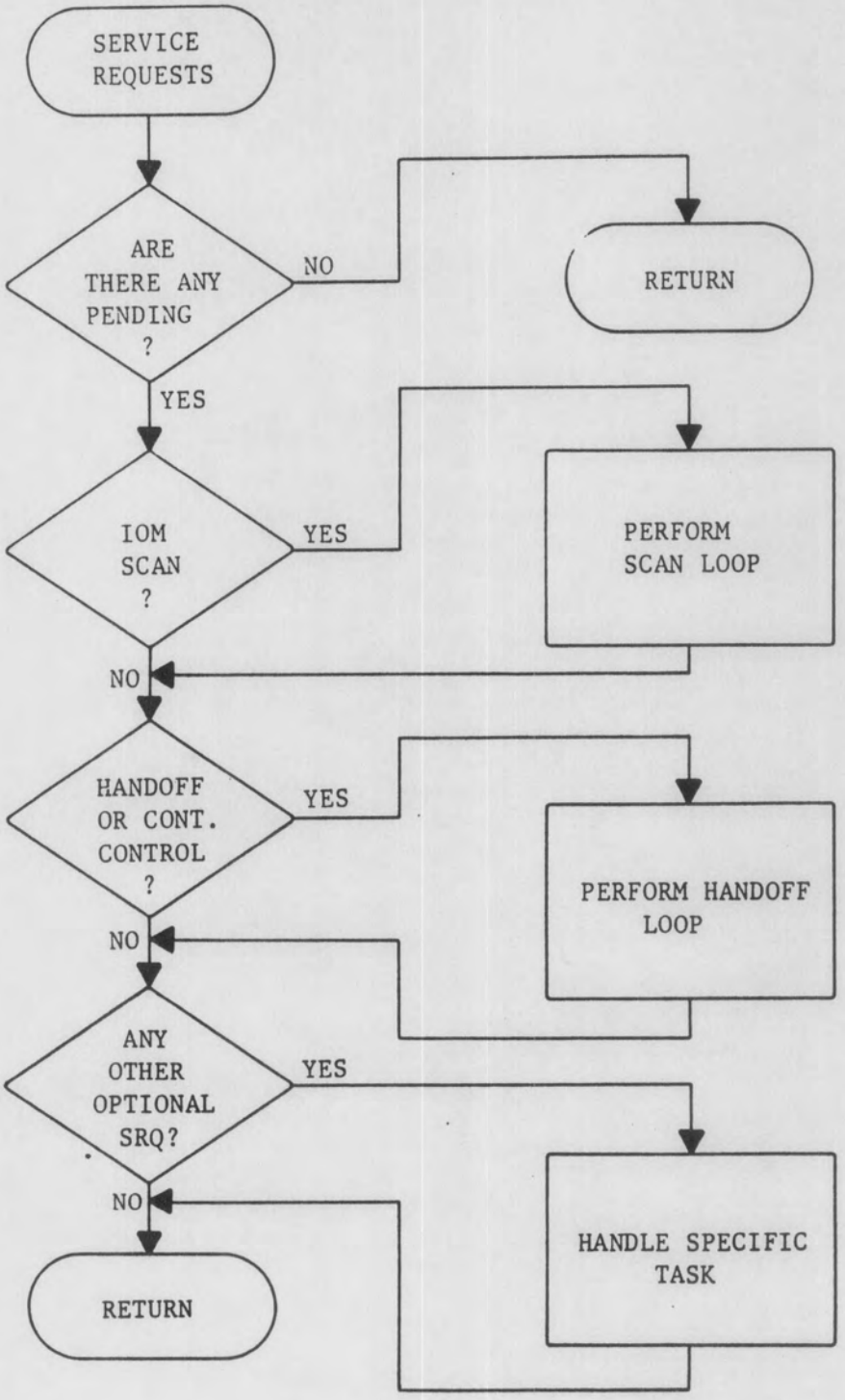


Figure 3-15. WJ-9040 Service Request Loop Software Flow Diagram

SECTION IV

MAINTENANCE

SECTION IV

MAINTENANCE

4.1 GENERAL

This section contains maintenance procedures for the WJ-9040 System Common Equipment. Included are preventive maintenance procedures, performance verification tests and troubleshooting.

4.2 MODULE ACCESS

The following paragraphs describe the procedures used to gain internal access to any of the four modules comprising the WJ-9040 System Common Equipment.

4.2.1 EFR100 EQUIPMENT FRAME

The following procedure is used to gain access to any of the eight receiver slots in the EFR100:

1. Remove the EFR100 from the equipment rack.
2. Use a Phillips screwdriver to loosen ten quarter turn fasteners securing the top cover.
3. Lift the top cover up and away from the frame.

4.2.2 IOM108 I/O CONTROL MODULE

The following procedure is used to gain access to any of the five IOM108 modules:

1. Locate the IOM108 module in the equipment frame.
2. Remove any cables connected to the module.
3. Remove four Phillips screws securing the top cover.
4. Remove nut and washer from BNC connector, if they exist on top.
5. Remove the top cover from the IOM108.

4.2.3 EPS100A POWER SUPPLY

The following procedure is used to gain internal access to the EPS100A Power Supply:

1. Locate the EPS100A module in the equipment frame.
2. Remove fourteen Phillips screws holding the top cover in place.
3. Remove the top cover from the EPS100A.

4.2.4 SRM105A SITE REFERENCE MODULE

The following procedure is used to gain internal access to the SRM105A module:

1. Locate the SRM105A in the equipment frame.
2. Remove the SRM105A from the equipment frame.
3. Remove four Phillips screws holding the side cover in place.
4. Remove the side cover from the SRM105A.

4.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of visual inspection and cleaning. The procedures described in this paragraph are designed to improve the module's reliability by preventing breakdowns and uncovering potential malfunctions before they impair operation of the unit. **Table 4-1** is the recommended schedule for performing preventive maintenance procedures.

Table 4-1. Preventive Maintenance Schedule

Procedure	Interval	Comments
Cleaning	60 days	Interval variable depending on operating environment.
Inspection for damage	60 days	Interval variable depending on operating environment and equipment use.
Performance tests	180 days	Interval variable depending on operating environment and equipment use.
Adjustment/Alignment		Not required.

4.3.1 VISUAL INSPECTION

Many potential or existing faults can be detected by making a visual inspection of the unit. For this reason, a complete visual inspection should be made on a routine basis and whenever the module is inoperative. At a minimum, the unit should be inspected for the following items:

1. Inspect the cover and enclosure for condition of finish and panel marking.
2. Inspect for dents, punctures, or warped areas.
3. Inspect for loose or missing screws or washers.
4. Inspect the receptacles for condition of pins, contacts, and mountings.
5. Inspect the internal components for signs of deterioration, discoloration or charring. Check for melted insulation and damaged, cracked, or broken components.
6. Inspect the printed circuit boards for damaged tracks, loose connections, corrosion, or other signs of deterioration.
7. Inspect the PC connectors, interface connectors, and chassis wiring for excessive wear, looseness, misalignment, corrosion, or other signs of deterioration.

4.3.2 CLEANING

Perform cleaning to remove accumulated dust and other contamination, and to ensure trouble-free operation.

1. Exterior - Dust the cabinet with a soft cloth or a small soft-bristled paint brush. Dirt clinging to the cabinet may be removed with a clean lint-free cloth dampened with a mild detergent and water solution. Avoid using abrasive cleaners. They will scratch the finish.
2. Interior - Dust in the interior of the unit should be removed before it builds up enough to cause arcing and short circuits during periods of high humidity. Dust is best removed by dry, low-pressure air. Dirt on surfaces may be removed with a soft-bristled paint brush or a clean, lint-free cloth dampened with a mild detergent and water solution. Use a cotton tipped applicator for cleaning in narrow spaces and on the circuit boards.

4.4 WJ-9040 SYSTEM COMMON EQUIPMENT PERFORMANCE TESTS

4.4.1 GENERAL

The Performance Tests outlined in this paragraph define the minimum performance standards which ensure proper unit functioning under local equipment frame control, IEEE-488/RS-232 control, and WJ-9040 System controller applications. The tests should be used for initial inspection, preventive maintenance checks, troubleshooting and post-repair performance verification.

4.4.2 MINIMUM PERFORMANCE STANDARDS

Table 4-2 summarizes the parameters tested by the Performance Tests. To be acceptable for use, the unit should meet or exceed all minimum performance standards listed.

Table 4-2. Minimum Performance Standards

Parameter to be Tested	Performance Standard
Power Supply Outputs	Voltages read at frame test points within ±10%.
Local frame command/control between a receiver controller and slave.	Controller initializes correctly, configures frame, and exercises control over slave.
IEEE-488/RS-232 command/control between external terminal and frame with IOM108.	External terminal communicates with IOM108 and exercises control over WJ-9040 modules in frame.
WJ-9040 System controller command/control of entire frame with IOM108.	System controller communicates with IOM108 and exercises control over WJ-9040 modules in frame.
Frequency Reference Outputs	Outputs are SRM105A J1-J4 are 0 dBm at 50.000000 MHz, ±5 Hz.

4.4.3 TEST EQUIPMENT REQUIRED

Table 4-3 lists the test equipment required for performance testing of the unit. Equivalent types may be used.

Table 4-3. Test Equipment Required

Instrument Type	Recommended Instrument
IOM108 Test Bed	EFR100 Equipment Frame with EPS100A Power Supply and one WJ-9040 receiving module
Computer Terminal equipped as a controller for IEEE-488 or RS-232 as required, with interface cable	Hewlett-Packard (HP) Model 85 (customer supplied equivalent is acceptable if properly configured)
System Controller	WJ-862X-4 Receiver/Controller with option MHO
Signal Generator	HP8640B
RF Voltmeter	Boonton 92B
Digital Voltmeter	Fluke 8800A
EFR100 frame extender cable (2)	W-J Part No. 271408
3' coaxial cable, BNC to BNC (2)	

4.4.4 PROCEDURE GUIDELINES

The WJ-9040 System Common Equipment performance test procedures are defined using the equipment listed in **Table 4-3** as a test bed. **Figure 4-1** is a block diagram showing the test bed configuration. The test bed in conjunction with the test procedures in **paragraph 4.4.5** and **paragraph 4.4.6** will permit the complete verification of all performance standards listed in **Table 4-2.** Customers whose systems are equipped for both IEEE-488/RS-232 and system control should perform both test procedures. Customers whose systems are equipped only for IEEE-488/RS-232 control should perform the procedure outlined in **paragraph 4.4.5.** Customers whose systems are equipped only for WJ-9040 system control should perform the procedure outlined in **paragraph 4.4.6.** When performing either of the tests, observe the following guidelines:

1. Ensure the test equipment is properly configured as shown in **Figure 4-1.** Test equipment not used in a particular test may be temporarily disconnected.

2. Read each test procedure thoroughly before attempting to perform the test.

3. The tests should be performed in the sequence given. If a malfunction is noted, refer to **paragraph 4.5** for troubleshooting.

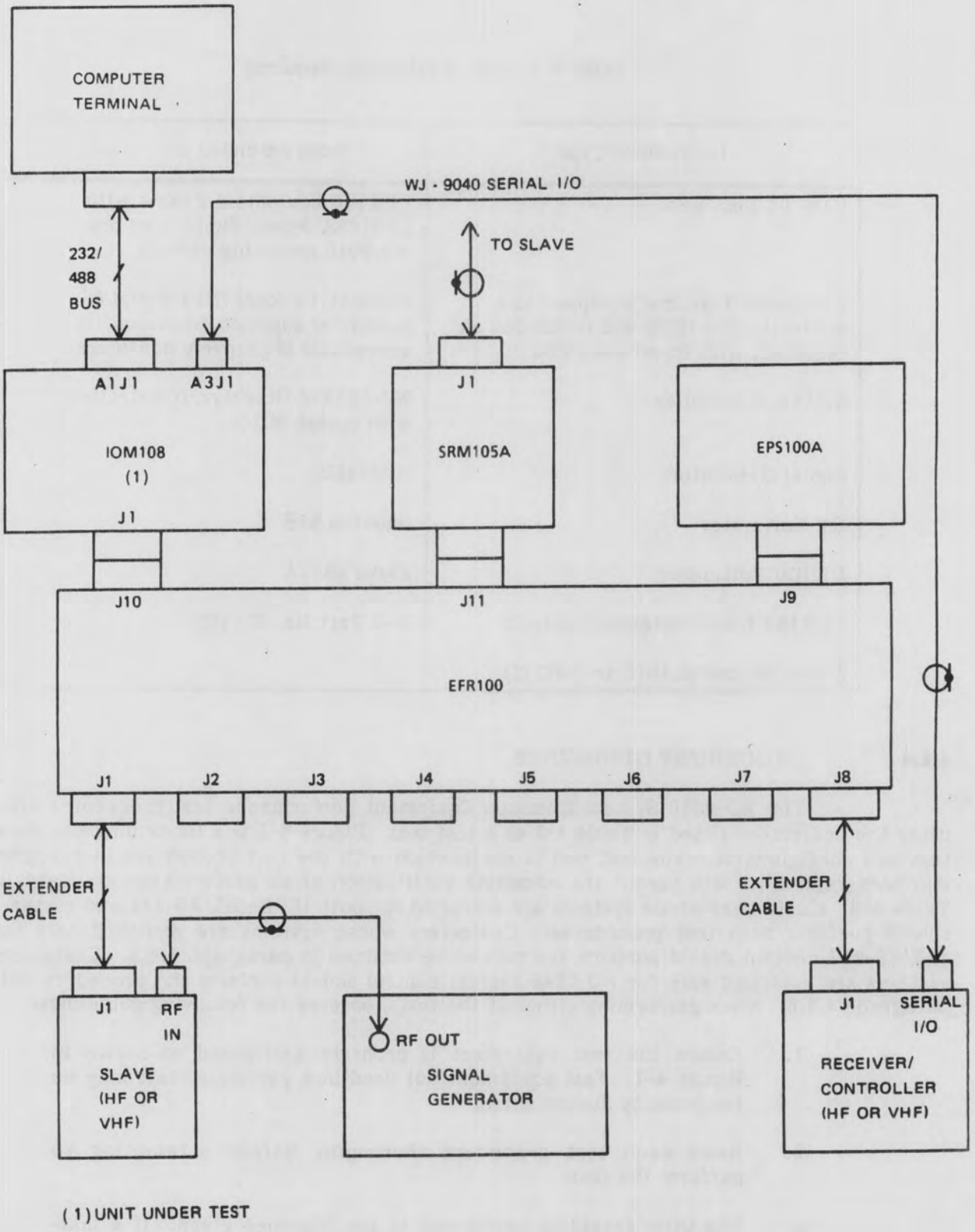


Figure 4-1. WJ-9040 System Common Equipment Test Bed Configuration

4.4.5 FUNCTIONAL TEST VIA IEEE-488/RS-232 PORT

This paragraph describes the procedure to test the operation of the WJ-9040 System Common Equipment by communicating through the IEEE-488/RS-232 port. An external computer configured to IEEE-488 or RS-232 operation, along with the EFR100 Equipment Frame and remotely controllable WJ-9040 receiving module (see **Table 4-3**) are required to perform this test. Since customer supplied computers vary widely in software structure, no attempt is made here to define all possible methods of transmitting commands to and receiving responses from the IOM108 port. The basic test structure and required ASCII commands are detailed. Each user is responsible for programming his computer to transmit the commands and display the responses from the IOM108. It should also be noted that the keyboard prompts and display responses may be slightly different between IEEE-488 and RS-232 operation. The main differences are noted as follows:

IEEE-488 Operation	RS-232 Operation
1. If an invalid query command (i.e., "FRS?") is entered, the IEEE-488 returns a response of "INVALID READ".	1. The command entered on the terminal is automatically echoed back by the IOM108.
2. If a question is sent to a slot where no unit is present, "INVALID READ" is returned as a response.	2. If an invalid query command (i.e., "FRS?") is entered, the question is ignored and no data is sent to the terminal.
	3. If a question is sent to a slot where no unit is present, a (CR) (LF) is returned as a response.

Perform the following procedure in the sequence given:

1. Configure the test equipment and the IOM108 as shown in **Figure 4-1**. The W-J receiver/controller may be omitted if not available.

2. Energize the EFR100 Equipment Frame.

3. Energize the computer terminal and implement any initializing routines required. Execute any terminal software required to place the terminal in an IEEE-488 or RS-232 communications mode. The terminal display should provide evidence that a valid "connect state" exists on the interface bus between the terminal and the IOM108.

4. Send the following ASCII characters from the terminal:

   "EXAM1" (CR) (LF)

The terminal should remain in a valid "connect state" after transmission (e.g., the terminal received the appropriate interface handshake with the IOM108 and is ready for the next command).

5. On the terminal, implement the appropriate "read routine" to read ASCII data from the IOM108 to the terminal. The terminal should display:

   "RCVR 5 kHz-30MHz" or
   "RCVR 20-512MHz"

   (Depending upon the type of receiving module installed.)

6. Execute the following series of keyboard commands. For each command, either a response will be noted on the receiver in the frame, or a display message will be seen at the terminal. For each terminal display message, it will be necessary to implement the appropriate "read routine" to read ASCII data from the IOM108 to the terminal.

Keyboard Entry:	"SLOT2" (CR) (LF)
Receiver Response:	Active light off
Keyboard Entry:	"SLOT1" (CR) (LF)
Receiver Response:	Active Light On
Keyboard Entry:	"COS63" (CR) (LF)
Receiver Response:	Squelch Light Off
Keyboard Entry:	"CST?" (CR) (LF)
Receiver Response:	"OFF" (CR) (LF)
Keyboard Entry:	"COSO" (CR) (LF)
Receiver Response:	Squelch Light On
Keyboard Entry:	"CST?" (CR) (LF)
Receiver Response:	"ON" (CR) (LF)

7. Connect the signal generator to the RF input terminal of the receiver in the equipment frame. Set the generator as follows:

   (Depending on type of receiving module installed.)

HF Receiver-Generator Frequency:	15.00000 MHz
Generator level:	-50 dBm
HF Receiver-Generator Frequency:	100.00000 MHz
Generator level:	-50 dBm

8. Send the following ASCII characters from the terminal:

   "FRQ 15.00000" or "FRQ 100.000" as appropriate.
   "AGC" (CR) (LF)
   "SS?" (CR) (LF)

9. On the terminal, implement the appropriate "read routine" to read ASCII data from the IOM108 to the terminal. The terminal should display a number between 20 and 80 as follows:

   "50" (CR) (LF)

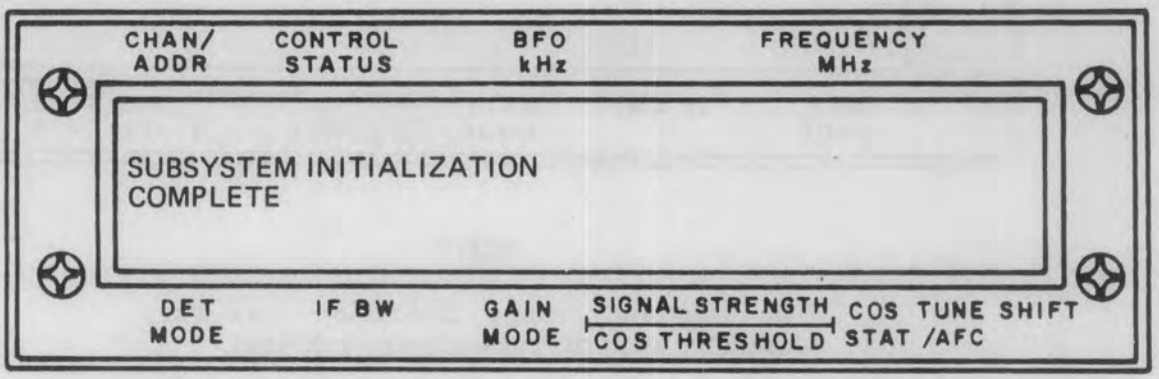
10. Each of the above steps should be repeated for slots 2 through 8. It will be necessary to deenergize the frame and move the receiver extension cable to the next frame connector before repeating the procedure. The EXAM and SLOT numbers used in the procedure will have to be changed to agree with the particular slot being tested.

4.4.6 FUNCTIONAL TEST VIA WJ-9040 SERIAL INTERFACE

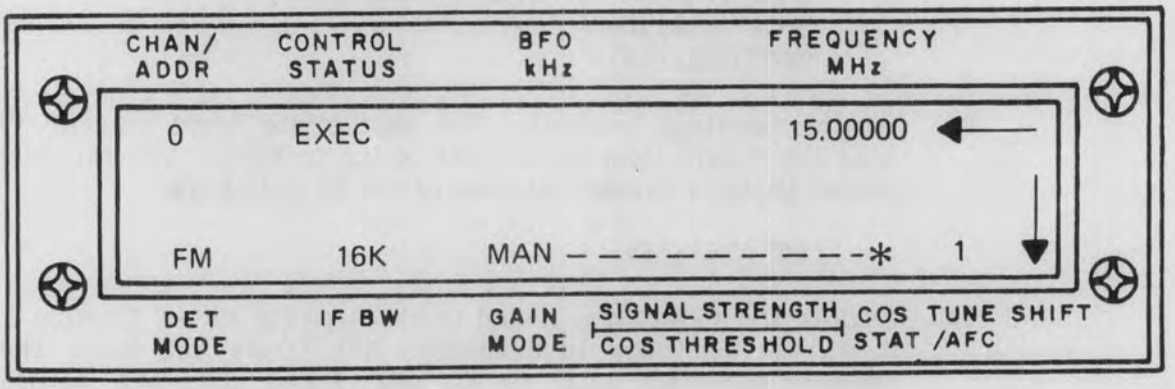
This paragraph describes the procedure for testing the operation of the WJ-9040 System Common Equipment by communicating through the WJ-9040 High Speed Serial Interface Port. A test bed consisting of an EFR100 Equipment Frame, one HF or VHF receiver/ controller (option MHO), and one remotely controllable WJ-9040 receiving module (see **Table 4-3**) are required to perform this test. This test is based on the front panel operator sequences defined for the W-J receiver/controllers. If it is desired to use a different controller for this test, the operation information in **paragraph 2.4.4** may be used to implement the data structure and commands used in this test. Perform the following procedures in the sequence given:

1. Configure the test equipment and the test bed as shown in **Figure 4-1.** The computer terminal may be omitted if not available.

2. Energize the EFR100 Equipment Frame. The receiver/ controller should display the following message briefly:



This will be replaced by a display of the receiver/controller status, shown typically as follows:



NOTE

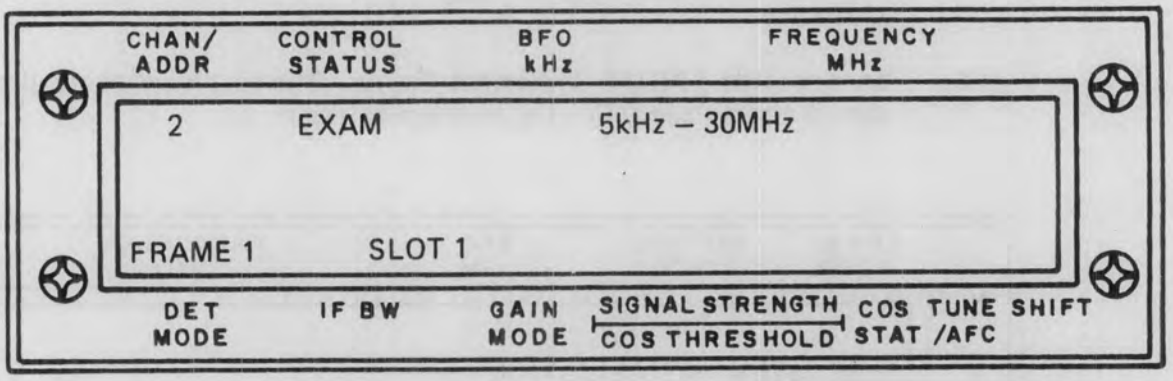
A failure of the serial I/O, polled or EFR100 backplane will result in the message:

"I/O ERROR ON POWERUP
ENTER (11) (OPR AID)"

3. Enter the following keystrokes on the receiver/controller keypad:

2 EXAM

The receiver/controller should display the following:



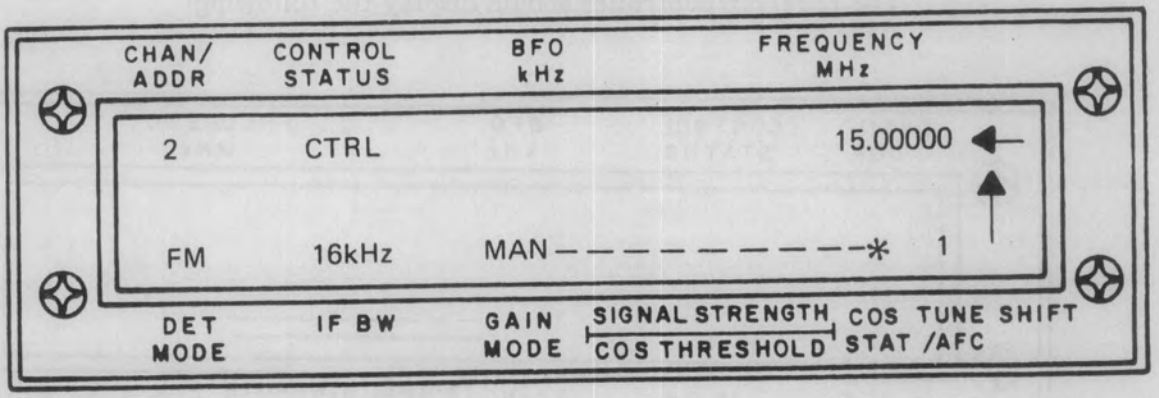
NOTE

The frequency range indication may vary depending upon the type of slave unit used.

4. Enter the following keystrokes on the receiver/controller keypad:

   2 CTRL

   The receiver/controller should display the following:



NOTE

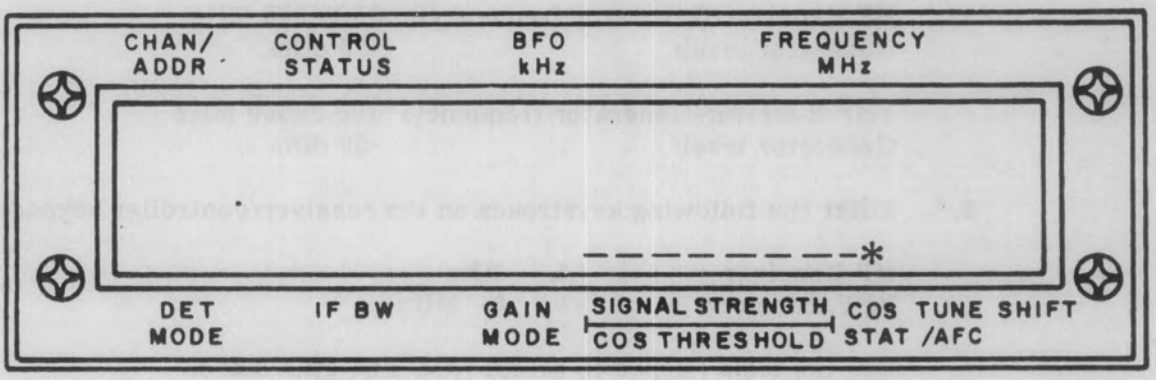
The status parameters (i.e., frequency, bandwidth) may be different.

5. Enter the following keystrokes on the receiver/controller keypad:

   0 COS

   The squelch light on the slave receiver should go on.

   The receiver/controller should display the following:



NOTE

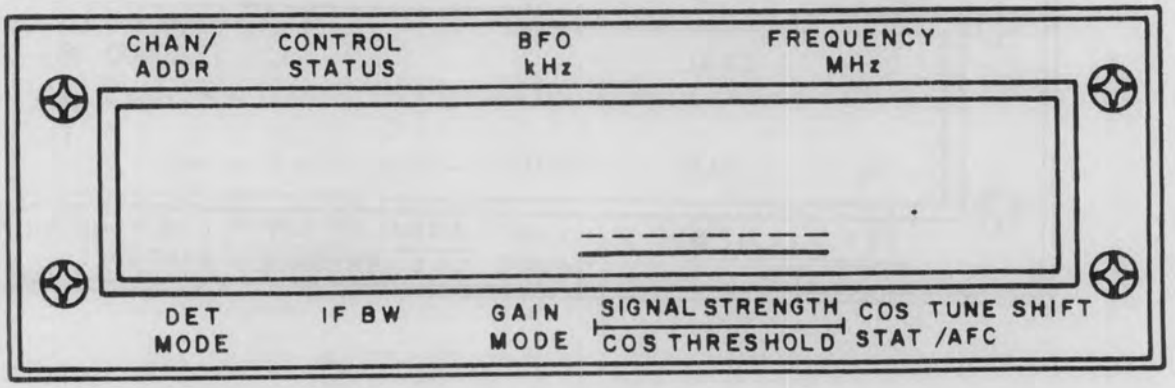
Verify that the asterisk above COS STAT is displayed.

6. Enter the following keystrokes on the receiver/controller keypad:

   63 COS

   The squelch light on the slave receiver should go off.

   The receiver/controller should display the following:



NOTE

Verify that the asterisk above COS STAT is erased.

7. Leave the receiver/controller in the 2 CTRL mode. Connect a signal generator to the RF input of the slave receiver in the EFR100 frame. Set the generator as follows:

   HF Receiver-Generator frequency: 15.00000 MHz
   Generator level: -50 dBm

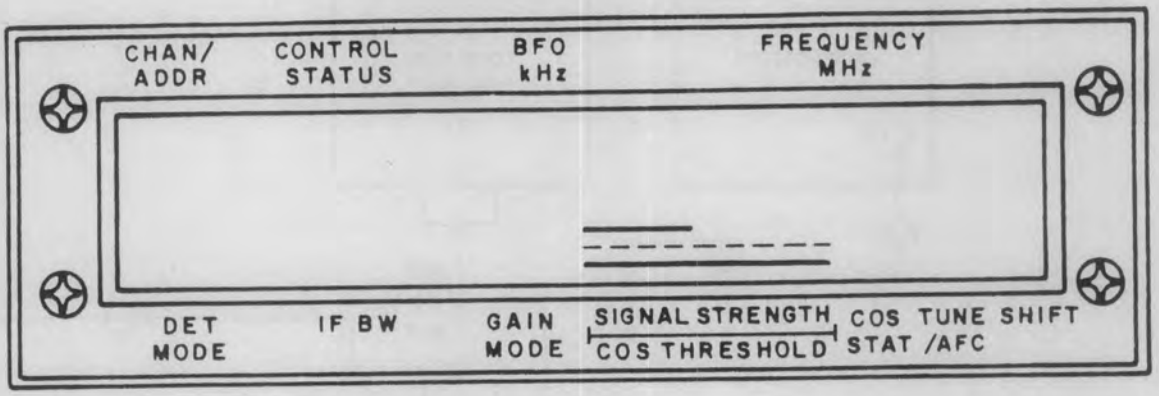
   VHF Receiver-Generator frequency: 100.00000 MHz
   Generator level: -50 dBm

8. Enter the following keystrokes on the receiver/controller keypad:

   HF Receiver - 1 5 MHz
   VHF Receiver - 1 0 0 MHz

   Use the main keypad to select AGC FST gain mode.

9. The signal strength bar on the receiver/controller display should deflect approximately half scale as shown below:



10. If AFC mode is enabled, indicated by the letter "A" above TUNE/AFC, disable AFC by pressing the AFC keypad.

11. Note the slave receiver IF bandwidth displayed on the receiver/ controller. Slowly change the signal generator frequency by an amount equal to one-half the displayed bandwidth. The tune indicator on the display should slowly move left and right as it tracks the signal generator frequency change.

12. Remove the 50 MHz reference input to the slave receiver. The receiver/controller should blink "UNLOCK" over the frequency display area.

13. Each of the above steps should be repeated for slots 2 through 8. Deenergize the frame and move the receiver extension cable to the next frame connector before repeating the procedure.

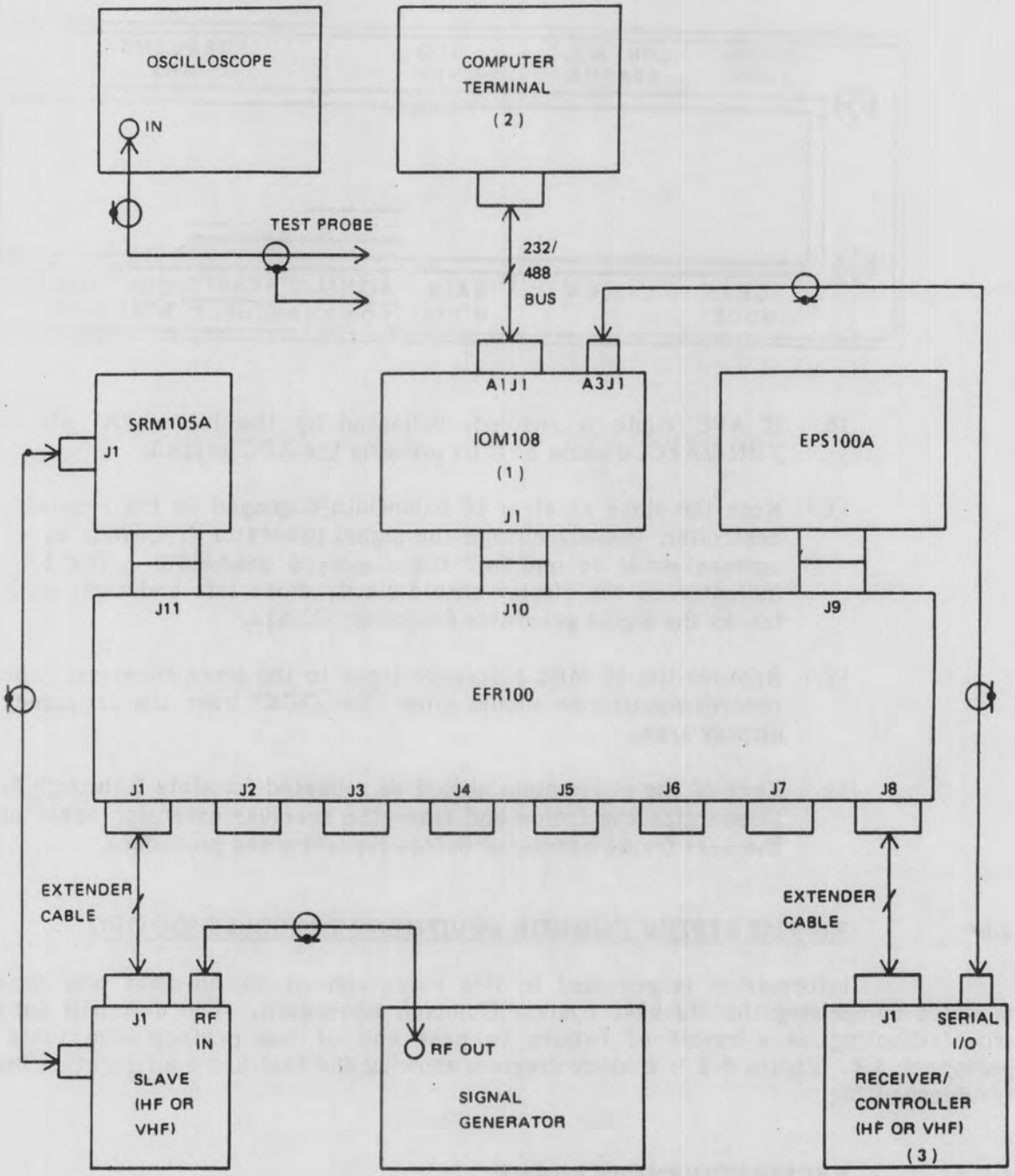
4.5 WJ-9040 SYSTEM COMMON EQUIPMENT TROUBLESHOOTING

Information is provided in this paragraph to troubleshoot and repair the four modules comprising the WJ-9040 System Common Equipment. The unit will normally require troubleshooting as a result of failure to pass any of the performance tests outlined in **paragraph 4.4. Figure 4-2** is a block diagram showing the test bed configuration used in module troubleshooting.

4.5.1 EFR100 EQUIPMENT FRAME

The equipment is a totally passive device and therefore no specific troubleshooting tests are prescribed. Equipment frame failures normally consist of erratic connector contacts or broken backplane flexwires. If the equipment frame is suspected of malfunctions the following general guidelines can be applied:

1. Equipment frame failures are classified as local (1 receiver slot affected) or general (all receiver slots affected).



(1) UNIT UNDER TEST

(2) REQUIRED FOR 232/488 INTERFACE MODULE TEST

(3) REQUIRED FOR SYSTEM I/O MODULE TEST

Figure 4-2. Module Test Bed Configuration

2. If only one slot is affected, check the affected connector for broken pins or for loose and broken flexwires attaching to the connector.

3. If all slots are affected, first verify correct power supply and IOM108 operation (substitute with new units). Then refer to the EFR100 schematic diagram and, using an ohmmeter, carefully check continuity of all backplane interconnections.

4. Visually inspect all connections to jacks, plugs and connectors. Visually inspect backplane wires for breaks.

4.5.2 EPS100A POWER SUPPLY

4.5.2.1 Preliminary Setup Procedure

The following steps should be performed prior to testing or troubleshooting the EPS100A:

1. Disconnect AC power from the EPS100A.

2. Refer to **paragraph 4.2.3** to remove the EPS100A from the equipment frame and gain access to the EPS100A circuits.

3. Ensure that the power switch on the EPS100A is in the OFF (out) position.

4. Connect an AC line cord to the AC input jack of the EPS100A.

5. Energize the EPS100A by depressing the power switch.

4.5.2.2 EPS100A Testing and Troubleshooting Procedure

The testing and troubleshooting information outlined in this paragraph is keyed to the EPS100A fault isolation table (**Table 4-4**) and the EPS100A component location diagram (**Figure 4-3**). The table is used to isolate the power supply fault to a major component or group of components. Perform the following procedure and replace any major components indicated in the table.

1. Perform the preliminary setup procedure in **paragraph 4.5.2.1.**

2. Use a digital voltmeter and check the DC voltages indicated in **Table 4-4.**

3. Replace the major components corresponding to a failure noted in the table. **Figure 4-3** is a guide to locating major components.

4. Replacement of the indicated major components will normally return the power supply to normal operation. If a failure is still noted, replace the power supply with a good unit. The defective power supply may be returned to the factory for repair.

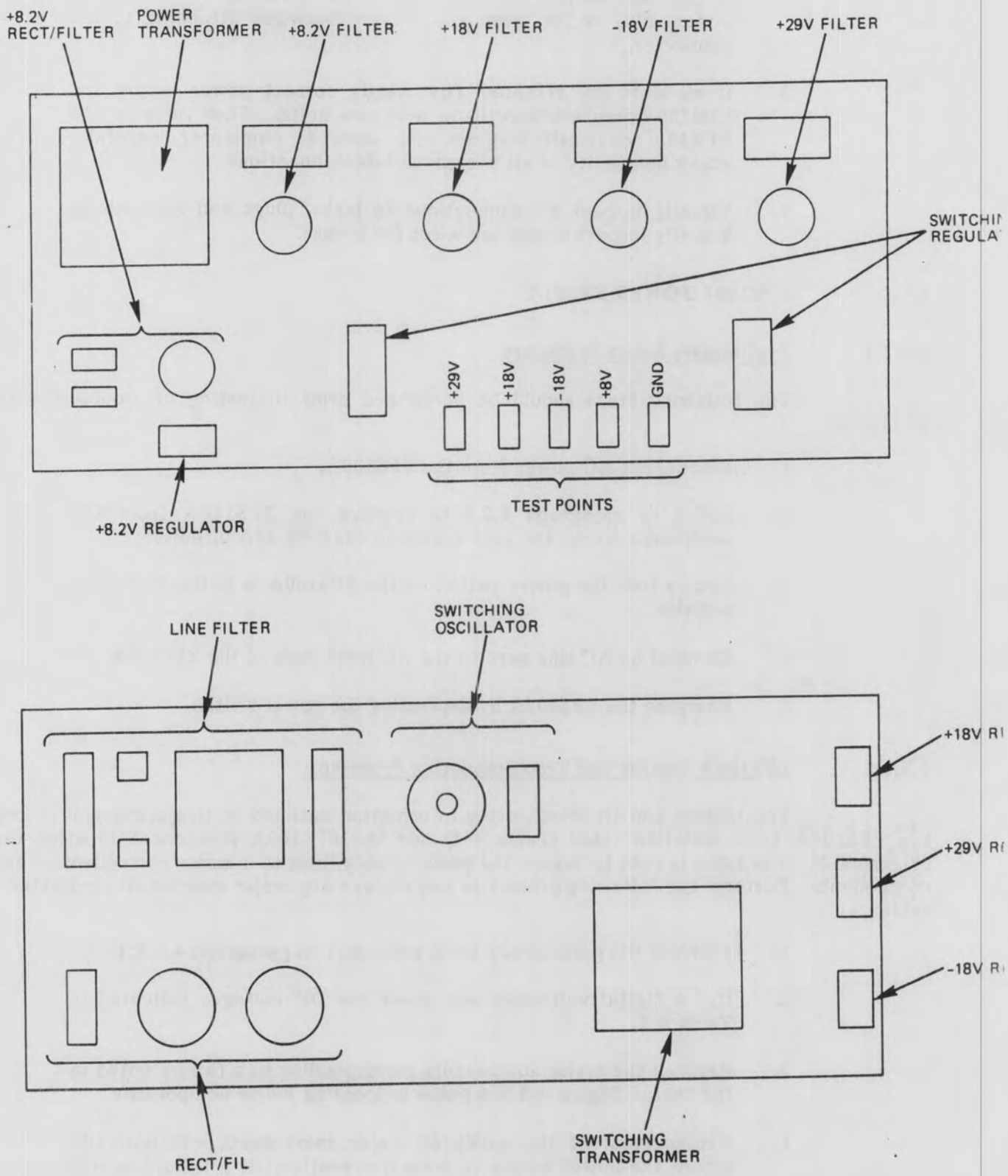


Figure 4-3. EPS100A Power Supply Component Location

Table 4-4. EPS100A Power Supply Fault Isolation Chart

Test Point	Normal Signal	Key Components	Comments
+8.2 V	+8.2 V ±10%	+8.2 V regulator +8.2 V rect/fil power transformer	Check this test point first
All	+29 V, +18.2 V, -18.2 V, +8.2 V ±10%	Sw. rect/fil, switch oscillator switch transformer	Assumes all test point outputs are dead.
+29 V	+29 V, ±10%	+29 V rect/fil	
+18.2 V	+18.2 V, ±10%	+18.2 rect/fil	
-18.2 V	-18.2 V, 10%	-18.2 rect/fil	
+8.2 V	+8.2 V, ±10%	+8.2 V rect/fil	

4.5.3 SRM105A SITE REFERENCE MODULE TESTING AND TROUBLESHOOTING

4.5.3.1 Preliminary Setup Procedure

The following steps should be performed prior to testing or troubleshooting the SRM105A:

1. Deenergize the EFR100 equipment frame.
2. Disconnect all cables from the SRM105A.
3. Refer to **paragraph 4.2.4** and use the procedure given to gain access to the SRM105A circuits.
4. Configure all test equipment per **Figure 4-2.**
5. Energize the EFR100 equipment frame.

4.5.3.2 SRM105A Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to a fault isolation table (**Table 4-5**). This table is used to isolate the module fault to a defective component or group of components. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Perform the preliminary setup procedure in **paragraph 4.5.3.1.**

2. Using an oscilloscope and high impedance probe, verify the SRM105A operation using **Table 4-5.** Signals should be checked with an external 1, 5, or 10 MHz reference connected.

3. Replacement of key components indicated in the table provided in this test procedure for the SRM105A will normally restore the faulty test point signal to normal. If a faulty signal is still observed after component replacement, additional troubleshooting is necessary. Refer to **Figure 6-10,** SRM105A Site Reference Module Main Chassis Schematic Diagram, as an aid in additional troubleshooting.

Table 4-5. SRM105A Site Reference Module Signal Check

Test Point	Normal Signal	Key Components	Comments
U9-3	+15 Vdc	U9	DC supply
U10-9	Square wave pulses at 1, 5, or 10 MHz	U10	External reference connected
U11-5	Square wave pulses at 0.5, 2.5, or 5.0 MHz	U11	External reference connected
U10-4	Square wave pulses at 0.5, 2.5, or 10 MHz	U10	U11 in the circuit
U3-5	50 MHz sine wave at 0.5 Vpp	U3	
U6-2	50 MHz sine wave at 2 Vpp	U4,U6	
U7-1,2,7,8	50 MHz sine wave at 0.5 Vpp	U7	
U5-20	2.5 MHz square wave, TTL level	U5	
U2-6	+2 to +5 Vdc	U1,U2	With S1 in the LOCKED position

4.5.4 IOM108 TROUBLESHOOTING PROCEDURES

Information is provided in this paragraph to troubleshoot the IOM108 first to a defective replaceable module and then to a defective replaceable component. The IOM108 will normally require troubleshooting as a result of failure to pass any of the performance tests listed in **paragraph 4.4,** or as a result of operator-observed malfunctions during normal operation.

4.5.4.1 **Module Level Troubleshooting Guidelines**

Figure 4-4, IOM108 Troubleshooting Flowchart, is provided as an aid in locating defective modules within the IOM108. Properly used, it is an effective guide to locating and correcting major IOM108 failures. It is not intended as a substitute for standard digital troubleshooting techniques performed by skilled technicians familiar with the IOM108 circuitry.

NOTE

Early IOM108 Module configurations have the Extended Memory (A1A4) and the CPU (A1A5) as separate boards. Current IOM108 Modules have these two boards combined as the Extended CPU (A1A5).

1. Refer to **Figure 4-4.** Locate the block labeled BEGIN. Proceed vertically through the flowchart. The flowchart is keyed to the performance tests and responses in **paragraph 4.4.**

2. Perform the tests in **paragraph 4.4** as instructed by the flowchart. When a test response failure is encountered, follow the fault isolation path for the failure as provided by the flow chart.

3. Perform any additional tests and corrective actions indicated by the flowchart. Replace any modules determined to be faulty.

4. Repeat the performance test that resulted in the failure to confirm the corrective action. Additional fault isolation will be required if the failure is still present.

5. The IOM108 may be returned to service if it passes all the performance tests as indicated by the flowchart.

6. Refer to **paragraph 4.5.4.2** to repair any modules found defective as a result of troubleshooting the IOM108.

4.5.4.2 **Component Level Troubleshooting Guidelines**

This paragraph provides the testing, troubleshooting and repair information necessary to restore a malfunctioning IOM108 module, A1A1-A1A5, to normal operation. The information provided consists of the following:

- Module test and troubleshooting procedures to assist signal tracing and localize faulty circuit areas.
- Fault isolation tables to assist in isolating defective semiconductor components in faulty circuit areas.
- A parts replacement guide, **paragraph 4.5.4.8,** to assist in repairing a defective module.

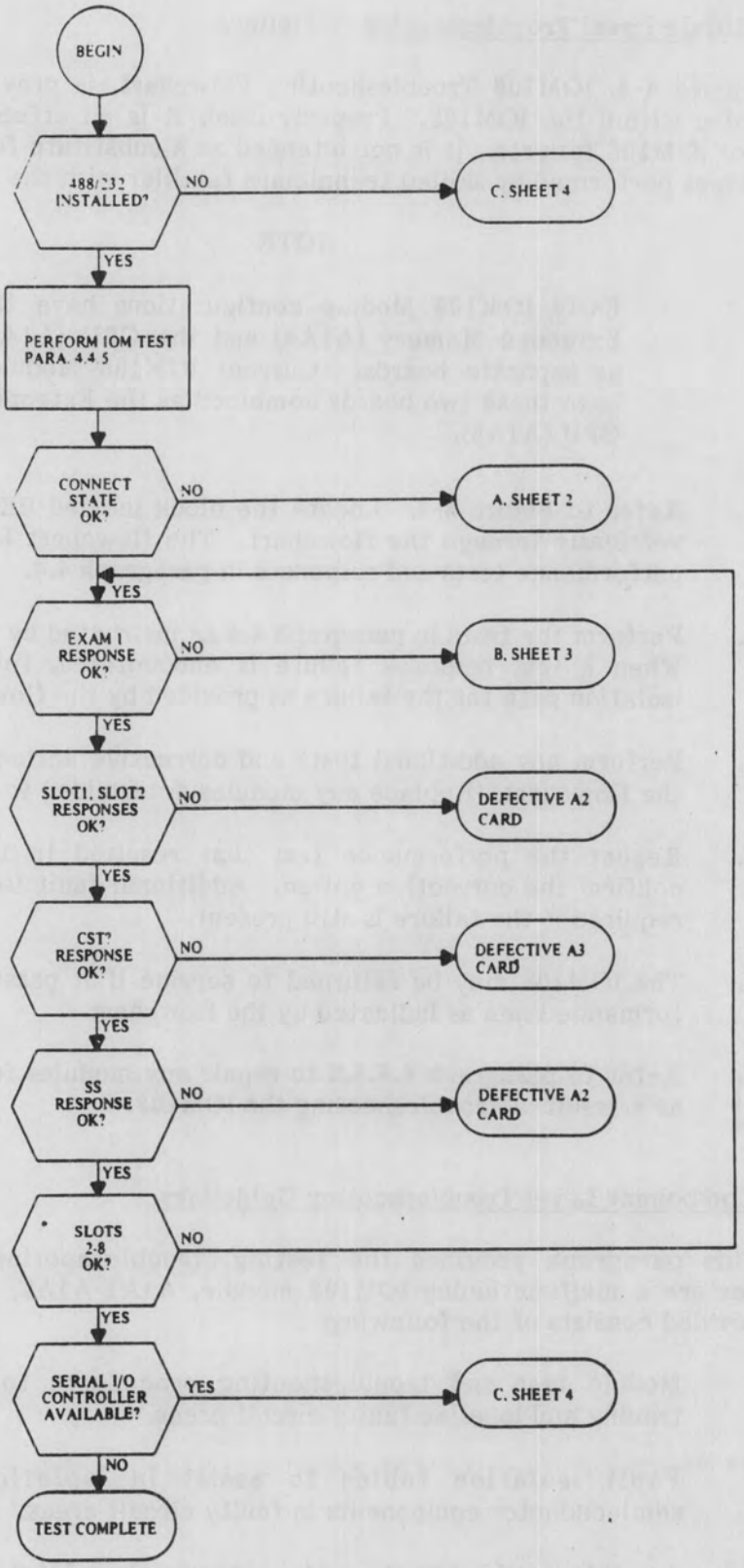


Figure 4-4. IOM108 Troubleshooting Flowchart (Sheet 1 of 5)

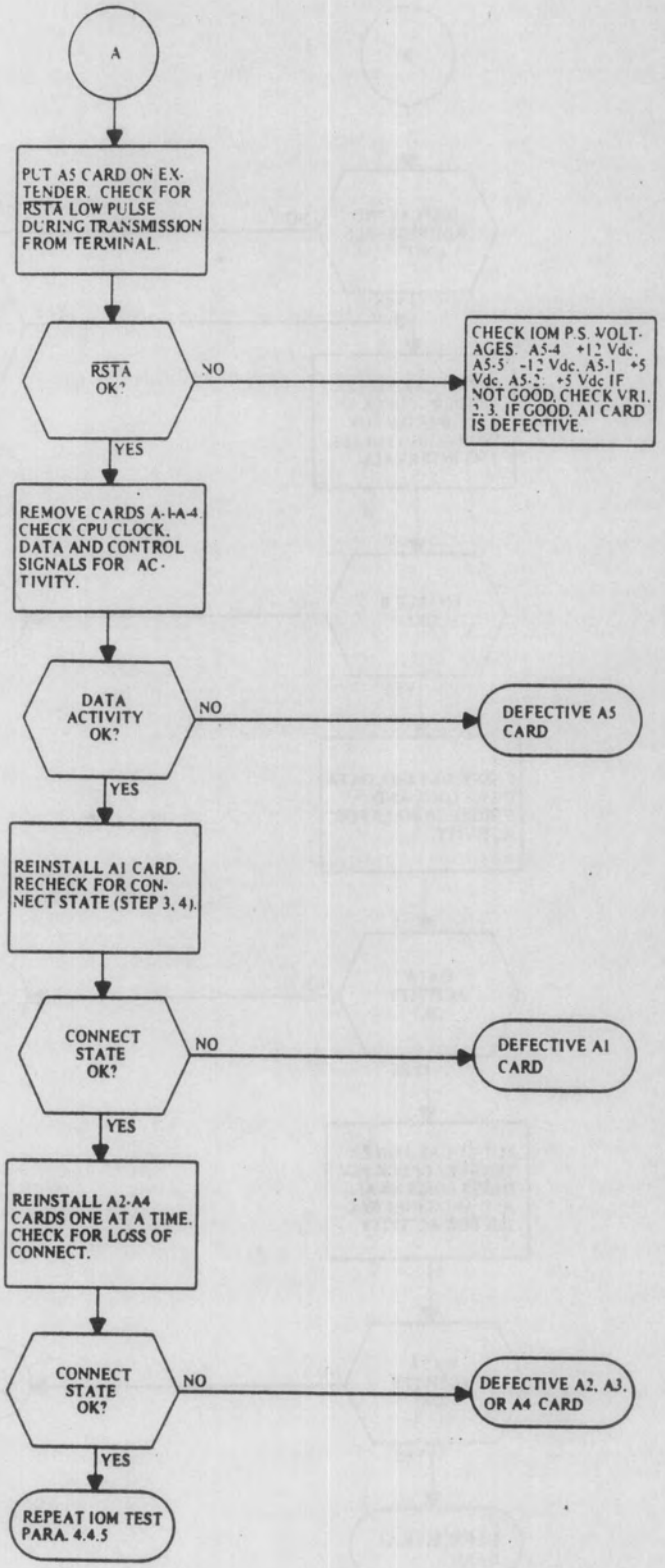


Figure 4-4. IOM108 Troubleshooting Flowchart (Sheet 2 of 5)

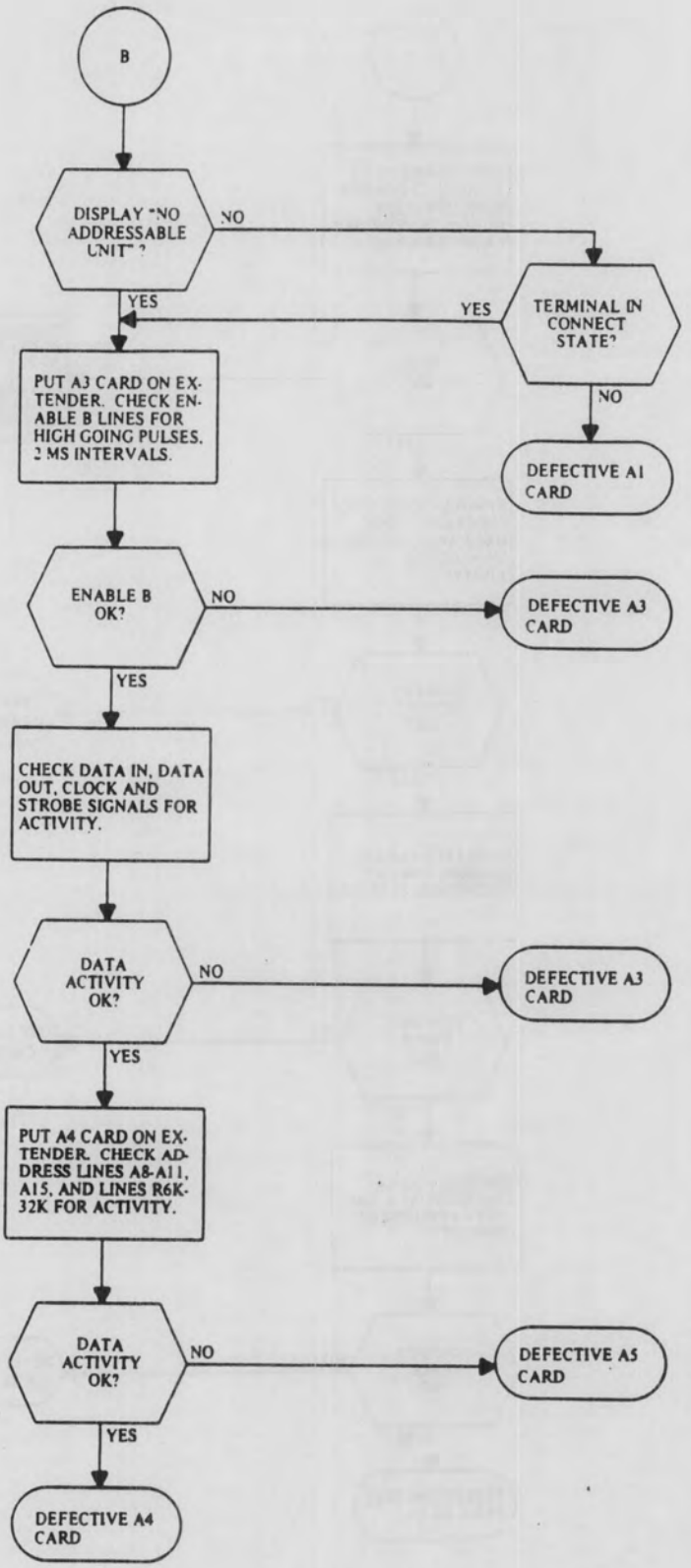


Figure 4-4. IOM108 Troubleshooting Flowchart (Sheet 3 of 5)

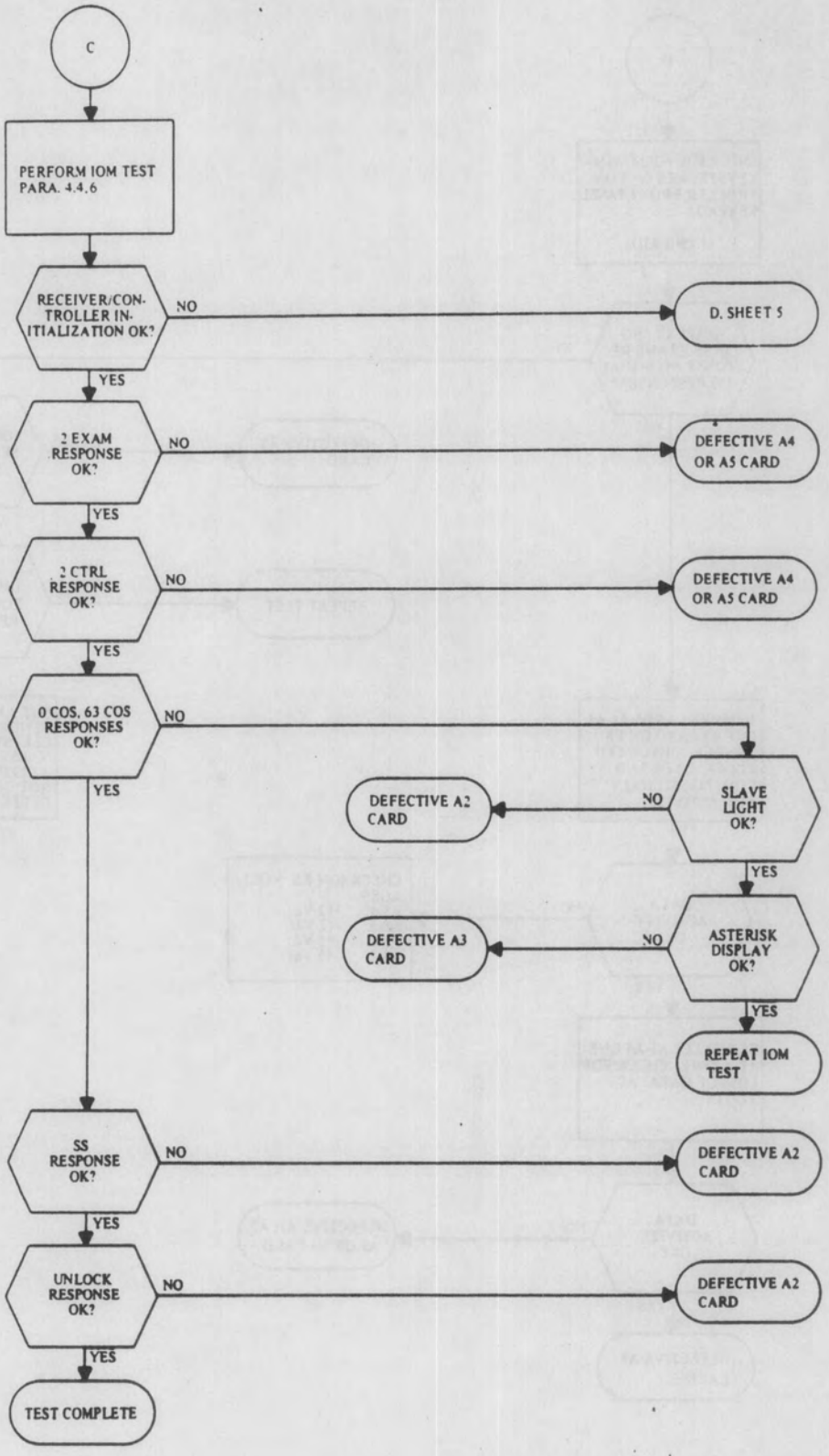


Figure 4-4. IOM108 Troubleshooting Flowchart (Sheet 4 of 5)

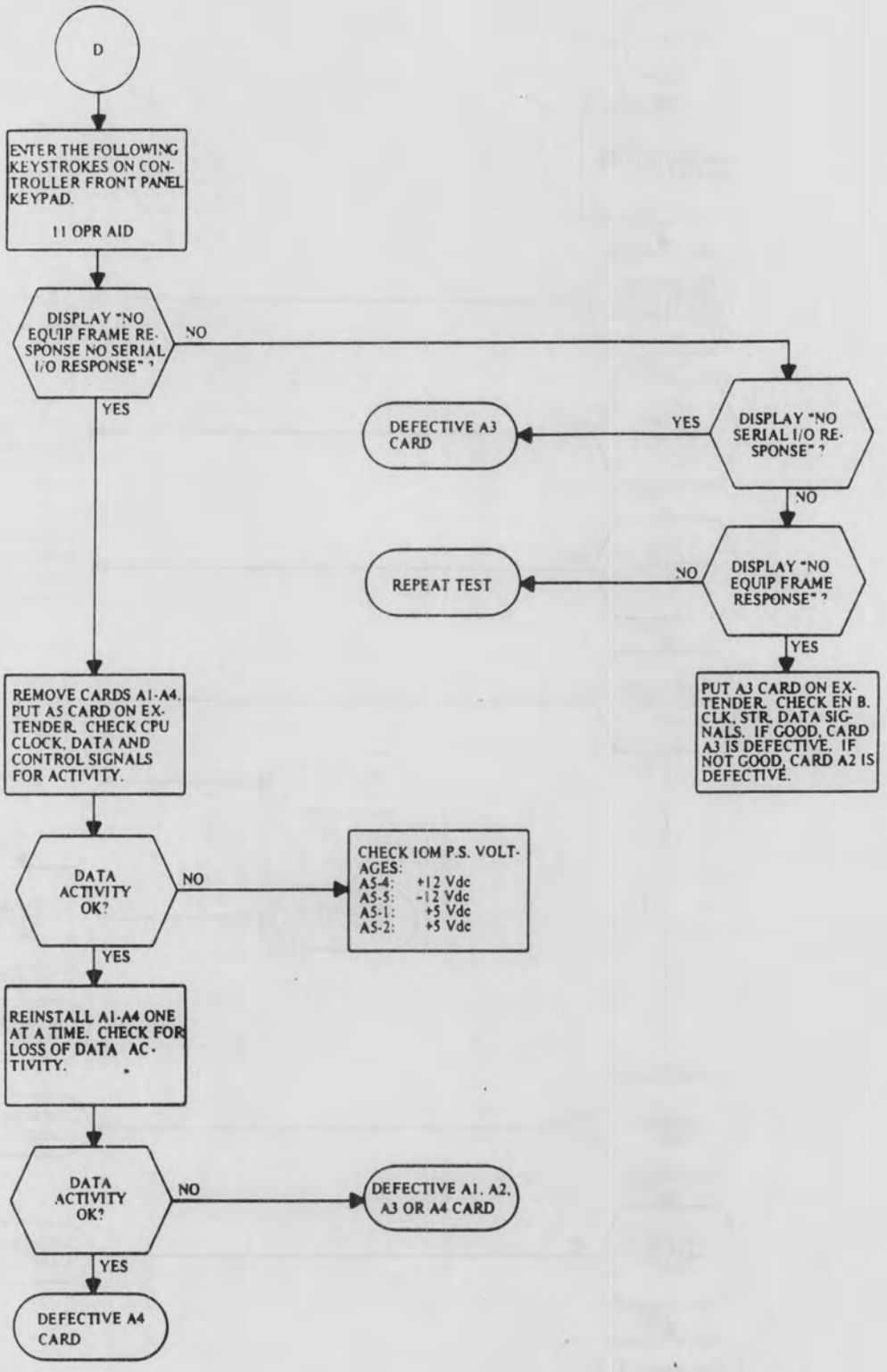


Figure 4-4. IOM108 Troubleshooting Flowchart (Sheet 5 of 5)

The module testing and troubleshooting procedures are defined using an EFR100 Equipment Frame, EPS100A Power Supply, WJ-9040 type receiver/controller, WJ-9040 type slave receiver, and a computer terminal as a test bed as shown in **Figure 4-2.** Each of the module test procedures is based on the presumption that the test bed is fully functional. If the integrity of the EFR100 backplane is in doubt, thoroughly check the backplane with an ohmmeter before proceeding with any of the tests. When testing and troubleshooting a defective module, observe the following guidelines:

1. Refer to the testing and troubleshooting paragraph for the desired module. Configure the test equipment as indicated in the module test procedure.

2. Perform the testing and troubleshooting procedure in the sequence given. If any failure is encountered or any desired results are not obtained, refer to the Fault Isolation Table for key components which would most likely cause the failure.

3. Replace the key components indicated as a result of performing step 2 above. Repeat the testing and troubleshooting procedure to confirm the corrective action.

4. If the module still fails, additional troubleshooting and fault isolation is required. Refer to the circuit descriptions in **Section III** and schematic diagrams in **Section VI** as aids in performing additional troubleshooting.

4.5.4.3 Digital I/O, RS-232 (A1A1) Testing and Troubleshooting

4.5.4.3.1 Preliminary Setup Procedure

The following steps should be performed prior to testing or troubleshooting the Digital I/O, RS-232.

1. Deenergize the EFR100 Equipment Frame.

2. Disconnect all I/O cables from the IOM108.

3. Refer to **paragraph 4.2.2** and use the procedure given to gain access to module A1A1. Remove modules A1A2 and A1A3.

4. Place module A1A1 on an extender card.

5. Configure all required test equipment per **Figure 4-2.**

6. Energize the EFR100 Equipment Frame.

4.5.4.3.2 Testing and Troubleshooting Procedure for DIO, RS-232 (A1A1)

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the tables.

1. Perform the preliminary setup procedure in **paragraph 4.5.4.3.1.**
2. Using the oscilloscope, verify the UART and I/O signal activity using **Tables 4-6** and **4-7.** Activity should be checked in conjunction with sending commands from the terminal to the IOM108.

Table 4-6. UART Signal Activity Check for DIO, RS-232

Test Point	Normal Signal	Key Components	Comments
U1-3	Square wave pulse train	U8	Send command from terminal to IOM108 while checking pin
U1-17,22	Low pulse when data is sent	U8	Send command from terminal to IOM108 while checking pin
U6-4	Negative going	U1, U6	Send command from terminal to IOM108 while checking pin
U1-9,20,25	Clean, square wave	U5,Y1	Send command from terminal to IOM108 while checking pin

4.5.4.4 Digital I/O, IEEE-488 (A1A1) Testing and Troubleshooting

4.5.4.4.1 Preliminary Setup Procedure

The following steps should be performed prior to testing or troubleshooting the Digital I/O, IEEE-488:

1. Deenergize the EFR100 Equipment Frame.
2. Disconnect all I/O cables from the IOM108.
3. Refer to **paragraph 4.2.2** and use the procedure given to gain access to module A1A1. Remove modules A1A2 and A1A3.

4. Place module A1 on the extender card.

5. Configure all required test equipment per **Figure 4-3.**

6. Energize the EFR100 Equipment Frame.

Table 4-7. I/O Signal Activity Check for DIO, RS-232

Test Point	Normal Signal	Key Components	Comments
U2-Q0 to Q7 outputs	Pulse train, less than 1 µs PW	U2	
U4-7	Sharp, negative going pulse, 10 µs prr	U4	
U4-9	Square wave, 2ms prr	U4	
U1-19	Square wave pulse train	U1	Present only when IOM108 transmits to terminal.
U1-23,24	Low pulse	U1	Present only when IOM108 transmits to terminal.

4.5.4.4.2 Testing and Troubleshooting Procedure for DIO, IEEE-488 (A1A1)

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Perform the preliminary setup procedure in paragraph **4.5.4.4.1.**

2. Using the oscilloscope, verify the GPIB Talker/Listener Device using **Table 4-8.** Activity should be checked in conjunction with sending commands from the terminal to the IOM108.

3. Using the oscilloscope, verify I/O signal activity using **Table 4-9.**

4. Replacement of key components indicated in the tables provided in this test procedure for the Digital I/O, IEEE-488 Module will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **Figure 6-4**, Digital I/O, IEEE-488 Schematic Diagram, as an aid in additional troubleshooting.

Table 4-8. GPIB Talker/Listener Device

Test Point	Normal Signal	Key Components	Comments
U1 pins 28-35 (DI01-DI08)	Rapidly changing logic levels	U1, U2	Send command from terminal to IOM108 while checking pins
U1-11	Sharp, negative going pulse, 2 µs PW	U1	Pulse should be seen for each command from terminal.
U1 pins 24-27	Rapidly changing logic levels	U1, U3	Send command from terminal to IOM108 while checking pins.

Table 4-9. I/O Signal Activity Check for DIO, IEEE-488

Test Point	Normal Signal	Key Components	Comments
U6 Q0-Q7 outputs	Pulse train, less than 1 µs PW on each pin	U6	
U7-7	Sharp, negative going pulse, 10 µs PW	U1	Chip select
U7-9	Square wave, 2 µs prr	U7	

4.5.4.5 Bidirectional Polled I/O (A1A2) Testing and Troubleshooting

4.5.4.5.1 Preliminary Setup Procedure

The following steps should be performed prior to testing or troubleshooting the Bidirectional Polled I/O Assembly, A1A2.

1. Deenergize the EFR100 Equipment Frame.
2. Disconnect all I/O cables from the IOM108.
3. Refer to **paragraph 4.2.2** and use the procedure given to gain access to module A1A2.
4. Place module A1A2 on an extender card.
5. Configure all required test equipment per **Figure 4-2.**
6. Energize the EFR100 Equipment Frame.
7. Using either the receiver/controller or the computer terminal, set the slave receiver to AGC FAST mode. Set the slave receiver frequency to 15.00000 MHz if HF or to 100.00000 MHz if VHF.
8. Set the signal generator output frequency to 15.00000 MHz for a HF receiver or to 100.00000 MHz for a VHF receiver. Set the output level to - 50 dBm.
9. Set all switch positions on A1A2S4 to the closed position.

4.5.4.5.2 Testing and Troubleshooting Procedure for Bidirectional Polled I/O (A1A2)

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Perform the preliminary setup procedure in **paragraph 4.5.4.5.1.**
2. Using the oscilloscope, verify data bus and I/O signal activity using **Table 4-10.**
3. Using the oscilloscope, verify signal strength, AFC, COS and Read Request signals using **Table 4-11.**
4. Replacement of key components indicated in the tables provided in this test procedure for the bidirectional polled I/O module will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **Figure 6-5,** Bidirectional Polled I/O Schematic Diagram, as an aid in additional troubleshooting.

Table 4-10. Data Bus and I/O Signal Check for A1A2, Bidirectional Polled I/O

Test Point	Normal Signal	Key Components	Comments
U12 pins 12-19	Rapidly changing logic levels on each pin	U12	Irregular pulse trains, trains should be observed.
U11-9,12,15 16,19	Rapidly changing logic levels on each pin	U11	Irregular pulse trains, trains should be observed.
U7-10	Sharp, negative going pulse, 20 µs prr	U7	Irregular pulse trains, trains should be observed.
U7-9	Sharp, negative going pulse	U7	Irregular pulse trains, trains should be observed.

Table 4-11. Polled I/O Signal Check for A1A2, Bidirectional Polled I/O

Test Point	Normal Signal	Key Components	Comments
U3-7	Square wave, 2 µs prr changing from 0 Vdc to +Vdc	U3	Increase signal generator frequency by 1/2 IF bandwidth.
U3-8	Square wave, 2 µs prr changing from 0 Vdc to +Vdc	U3	
U2-14	Pulse train, less than 1 µs prr	U2, U3A	
U1-1	0 Vdc +5 Vdc	U1	CST = OFF CST = ON
U1-8	Square wave pulse train, 2 µs prr	U1	
U10-17	Square wave clock	U10	
U10-14	Pulse train, less than 1 µs prr		

4.5.4.6 System I/O (A1A3) Testing and Troubleshooting

4.5.4.6.1 Preliminary Setup Procedure

The following steps should be performed prior to testing or troubleshooting the System I/O Assembly, A1A3.

1. Deenergize the EFR100 Equipment Frame.
2. Disconnect all I/O cables from the IOM108.
3. Refer to **paragraph 4.2.2** and use the procedure given to gain access to module A1A3.
4. Place module A1A3 on an extender card.
5. Configure all required test equipment per **Figure 4-2.**
6. Energize the EFR100 Equipment Frame.

4.5.4.6.2 Testing and Troubleshooting Procedure for System I/O (A1A3)

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Perform the preliminary setup procedure in **paragraph 4.5.4.6.1.**
2. If a receiver/controller is available, use the oscilloscope to verify UART activity using **Table 4-12.** If no receiver/controller is available, this step may be ignored.
3. Using the oscilloscope, verify I/O signal activity using **Table 4-13.**
4. Replacement of key components indicated in the tables provided in this test procedure for the system I/O module will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **Figure 6-6,** System I/O Schematic Diagram as an aid in additional troubleshooting.

Table 4-12. UART Activity Signal Check

Test Point	Normal Signal	Key Components	Comments
U4-20	Short bursts of 25 µs prr pulses; each burst 100 µs apart	U2, U5	Present when receiver/ controller transmits to IOM108.
U4-25	Short Bursts of 25 µs prr pulses; each burst 100 µs apart	U4	Present when IOM108 transmits to receiver/ controller.
U4-13,14,15	Sharp, negative going pulse, 200 µs prr	U4	
U1-6	Short bursts of 25 µs prr pulses; each burst 100 µs apart	U1, U3, U9	Present when IOM108 transmits to receiver/ controller.

Table 4-13. System I/O Signal Check

Test Point	Normal Signal	Key Components	Comments
U6-Q1 to Q8 outputs	Pulse train, less than 1 µs prr	U6	
U8-Q1 to Q8 outputs	Pulse train, less than 1 µs prr	U8	
U7-YO,Y1,Y2	Pulse train, less than 1 µs prr	U7	Present when WJ-9040 serial I/O occurs.
U7-Y3,Y4	Pulse train, less than 1 µs prr	U7	Present when back-plan I/O occurs
U7-Y6	Pulse train, less than 1 µs prr	U7	
U7-Y7	Pulse train, less than 1 µs prr	U7	
U10-Q1 to Q8 outputs	Square wave, 2 ms prr	U10	ENABLE B signals

4.5.4.7 Extended CPU (A1A5) Testing and Troubleshooting

4.5.4.7.1 Preliminary Setup Procedure

The following steps should be performed prior to testing or troubleshooting the Extended CPU, A1A5:

NOTE

Early IOM108 Module configurations have the Extended Memory (A1A4) and the CPU (A1A5) as separate boards. Current IOM108 Modules have these two boards combined as the Extended CPU (A1A5).

1. Deenergize the EFR100 Equipment Frame.
2. Disconnect all I/O cables from IOM108.
3. Refer to **paragraph 4.2.2** and use the procedure given to gain access to the IOM modules. Remove all modules.
4. Place module A1A5 on an extender card.
5. Configure all required test equipment per **Figure 4-2.**
6. Energize the EFR100 Equipment Frame.

4.5.4.7.2 Testing and Troubleshooting Procedure for Extended CPU (A1A5)

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Perform the preliminary setup procedure in **paragraph 4.5.4.7.1.**
2. Using the oscilloscope, verify the external input signals to the microcontroller U1 using **Table 4-14.**
3. Using the oscilloscope, verify microcontroller U1 data bus and control signal activity using **Table 4-15.**
4. Using the oscilloscope, verify I/O signal activity using **Table 4-16.**

Table 4-14. Microcontroller Input Signals

Test Point	Normal Signal	Key Components	Comments
U3-U11	Clock signal	U1, Y1	System clock
U3-33	+5 Vdc	R6, C4	
U3-36	+5 Vdc	U1, R3, C3	
U3-21	+5 Vdc	R7, U3	
U3-22	+5 Vdc	R8, U3	
U3-23	+5 Vdc	R9, U3	
U3-24	+5 Vdc	R10, U3	

Table 4-15. Microcontroller Bus Activity Check

Test Point	Normal Signal	Key Components	Comments
U3 pins 12-19	Pulse train, less than 1 µs prr	U1, U4, U5, U8, U9	Slowly cycle EFR100 power on/off while checking to eliminate software hangup.
U3 pins 1-8	Pulse train, less than 1 µs prr	U1, U4, U5, U8, U9	Slowly cycle EFR100 power on/off while checking to eliminate software hangup.
U3-31, 32	Pulse train, less than 1 µs prr	U1, U4, U5, U8, U9	Slowly cycle EFR100 power on/off while checking to eliminate software hangup.
U3-30, 34	Pulse train, 4 µs prr	U1, U4, U5, U8, U9	Slowly cycle EFR100 power on/off while checking to eliminate software hangup.
U3-9	Clock pulse	U1	

Table 4-16. CPU I/O Signal Check

Test Point	Normal Signal	Key Components	Comments
U5-11 to 18	Pulse train, less than 1 µs prr	U5	
U4-2,5,6,9 12,15,16,19	Pulse train, less than 1 µs prr	U4	
U6-12,13,14,15	Square wave, 1 ms prr	U6, U7	

5. If no failures have been encountered, deenergize the EFR100 Equipment Frame. Install a good system I/O card or a good digital I/O card.

6. Energize the EFR100 Equipment Frame. If communication cannot be established between the controller and the CPU or between the computer terminal and the CPU, the fault is ROM U8, U9 or RAM U10. These chips should be selectively replaced to locate the defect.

7. Replacement of key components indicated in the tables provided in this test procedure for the CPU module will normally restore the faulty test point signal to normal. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **Figure 6-7**, Extended Memory Schematic Diagram and **Figure 6-8**, CPU Schematic Diagram, as an aid in additional troubleshooting.

4.5.4.8 **Parts Replacement Guidelines**

This paragraph provides techniques to assist the technician in replacing components on PC boards.

WARNING

To prevent electrical shock or damage to the unit, always disconnect the receiver from the AC power source before soldering or replacing components.

4.5.4.8.1 Soldering Techniques

When removing components from a printed circuit board for inspection or replacement, be especially careful not to damage the track. The soldering iron power should be no higher than 40 W, and a solder sipper or wicking procedure should be employed when removing solder. Noncorrosive soldering flux should be used when removing solder by wicking. In returning components to the board, make sure that holes are clear and that leads do not catch the edge of the track and lift it from the board. A good grade of rosin core 60/40 solder should be used. Do not heat longer than is necessary to achieve a good joint. A heat sink should be used where possible.

4.5.4.8.2 Component Replacement

The following are specific guidelines for replacing the various kinds of components:

1. When soldering or unsoldering diodes or resistors, solder quickly to allow as little heat conduction as possible. When wiring permits, use a heat sink between the soldering iron and the part.

2. When soldering or unsoldering transistors, use a low wattage iron and a heat sink. Solder as quickly as possible. The use of a circular solder tip to heat all three to four joints simultaneously is recommended.

3. When soldering or unsoldering glass or ceramic capacitors, use a heat sink between the capacitor and the iron. Excessive heat will crack the capacitor body.

4. When any electronic part is removed, note the position of the part and its leads, and replace it the same way.

4.6 ALIGNMENT PROCEDURES

No alignment procedures are specified for the WJ-9040 System Common Equipment.

SECTION V

REPLACEMENT PARTS LIST

SECTION V

REPLACEMENT PARTS LIST

5.1 UNIT NUMBERING METHOD

The method of numbering used throughout the unit is assigning reference designations (electrical symbol numbers) to identify: assemblies, subassemblies, modules within a subassembly, and discrete components. An example of the unit numbering method used is as follows:

Subassembly Designation A1	R1 Class and No. of Item
Identify from right to left as:	First (1) resistor (R) of first (1) subassembly (A)

On the main chassis schematic, components which are an integral part of the main chassis have no subassembly designations.

5.2 REFERENCE DESIGNATION PREFIX

The use of partial reference designations are used on the equipment and on the manual illustrations. This partial reference designation consists of the component type letter(s) and the identifying component number. The complete reference designation may be obtained by placing the proper prefix before the partial reference designation. Reference designation prefixes are included on the drawings and illustrations in the figure titles (in parenthesis).

5.3 LIST OF MANUFACTURERS

Mfr. Code	Name and Address	Mfr. Code	Name and Address
00681	Catalyst Research Corporation 1421 Clarkview Road Baltimore, MD 21209	02735	RCA Corporation Solid State Division Route 202 Somerville, NJ 08876
00779	AMP, Incorporated P.O Box 3608 Harrisburg, PA 17105	04713	Motorola Incorporated Semiconductor Products Div. 5005 East McDowell Road Phoenix, AZ 85880
01295	Texas Instruments, Inc. Semiconductor-Components Div. 15300 North Central Expressway Dallas, TX 75231	06776	Robinson Nugent, Inc. 800 E. 8th Street P.O. Box 1208 New Albany, IN 47150

Mfr. Code	Name and Address
09021	Airco Inc. Airco Electronics Bradford, PA 17055
14632	Watkins-Johnson Company 700 Quince Orchard Road Gaithersburg, MD 20878
15542	Mini-Circuits Laboratories Division of Scientific Components Corporation 2625 E. 14th Street Brooklyn, NY 11235
18324	Signetics Corporation 811 East Argues Avenue Sunnyvale, CA 94086
22526	Du Pont EI De Nemours and Company, Inc. Photo Products Dept. Berg Electronics Div. Route 83 New Cumberland, PA 17070
24355	Analog Devices, Inc. Route 1 Industrial Park P.O. Box 280 Norwood, MA 02062
26805	M/A-COM Omni Spectra, Inc. 140 Fourth Avenue Walton, MA 02154
27014	National Semi-Conductor Corp. 2950 San Ysidro Way Santa Clara, CA 95051
28480	Hewlett-Packard Company Corporate Headquarters 1501 Page Mill Road Palo Alto, CA 94304
31745	Rogers Corporation Flexible Circuits Division Williams Field and Dobson Road P.O. Box 700 Chandler, AZ 85224
32293	Intersil, Inc. Subdivision of General Electric Company 10600 Ridgeview Court Cupertino, CA 95014
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051
49956	Raytheon Co. 141 Spring Street Lexington, MA 02173
51642	Centre Enginering, Inc. 2820 E. College Avenue State College, PA 16801
51791	State K Corporation 512 North Main Street Orange, CA 92668
52648	Plessey Trading Corp. Plessey Optoelectronics and Microwave 1641 Raiser Avenue Irvine, CA 92714
53848	Standard Microsystems Corp. 35 Marcus Blvd Hauppauge, NY 11787
56289	Sprague Electric Company Marshall Street North Adams, MA 01247

Mfr. Code	Name and Address
59660	Tusonix, Inc. 2155 N. Forbes Blvd. Suite 107 Tucson, AZ 85745
60395	Xicor, Inc. 851 Buckeye Court Milpitas, CA 95035
61271	Fujitsu Microelectronics, Inc. 2985 Kifer Road Santa Clara, CA 95051
62786	Hitachi America Ltd 1800 Bering Drive San Jose, CA 95122
71279	Cambridge Thermionic Corp. 445 Concord Avenue Cambridge, MA 02138
71400	Bussman Manufacturing Division of McGraw-Edison Co. 2536 W. University Street St. Louis, MO 63107
71450	CTS Corporation 905 N. West Blvd. Elkhart, IN 46514
71468	ITT Cannon Electric 10550 Talbert Ave. P.O. Box 8040 Fountain Valley, CA 92708
72136	Electro Motive Mfg. Co., Inc. South Park & John Streets Willimantic, CT 06226
72982	Murata Erie North America, Incorporated 645 West 11th Street Erie, PA 16512
73138	Beckman Instruments, Inc. Helipot Division 2500 Harbor Boulevard Fullterton, CA 92634
75378	CTS Knights Inc. 400 Reimann Ave. Sandwich, IL 60548
76055	Mallory Controls Co. State Rd. 28 W. P.O. Box 327 Frankfort, IN 46041
80131	Electronic Industries Assoc. 2001 Eye Street, N.W. Washington, DC 20006
81073	Grayhill, Inc. 561 Hillgrove Avenue P.O. Box 10373 LaGrange, IL 60525
80294	Bourns, Incorporated 6135 Magnolia Avenue Riverside, CA 92506
81349	Military Specifications
99800	American Precision Industries Delevan Electronics Division 270 Quaker Road East Aurora, NY 14052

5.4 PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear or damage. When ordering replacement parts from Watkins-Johnson Company, specify the type and serial number of the equipment and the reference designation and description of each part ordered. The list of manufacturers provided in **paragraph 5.3** and the manufacturer's part number for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment; however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

NOTE

As improvements in semiconductors are made, it is the policy of Watkins-Johnson to incorporate them in proprietary products. As a result, some transistors, diodes and integrated circuits which are installed in the unit may not agree with the parts lists or schematic diagrams of this manual. However, substitution of the semiconductor devices listed in this manual may be substituted with satisfactory results.

5.5 TYPE WJ-9040 SYSTEM COMMON EQUIPMENT — MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
MC	EFR100-1 Equipment Frame	1	WJ-9040 EFR100-1	14632	
MC	IOM108-1 I/O Control Module	1	WJ-9040 IOM108-1	14632	
MC	EPS100A Power Supply	1	WJ-9040 EPS100A	14632	
MC	SRM105A 1, 5, 10 MHz Site Reference Module	1	WJ-9040 SRM105A	14632	

Figure 5-1. Type WJ-9040 System Common Equipment, Location of Components (3/4 Rear View)

5.6 **TYPE WJ-9040 EFR100 EQUIPMENT FRAME** **MAIN CHASSIS**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision C1				
A1	Connector Interface Module	1	794293-1	14632	
MP1	Handle, Front	2	32306-1	14632	
MP2	Same as MP1				

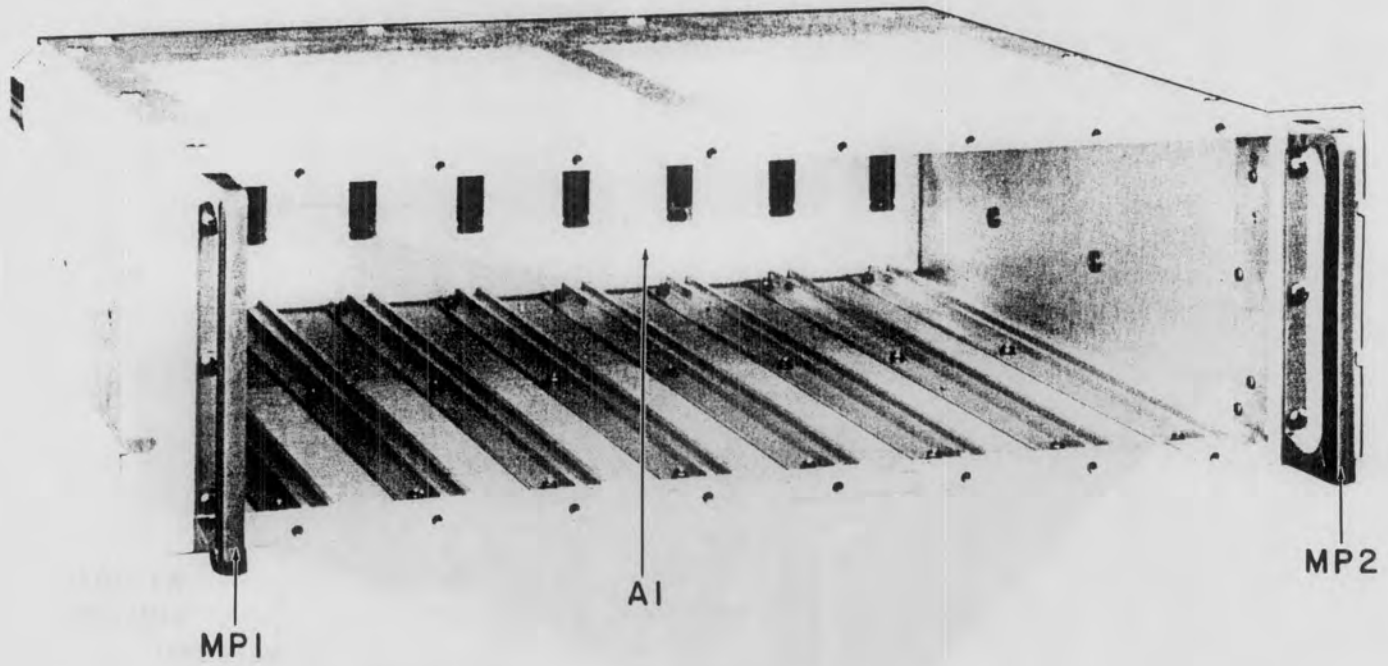


Figure 5-2. Type WJ-9040 EFR100 Equipment Frame, Location of Components

5.6.1 TYPE 794293-1 CONNECTOR INTERFACE MODULE

REF DESIG PREFIX A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision D1				
A1	Connector Interface	1	794294-1	14632	
J1	Connector, Receptacle, Multipin	8	DB25SU	71468	
J2 Thru J8	Same as J1				
J9	Connector, Receptacle, Multipin	1	DAF15PU	71468	
J10	Connector, Receptacle, Multipin	1	DCF37SU	71468	
J11	Connector, Receptacle, Multipin	1	DBF25SU	71468	

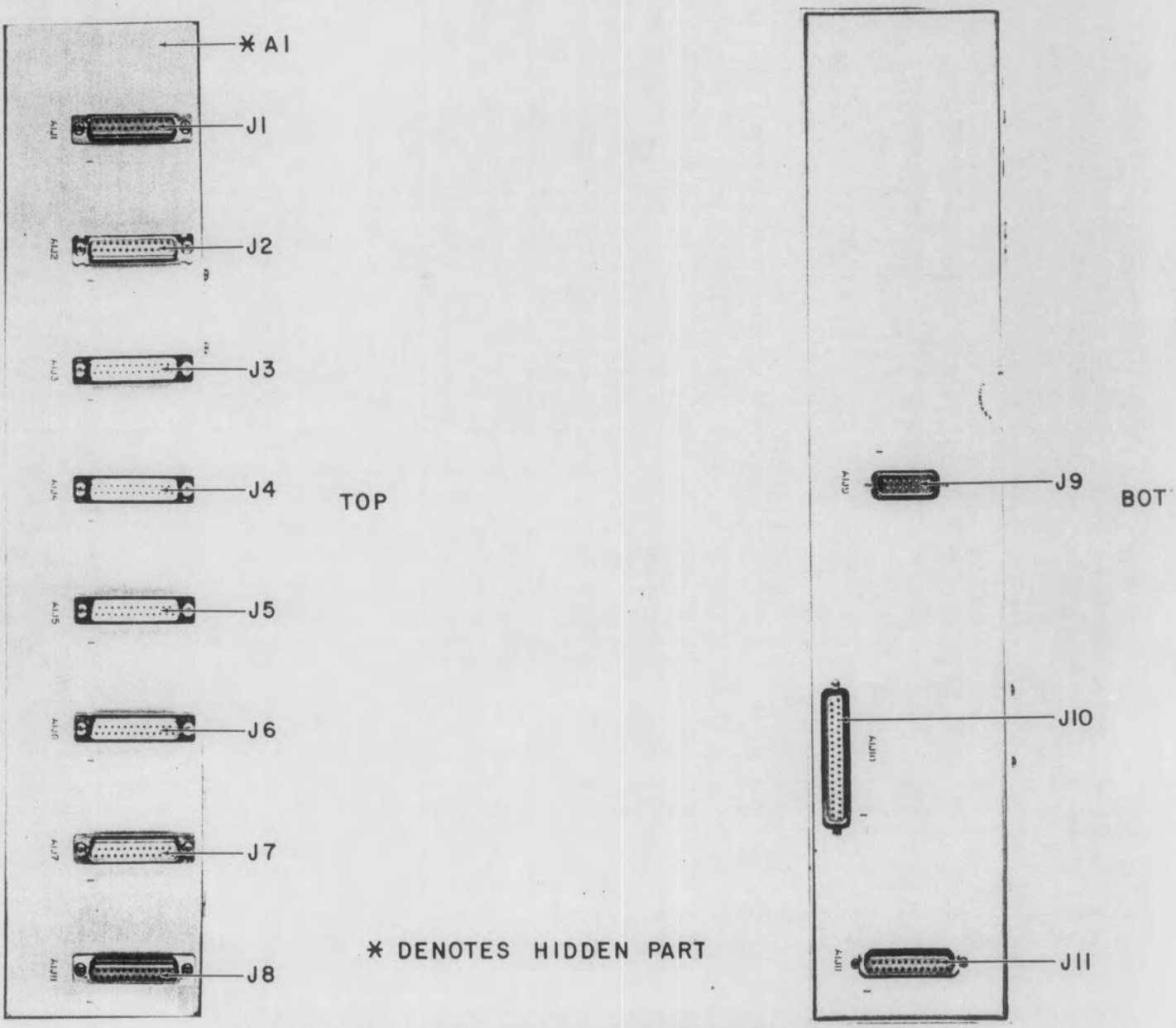


Figure 5-3. Type 794293-1 Connector Interface Module (A1), Location of Components

5.6.1.1 **Part 794294-1 Connector Interface** REF DESIG PREFIX A1A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision A				
S1	Switch, Toggle Rocker	1	76SB06S	81073	
TP1	Jack, Tip, Vertical	5	TJ358W	49956	
TP2 Thru TP5	Same as TP1				

5.7 TYPE WJ-9040 IOM108 I/O CONTROL MODULE — MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision B1				
A1	I/O Interface Motherboard	1	794291-1	14632	
A1A1	Digital I/O, RS-232C (Customer Selected Option)	1	794284-1	14632	
A1A1	Digital I/O, IEEE-488 (Customer Selected Option)	1	794285-1	14632	
A1A2	Bidirectional Polled I/O	1	794286-2	14632	
A1A3	System I/O	1	794287-1	14632	
A1A4	Not Used				
A1A5	Extended CPU	1	794444-X	14632	
AI-1	Extender Board	1	370751-1	14632	

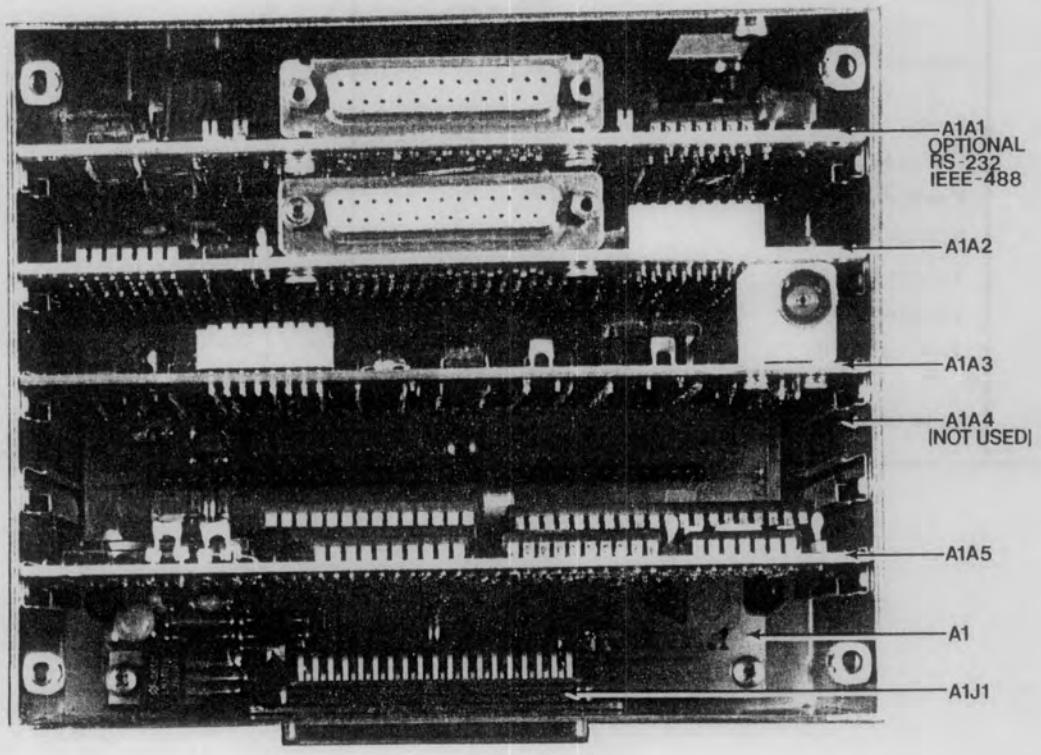


Figure 5-4. WJ-9040 IOM108 I/O Control Module, Top View, Location of Components

5.7.1 TYPE 794291-1 I/O INTERFACE MOTHERBOARD REF DESIG PREFIX A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision B1				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	15	34475-1	14632	
C2 Thru C15	Same as C1				
C16	Capacitor, Electrolytic, Tantalum: 2.2 µF, 20%, 35 V	3	196D225X0035TE3	56289	
C17	Capacitor, Electrolytic, Tantalum: 2.7 µF, 10%, 35 V	2	196D276X9035TE4	56289	
C18	Same as C16				
C19	Same as C17				
C20	Same as C16				
C21	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	1	34452-1	14632	
C22	Capacitor, Electrolytic, Tantalum: 1 µF, 20%, 35 V	1	196D105X0035HE3	56289	
C23	Capacitor, Electrolytic, Tantalum: 220 µF, 20%, 10 V	1	196D227X0010TE4	56289	
CR1	Diode	6	IN4003	80131	
CR2 Thru CR6	Same as CR1				
CR8	Diode	1	IN5819	80131	
J1	Connector, Multipin	1	DC-37PC	71468	
R1	Resistor, Fixed, Composition: 10Ω, 5%, 1/2 W	1	RCR20G100JS	80131	
VR1	Voltage Regulator	1	LM340T-12	27014	
VR2	Voltage Regulator	1	LM320-12	27014	
VR3	Voltage Regulator	1	LM340T-5.0	27014	
XA1	Terminal, Strip	10	65500-120	22526	
XA2 Thru XA5	Same as XA1				

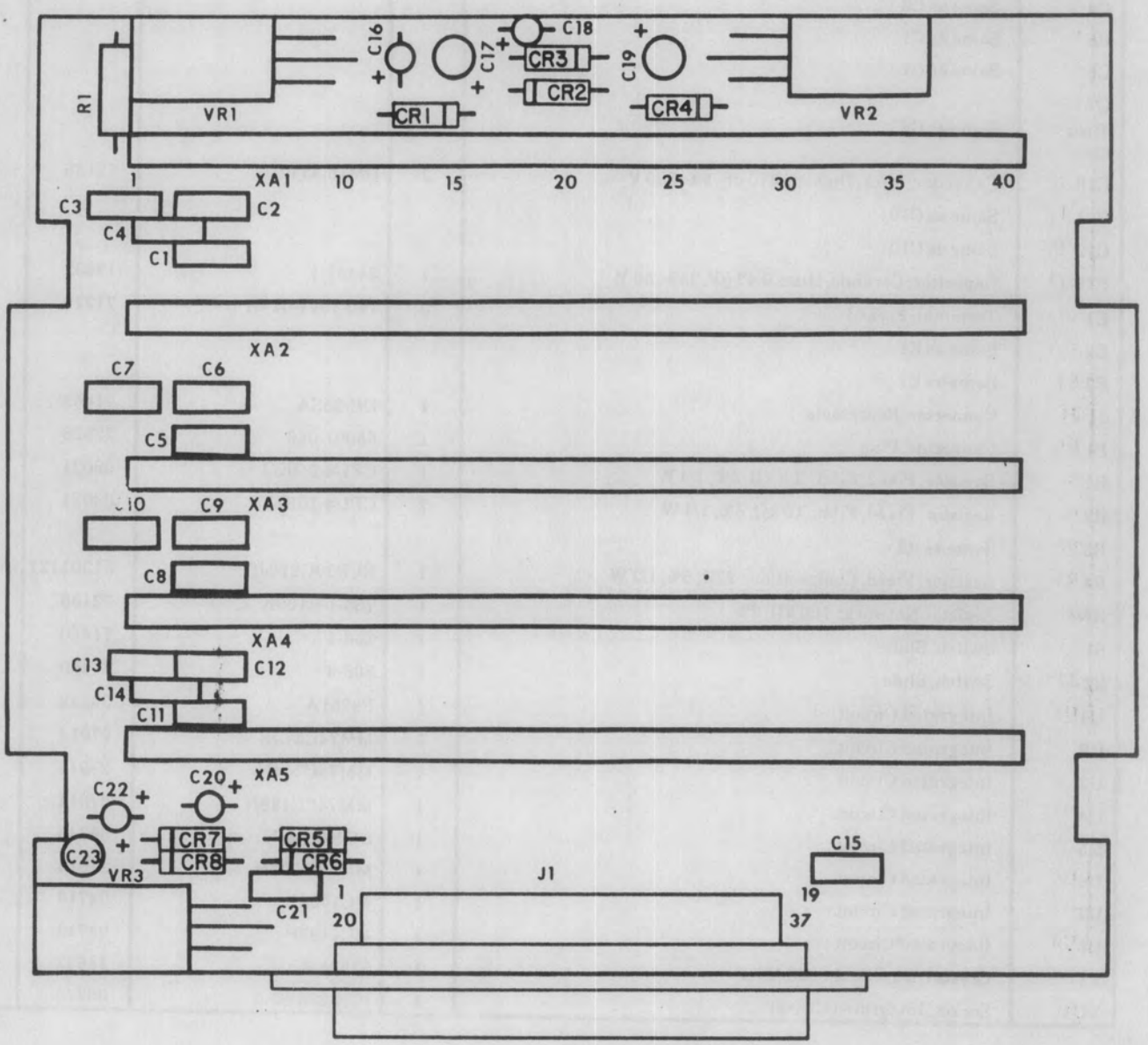


Figure 5-5. Type 794291-1 I/O Interface Motherboard (A1), Location of Components

5.7.1.1 Type 794284-1 Digital I/O RS-232C (Option) REF DESIG PREFIX A1A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision A				
C1	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	3	196D475X0035JE3	56289	
C2	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	6	34475-1	14632	
C3	Same as C2				
C4	Same as C2				
C5	Same as C1				
C6	Same as C1				
C7 Thru C9	Same as C2				
C10	Capacitor, Mica, Dipped: 470 pF, 5%, 500 V	3	DM15-471J	72136	
C11	Same as C10				
C12	Same as C10				
C13	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	1	34452-1	14632	
E1	Terminal, Forked	3	140-1941-02-01	71279	
E2	Same as E1				
E3	Same as E1				
J1	Connector, Receptacle	1	DB-25SA	71468	
P1	Connector, Plug	1	65001-066	22526	
R1	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/4 W	1	CF1/4-3.3K/J	09021	
R2	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	2	CF1/4-10K/J	09021	
R3	Same as R2				
R4	Resistor, Fixed, Composition: 22Ω, 5%, 1/2 W	1	RCR20G220JS	81301121	
RN1	Resistor Network: 100 kΩ, 2%	1	765-1-R100K	73138	
S1	Switch, Slide	1	206-4	71450	
S2	Switch, Slide	1	206-8	71450	
U1	Integrated Circuit	1	P8251A	34649	
U2	Integrated Circuit	1	MM74C373N	27014	
U3	Integrated Circuit	1	MM74C244N	27014	
U4	Integrated Circuit	1	MM74PC138N	27014	
U5	Integrated Circuit	1	COM5046P	53848	
U6	Integrated Circuit	1	MM74PC02N	27014	
U7	Integrated Circuit	1	MC1488L	04713	
U8	Integrated Circuit	1	MC1489P	04713	
Y1	Crystal, Quartz: 5.0688 MHz	1	91805-4	14632	
XU1	Socket, Integrated Circuit	1	ICN-286-S5-T	06776	

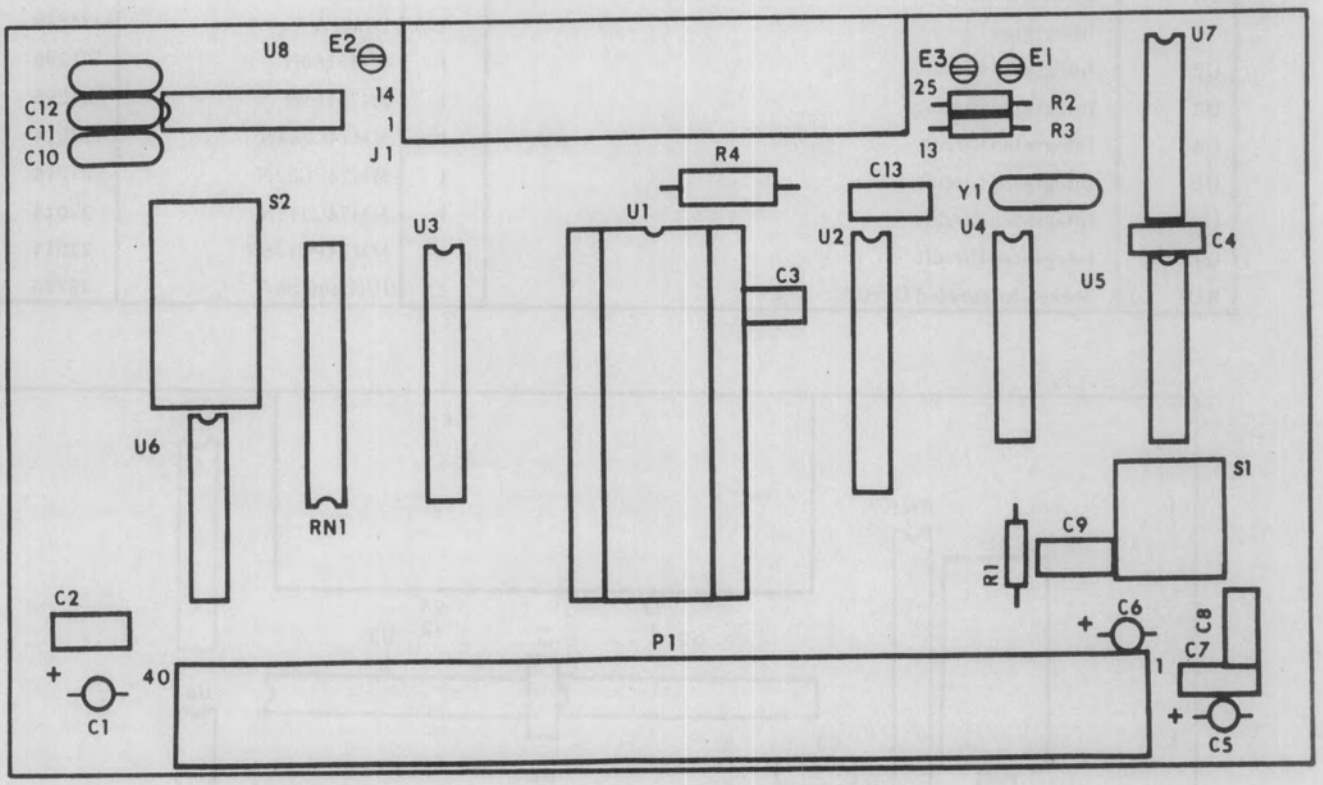


Figure 5-6. Type 794284-1 Digital I/O RS-232C (Option), (A1A1), Location of Components

5.7.1.2 Type 794285-1 Digital I/O IEEE-488 (Option) REF DESIG PREFIX A1A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision A				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	34475-1	14632	
C2	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	1	196D475X0035JE3	56289	
C3	Same as C1				
J1	Connector, Receptacle	1	552791-1	00779	
P1	Connector, Plug	1	65001-066	22526	
RN1	Resistor, Network: 100 kΩ, 2%	1	765-1-R100K	73138	
S1	Switch, Slide	1	206-8	71450	
U1	Integrated Circuit	1	P8291A	34649	
U2	Integrated Circuit	1	SN75160N	01295	
U3	Integrated Circuit	1	SN75161N	01295	
U4	Integrated Circuit	1	MM74C244N	27014	
U5	Integrated Circuit	1	MM74PC32N	27014	
U6	Integrated Circuit	1	MM74C373N	27014	
U7	Integrated Circuit	1	MM74PC138N	27014	
XU1	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	

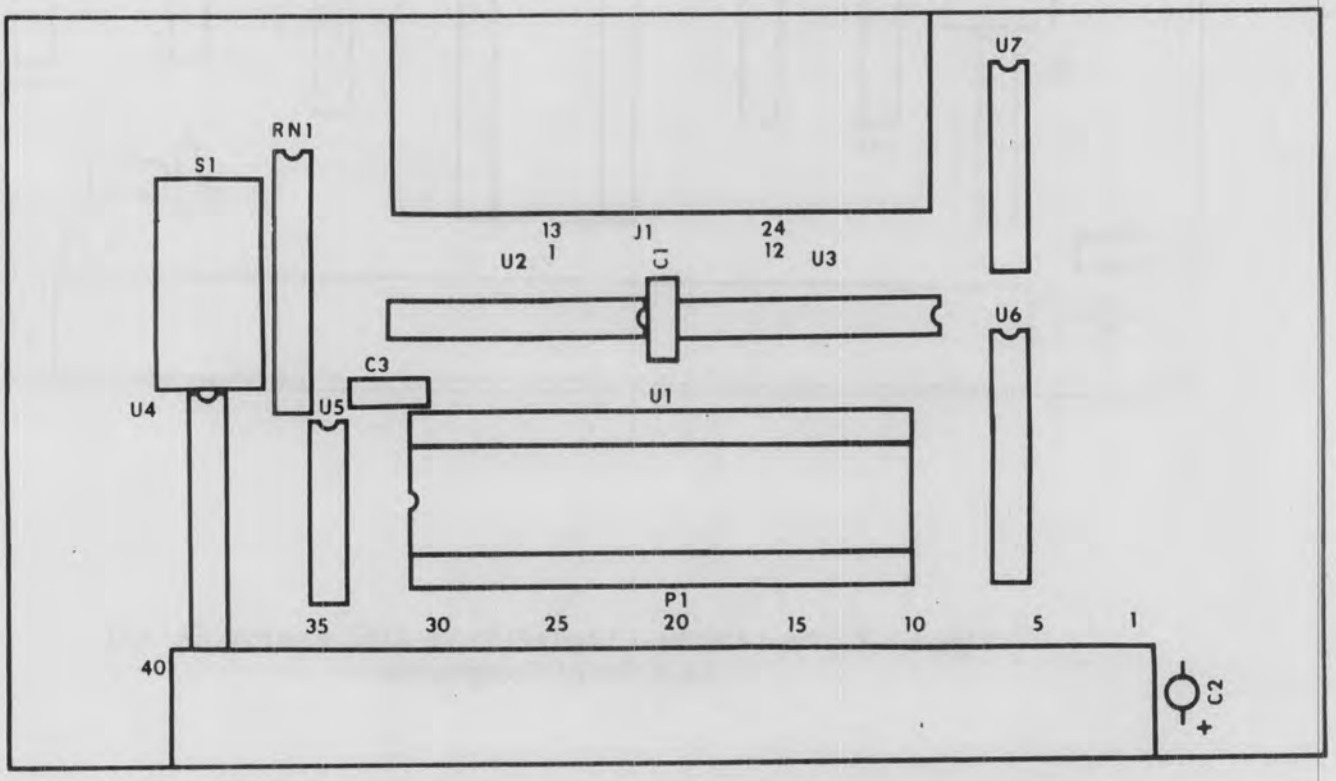


Figure 5-7. Type 794285-1 Digital I/O IEEE-488 (Option), (A1A1), Location of Components

5.7.1.3 **Type 794286-2 Bidirectional Polled I/O** REF DESIG PREFIX A1A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision F				
C1	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	4	196D475X0035JE3	56289	
C2	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	7	34475-1	14632	
C3 Thru C7	Same as C2				
C8	Capacitor, Mica, Dipped: 100 pF, 2%, 500 V	1	CM05FD101G03	81349	
C9	Same as C2				
C10 Thru C12	Same as C1				
CR1	Diode	1	1N4449	80131	
P1	Connector, Plug	1	65001-066	22526	
R1	Resistor, Fixed, Film: 47.5 kΩ, 1%, 1/10 W	7	RN55C4752F	81349	
R2	Same as R1				
R3	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	2	CF1/4-10K/J	09021	
R4	Resistor, Fixed, Film: 681Ω, 1%, 1/10 W	1	RN55C6810F	81349	
R5	Same as R3				
R6	Resistor, Fixed, Film: 11 kΩ, 1%, 1/10 W	2	RN55C1102F	81349	
R7	Same as R6				
R8	Same as R1				
R9	Same as R1				
R10	Resistor, Fixed, Film: 1.0 kΩ, 1%, 1/4 W	1	RN60D1001F	81349	
R11	Resistor, Fixed, Film: 22.1 kΩ, 1%, 1/10 W	1	RN55C2212F	81349	
R12 Thru R14	Same as R1				
R15	Resistor, Fixed, Film: 3.16 kΩ, 1%, 1/4 W	1	RN60D3161F	81349	
R16	Resistor, Fixed, Film: 120 kΩ, 5%, 1/4 W	1	CF1/4-120K/J	09021	
S1	Switch, Slide	4	206-8	71450	
S2 Thru S4	Same as S1				
U1	Integrated Circuit	2	TL064CN	01295	
U2	Integrated Circuit	1	MC14053BCP	04713	
U3	Same as U1				
U4	Integrated Circuit	2	DG201ACS	17856	
U5	Same as U4				
U6	Integrated Circuit	1	NSC810AN-3	27014	
U7	Integrated Circuit	1	MM74HC138N	27014	
U8	Integrated Circuit	1	MM74HC00N	27014	
U9	Integrated Circuit	1	MM74HC02N	27014	
U10	Integrated Circuit	1	AD7574JN	24355	
U11	Integrated Circuit	1	MM74HC373N	27014	

REF DESIG PREFIX A1A2

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U12	Integrated Circuit	1	MM82PC08NI	27014	
VR1	Diode, Zener: 5.1 V	2	IN751A	80131	
VR2	Same as VR1				

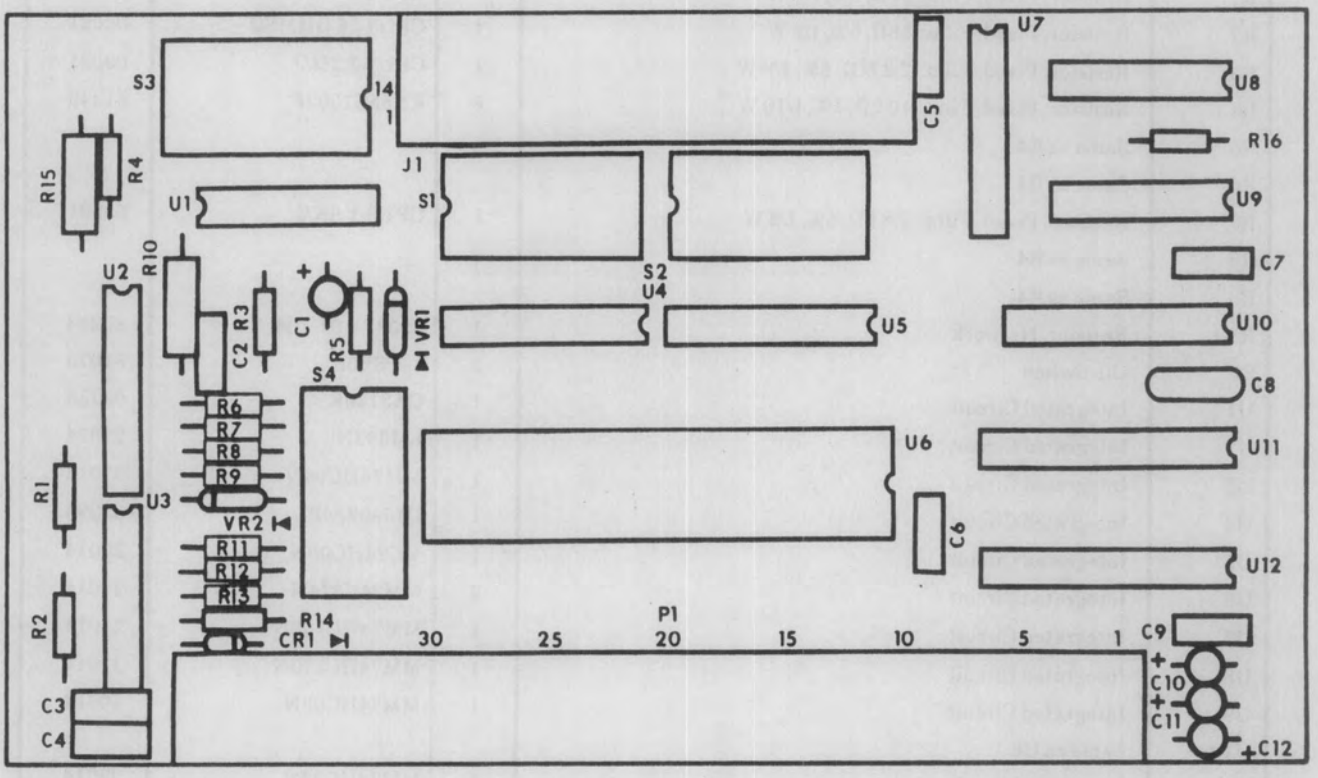


Figure 5-8. Type 794286-1 Bidirectional Polled I/O (A1A2), Location of Components

5.7.1.4 Type 794287-1 System I/O REF DESIG PREFIX A1A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	6	34475-1	14632	
C2 Thru C6	Same as C1				
C7	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	1	196D475X0035JE3	56289	
CR1	Diode	1	IN4449	80131	
CR2	Diode	1	IN746A	80131	
P1	Connector, Plug	1	65001-066	22526	
R1	Resistor, Fixed, Film: 39Ω, 5%, 1/8 W	1	CF1/8-39 OHMS/J	09021	
R2	Resistor, Fixed, Film: 56Ω, 5%, 1/8 W	1	CF1/8-56 OHMS/J	09021	
R3	Resistor, Fixed, Film: 2.2 MΩ, 5%, 1/8 W	1	CF1/8-2.2M/J	09021	
R4	Resistor, Fixed, Film: 10 kΩ, 1%, 1/10 W	5	RN55C1002F	81349	
R5	Same as R4				
R6	Same as R4				
R7	Resistor, Fixed, Film: 1.8 kΩ, 5%, 1/8 W	1	CF1/8-1.8K/J	09021	
R8	Same as R4				
R9	Same as R4				
RN1	Resistor, Network	1	4308R-101-104	80294	
S1	Dip Switch	1	76PSB08	81073	
U1	Integrated Circuit	1	CA3140E	02735	
U2	Integrated Circuit	1	LM393N	27014	
U3	Integrated Circuit	1	MM74HC04N	27014	
U4	Integrated Circuit	1	IM6402AIPL	32293	
U5	Integrated Circuit	1	MC74HC00N	27014	
U6	Integrated Circuit	2	MM74C374N	27014	
U7	Integrated Circuit	1	MM74HC138N	27014	
U8	Integrated Circuit	1	MM74HC373N	27014	
U9	Integrated Circuit	1	MM74HC08N	20714	
U10	Same as U6				
U11	Integrated Circuit	1	MM74HC32N	27014	
U12	Integrated Circuit	1	CD4094BE	02735	
U13	Integrated Circuit	2	MM74C244N	27014	
U14	Same as U13				
U15	Integrated Circuit, Register	1	MM74HC165N	27014	

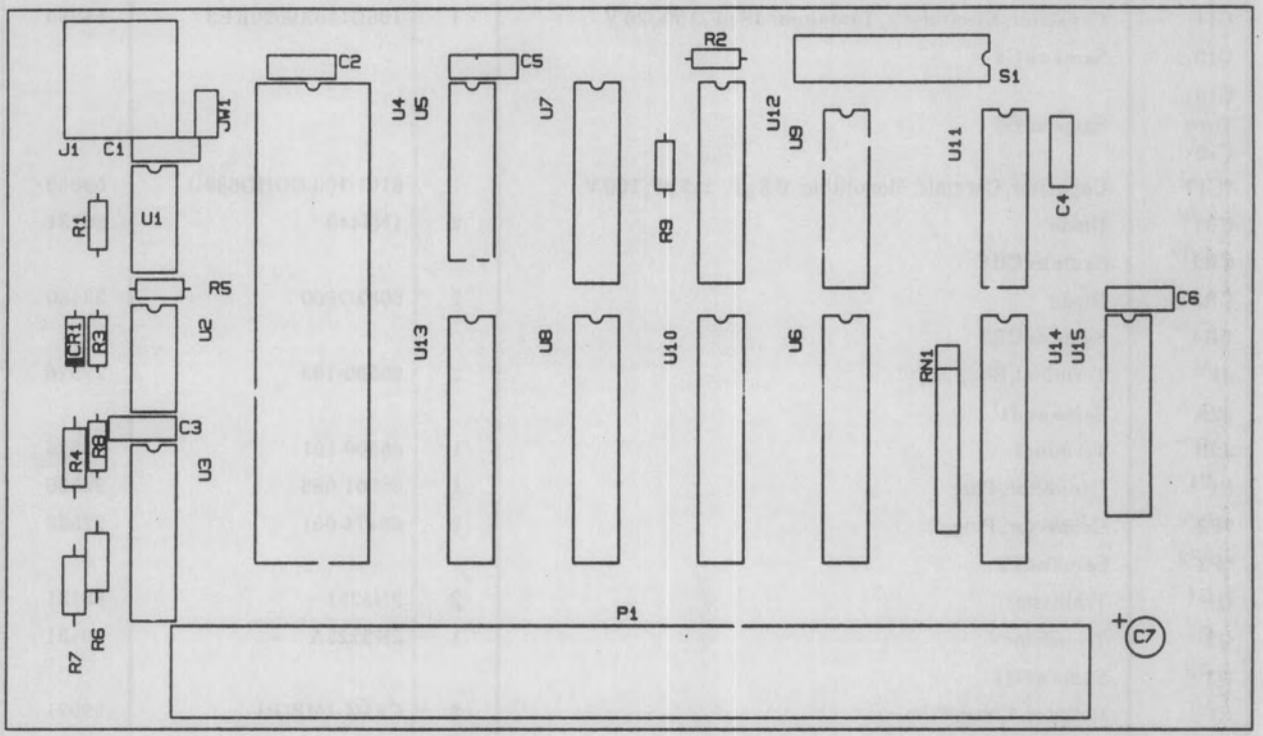


Figure 5-9. Type 794287-1 System I/O (A1A3), Location of Components

5.7.1.5 **Type 794444-X Extended CPU** REF DESIG PREFIX A1A5

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision E1				
BT1	Battery, Lithium	1	2736	00681	
C1	Capacitor, Ceramic, Disc: 39 pF, 5%, 100 V	2	8121-100-COGO-390J	59660	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: .1 µF, 20%, 50 V	5	34475-1	14632	
C4	Capacitor, Ceramic, Disc: .01 µF, 20%, 50 V	2	34453-1	14632	
C5	Capacitor, Micro-Q, Dipped: .03 µF, 50 VDC	3	1R0GUQ08A	31745	
C6	Same as C5				
C7	Same as C5				
C8	Same as C3				
*C9	Capacitor, Ceramic, Monolithic: 20 pF, 5%, 100 V	1	100-100-NPO-200J	51642	
*C10	Capacitor, Variable, Ceramic: 5 - 25 pF, 100 V	1	518-000A5-25	59660	
C11	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	1	196D186X9020KE3	56289	
C12	Same as C4				
C13 Thru C15	Same as C3				
*C17	Capacitor, Ceramic, Monolithic: 6.8 pF, ±.5 pF, 100 V	1	8101-100-COHO689D	59660	
CR1	Diode	2	1N4449	80131	
CR2	Same as CR1				
CR3	Diode	2	5082-2800	28480	
CR4	Same as CR3				
J1	Terminal, Strip	2	65500-103	22526	
J2A	Same as J1				
J2B	Terminal	1	65500-101	22526	
P1	Connector, Plug	1	65001-066	22526	
*P2	Connector, Plug	2	65474-001	22526	
*P3	Same as P2				
Q1	Transistor	2	2N3251	80131	
Q2	Transistor	1	2N2222A	80131	
Q3	Same as Q1				
R1	Resistor, Fixed, Film	2	CF1/4-1MEG/J	09021	
R2	Same as R1				
R3	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	5	CF1/8-10 K/J	09021	
R4	Same as R3				
R5	Resistor, Fixed, Film: 47 kΩ, 5%, 1/4 W	1	CF1/4-47K/J	09021	
R6	Same as R3				
R7	Same as R3				
R8	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	1	CF1/8-3.3K/J	09021	
R9	Resistor, Fixed, Film: 6.8 kΩ, 5%, 1/8 W	1	CF1/8-6.8K/J	09021	

***Note: These are used on the -2 Parts List Only.**

REF DESIG PREFIX A1A5

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R10	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	6	CF1/8-100K/J	09021	
R11	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	2	CF1/8-2.2K/J	09021	
R12	Resistor, Fixed, Film: 2.7Ω, 5%, 1/8 W	1	CF1/8-2.7 OHMS/J	09021	
R13	Same as R3				
R14	Same as R11				
R15	Resistor, Fixed, Film: 100Ω, 5%, 1/8 W	1	CF1/8-100 OHMS/J	09021	
R16 Thru R20	Same as R10				
R21	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	1	CF1/8-1.0K/J	09021	
RN1	Resistor, Network: 100 kΩ, 2%	1	4308R-101-104	80294	
U1	Integrated Circuit	1	NSC800N	27014	
U2	Integrated Circuit	1	MM74HC00N	27014	
U3	Integrated Circuit	1	MM74HC244N	27014	
U4	Integrated Circuit, Latch	1	MM74HC373N	27014	
U5	Integrated Circuit	2	MM74HC138N	27014	
U6	Integrated Circuit	1	MM74HC245N	27014	
U7	Integrated Circuit	2	MBM27C256-25	61271	
U8	Same as U7				
U9	Integrated Circuit: RAM	1	HM6264LP-15	62786	
U10	Integrated Circuit	1	MM74HC08N	27014	
U11	Integrated Circuit	1	LM393N	27014	
U12	Same as U5				
U13	Integrated Circuit	1	MM74C174N	27014	
*U14	Integrated Circuit, Timer	1	MM58274N	27014	
U15	Integrated Circuit	1	MM74HC32N	27014	
VR1	Diode Zener: 4.3 V	1	1N749A	80131	
XU1	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	
XU7	Socket, Integrated Circuit	3	ICN-286-S5-T	06776	
XU8	Same as XU7				
XU9	Same as XU7				
Y1	Crystal, Quartz	1	CSA4.91MG	72982	
*Y2	Crystal, Quartz	1	CX-.03	51791	

***Note: These are used on the -2 Parts List Only.**

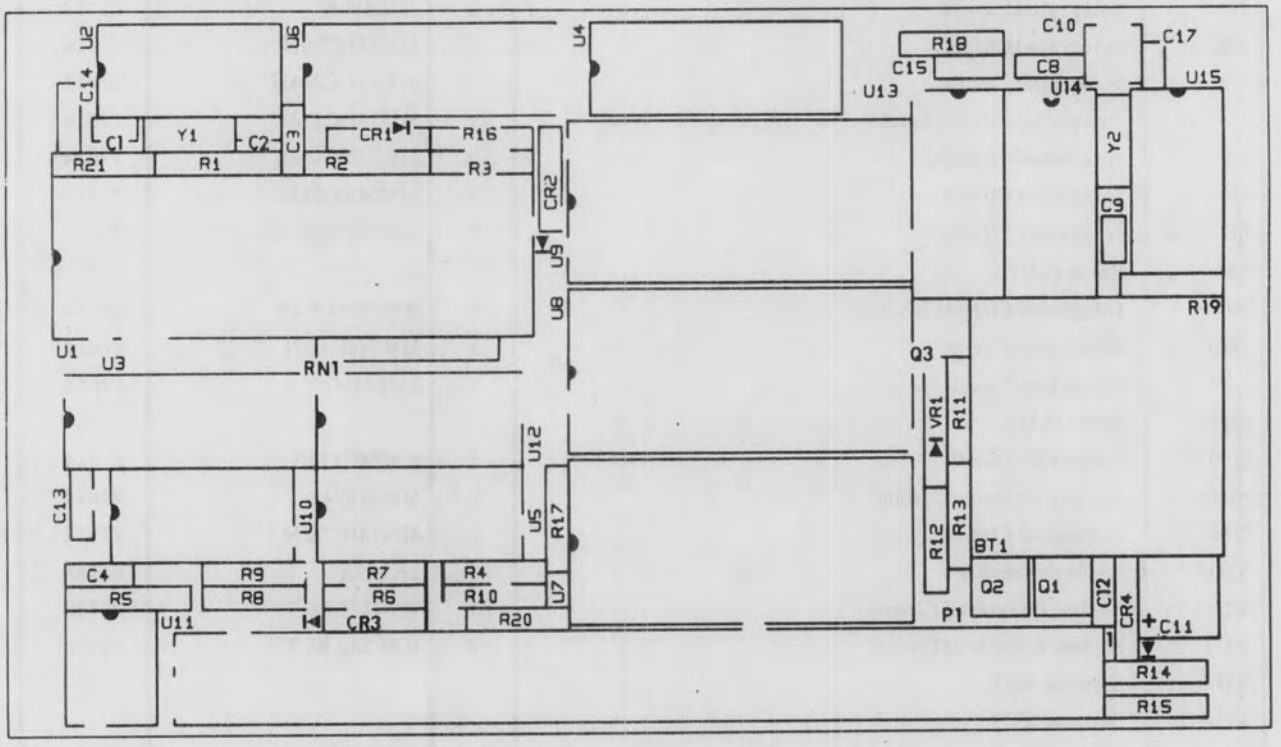


Figure 5-10. Type 794444-X Extended CPU (A1A5), Location of Components

5.8 TYPE WJ-9040 EPS100A POWER SUPPLY — MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
F1	Fuse, Cartridge, 3 Amp	1	MDX5	71400	

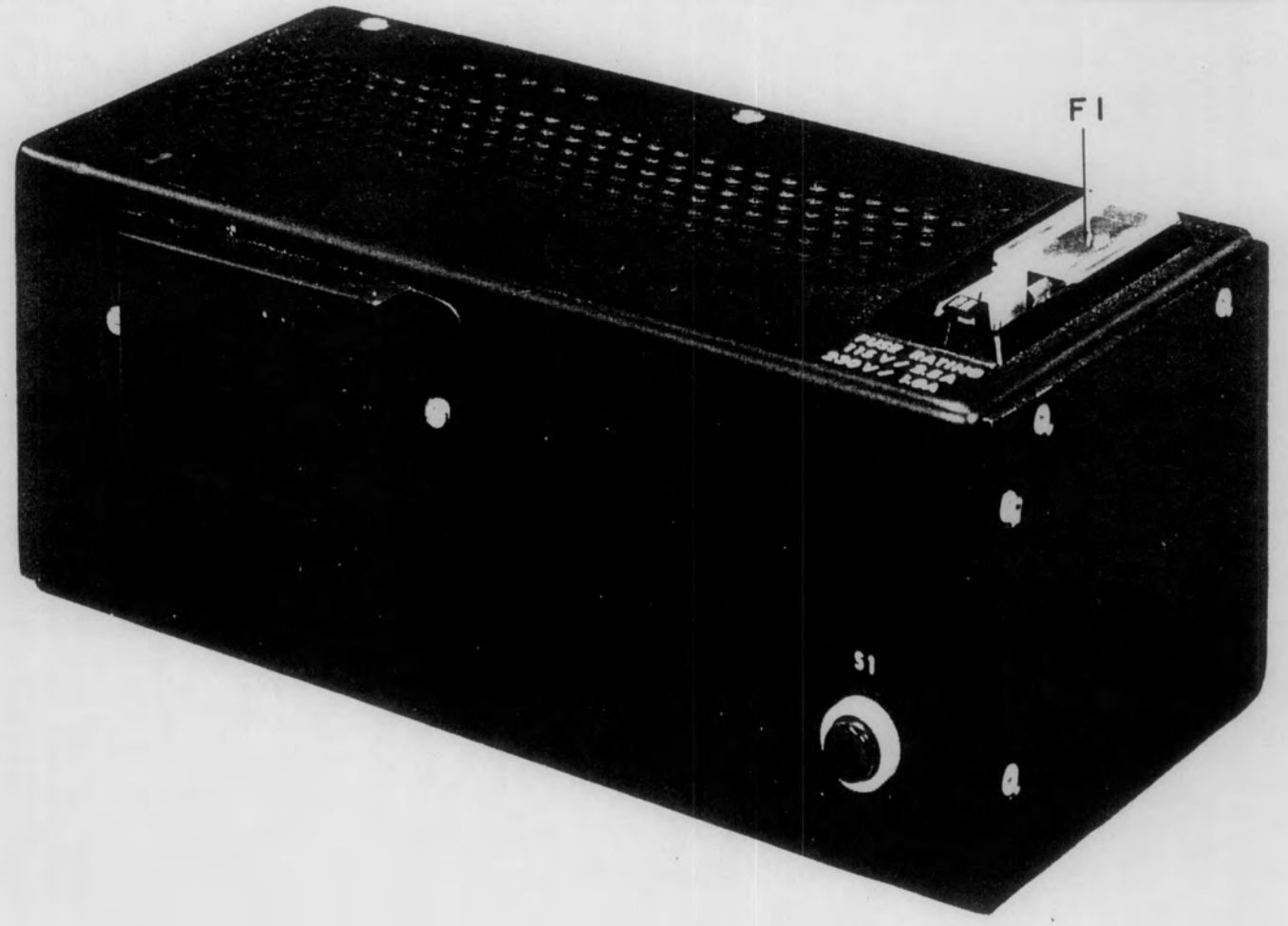


Figure 5-11. Type WJ-9040 EPS100A Power Supply, Location of Components

5.9 **TYPE WJ-9040 SRM105A 1, 5, 10 MHz SITE REFERENCE MODULE** MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision B1				
A1	1, 5, 10 MHz, Site Reference	1	371343-1	14632	
J1	Connector, Receptacle	5	2058-0000-00	26805	
J2 Thru J5	Same as J1				

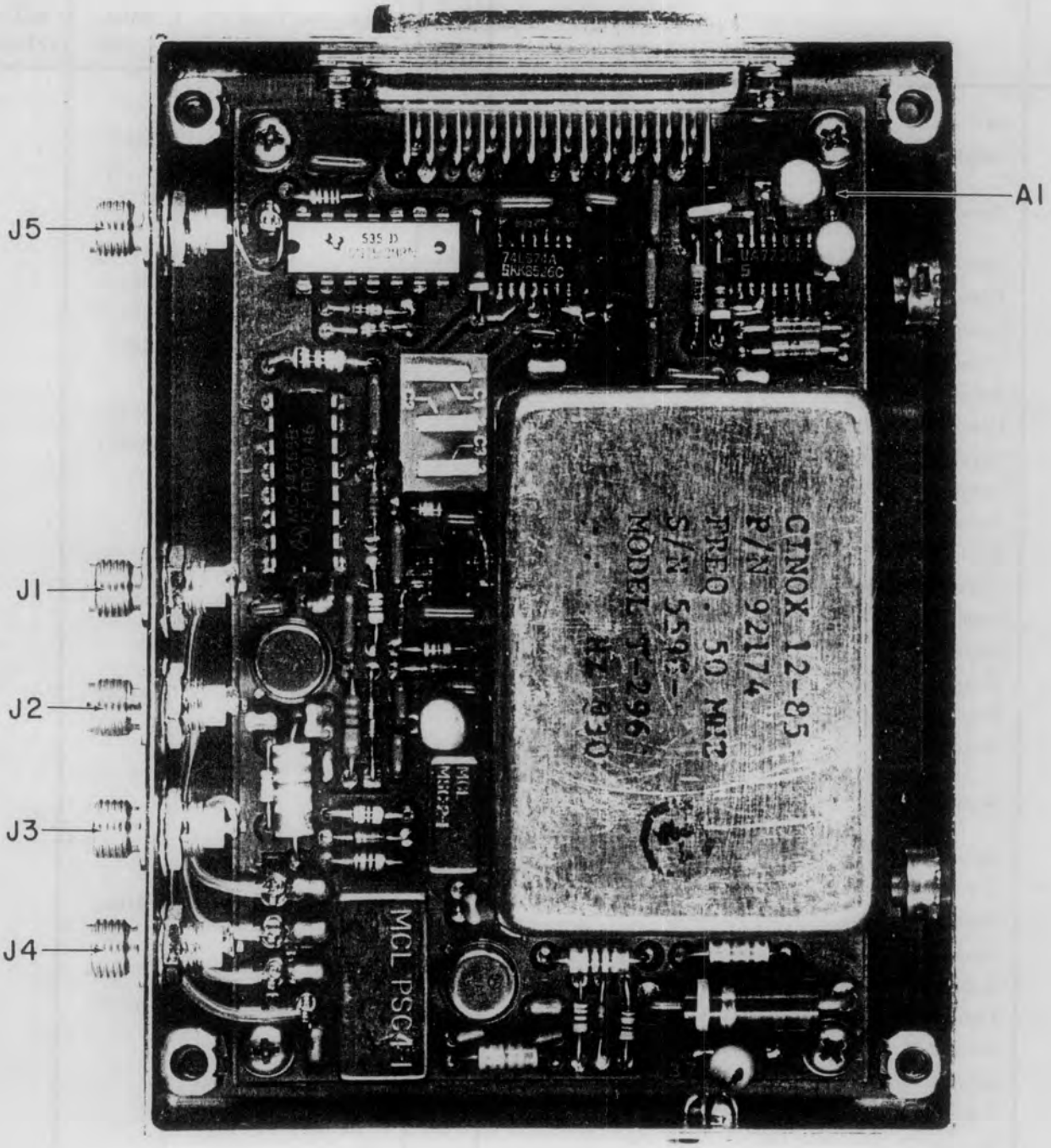


Figure 5-12. Type WJ-9040 SRM105A 1, 5, 10 MHz Site Reference Module, Location of Components

5.9.1 TYPE 371343-1 1, 5, 10 MHz SITE REFERENCE MODULE REF DESIG PREFIX A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
	Revision D1				
C1	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 100 V	8	8131M100-651-474M	59660	
C2 Thru C4	Same as C1				
C5	Capactior, Ceramic, Disc: 0.01 µF, 20%, 50 V	1	34453-1	14632	
C6	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	2	8131-050-651-105M	59660	
C7	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	7	8121-050-651-104M	59660	
C8	Capacitor, Ceramic, Disc: 6.8 pF, ±0.5 pF, 100 V	1	8101-100-COHO-689D	59660	
C9	Same as C7				
C10	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	4	196D475X0035JE3	56289	
C11	Capacitor, Ceramic, Disc: 1000 pF, 5%, 100 V	2	8121-100-COGO-102J	59660	
C12	Same as C1				
C13	Same as C7				
C14	Same as C10				
C15	Capacitor, Ceramic, Disc: 180 pF, ±2%, 100 V	7	150-100-NPO-181G	51642	
C16	Capacitor, Ceramic, Disc: 10 pF, ±0.5 pF, 100 V	1	8101-100-COGO-100D	59660	
C17	Same as C15				
C18	Same as C15				
C19	Capacitor, Ceramic, Disc: 62 pF, ±2%, 100 V	2	150-100-NPO-620G	51642	
C20	Same as C19				
C21 Thru C24	Same as C15				
C25	Same as C10				
C26	Same as C10				
C27	Capacitor, Ceramic, Disc: 100 pF, ±2%, 100 V	1	200-100-NPO-101G	51642	
C28	Same as C11				
C29	Same as C1				
C30	Capacitor, Ceramic, Disc: 0.047 µF, 10%, 100 V	1	8121-100-X7RO-473K	59660	
C31	Same as C6				
C32	Same as C1				
C33	Same as C7				
C34	Same as C7				
C35	Same as C1				
C36	Same as C7				
C37	Same as C7				
E1	Terminal, Forked	11	140-1941-02-01	71279	
E2 Thru E11	Same as E1				
J1	Connector, Multipin	1	DB25PC	71468	
L1	Coil, Fixed: 2.2 µH, 10%	1	1025-28	99800	

REF DESIG PREFIX A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
L2	Coil, Fixed: 0.82 µH, 10%	1	1537-10	99800	
L3	Coil, Fixed, Molded: 10 µH	1	1025-44	99800	
L4	Coil, Fixed, Molded: 18 µH	1	1025-02	99800	
R1	Resistor, Fixed, Film: 56Ω, 5%, 1/8 W	1	CF1/8-56 OHMS/J	09021	
R2	Resistor, Fixed, Film: 560Ω, 5%, 1/4 W	1	CF1/4-560 OHMS/J	09021	
R3	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	3	CF1/8-10 K/J	09021	
R4	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	1	CF1/8-2.2K/J	09021	
R5	Resistor, Fixed, Film: 68 kΩ, 5%, 1/8 W	1	CF1/8-68K/J	09021	
R6	Same as R3				
R7	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/8 W	2	CF1/8-4.7K/J	09021	
R8	Same as R7				
R9	Resistor, Fixed, Film: 39 kΩ, 5%, 1/8 W	1	CF1/8-39K/J	09021	
R10	Resistor, Fixed, Film: 820Ω, 5%, 1/4 W	1	CF1/4-820 OHMS/J	09021	
R11	Resistor, Fixed, Film: 470Ω, 5%, 1/8 W	4	CF1/8-470 OHMS/J	09021	
R12	Resistor, Fixed, Film: 6.8Ω, 5%, 1/8 W	2	CF1/8-6.8 OHMS/J	09021	
R13	Same as R11				
R14	Resistor, Fixed, Composition: 220Ω, 5%, 1 W	1	RCR32G221JS	81349	
R15	Same as R11				
R16	Same as R12				
R17	Same as R11				
R18	Resistor, Fixed, Film: 12.7 kΩ, 1%, 1/10 W	1	RN55C1272F	81349	
R19	Resistor, Fixed, Film: 5.6Ω, 5%, 1/4 W	1	CF1/4-5.6 OHMS/J	09021	
R20	Resistor, Fixed, Film: 13.3 kΩ, 1%, 1/10 W	1	RN55C1332F	81349	
R21	Resistor, Fixed, Film: 12.1 kΩ, 1%, 1/10 W	1	RN55C1212F	81349	
R22	Same as R3				
R23	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	1	CF1/4-1.0K/J	09021	
S1	Switch, Rocker	1	76STC03	81073	
U1	Integrated Circuit	1	MC14568BCP	04713	
U2	Integrated Circuit	1	NE5534D	18324	
U3	Integrated Circuit	1	92174	14632	
U4	Integrated Circuit	1	MSC-2-1	15542	
U5	Integrated Circuit	1	SP8657B	52648	
U6	Integrated Circuit	1	MWA130	04713	
U7	Integrated Circuit	1	PSC-4-1	15542	
U8	Integrated Circuit	1	MC79L15ACP	04713	
U9	Integrated Circuit	1	UA723CD	18324	
U10	Integrated Circuit	1	SN75108B	01295	
U11	Integrated Circuit	1	SN74LS74D	01295	
U12	Integrated Circuit	1	MC79L05ACP	04713	
U13	Integrated Circuit	1	LM78L05ACZ	04713	
VR1	Diode, Zener: 5.1 V	1	1N751A	80131	

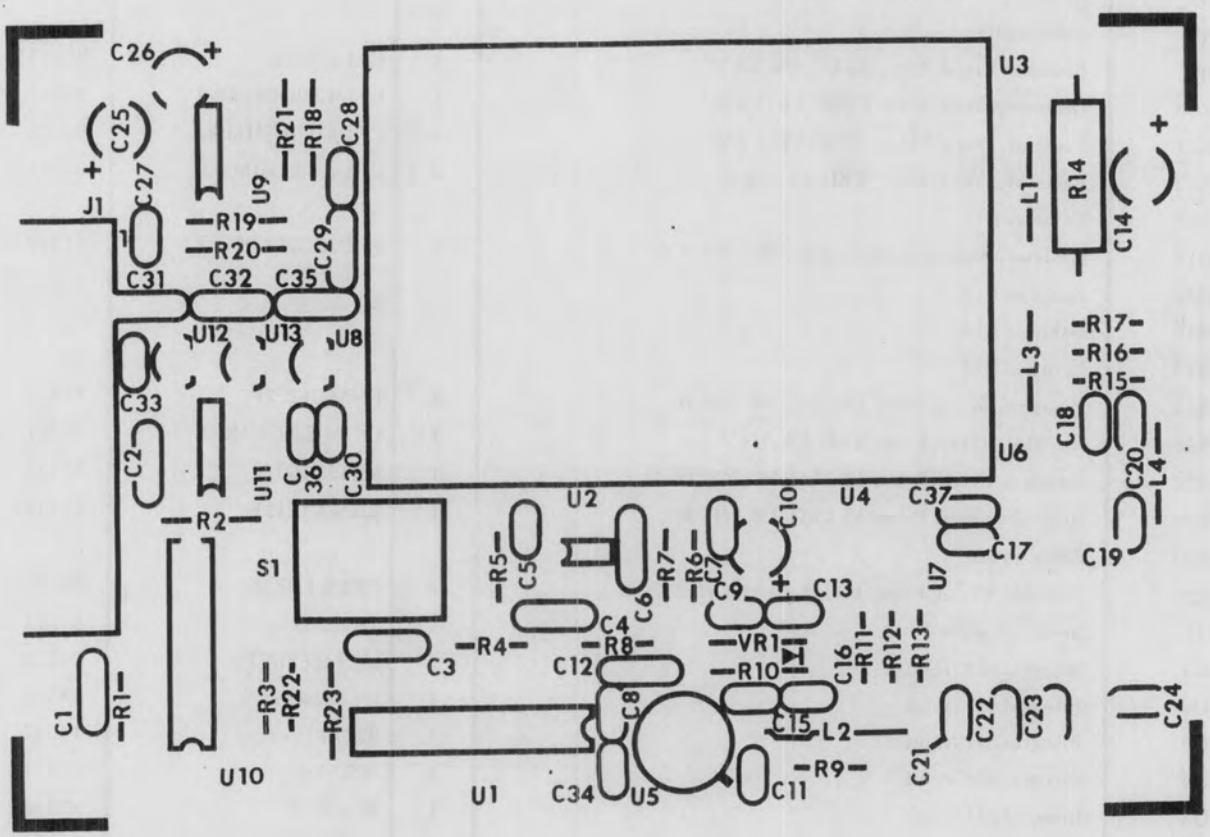
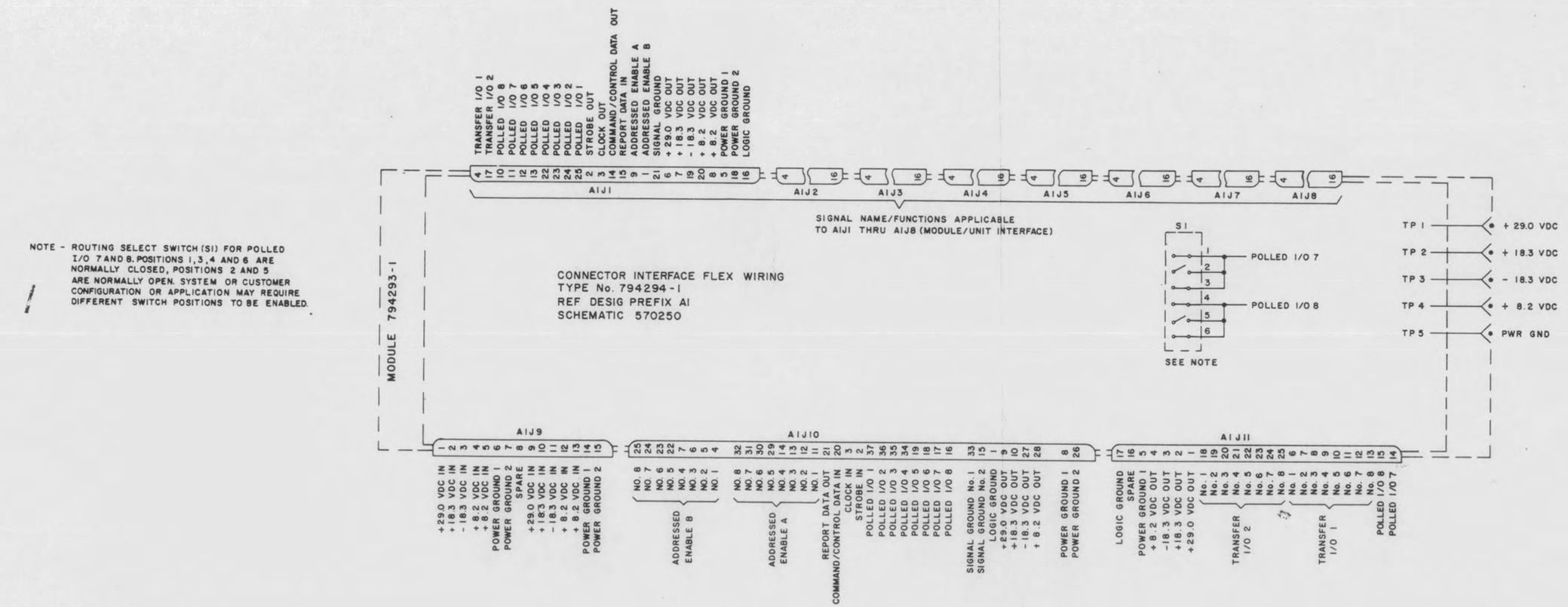


Figure 5-13. Type 371343-1 1, 5, 10 MHz Site Reference Module (A1), Location of Components

SECTION VI

SCHEMATIC DIAGRAMS



NOTE - ROUTING SELECT SWITCH (S1) FOR POLLED I/O 7 AND 8. POSITIONS 1, 3, 4 AND 6 ARE NORMALLY CLOSED, POSITIONS 2 AND 5 ARE NORMALLY OPEN. SYSTEM OR CUSTOMER CONFIGURATION OR APPLICATION MAY REQUIRE DIFFERENT SWITCH POSITIONS TO BE ENABLED.

Figure 6-1. Type 794293-1, Connector Interface Module (A1), Schematic Diagram 470661 (A)

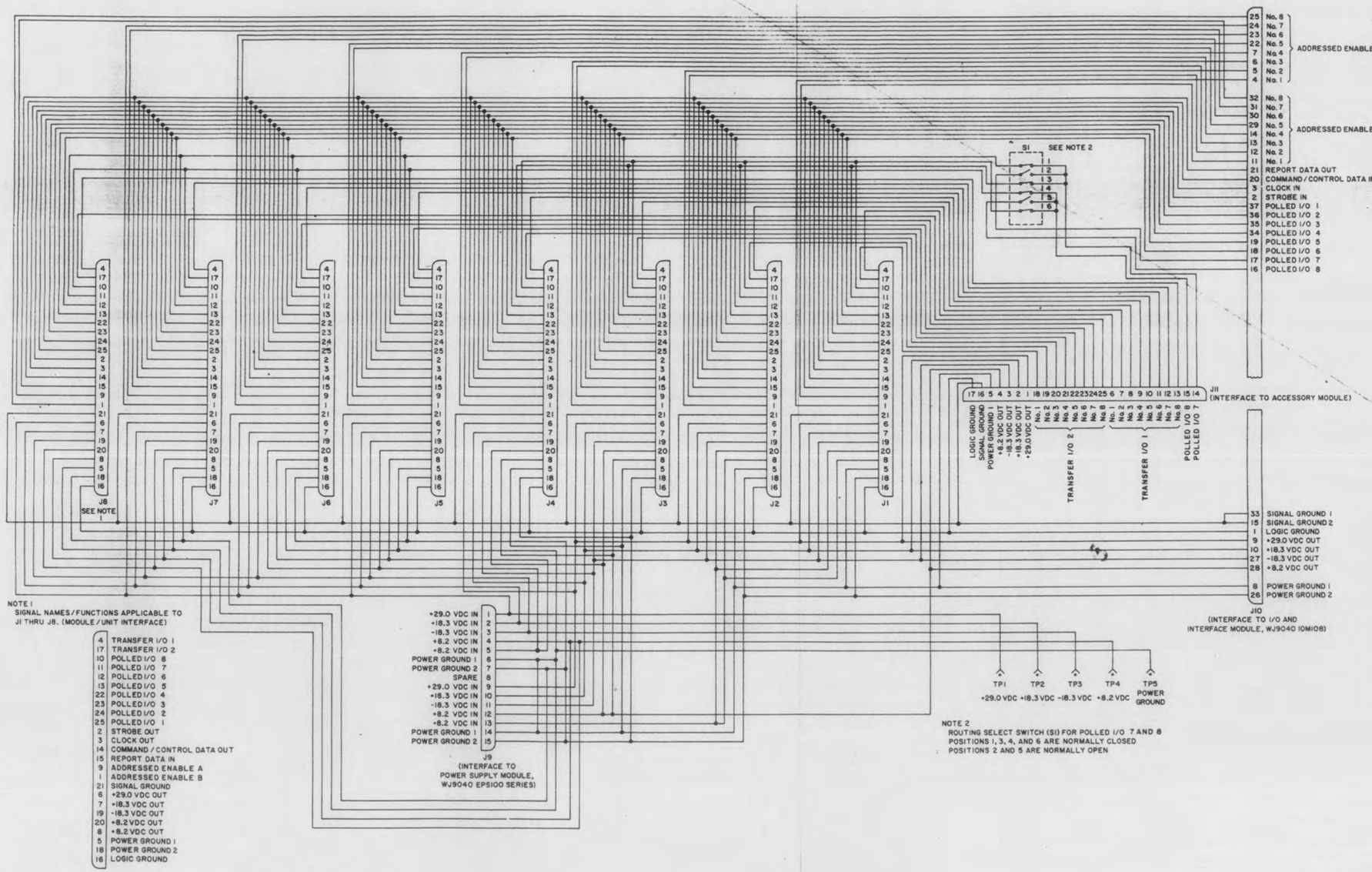
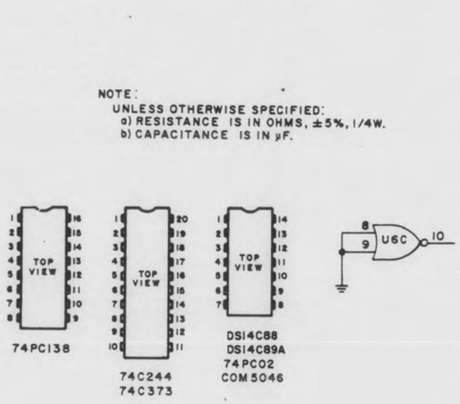


Figure 6-2. Type 794294-1, Connector Interface (A1A1), Schematic Diagram 570250 (B)

NOTE:
UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
b) CAPACITANCE IS IN μF.



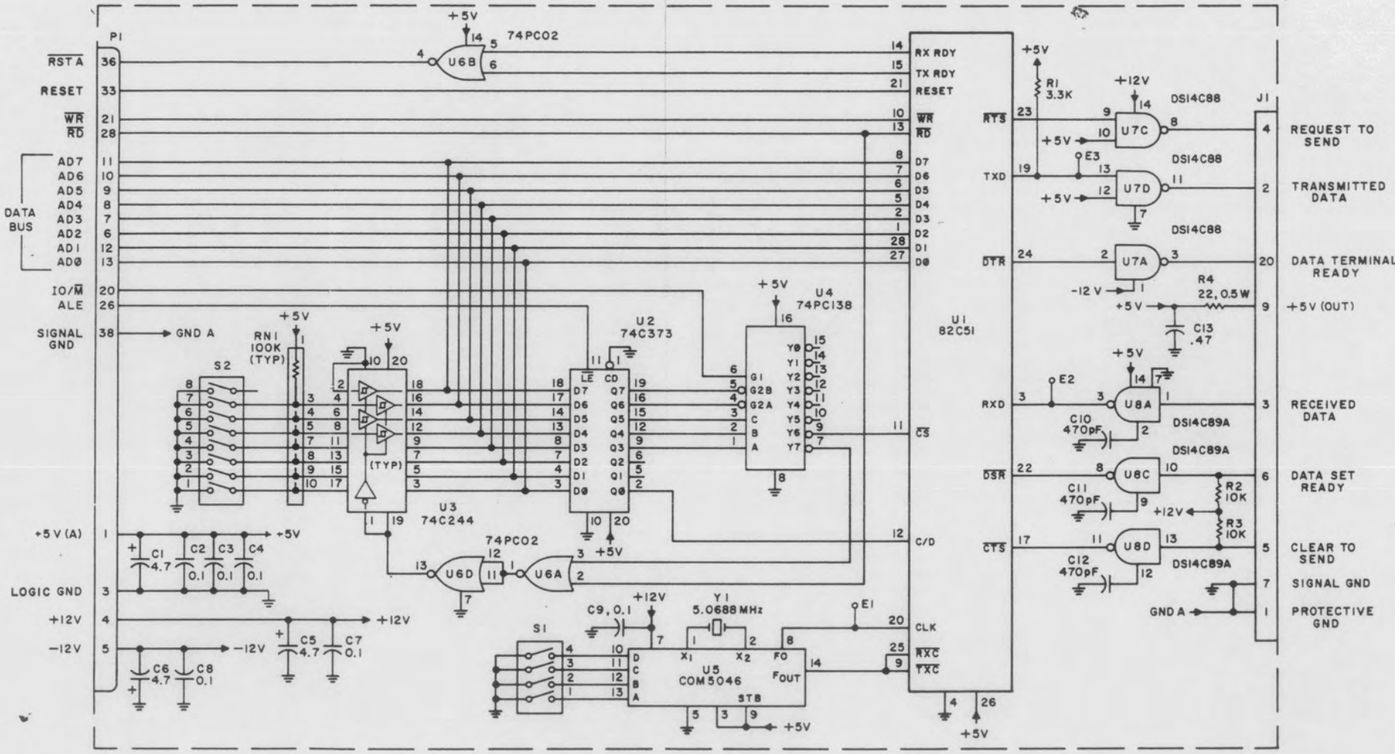


Figure 6-3. Type 794284-1, Digital I/O RS-232 (Optional), (A1A1), Schematic Diagram 470494 (B)

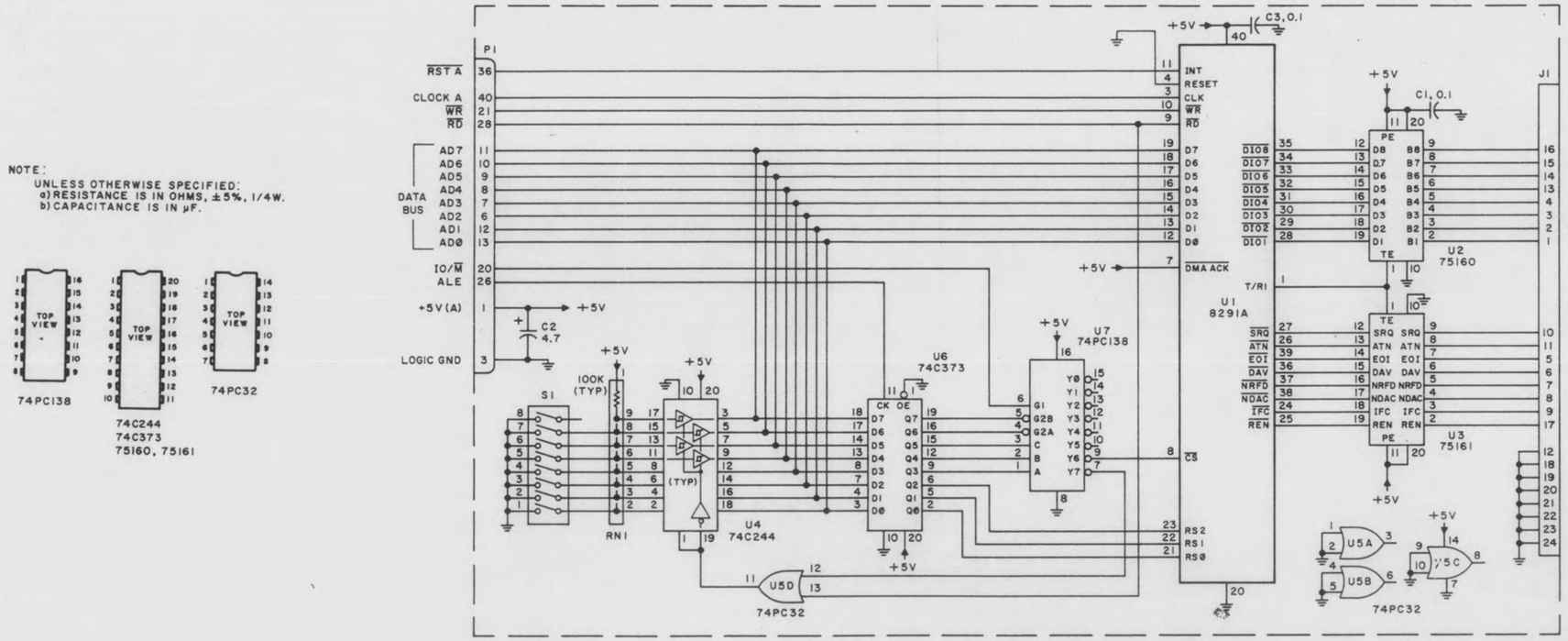
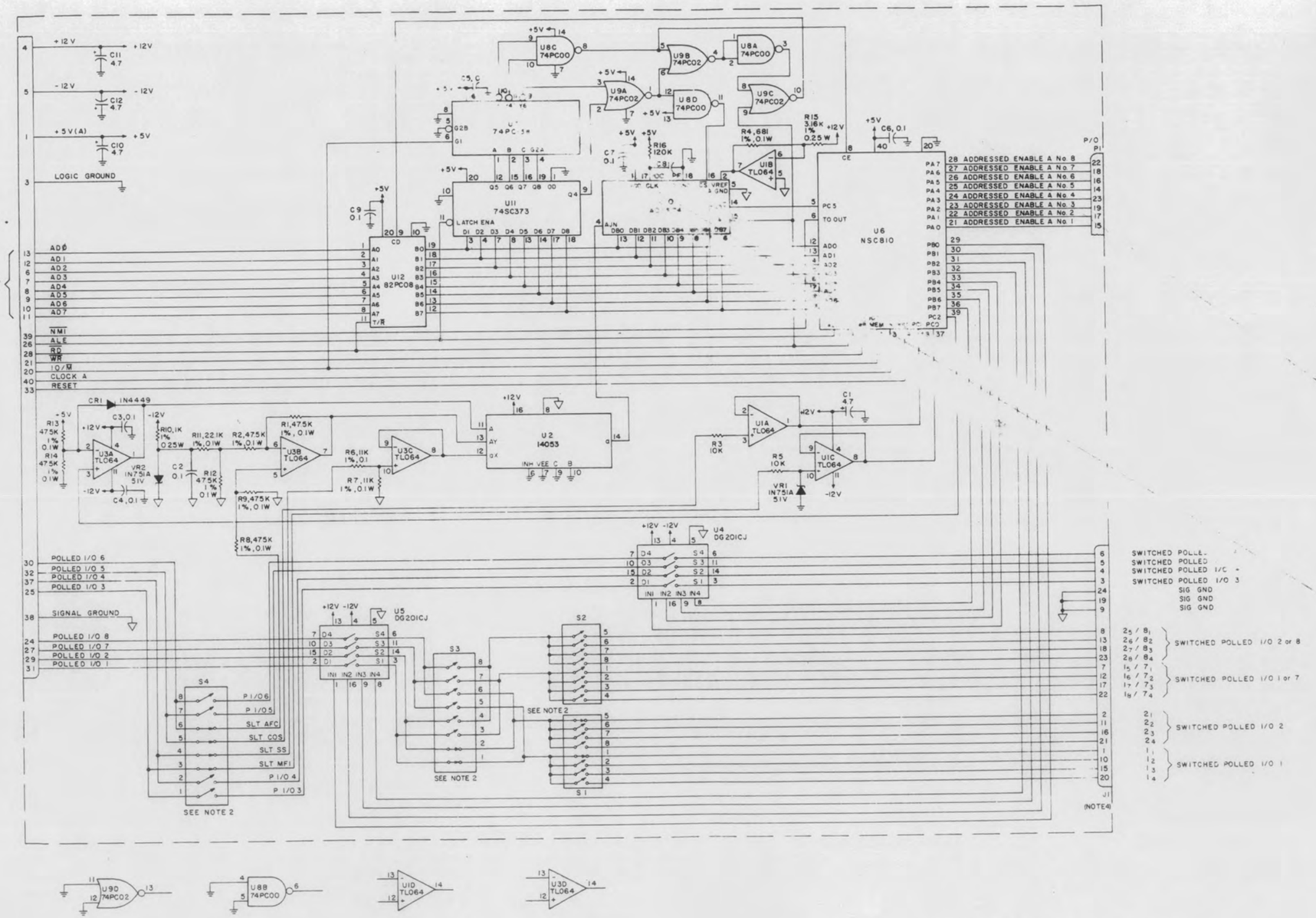


Figure 6-4. Type 794285-1, Digital I/O IEEE-488 (Option), (A1A1), Schematic Diagram 470493 (A)



NOTES

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, ±5%, 0.25W CAPACITOR VALUES ARE IN MICROFARADS
2. STANDARD SWITCH CONFIGURATION IS:
   S1 - POS 1 AND 5 NORMALLY CLOSED
   POS 2, 3, 4, 6, 7 AND 8 NORMALLY OPEN
   S2 - POS 1, 2, 3, 4, 5, 6, 7 AND 8 NORMALLY OPEN
   S3 - POS 1, AND 2 NORMALLY CLOSED
   POS 3, 4, 5, 6, 7 AND 8 NORMALLY OPEN
   S4 - POS 1, 2, 7 AND 8 NORMALLY OPEN
   POS 3, 4, 5 AND 6 NORMALLY CLOSED
   SYSTEM OR CUSTOMER CONFIGURATION OR APPLICATION MAY REQUIRE DIFFERENT SWITCH POSITION TO BE ENABLED
3. ⏚ INDICATES SIGNAL GROUND CONNECTION
4. DIFFERANCE BETWEEN TYPES, SEE TABULATION BLOCK.

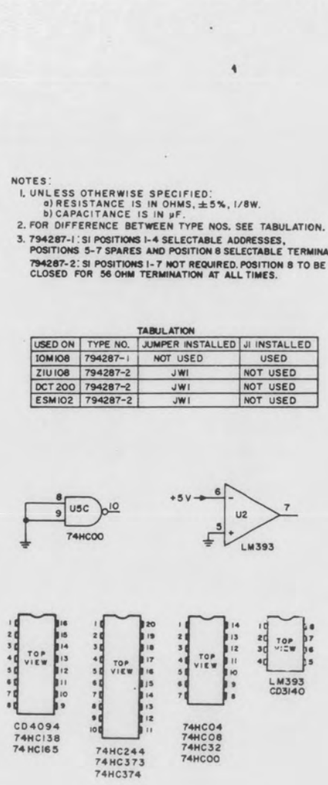
TYPE NO.	J1
794286-1	USED
794286-2	NOT USED

Figure 6-5. Type 794286-2, Bidirectional Polled I/O (A1A2), Schematic Diagram 570245 (D)

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN μF.
2. FOR DIFFERENCE BETWEEN TYPE NOS. SEE TABULATION.
3. 794287-1: SI POSITIONS 1-4 SELECTABLE ADDRESSES, POSITIONS 5-7 SPARES AND POSITION 8 SELECTABLE TERMINATION.
   794287-2: SI POSITIONS 1-7 NOT REQUIRED. POSITION 8 TO BE CLOSED FOR 56 OHM TERMINATION AT ALL TIMES.

TABULATION

USED ON	TYPE NO.	JUMPER INSTALLED	J1 INSTALLED
10M108	794287-1	NOT USED	USED
ZIU108	794287-2	JW1	NOT USED
DCT200	794287-2	JW1	NOT USED
ESM102	794287-2	JW1	NOT USED



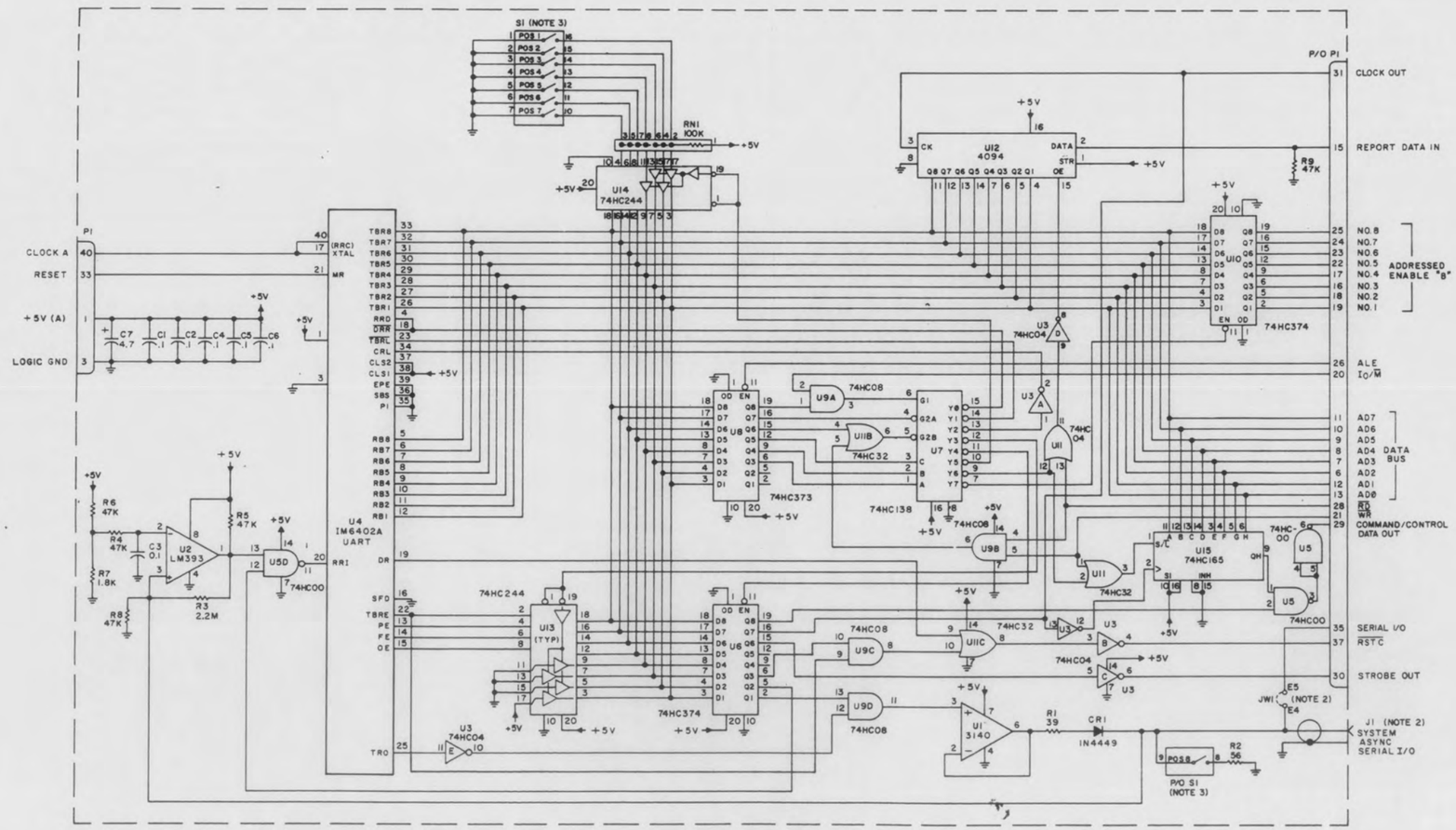


Figure 6-6. Type 794287-2, System I/O (A1A3), Schematic Diagram 570214 (F)

OTHERWISE SPECIFIED:
STANCE IS IN OHMS, ±5%, 1/8W.
ACITANCE IS μF.
ENCES BETWEEN DASH NUMBERS IS SHOWN IN ONE.

TABLE 1

R		U14	Y2	C9	C10	C17	J1	J2
		N/U	N/U	N/U	N/U	N/U	1,2	2,4
		AS SHOWN					1,2	2,4

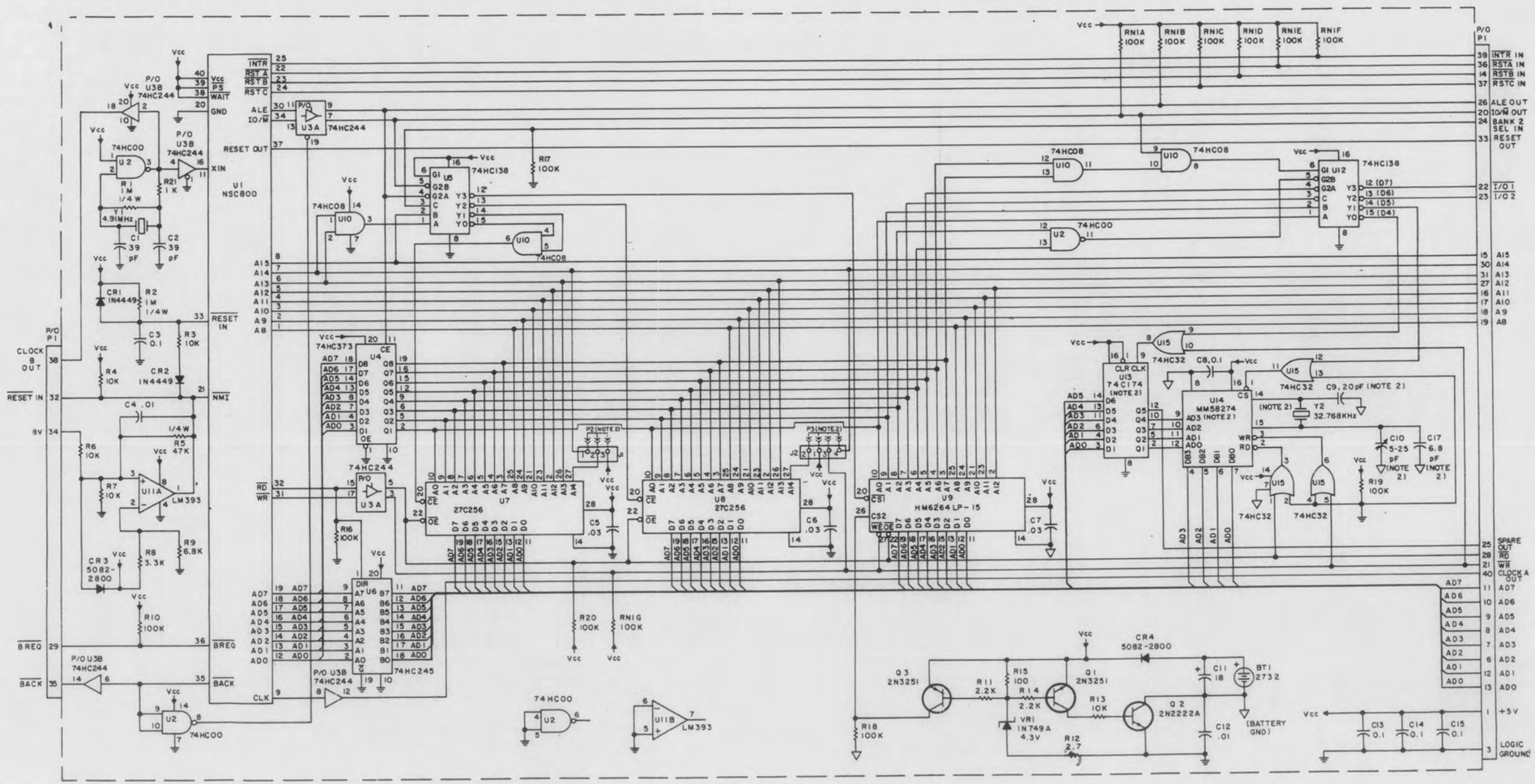


Figure 6-7. Type 794444-X, Extended CPU (A1A5), Schematic Diagram 570353 (D)

NOTE:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%.
   b) CAPACITANCE IS IN μF.
2. DIFFERANCE BETWEEN UNITS SEE TABULATION BLOCK.

	TITLE	IOM108 TYPE	SCHEM	IOM108-1 TYPE
XA1	DIGITAL I/O, RS-232/C	9040 DIO232	470494	NOT USED
(OPT 1)	DIGITAL I/O, IEEE 488	9040 DIO488	470493	NOT USED
XA2	BI-DIRECTIONAL POLLED I/O	794286-1	570245	794286-2
XA3	SYSTEM I/O	794287-1	570214	794287-2
XA4				
(OPT 2)	ANCILLARY DIGITAL	794289-1		794289-1
XA5	EXTENDER CPU	794444-1	570353	794444-1
(OPT 3)	EXTENDER CPU W/TIME & DATA	794444-2	570353	794444-2

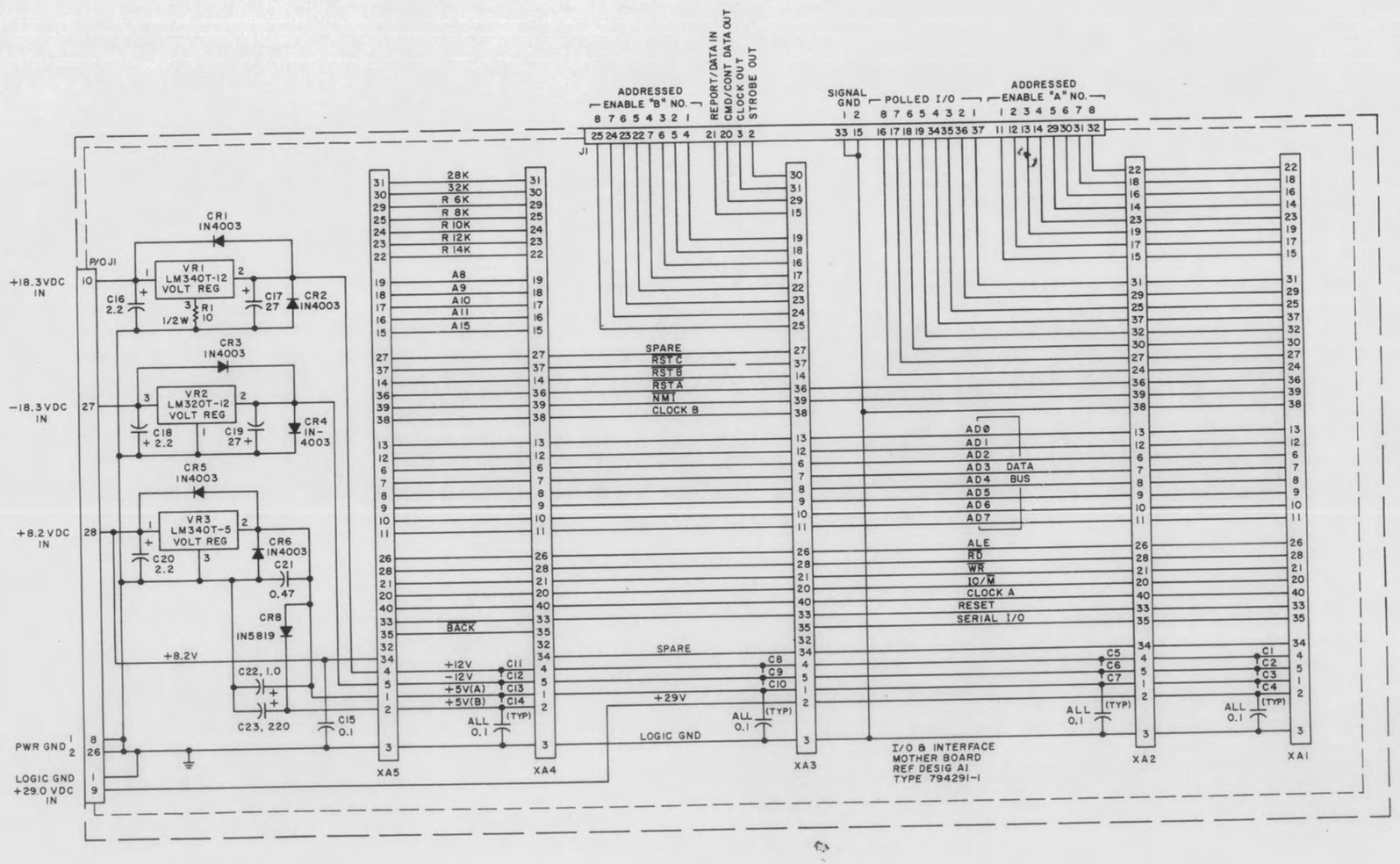


Figure 6-8. WJ-9040 IOM108-1, I/O Interface Module, Main Chassis Schematic Diagram 470497 (F)

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN µF.
   c) INDUCTANCE IS IN µH.
2. NOMINAL VALUE, FINAL VALUE FACTORY SELECTED (R15, R16 & R17).

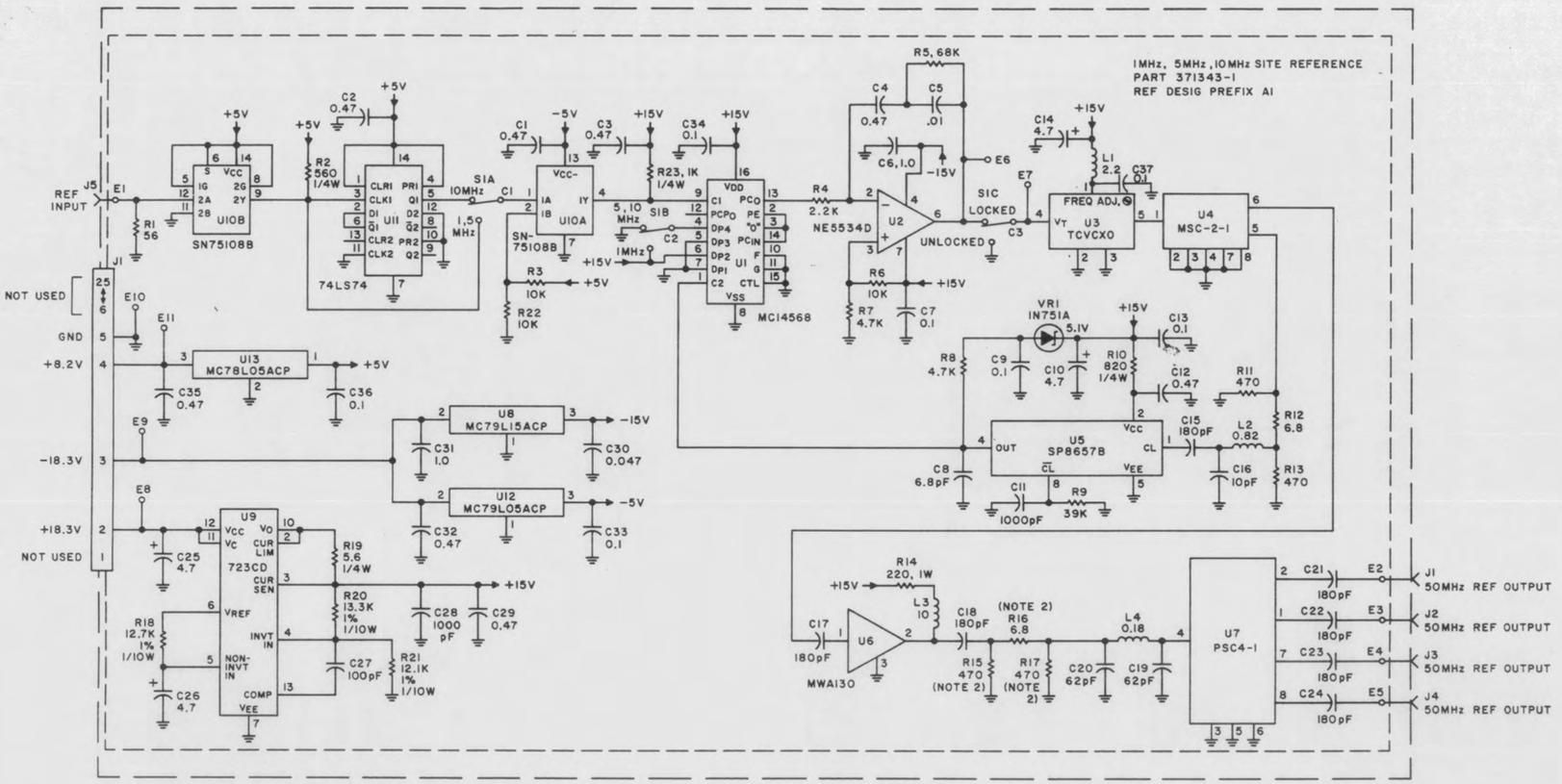


Figure 6-9. Type WJ-9040 SRM105A 1MHz, 5MHz, 10MHz Site Reference Module, Main Chassis, Schematic Diagram 471075 (B)