

# SUPPLEMENT <br> FOR THE <br> WJ-8770-1 <br> HF TRANSPORTABLE RECEIVER 

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04/81 1st Printing
08/82 2nd Printing

## WJ-8770-1 HF TRANSPORTABLE RECEIVER

## 1.1 <br> GENERAL

The WJ-8770-1 HF Transportable Receiver is virtually identical to the WJ-8770 model. There is but one basic difference, the ability of the WJ-8770-1 to accept power from a 24 Vdc battery pack.

### 1.2 FUNCTIONAL DESCRIPTION

The WJ-8770-1 differs physically from the WJ-8770 in that it has an additional power input plug on the rear panel, designated jack J8. As can be seen from the Main Chassis schematic, Figure 6-28, jack J8, when installed, ties to the input power line from the normal power input jack, J1. The battery pack supplies 24 Vdc for operations, falling well within the equipment's normal power requirements of $22-32 \mathrm{Vdc}$. There are no other wiring or physical differences between the two models. Figure $2-3$ shows the location of the battery power plug. A battery cover is available that provides a mounting for the battery and acts as a rear cover for the receiver.

## WJ-8770-1 HF Transportable Receiver

A discrepancy was found regarding the audio response measurement while testing the production of the WJ-8770-1. A different set of data sometimes resulted when the BFO had a positive or negative offset with the negative offset typically yielding an out of tolerance result for the upper 3 dB limit.

An investigation of the product detector linearity, BFO level and variation, audio roll-off etc. was conducted. Some product detectors were found to be oscillating at approximately 100 MHz . Proper product detector gain/frequency response was restored with the spurious oscillation suppressed giving symmetrical data well within specification.

The oscillation was suppressed by lowering the terminating resistor (A4A1A10 R52) on the product detector's carrier input from $1 \mathrm{k} \Omega$ to $100 \Omega$. The source resister (A5A4 R19) on the BFO module was reduced from $510 \Omega$ to $270 \Omega$ to restore the proper drive level.

Approximately 25 receivers were shipped prior to the incorporation of these changes, and will possibly have slightly reduced audio performance in the CW mode. Since most CW operators work in the $400-2000 \mathrm{~Hz}$ range, there should be no problem. The audio response in other reception modes is not affected by these changes.

If there is a problem relating to this in the field, and units are to be modified, there is no re-alignment or adjustments involved with the resistor changes.

The customer may modify the units if he determines the above problem exists or return the units to the factory for repair. If there are questions regarding this bulletin, contact your local Watkins-Johnson Company Representative or the factory directly.

### 1.1 GENERAL

The following paragraphs describe the changes incorporated into the WJ-8770 HF Transportable Receiver. The changes made improve the overall function and redesignate the equipment as the WJ-8770-1 HF Transportable Receiver.

The following paragraphs will describe the changes and if necessary illustrate the additions. The change descriptions start with the main chassis and proceed in reference designation sequence.

### 1.2 MAIN CHASSIS

1.2.1 In order to agree with the WJ-8770-1 HF Transportable Receiver Main Chassis, the following has been changed:

R4-FROM: Resistor, Fixed, Composition: 120 $2,5 \%, 1 / 4 \mathrm{~W}$ P/N RCR07G121JS
TO: $\quad$ Resistor, Fixed, Composition: $120 \mathrm{~K} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ P/N RCR07G124JS

R8 - FROM: Resistor, Fixed, Composition: $82 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ P/N RCR07G820JS
TO: Resistor, Fixed, Composition: 130 , 5\%, 1/4W P/N RCR07G131JS

S4 - FROM: Switch, Rotary, P/N 51530-01-2-GS
TO: Switch, Rotary, P/N 51530-01-2-GN
1.3 INPUT CONVERTER TYPE 796099 (A3)
1.3.1 The Type 796099 Input Converter has been changed to redistribute the power supply load from +15 Vde to -15 Vdc . The parts list changes are listed below.

| $\begin{gathered} \text { A1 - FROM: } \\ \text { TO: } \end{gathered}$ | 1st Mixer/1st IF Type 34748-3 <br> 1st Mixer/1st IF Type 370417-1 |
| :---: | :---: |
| $\begin{gathered} \text { A2 - FROM: } \\ \text { TO: } \end{gathered}$ | 2nd Mixer/2nd IF Type 34748-3 <br> 2nd Mixer/2nd IF Type 370417-1 |
| $\begin{gathered} \text { C1- FROM: } \\ \text { TO: } \end{gathered}$ | Capacitor, Ceramic, Feed-thru: $1000 \mathrm{pF}, \mathrm{GMV}, 500 \mathrm{~V}$ P/N 54-794-009-102W, Qty. 4 <br> Capacitor, Ceramic, Feed-thru: 1000 pF , GMV, 500 V P/N 54-794-009-102W, Qty. 3 |
| $\begin{gathered} \text { C3- FROM: } \\ \text { TO: } \end{gathered}$ | Same as C1 <br> Not Used |
| C5-ADD: | Capacitor, Ceramic, Dise: $2200 \mathrm{pF}, 5 \%, 100 \mathrm{~V}$ P/N 8131-100-COGO-222U, Qty. 1 |





Figure 1-1. Type 796099 Input Converter (A3) Schematic Diagram 470388
1.3.2 Refer to Figure 1-2 for Type 370417-1 1st Mixer/1st IF Location of Components. Paragraph 1.3.2.1 is the new Parts List. Figure 1-1 is the Schematic Diagram.


Figure 1-2. Type 370417-1, 1st Mixer/1st IF (A3A1) Location of Components

| 1.3.2.1 | Type $370417-1,1$ st Mixer/1st IF PC Assembly | REF DESIG PREFIX A3A1 |
| :--- | :--- | :--- | :--- |


| REF <br> DESIG | DESCRIPTION | $\begin{aligned} & \text { QTY } \\ & \text { PER } \\ & \text { ASS } \end{aligned}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Ceramic, Dise: 1000 pF GMV 500 V | 2 | B-GP1000PFP | 91418 |  |
| C2 | Same as C1 |  |  |  |  |
| C3 | Capacitor, Variable, Ceramic: $2.5-9 \mathrm{pF} 25 \mathrm{~V}$ | 1 | 518-000A2.5-9 | 72982 |  |
| CR1 | Diode | 1 | 1N4446 | 80131 |  |
| FL1 | Filter BP, 42.905 MHz CF 40 kHz BW | 1 | 92212 | 14632 |  |
| J1 | Connector, Receptacle | 2 | 34520-1 | 14632 |  |
| J2 | Same as J1 |  |  |  |  |
| L1 | Coil/Fixed $10 \mu \mathrm{H} 10 \%$ | 2 | 1537-36 | 99800 |  |
| L2 | Same as L1 |  |  |  |  |
| Q1 | Transistor | 1 | 2N2222A | 80131 |  |
| Q2 | Transistor | 1 | CP643 | 12498 |  |
| RA1 | Heatsink | 1 | 1118C | 13103 |  |
| R1 | Resistor, Fixed, Composition: $4.3 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G432JS | 81349 |  |
| R2 | Resistor, Fixed, Composition: $82 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G820JS | 81349 |  |
| R3 | Resistor, Fixed, Composition: 10ת, 5\%, 1/4 W | 1 | RCR07G100JS | 81349 |  |
| R4 | Resistor, Fixed, Composition: 150 1 , 5\%, 1/8 W | 1 | RCR05G151JS | 81349 |  |
| T1 | Transformer Assembly | 1 | 22295-52 | 14632 |  |
| U1 | Mixer/Balanced 2-500 MHz Double Bal | 1 | M9D | 27956 |  |

1.3.3 Refer to Figure 1-3 for Type 370591 2nd Mixer/2nd IF Location of Components. Paragraph 1.3.3.1 is the new Parts List.


Figure 1-3. Type 370591, 2nd Mixer/2nd IF (A3A2) Location of Components
1.3.3.1 Type 370591, 2nd Mixer/2nd IF Printed Wiring Assembly PREF DISG PREFIX A3A2

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSYY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Variable, Ceramic: $2.5-11 \mathrm{pF}, 305 \mathrm{~V}$ | 1 | 538-01182.5-11 | 72982 |  |
| C2 | Capacitor, Ceramic, Dise: $1000 \mathrm{pF}, \mathrm{GMV}, 500 \mathrm{~V}$ | 2 | B-GP1000PFP | 91418 |  |
| C3 | Same as C2 |  |  |  |  |
| C4 | Capacitor, Ceramic, Disc: . $01 \mu \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 5 | 34453-1 | 14632 |  |
| C5 | Same as C4 |  |  |  |  |
| C6 | Same as C4 |  |  |  |  |
| C7 | Same as C4 |  |  |  |  |
| C8 | Same as C4 |  |  |  |  |
| C9 | Capacitor, Ceramic, Dise: . $1 \mu \mathrm{~F}, 20 \% 50 \mathrm{~V}$ | 1 | 34475-1 | 14632 |  |
| C10 | Capacitor, Ceramic, Disc: 4.7 pF, PORM 0.25 pF 100 V | 1 | 8108-100-COHO-479C | 72982 |  |
| C11 | Capacitor, Mica, Dipped: $47 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM05ED470G03 | 81349 |  |
| C12 | Capacitor, Ceramic Disc: $470 \mathrm{pF}, 20 \%, 1000 \mathrm{~V}$ | 2 | BHD470-20PCT | 91418 |  |
| C13 | Same as C12 |  |  |  |  |
| C14 | Capacitor, Variable, Ceramic: $9 \mathbf{- 3 5} \mathrm{pF}, 350 \mathrm{~V}$ | 1 | 538-01109-35 | 72982 |  |
| C15 | Capacitor, Mica, Dipped: $91 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 2 | CM05FD910G03 | 81349 |  |
| C16 | Same as C15 |  |  |  |  |
| C17 | Capacitor, Mica, Dipped: $39 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM05ED390G03 | 81349 |  |
| C18 | Capacitor, Electrolytic, Tentalum: $100 \mu \mathrm{~F}, 20 \%, 20 \mathrm{~V}$ | 2 | 196D107X0020TE4 | 56289 |  |
| C19 | Same as C18 |  | * |  |  |
| CR1 | Diode HI Conductance PRV Silicon | 1 | 1N4446 | 80131 |  |
| CR2 | Diode $.040 \mathrm{pF} 1 / 4$ W Glass Hermetic Seal with Dumet Lead | 1 | 5082-3039 | 28480 |  |
| FB1 | Ferrite Bread | 3 | 56-590-65-4A | 02114 |  |
| FB2 | Same as FB1 |  |  |  |  |
| FB3 | Same as FB1 |  |  |  |  |
| FLI | Filter BP 10.7 MHz | 1 | 92211 | 14632 |  |
| L1 | Coil/Fixed $10 \mu \mathrm{H}$ 10\% | 4 | 1537-36 | 99800 |  |
| L2 | Same as L1 |  |  |  |  |
| L3 | Same as L1 |  |  |  |  |
| L4 | Coil Fixed $0.56 \mu \mathrm{H} 15 \%$ | 1 | 202-11 | 99848 |  |
| L5 | Same as L1 |  |  |  |  |
| L6 | Coil Fixed: $0.33 \mu \mathrm{H} 10 \%$ | 1 | 1537-04 | 99800 |  |
| L7 | Coil Fixed Mold: $1.8 \mu \mathrm{H}, 10 \%$ | 1 | 1537-18 | 99800 |  |
| L8 | Coil Fixed Mold: $.22 \mu \mathrm{H}, 10 \%$ | 2 | 1537-02 | 99800 |  |
| L9 | Coil Fixed Mold: . $47 \mu \mathrm{H}, 10 \%$ | 1 | 1537-06 | 99800 |  |
| L10 | Same as L8 |  |  |  |  |
| Q1 | Transistor | 1 | 2N2222A | 80131 |  |
| Q2 | Transistor | 1 | CP643 | 12498 |  |
| Q3 | Transistor | 3 | 2N5109 | 80131 |  |

PREF DISG PREFIX A3A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \hline \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | RECM VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Q4 | Same as Q3 |  |  |  |  |
| Q5 | Same as Q3 |  |  |  |  |
| RA1 | Heatsink | 1 | 1118 C | 13103 |  |
| R1 | Resister, Fixed, Composition: $4.3 \mathrm{~K}, 5 \% 1 / 4 \mathrm{~W}$ | 1 | RCR07G432JS | 81349 |  |
| R2 | Resister, Fixed, Composition: $82 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G820JS | 81349 |  |
| R3 | Resister, Fixed, Composition: 10ת, 5\%, 1/4 W | 3 | RCR07G100JS | 81349 |  |
| R4 | Resister, Fixed, Composition: $1.8 \mathrm{~K}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G182JS | 81349 |  |
| R5 | Resister, Fixed, Composition: 688, $5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G680JS | 81349 |  |
| R6 | Resister, Fixed, Composition: $3.3 \mathrm{~K}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G332JS | 81349 |  |
| R7 | Resister, Fixed, Composition: $2.2 \mathrm{~K}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G222JS | 81349 |  |
| R8 | Resister, Fixed, Composition: $1.0 \mathrm{~K}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G102JS | 81349 |  |
| R9 | Resister, Fixed, Composition: $200 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G201JS | 81349 |  |
| R10 | Same as R3 |  |  |  |  |
| R11 | Resister, Fixed, Composition: 47R, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G470JS | 81349 |  |
| R12 | Resister, Fixed, Composition: 4.7R,5\%, 1/4 W | 1 | RCR07G4R7JS | 81349 |  |
| R13 | Same as R5 |  |  |  |  |
| R14 | Resister, Fixed, Composition: $390 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G391JS | 81349 |  |
| R15 | Resister, Fixed, Composition: $3308,5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G331JS | 81349 |  |
| R16 | Resister, Fixed, Composition: 15ת,5\%, 1/4 W | 1 | RCR07G150JS | 81349 |  |
| R17 | Resister, Fixed, Composition: $2.0 \mathrm{~K}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G202JS | 81349 |  |
| R18 | Same as R8 |  |  |  |  |
| R19 | Same as R15 |  |  |  |  |
| R20 | Same as R3 |  |  |  |  |
| R21 | Resister, Fixed, Composition: $12 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G120JS | 81349 |  |
| R22 | Same as R9 |  |  |  |  |
| R23 | Resister, Fixed, Composition: 6.8R, 5\%, $1 / 4 \mathrm{~W}$ | 1 | RCR07G6R8JS | 81349 |  |
| T1 | Transformer Assembly | 1 | 22295-53 | 14632 |  |
| T2 | Transformer Assembly | 1 | 22295-54 | 14632 |  |
| T3 | Transformer Assembly | 1 | 22295-55 | 14632 |  |
| U1 | Mixer/Balanced $0.05-200 \mathrm{MHz}$ |  |  |  |  |

### 1.4 DEMODULATOR/AGC AMPLIFIER TYPE 796113 (A4A1A10)

1.4.1 The following components have been changed to upgrade the performance of this module:

R7-FROM: Resistor, Fixed, Composition: 100 , 5\% 1/4 W P/N RCR07G101JS QTY. 7
TO: $\quad$ Resistor, Fixed, Composition: 1000, $5 \% 1 / 4 \mathrm{~W}$ P/N RCR07G101JS QTY. 9

R29-FROM: Resistor, Fixed, Composition: $1.0 \mathrm{~K}^{\text {?, }} 5 \% 1 / 4 \mathrm{~W}$ P/N RCR07G102JS QTY. 5
TO: $\quad$ Resistor, Fixed, Composition: $1.0 \mathrm{~K} \Omega, 5 \% 1 / 4 \mathrm{~W}$ P/N RCR07G102JS QTY. 3

R52-FROM: Same as R29
TO: Same as R7
R54-FROM: Same as R29
TO: Same as R7
1.5 SYNTHESIZER MOTHERBOARD TYPE 796117 (A5)
1.5.1 The following component has been changed to upgrade the performance of this module:

$$
\begin{array}{cl}
\text { J2 - FROM: } & \text { Connector, Receptacle, P/N 1-87227-0 } \\
\text { TO: } & \text { Connector, Receptacle, P/N 2-87227-0 }
\end{array}
$$

## 1.6 <br> PHASE LOCK LOOP TYPE 796115 (A5A2A1)

1.6.1 The following components have been changed to upgrade the performance of this module.

| R1- FROM: | Resistor, Fixed, Composition: | $1.0 \mathrm{~K} \Omega, 5 \% 1 / 4 \mathrm{~W}$ |
| :---: | :--- | :--- |
|  | P/N RCR07G102JS QTY. 3 |  |

R9 - FROM: Same as R1<br>TO: Resistor, Fixed, Composition: 3900, 5\% 1/4 W<br>P/N RCR07G391JS

## $1.7 \quad$ VCO ASSEMBLY TYPE 796131 (A5A2A2A1)

1.7.1 The following components have changed to upgrade the performance of this module:

CR1 - FROM: $\quad$ Diode, P/N IN4446, QTY 3
TO: $\quad$ Diode, P/N BB109/Yellow, QTY 1
CR2 - FROM: Same as CR1
TO: $\quad$ Diode, P/N MPN3401, Qty 3
CR3- FROM: Same as CR1
TO: Same as CR2
CR4- FROM: Diode/Varicap, P/N BB109/Yellow
TO: Same as CR2
C1- FROM: Capacitor, Ceramic, Dise: 1000 pF , GMV, 500 V
P/N B-GP1000PFP QTY 13
TO: Capacitor, Ceramic, Dise: $1000 \mathrm{pF}, \mathrm{GMV}, 500 \mathrm{~V}$
P/N B-GP1000PFP QTY 12
Q2- FROM: Transistor, P/N 2N3251, QTY 2 TO: Transistor, P/N 2N3251, QTY 1

Q3 - FROM: Same as Q2
TO: Transistor, P/N 2N3906

## 1.8 <br> 2nd LO SYNTHESIZER TYPE 796107 (A5A3)

1.8.1 The following components have been changed to upgrade the performance of this module. Refer to Figure 1-4 for the new Location of Components.

C1 - FROM: Capacitor, Ceramic, Dise: $0.1 \mathrm{pF}, 10 \%, 50 \mathrm{~V}$
P/N 8121-050-X7R0-104K, QTY 14
TO: Capacitor, Ceramic, Dise: $0.1 \mathrm{pF}, 10 \%, 50 \mathrm{~V}$
P/N 8121-050-X7R0-104K, QTY 15
C25- FROM: Same as C1
TO: Same as C2
R9- FROM: Resistor, Fixed, Composition: $1.0 \mathrm{~K} \Omega, 5 \% 1 / 8 \mathrm{~W}$ P/N RCR05G102JS QTY. 5
TO: Resistor, Fixed, Composition: $1.0 \mathrm{~K} \Omega, 5 \% 1 / 8 \mathrm{~W}$ P/N RCR05G102JS QTY. 4

R70 - FROM: Same as R9
TO: Resistor, Fixed, Composition: $560 \Omega, 5 \%, 1 / 8 \mathrm{~W}$
P/N RCR05G561JS


Figure 1-4. Type 796107, 2nd LO Synthesizer (A5A3) Location of Components

U6 - $\quad$ FROM: $\quad$ Spacer/Hex, P/N 8213-55-0440-7
TO: IC, Divide by $20, \mathrm{P} / \mathrm{N}$ SP 8657 M

## $1.9 \quad$ BFO 3rd LO TYPE 796109 (A5A4)

1.9.1 The following components have been changed to upgrade performance of this module:

C12- FROM: Capacitor, Ceramic, Disc: .47pF, 20\%, 50V
P/N 34452-1, QTY 2
TO: Capacitor, Ceramic, Disc: . $47 \mathrm{pF}, 20 \%, 50 \mathrm{~V}$ P/N 34452-1, QTY 3

C18- FROM: Capacitor, Electrolytic, Tantalum: 100pF, 20\%, 20V
P/N 196D107XZ0020TE4, QTY 2
TO: $\quad$ Capacitor, Electrolytic, Tantalum: $100 \mathrm{pF}, 20 \%, 20 \mathrm{~V}$
P/N 196 D107X002TE4, QTY 1

```
C50- FROM: Same as C18
    TO: Same as C12
R19 - FROM: Resistor, Fixed, Composition: 510\Omega, 5%, 1/4W
    P/N RCR07G511JS
    TO: Resistor, Fixed, Composition: 270?,5% 1/4W
        P/N RCR07G271JS
```

$1.10 \quad$ AUDIO AMPLIFIER TYPE 796116 (A9)
1.10.1 The following components have been changed to upgrade the performance of this module:

```
R3 - FROM: . Resistor, Fixed, Film: 6.81K\Omega.1%, 1/10W P/N RN55C6811F
TO: Resistor, Fixed, Film: 68.1K \({ }^{\circ}\), 1\%, 1/10W P/N RN55C6812F
```

R7 - FROM: Resistor, Fixed, Film: 9.09K $, 1 \%, 1 / 10 \mathrm{~W}$ P/N RN55C9091F
Resistor, Fixed, Film: $90.9 \mathrm{~K} \Omega, 1 \%, 1 / 10 \mathrm{~W}$ P/N RN55C9092F
1.11 FRONT COVER ASSEMBLY WITH REMOVABLE SPEAKER TYPE 796140-2 (A11)
1.11.1 Refer to paragraph 1.11 .2 for the new Parts List. Figure 1-5 is the location of Components following the Parts List. Subassemblies follow (A11) in Reference Designation sequence:
(A11A1) - Speaker Amplifier Assembly, Type 796134-3
(A11A1A1) - Speaker Amplifier P.C. Assembly, Part 270784-1

ADDENDUM 1
30 July 1982
1.11.2 TYPE 796140-2, FRONT COVER ASSEMBLY w/REMOVABLE SPEAK ASSEMBLY REF DESIG PREFIX A11

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | $\left\|\begin{array}{c} \text { MFR. } \\ \text { CODE } \end{array}\right\|$ | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | Removable Speaker Assembly | 1 | 796134-3 | 14632 |  |

1.11.2.1 Type 796134-3, Removable Housing Assembly with Speak Ampl

REF DESIG PREFIX A11A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASS'Y } \end{array}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | Speaker Amplifier PC Assembly | 1 | 270784-1 | 14632 |  |
| LS1 | Speaker | 1 | 25A070T | 74199 |  |
| P1 | Plug Multipin | 1 | GC329 | 25330 |  |
| R1 | Resistor, Fixed, Composition: $50 \mathrm{~K}, 10 \%$, 1 W | 1 | 70A3N056L503A | 01121 |  |

ADDENDUM I
30 July 1982
1.11.2.2 Part 270784-1, Speaker Amplifier Printed Wiring Assembly REF DESIG PREFIX A11A1A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Electrolytic, Tantalum: $200 \mu \mathrm{~F}, 20 \%, 15 \mathrm{~V}$ | 3 | MTP207M015P1C | 76055 |  |
| C2 | Capacitor, Ceramic, Disc: . $05 \mu \mathrm{~F}, \mathrm{M} 20 \mathrm{P} 80,25 \mathrm{~V}$ | 1 | DFJ1 | 73899 |  |
| C3 | Same as C1 |  |  |  |  |
| C4 | Same as C1 |  |  |  |  |
| C5 | Capacitor, Ceramic, Disc: $0.47 \mu \mathrm{~F}, 20 \%, 100 \mathrm{~V}$ | 1 | 8131M100-651-474M | 72982 |  |
| R1 | Resistor, Fixed, Composition: 10ת, 5\%, 1/4 W | 1 | RCR07G100JS | 81349 |  |
| R2 | Resistor, Fixed, Composition: 510 , 5\%, 1/2 W | 1 | RCR20G511JS | 81349 |  |
| R3 | Resistor, Fixed, Composition: $7.5 \mathrm{~K}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G752JS | 81349 |  |
| U1 | Integrated Circuit | 1 | LM386N | 27014 |  |
| VR1 | Diode Zener 6.2 V | 1 | 1N4735 | 80131 |  |



Figure 1-5. Part 270784-1, Speaker Amplifier (A11A1A1)
Location of Components


Incorporate the information contained in this addendum into the Instruction Manual for WJ-8770-1 HF Transportable Receiver.

## PURPOSE OF ADDENDUM

The purpose of this addendum is to deseribe product improvement modifications. The modifications have been incorporated into the Type 796139-2 Power Supply (A10). The Type 796139-2 module supercedes the previously utilized Type 796139.

## A. TYPE 796139-2 POWER SUPPLY (A10), CIRCUIT DESCRIPTION

Refer to the Type 796139-2 Schematic Diagram, Figure 4, page 9 of this addendum.

The new power supply circuitry is located on the Type 794302-1 DC-DC Converter (A10A1). The Part 270990-1 Sense Circuit (A10A1A1) is plug-in mounted to the DC-DC Converter main printed circuit board. The Type 794302-1 module supercedes the previously utilized Type 796110.

Delete paragraph 3.6.9.1 in the WJ-8770-1 Instruction Manual and replace with the following.

### 3.6.9.1 Type 794302-1 DC-DC Converter (A10A1), Circuit Description

The Type 794302-1 is a pulse width modulation (PWM) regulated DC to DC Converter. It receives an input voltage of 22 to 32 Vdc from the receiver rear panel and provides regulated/current limited power supply outputs of $+5 \mathrm{Vdc},+15 \mathrm{Vde}$ and -15 Vde .

The +24 Vdc input is filtered and over-voltage regulated by series regulator Q4-VR1. Regulation of the +5 Vdc and $\pm 15$ Vdc supplies is provided by integrated circuits U1 and U2 respectively. Darlington switch Q1 provides current gain for the +5 Vdc supply. Darlington switch Q2 provides current gain for the $\pm 15$ Vde supply.

Current limiting (overload protection) of the +5 Vdc supply is provided by U1's internal current sensing circuitry. Current sensing amplifier Q3 provides current limiting of the $\pm 15$ Vde supply.

### 3.6.9.1.1 Series Voltage Regulator Q4, VR1

Integrated circuits U1 and U2 operate most efficiently when the input voltage is held in the +22 to +24 Vdc range. Q4, VR1 and their associated components make up a series regulator which keeps the input voltage to U1 and U2 from exceeding +24 Vde approximately. When the DC level at Q4's base attempts to exceed +24 Vdc , VR1 becomes clamped and maintains the +24 V de level for module input voltages in the +24 to +32 V de range.

### 3.6.9.1.2 Sense Circuit A1

Refer to the Part 270990-1 Schematic Diagram, Figure 5, page 10 of this addendum.

Sense Circuit A1 shuts down the DC-DC Converter if the module input level falls below approximately +22 Vdc. The input voltage is applied to A1 at input terminal E1. At input levels exceeding +22 Vde CR1 and CR2 clamp. The resulting current develops a positive voltage across R1, thereby driving Q1 and Q2 into saturation. This action keeps the collectors of Q1 and Q2 and therefore A1's E2 and E3 outputs, at 0 Vde.

When the DC input level drops below approximately +22 Vdc CR1 and CR2 no longer conduct. Q1 and Q2 are then turned off, resulting in a positive voltage at the A1 modules E2 and E3 outputs.

The Sense Circuit's E2 and E3 outputs are applied to the SHUT-DOWN inputs of U1 and U2 respectively. When the level at either of the SHUT-DOWN inputs exceeds approximately +0.7 Vde the corresponding IC becomes disabled, thereby avoiding excessive current due to under-voltage operation.

### 3.6.9.1.3 Pulse Width Modulators U1 and U2

U1 and U2 are regulating pulse width modulators (PWM) for the +5 Vdc and $\pm 15 \mathrm{Vdc}$ supplies respectively. Each provides pulse outputs utilized by the +5 Vde and $\pm 15$ Vde converter circuitry. Each also contains internal voltage regulation and current sensing (overload protection) circuitry.

Voltage regulation of both the +5 Vdc and $\pm 15 \mathrm{Vdc}$ supplies is accomplished in the same way. A sample of the supply output is applied to a precision voltage divider. The resistance values utilized in the voltage divider (R1-R2 for the +5 Vde supply, R10-R11-R12 for the $\pm 15$ Vde supply) are selected to establish a +2.5 Vdc level at the INV inputs of U1 and U2. Each IC's +5 Vdc reference voltage, $\mathrm{V}_{\mathrm{R}}$, is divided down in the same way to provide a +2.5 Vdc reference voltage at their NON INV inputs.

When the power supply load is increased the level at the INV input tends to decrease. At that time the PWM regulator increases the duty eycle of the pulses at its output, supplying more energy to the converter in order to maintain the proper supply output voltage level. When the INV input level tries to increase the pulse duty cycle decreases.

U1 and U2 each have an internal oscillator. The OSC outputs of U1 and U2 are connected. This synchronizes the operating frequency of the two devices at a frequency established by R5 and C6. The operating frequency is approximately 20 kHz .

### 3.6.9.1.4 +5 Vde Supply

U1's $C_{A}$ and $C_{B}$ outputs are summed and applied via $R 7$ to the base of Darlington switch Q1. Q1 provides the current gain necessary to drive a forward converter made up of CR1, L1 and their associated components.


Figure 1. Forward Converter Operation.

Figure 1 illustrates forward converter operation. When the switch representing Q1 is closed (Q1 on), current is passed directly to the load and energy is stored in the field around inductor L1. When the switch opens (Q1 off) the energy stored in L1's collapsing field reverses the inductor's polarity and forces CR1 into conduction. The arrows shown in Figure 1 illustrate current flow. It can be seen that even when Q1 is off energy continues to be supplied to the load because CR1 allows prolonged circulation of inductive current.

### 3.6.9.1.5 $\pm 15$ Vde Supply

U2's $E_{A}$ and $E_{B}$ outputs are summed and applied to the base of Darlington switch Q2. Q2's output is applied to the primary of transformer T1. T1 is wound by a special technique to minimize leakage inductance.

T1 is the transformer component of two separate full-wave rectifiers. CR2 and CR4 rectify the signal from T1's secondary, producing +15 Vdc. CR3 and CR5 rectify the signal from T1's secondary, producing -15 Vdc. Filters C13-L4-C2 and C12-L3-C3 remove residual 20 kHz components from the +15 and -15 Vdc supplies respectively.

Current sensing amplifier Q3 provides overload protection for the $\pm 15 \mathrm{Vde}$ supply. Excessive current through R14 and R15 will forward bias Q3 into saturation. This action grounds pin 9 of U2, thereby limiting the pulse duty cycle at U2's output.

## B. POWER SUPPLY TROUBLESHOOTING

Delete Table 4-4 in the WJ-8770-1 Instruction Manual and replace with Table A. Utilize Table A to isolate the cause of failure to one of the problem areas listed in the right-
hand column. Refer to the Power Supply circuit description and schematic diagrams to aid in additional signal tracing and fault isolation.

Table A. Troubleshooting Guide

| Test Point | Typical <br> DC Voltage | Possible Problem Area |  |
| :--- | ---: | :--- | :--- |
| TP1 | +24 | V | J1, Main Chassis Wiring |
| U1-15 | +24 | V | Q4, VR1 and associated components |
| U1-10 | 0 | $V$ | A1 |
| U2-10 | 0 | V | A1 |
| U1-2 | +2.5 | $V$ | U1 or voltage divider R3-R4 |
| U2-2 | +2.5 | V | U2 or voltage divider R8-R9 |
| TP2 | +5 | V | Q1, CR1 and associated components |
| TP3 | +15 | V | CR2, CR4, Q2, Q3 and associated components |
| TP4 | -15 | $V$ | CR3, CR5, Q2, Q3 and associated components |

## C. REPLACEMENT PARTS LISTS AND SCHEMATIC DIAGRAMS

The following are replacement parts lists and schematic diagrams for the Type 796139-2 Power Supply.

TYPE 794302-1 DC-DC CONVERTER
REF DESIG PREFIX A10A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | Sense Circuit | 1 | 270990-1 | 14632 |  |
| C1 | Capacitor, Electrolytic, Tentalum: $100 \mu \mathrm{~F}, 20 \%, 20 \mathrm{~V}$ | 4 | 196D107X0020TE4 | 56289 |  |
| C2 |  |  |  |  |  |
| Thru | Same as C1 |  |  |  |  |
| C4 |  |  |  |  |  |
| C5 | Capacitor, Ceramic, Dise: . $47 \mu \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 2 | 34452-1 | 14632 |  |
| C6 | Capacitor, Ceramic, Disc: $.01 \mu \mathrm{~F}, 5 \%, 100 \mathrm{~V}$ | 1 | 8131-100C0G0-103J | 72982 |  |
| C7 | Capacitor, Ceramic, Dise: . $01 \mu \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 6 | 34453-1 | 14632 |  |
| C8 | Same as C7 |  |  |  |  |
| C9 | Capacitor, Ceramic, Disc: $1000 \mathrm{pF}, \mathrm{GMV}, 500 \mathrm{~V}$ | 1 | B-GP1000PFP | 91418 |  |
| C10 | Capacitor, Electrolytic, Tantalum: $2.2 \mu \mathrm{~F}, 10 \%, 35 \mathrm{~V}$ | 1 | CS13BF225K | 81349 | 56289 |
| C11 | Capacitor, Ceramic, Disc: $0.1 \mu \mathrm{~F}, 20 \%, 100 \mathrm{~V}$ | 1 | 8131M100-651-104M | 72982 |  |
| C12 | Capacitor, Electrolytic, Tentalum: $27 \mu \mathrm{~F}, 10 \%, 35 \mathrm{~V}$ | 2 | 196D276X9035TE4 | 56289 |  |
| C13 | Same as C12 |  |  |  |  |
| C14 | Capacitor, Electrolytic, Tantalum: $27 \mu \mathrm{~F}, 10 \%, 35 \mathrm{~V}$ | 2 | CS13BF276K | 81349 | 56289 |
| C15 | Same as C14 |  |  |  |  |
| C16 |  |  |  |  |  |
| Thru | Same as C7 |  |  |  |  |
| C19 |  |  |  |  |  |
| C20 | Same as C5 |  |  |  |  |
| C21 | Capacitor, Electrolytic, Tantalum: $2.2 . \mu \mathrm{F}, 20 \%, 35 \mathrm{~V}$ | 1 | 196D225X00JE3 | 56289 |  |
| CR1 | Diode, Schottky: $40 \mathrm{~V}, 1 \mathrm{~A}$ | 1 | 1N5819 | 80131 | 04713 |
| CR2 | Diode | 4 | VHE240 | 21845 |  |
| CR3 |  |  |  |  |  |
| Thru | Same as CR2 |  |  |  |  |
| CR5 |  |  |  |  |  |
| CR6 | Diode | 1 | 1N4449 | 80131 | 93332 |
| J1 | Connector | 10 | 62073-1 | 00779 |  |
|  |  |  |  |  |  |
| Thru | Same as JI |  |  |  |  |
| J10 |  |  |  |  |  |
| L1 | Coil | 1 | 30314-13 | 14632 |  |
| L2 | Coil | 4 | 20681-228 | 14632 |  |
| L3 |  |  |  |  |  |
| Thru | Same as L2 |  |  |  |  |
| L5 |  |  |  |  |  |
| Q1 | Transistor | 1 | T1P117 | 01295 |  |
| Q2 | Transistor | 1 | T1P112 | 01295 |  |
| Q3 | Transistor | 1 | 2N3904 | 80131 | 04713 |
| Q4 | Transistor | 1 | 2N6121 | 80131 | 04713 |
| R1 | Resistor, Fixed, Film: $5.11 \mathrm{k} \Omega, 1 \%, 1 / 10 \mathrm{~W}$ | 8 | RN55C5111F | 81349 | 75042 |

REF DESIG PREFIX A10A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R2 |  |  |  |  |  |
| Thru | Same as R1 |  |  |  |  |
| R5 |  |  |  |  |  |
| R6 | Resistor, Fixed, Composition: $330 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G331JS | 81349 | 01121 |
| R7 | Resistor, Fixed, Composition: $2.0 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G202JS | 81349 | 01121 |
| R8 |  |  |  |  |  |
| Thru | Same as R1 |  |  |  |  |
| R10 |  |  |  |  |  |
| R11 | Resistor, Fixed, Film: $23.7 \mathrm{k} \Omega, 1 \%, 1 / 10 \mathrm{~W}$ | 2 | RN55C2372F | 81349 | 75042 |
| R12* | Same as R11 |  |  |  |  |
| R13 | Resistor, Fixed, Composition: $510 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G511JS | 81349 | 01121 |
| R14 | Resistor, Fixed, Wire wound: $.22 \Omega, 5 \%, 2 \mathrm{~W}$ | 4 | BWH0.22J | 75042 |  |
| R15  <br> Thru Same as 14 <br> R17  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
| R18 | Resistor, Fixed, Composition: $1.0 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G102JS | 81349 | 01121 |
| R19 | Resistor, Fixed, Composition: $4.3 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G432JS | 81349 | 01121 |
| R20 | Same as R18 |  |  |  |  |
| R21 | Resistor, Fixed, Composition: $100 \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G101JS | 81349 | 01121 |
| R22 | Resistor, Fixed, Composition: $82 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G823JS | 81349 | 01121 |
| T1 | Transformer | 1 | 370768-1 | 14632 |  |
| TP1 | Jack, Test Point, Red | 1 | TJ203R | 49956 |  |
| TP2 | Jack, Test Point, Orange | 1 | TJ2040R | 49956 |  |
| TP3 | Jack, Test Point, Blue | 1 | TJ207MB | 49956 |  |
| TP4 | Jack, Test Point, Violet | 1 | TJ210V | 49956 |  |
| U1 | Integrated Circuit | 2 | UC1524A | 61637 |  |
| U2 | Same as U1 |  |  |  |  |
| VR1 | Diode, Zener: $24 \mathrm{~V}, 1 \mathrm{~W}$ | 1 | 1N4749 | 80131 | 04713 |
| * | Nominal Value, Final Value Factory Selected |  |  |  |  |



Figure 2. Type 794302-1 DC-DC Converter, Location of Components.

Part 270990-1 Sense Circuit REF DESIG PREFIX A10A1A1

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CR1 | Diode, Zener: 15 V , Silicon | 1 | 1N965B | 80131 | 04713 |
| CR2 | Diode, Zener: 5.1 V , Silicon | 1 | 1N751A | 80131 | 04713 |
| Q1 | Transistor | 2 | 2N3904 | 80131 | 04713 |
| Q2 | Same as Q1 |  |  |  |  |
| R1 | Resistor, Fixed, Composition: $1.0 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G102JS | 81349 | 01121 |
| R2 | Resistor, Fixed, Composition: $4.7 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G472JS | 81349 | 01121 |
| R3 | Same as R2 |  |  |  |  |
| R4 | Resistor, Fixed, Composition: $39 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G393JS | 81349 | 01121 |
| R5 | Same as R4 |  |  |  |  |



Figure 3. Part 270990-1 Sense Circuit, Location of Components.


Type 796139-2 Power Supply (A|O)
Schematic Diagram


Part 270990 Sance Circuit (AIOAIAI) Schematic Diagram

# INSTRUCTION MANUAL 

FOR THE
WJ-8770

HF TRANSPORTABLE RECEIVER

```
    WATKINS-JOHNSON COMPANY
    700 QUINCE ORCHARD ROAD
GAITHERSBURG, MARYLAND 20878
```


## WARNING

This equipment employs voltages which are dangerous and may be fatal if contacted. Extreme caution should be exercised when working on this equipment with any protective covers removed.

## EQUIPMENT AND PROCEDURAL SAFETY

Equipment and procedural safety practices are paramount to both the user and manufacturer of this equipment. As a result, the following general guidelines are presented as a reminder to prevent possible injury and equipment damage.

1. Preventive and corrective maintenance on this equipment, with the protective covers removed and power applied, should be performed by skilled technicians familiar with this equipment.
2. With equipment power off and with the equipment power cord disconnected from a power source, there is a possibility that eapacitors in the equipment may still be charged.
3. Replace defective equipment power fuses with fuses of the same size and type which are both specified on the equipment and in this publication.

## TABLE OF CONTENTS

## SECTION I

## GENERAL DESCRIPTION

Paragraph Page
1.1 General ..... 1-1
1.2 Electrical Characteristics ..... 1-1
1.3 Mechanical Characteristics ..... 1-2
1.4 Equipment Supplied ..... 1-2
1.5 Equipment Required But Not Supplied. ..... 1-2
1.6 Type WJ-8770 HF Receiver Specifications ..... 1-2
SECTION II
INSTALLATION AND OPERATION
2.1 General. ..... 2-1
2.2 Receipt Inspection ..... 2-1
2.3 Unpacking, Inspection and Inventory ..... 2-1
2.4 Preparation for Reshipment and Storage ..... 2-1
2.5 Installation ..... 2-1
2.6 Input/Output Connections ..... 2-3
2.6.1 Antenna Input ..... 2-3
2.6.2 RF Input ..... 2-3
2.6.3 Power Input ..... 2-3
2.6.4 IF Output ..... 2-3
2.6 .5 SM Output ..... 2-3
2.6.6 Record Audio Output ..... 2-3
2.6.7 Phone Audio Output ..... 2-3
2.6.8 BCD Output ..... 2-4
2.7 Operation ..... 2-5
2.7.1 Power-On. ..... 2-5
2.7.2 Signal Strength ..... 2-5
2.7.3 RF Gain ..... 2-5
2.7.4 Detection Mode ..... 2-5
2.7.5 IF Bandwidth ..... 2-5
2.7.6 BFO Offset ..... 2-5
2.7.7 Tune Rate/Hz ..... 2-5
2.7.8 Tune ..... 2-6
2.7.9 Volume ..... 2-6
2.7.10 Level. ..... 2-6
2.7.11 Speaker Amplifier ..... 2-6

## TABLE OF CONTENTS (Cont'd)

## SECTION III

## CIRCUIT DESCRIPTION

Paragraph Page
3.1 General. ..... 3-1
3.1.1 Overall Description ..... 3-1
3.2 Receiver Section ..... 3-1
3.2.1 Functional Description ..... 3-1
3.2.2 Type $796123 \mathrm{DC}-30 \mathrm{MHz}$ Input Filter (A1) ..... 3-2
3.2.3 Type 796100 Input Preselector (A2) ..... 3-2
3.2.3.1 Type 791821-2 Digital Control ..... 3-2
3.2.3.2 Sub-Octave Filters ..... 3-4
3.2.4 Type 796099 Input Converter (A3) ..... 3-5
3.2.4.1 1 st Mixer/1st IF ..... 3-5
3.2.4.2 2nd Mixer/2nd IF ..... 3-5
3.2.5 Type 796120 IF Motherboard (A4) ..... 3-9
3.2.6 Type $79610110.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter (A4A1) ..... 3-13
3.2.7 IF Filters ..... 3-13
3.2.7.1 Type 72463-(XX) IF Filter (A4A2 through A4A5) ..... 3-13
3.2.7.2 Type 72463-17 LSB Filter (A4A6) ..... 3-16
3.2.7.3 Type 72463-18 USB Filter (A4A7) ..... 3-16
3.2.8 Type 796103455 kHz IF Amplifier ..... 3-16
3.2.9 Type 796102 Wide Band/Narrow Band IF Amplifier ..... 3-18
3.2.10 Type 796113 Demodulator/AGC Amplifier (A4A10) ..... 3-18
3.2.10.1 AM Detection Mode ..... 3-21
3.2.10.2 FM Detection Mode ..... 3-21
3.2.10.3 CW Detection Mode ..... 3-21
3.2.10.4 USB/LSB Detection Modes ..... 3-22
3.2.10.5 AGC Mode ..... 3-22
3.2.10.6 Manual Gain Mode ..... 3-22
3.2.11 Type 796116 Audio Amplifier (A9) ..... 3-23
3.3 Type 796106 Digital Control Unit (A6) ..... 3-23
3.3.1 AM, FM Detection Modes ..... 3-27
3.3.2 USB, LSB Detection Modes - BFO Zero ..... 3-31
3.3.3 CW Detection Modes - BFO Variable ..... 3-32
3.3.4 Preselector Decode ..... 3-34
3.4 Type 796105 Display Driver Assembly (A7) ..... 3-34
3.5 Type 796104 Display Assembly (A8). ..... 3-37
3.6 Synthesizer Section ..... 3-37
3.6.1 Synthesizer Relationships ..... 3-37
3.6.2 Phase Lock Loops ..... 3-40
3.6.2.1 General. ..... 3-40
3.6.2.2 Basic Phase Loek Loop ..... 3-42
3.6.2.3 Phase Lock Loop Prescaling Technique ..... 3-42
3.6.2.4 Phase Detector ..... 3-45
3.6.3 Type 796133 1st LO Synthesizer ..... 3-48

# TABLE OF CONTENTS (Cont'd) 

## SECTION III (Cont'd)

## CIRCUIT DESCRIPTION

Paragraph Page
3.6.3.1 Functional Deseription ..... 3-48
3.6.3.2 Circuit Description ..... 3-50
3.6.3.2.1 Counting Cycle ..... 3-50
3.6.3.2.2 Prescaler, U4 ..... 3-50
3.6.3.2.3 BCD Adders U9, U10, U11 and U12 ..... 3-50
3.6.3.2.4 Programmable Counter U5, U6 and U7 ..... 3-52
3.6.3.2.5 Swallow Counter, U8 ..... 3-52
3.6.3.2.6 Count Sequence ..... 3-52
3.6.4 Type 796107 2nd LO Synthesizer ..... 3-52
3.6.4.1 Functional Description ..... 3-52
3.6.4.2 Circuit Description. ..... 3-55
3.6.5 Type 796109 3rd LO Synthesizer ..... 3-57
3.6.5.1 Functional Description ..... 3-57
3.6.5.2 Circuit Deseription ..... 3-57
3.6.6 Type 796109 BFO Synthesizer ..... 3-59
3.6.6.1 Functional Description ..... 3-59
3.6.6.2 Circuit Description. ..... 3-59
3,6.6.2.1 Counting Cycle ..... 3-59
3.6.6.2.2 Prescaler, U12. ..... 3-61
3.6.6.2.3 Swallow Counter ..... 3-61
3.6.6.2.4 Programmable Counter ..... 3-61
3.6.6.2.5 End of Cycle Detector ..... 3-61
3.6.6.2.6 Count Sequence ..... 3-62
3.6.7 Type 796111 Time Base Generator ..... 3-62
3.6.7.1 Functional Description ..... 3-62
3.6.7.2 Circuit Description. ..... 3-64
3.6.8 Type 796117 Synthesizer Motherboard ..... 3-64
3.6.8.1 Circuit Deseription ..... 3-65
3.6.9 Type 796139 Power Supply ..... 3-65
3.6.9.1 Circuit Deseription. ..... 3-65
SECTION IV
MAINTENANCE
4.1 General. ..... 4-1
4.2 Test Equipment Required ..... 4-1
4.3 Test Facilities ..... 4-1
4.4 Preventative Maintenance ..... 4-1
4.4.1 Cleaning ..... 4-3
4.4.2 Lubrication ..... 4-3

## TABLE OF CONTENTS (Cont'd)

## SECTION IV (Cont'd)

## MAINTENANCE

Paragraph Page
4.4.3 Inspection for Damage or Wear ..... 4-4
4.5 Performance Tests ..... 4-4
4.5.1 General ..... 4-4
4.5.2 Minimum Performance Standards ..... 4-4
4.5.3 Procedure Guidelines ..... 4-5
4.5.4 Power-Up Test ..... 4-6
4.5.5 IF Gain Test ..... 4-6
4.5.6 Detection Mode Performance Test ..... 4-8
4.5.7 MAN/AGC Performance Test ..... 4-11
4.5.8 Frequency Tuning Performance Test ..... 4-13
4.6 Corrective Maintenance ..... 4-13
4.6.1 General ..... 4-13
4.6.2 Corrective Maintenance Guidelines ..... 4-13
4.7 Component Level Troubleshooting and Repair ..... 4-15
4.7.1 General ..... 4-15
4.7.2 Procedure Guidelines ..... 4-15
4.7.3 Power Supply Testing and Troubleshooting ..... 4-21
4.7.3.1 Pre-test Setup, ..... 4-21
4.7.3.2 Test Procedure ..... 4-21
4.7.4 Input Filter Testing and Troubleshooting ..... 4-21
4.7.4.1 Pre-test Setup. ..... 4-21
4.7.4.2 Test Procedure ..... 4-22
4.7.5 Preselector Testing and Troubleshooting ..... 4-22
4.7.5.1 Pre-test Setup ..... 4-22
4.7.5.2 Test Procedure ..... 4-23
4.7.6 Input Converter Testing and Troubleshooting ..... 4-23
4.7.6.1 Pre-test Setup. ..... 4-23
4.7.6.2 Test Procedure ..... 4-24
4.7.7 $\quad 10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Testing and Troubleshooting ..... 4-25
4.7.7.1 Pre-test Setup. ..... 4-25
4.7.7.2 Test Procedure ..... 4-25
4.7.8 IF Filter Testing and Troubleshooting ..... 4-26
4.7.8.1 Pre-test Setup ..... 4-26
4.7.8.2 Test Procedure ..... 4-26
4.7.9 $\quad 455 \mathrm{kHz}$ IF Amplifier Testing and Troubleshooting ..... 4-27
4.7.9.1 Pre-test Setup ..... 4-27
4.7.9.2 Test Procedure ..... 4-27
4.7.10 Wide/Narrow Filter Testing and Troubleshooting ..... 4-28
4.7.10.1 Pre-test Setup ..... 4-28
4.7.10.2 Test Procedure ..... 4-28
4.7.11 Demod/AGC Amplifier Testing and Troubleshooting ..... 4-29
4.7.11.1 Pre-test Setup ..... 4-29

# TABLE OF CONTENTS (Cont'd) 

## SECTION IV (Cont'd)

## MAINTENANCE

Paragraph ..... Page
4.7.11.2 Test Procedure ..... 4-29
4.7.12 Audio Amplifier Testing and Troubleshooting ..... 4-29
4.7.12.1 Pre-test Setup ..... 4-29
4.7.12.2 Test Procedure ..... 4-30
4.7.13 Digital Control Testing and Troubleshooting ..... 4-31
4.7.14 Display Driver/Assembly Testing and Troubleshooting ..... 4-32
4.7.15 Time Base Testing and Troubleshooting ..... 4-32
4.7.16 $\quad$ 1st LO Testing and Troubleshooting ..... 4-32
4.7.17 2nd LO Testing and Troubleshooting ..... 4-33
4.7.18 $\quad$ 3rd LO Testing and Troubleshooting ..... 4-35
4.7.19 BFO Testing and Troubleshooting. ..... 4-35
4.8 Alignment/Adjustment Procedures ..... 4-36
4.8.1 General. ..... 4-36
4.8.2 Input Converter Adjustment ..... 4-36
4.8.3 IF Gain Adjustment ..... 4-38
4.8.4 Synthesizer Alignment ..... 4-40
4.8.4.1 $\quad$ 1st LO Synthesizer Alignment ..... 4-40
4.8.4.2 2nd LO Synthesizer Alignment ..... 4-40
4.8.4.3 3 rd LO Synthesizer Alignment ..... 4-41
4.8.4.4 BFO Synthesizer Alignment ..... 4-41
4.8.4.5 Time Base Alignment ..... 4-42
SECTION V
REPLACEMENT PARTS LIST
5.1 Unit Numbering Method ..... 5-1
5.2 Reference Designation Prefix ..... 5-1
5.3 Parts List ..... 5-1
5.4 Assembly Revision Level ..... 5-2
5.5 List of Manufacturers ..... 5-2
SECTION VI
SCHEMATIC DIAGRAMS

# TABLE OF CONTENTS (Cont'd) 

## LIST OF ILLUSTRATIONS

Figure Page
1-1 WJ-8770 HF Receiver ..... 1-0
2-1 WJ-8770 Receiver, Critical Dimensions ..... 2-0
2-2 WJ-8770 Receiver, Front Panel View ..... 2-2
2-3 WJ-8770 Receiver, Rear Panel View ..... 2-2
3-1 WJ-8770 Receiver, Simplified Block Diagram ..... 3-0
3-2 Input Preselector Functional Block Diagram ..... 3-3
3-3 Input Converter Functional Block Diagram ..... 3-7
3-4 IF Motherboard Functional Block Diagram ..... 3-11
3-5 $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Block Diagram ..... 3-14
3-6 IF Filter Block Diagram. ..... 3-15
3-7455 kHz IF and WB/NB IF Amplifier Block Diagram3-17
3-8 IF Demodulator Block Diagram ..... 3-19
3-9 Digital Control Block Diagram ..... 3-25
3-10 Digital Control BFO Tuning ..... 3-29
3-11 Display Driver Block Diagram ..... 3-35
3-12 Basic Phase Lock Loop Configuration ..... 3-41
3-13 Programmable Phase Lock Loop ..... 3-43
3-14 Two-Modulus Prescaling in the Phase Loek Loop ..... 3-44
3-15 Two-Modulus Dividing Technique ..... 3-46
3-16 Phase Detector Timing Diagram ..... 3-47
3-17 1st LO Functional Block Diagram ..... 3-49
3-18 1st LO Counting Cycle ..... 3-51
3-19 2nd LO Functional Block Diagram ..... 3-54
3-20 3rd LO Functional Block Diagram ..... 3-58
3-21 BFO Functional Block Diagram ..... 3-60
3-22 Time Base Functional Block Diagram ..... 3-63
4-1 IF Gain Test . ..... 4-7
4-2 Detection Mode Performance Test ..... 4-9
4-3 MAN/AGC Performance Test ..... 4-12
4-4 Frequency Tuning Performance Test ..... 4-14
4-5
Troubleshooting Flowehart ..... 4-18
4-6
Input Converter Alignment ..... 4-37
4-7
IF Gain Adjustment ..... 4-39
5-1 WJ- 8770 HF Receiver, Front View, Location of Components ..... 5-8
5-2 WJ- 8770 HF Receiver, Rear View, Location of Components ..... 5-8
5-3
WJ-8770 HF Receiver, Top View, Location of Components ..... 5-11
5-45-5
Type 796123 Input Filter Assembly (A1), Location of Components ..... 5-18
Type 796112 Input Filter (A1A1), Location of Components ..... 5-20

## TABLE OF CONTENTS (Con'd)

## LIST OF ILLUSTRATIONS (Cont'd)

Figure Page
5-6 Type 796100 Input Preselector (A2), Location of Components ..... 5-22
5-7 Type 34936 Preselector Motherboard (A2A1), Location of Components ..... 5-26
5-8 Type 796016 Input Filter (A2A1A1), Location of Components. ..... 5-28
5-9 Type 791769 Input Filter (A2A1A2), Location of Components. ..... 5-32
5-10 Type 791770 Input Filter (A2A1A3), Location of Components. ..... 5-36
5-11 Type 791771 Input Filter (A2A1A4), Location of Components. ..... 5-42
5-12 Type 791722 Input Filter (A2A1A5), Location of Components. ..... 5-47
5-13 Type 791821-2 Digital Control (A2A1A6), Location of Components ..... 5-52
5-14 Type 796099 Input Converter (A3), Location of Components ..... 5-54
5-15Type 34748-3 1st Mixer/1st IF (A3A1), Location of Components5-56
5-16Type 796108 2nd Mixer/2nd IF (A3A2), Location of Components5-60
5-17 Type 796121 IF/Demodulator Assembly (A4), Location of Components ..... 5-66
5-18 Type 796120 IF Motherboard (A4A1), Location of Components ..... 5-68
5-19Location of Components5-71
5-20 Type 72463-17 through 22 IF Filter (A4A1A2 through A4A1A7), Location of Components ..... 5-75
5-21 Type 796103455 kHz IF Amplifier (A4A1A8), Location of Components ..... 5-95
5-22
Type 796102 WB/NB Filter (A4A1A9), Location of Components ..... 5-98
5-23
Type 796113 Demodulator/AGC Amplifier (A4A1A10),Location of Components5-102
5-24 Type 796117 Synthesizer Motherboard (A5), Location of Components .....  $5-114$
5-25 Type 796111 Time Base Generator (A5A1), Location of Components. ..... 5-118
5-265-27
5-285-295-305-31
5-32
5-335-345-35
Type 796133 1st LO Synthesizer (A5A2), Location of Components. .....  $5-120$
Type 796115 Phase Lock Loop (A5A2A1), Location of Components .....  5-122
Type 796132 VCO Assembly (A5A2A2), Location of Components .....  5-128
Type 796131 VCO P.C. Assembly (A5A2A2A1), Location of Components .....  $5-130$
Type 796107 2nd LO Synthesizer (A5A3), Location of Components ..... 5-136
Type 796109 BFO/3rd LO (A5A4), Location of Components ..... $.5-150$
Type 796106 Digital Control (A6), Location of Components ..... 5-160
Type 796105 Display Driver (A7), Location of Components. .....  $5-166$
Type 796104 Display P.C. Assembly (A8), Location of Components ..... 5-170
Type 796116 Audio Amplifier (A9), Location of Components .....  $5-172$
Type 796139 Power Supply Assembly (A10), Location of Components ..... 5-174
Type 796110 Power Supply P.C. Assembly (A10A1),
Location of Components ..... 5-177
5-180
Assembly (A11), Location of Components5-182
5-40 ..... 5-184Type 796134-1 Speaker Amplifier Assembly (A11A1),Location of Components

## TABLE OF CONTENTS (Cont'd)

## LIST OF ILLUSTRATIONS (Cont'd)

Figure Page
6-1 Type 796123 Input Filter (A1), Schematic Diargram ..... 6-3
6-2 Type 796100 Input Filter (A2), Schematic Diagram ..... 6-5
6-3 Type $7960165-750 \mathrm{kHz} / 0.75-1.1 \mathrm{MHz}$ Filter (A2A1A1),Schematic Diagram6-7
6-4 Type 791769 Input Preselector Filter (A2A1A2), Schematic Diagram ..... 6-9
6-5 Type 791770 Input Preselector Filter (A2A1A3), Schematic Diagram ..... 6-11
6-6
Type 791771 Input Preselector Filter (A2A1A4), Schematic Diagram ..... 6-13
Type 791772 Input Preselector Filter (A2A1A5), Schematic Diagram ..... 6-15
6-8
Type 791821-2 Input Preselector Digital Control (A2A1A6),Schematic Diagram6-17
6-9 Type 796099 Input Converter (A3), Schematic Diagram ..... 6-19
6-10 Type 796121 IF/Demodulator (A4), Schematic Diagram, ..... 6-21Type $796101 \quad 10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter (A4A1A1),Schematic Diagram6-23
6-12 Type 72463 IF Filters (A4A1A2-A4A1A7), Schematic Diagram ..... 6-25
6-13 Type 796103455 kHz IF Amplifier (A4A1A8), Schematic Diagram ..... 6-27
6-14 Type 796102 WB/NB Amplifier (A4A1A9), Schematic Diagram ..... 6-29Type 796113 Demodulator/AGC Amplifier (A4A1A10),Schematic Diagram6-31
6-16 Type 796117 Synthesizer Motherboard (A5), Schematic Diagram ..... 6-33
6-17 Type 796111 Time Base Generator (A5A1), Schematic Diagram . ..... 6-35
6-18 Type 796133 1st LO/Synthesizer (A5A2), Schematic Diagram ..... 6-37
6-19 Type 796132 VCO Assembly (A5A2A2), Schematic Diagram ..... 6-39
6-206-216-226-23Type 796107 2nd LO Synthesizer (A5A3), Schematic Diagram6-41
6-24Type 796109 BFO/3rd LO Synthesizer (A5A4), Schematic Diagram6-43
6-25Type 796106 Digital Control (A6), Schematic Diagram6-45
Type 796105 Display Driver (A7), Schematic Diagram ..... 6-47Type 796104 Display Board (A8), Schematic Diagram6-49
6-26
6-26Type 796116 Audio Amplifier (A9), Schematic Diagram6-51
6-27Type 796139 Power Supply (A10), Schematic Diagram6-53
6-28
Type 796134-1 Speaker Amplifier (A11), Schematic Díagram ..... 6-55
Type WJ-8770 HF Transportable Receiver (Main Chassis), Schematic Diagram ..... 6-57
LIST OF TABLES
Table
Page
1-1 Type WJ-8770 HF Receiver Specifications ..... 1-3
2-1 BCD Output Lines Identification ..... 2-4

## TABLE OF CONTENTS (Cont'd)

## LIST OF TABLES (Cont'd)

Table ..... Page
3-1 Tuned Frequency to U1 Output Conversion ..... 3-4
3-2 Display Driver Input to Output Relationships ..... 3-37
3-3 Display Input to Segment Relationships ..... 3-38
3-4 1st and 2nd LO Tuning Increments ..... 3-39
3-5 1st and 2nd LO Frequencies Versus Tuned Frequency ..... 3-40
3-6 Receiver's Phase Lock Loop Characteristics ..... 3-45
3-7
1st LO Divider Countdown Cycles ..... 3-53
4-1 Test Equipment Required ..... 4-2
4-2 Periodic Maintenance Schedule ..... 4-2
4-3 Receiver Minimum Performance Standards ..... 4-5
4-4 Power Supply Voltage Level Checks ..... 4-21
4-5 Preselector Filter Parameters ..... 4-23
4-6 Input Converter Signal Level Cheeks ..... 4-24
4-7 $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Signal Level Checks ..... 4-25IF Filter Signal Level Checks4-26
4-9455 kHz IF Amplifier Signal Level Cheeks4-27
4-10 WB/NB Filter Signal Level Checks ..... 4-28
4-11 Demod/AGC Amplifier Signal Level Checks ..... 4-30
4-12 Audio Amplifier Signal Level Checks ..... 4-31
4-13 Time Base Parameters ..... 4-32
4-14 VCO Band Select Code ..... 4-33
4-15 VCO Alignment Procedures ..... 4-40
5-1 Parts List Addendum A ..... 5-185


Figure 1-1. WJ-8770 HF Receiver

## SECTION I

## GENERAL DESCRIPTION

### 1.1 GENERAL

This section contains a general deseription of the Watkins-Johnson 8770 HF Transportable Receiver, hereafter referred to as the WJ-8770 HF Receiver or, the Receiver. Included in this section are electrical and mechanical characteristics; equipment supplied; equipment required, but not supplied and a receiver specification table for the WJ-8770 HF Receiver.

### 1.2 ELECTRICAL CHARACTERISTICS

The WJ-8770 HF Receiver, Figure 1-1, is designed to receive AM, FM, CW, USB, and LSB emissions over the frequency range of 5 kHz to 30.00000 MHz . The tuning knob, along with the multi-position TUNE RATE/Hz switch, provide a choice of four tuning rates; 10 Hz , $100 \mathrm{~Hz}, 1 \mathrm{kHz}$, or 10 kHz . The selected frequency, to a resolution of 10 Hz , is displayed via the seven digit LED FREQ MHz display. The TUNE RATE/Hz switch also provides selection of a LOCK position, which prevents accidental operator frequency changes, and a BFO position which, along with the BFO OFFSET switch, provides either a fixed or variable BFO offset frequency for use in the CW detection mode.

Other operator selectable parameters, in addition to the operating modes, are IF Bandwidths and Gain Mode. Selectable IF bandwidths of $1 \mathrm{kHz}, 4 \mathrm{kHz}, 8 \mathrm{kHz}$, and 16 kHz operate in conjunction with the AM, FM, or CW detection modes. When USB or LSB detection modes are selected, IF bandwidth selection is disabled by the DETECTION MODE switch. RF gain is controlled by the RF GAIN switch in either the variable manual mode or AGC mode. The intensity of LED FREQ MHz display is adjusted by varying the position of the DISPL INTENSITY control.

Other front panel features include the antenna (ANT) mounting/connection and its associated coax and connector to the RF input (RF INPUT) connector; a received signal strength (SIGNAL STR) meter; the signal monitor (SM OUTPUT), the intermediate frequency (IF OUTPUT), and BCD OUTPUT connectors; and the RECORD and PHONES output connectors.

The RECORD and PHONES output connectors provide the qudio outputs from the Receiver. The RECORD output is a multipin connector which can be connected to either a recorder or to the speaker located in the front cover assembly. The PHONES output is a singleended output which can be used to drive a headset.

Power input for the Receiver is via a rear panel mounted connector, J1, which accepts a $22-32$ Vde input.

## 1.3 <br> MECHANICAL CHARACTERISTICS

The Receiver is compatible for use with WJ-8640/MT Mounting Trays with shock mount. It is 11.38 inches ( 28.90 cm ) wide by 4.26 inches ( 10.82 cm ) high and is 18.67 inches ( 47.42 cm ) deep including front cover assembly. The Receiver is constructed of aluminum with the overall weight of a complete Receiver being approximately 19.57 pounds $(8.88 \mathrm{Kg}$ ). All operating controls, indicators, and connectors (excluding the rear panel mounted power input connector, J1) are on the Receiver front panel.

The VOLUME, RF GAIN, TUNE, and DISPL INTENSITY controls each have a different shape and color to aid in their identification under minimal or adverse lighting conditions. The BFO SELECT; IF BANDWIDTH; AM, FM, CW, USB, LSB; and TUNE RATE/Hz select switches all have the same shape and color but are easily identified by their relative proximity to each other and the other front panel controls.

### 1.4 EQUIPMENT SUPPLIED

The equipment supplied consists of the WJ-8770 HF Receiver.

### 1.5 EQUIPMENT REQUIRED BUT NOT SUPPLIED

Select equipment from the following general classifications to obtain full use of the WJ-8770 HF Receiver.

1. Antenna, $50 \Omega$
2. Audio monitoring equipment such as the following, if the speaker amplifier contained in the Type 796140 Front Cover Assembly is not used:
a. Headphones, $600 \Omega$
b. Tape recorder, $600 \Omega$
1.6 TYPE WJ-8770 HF RECEIVER SPECIFICATIONS

Table 1-1 lists the specifications and electrical characteristics of the WJ-8770 HF Receiver.

Table 1-1. Type WJ-8770 HF Receiver Specifications

| Tuning Range | 5 kHz to 30.00000 MHz |
| :---: | :---: |
| Tuning Resolution | 10 Hz |
| Antenna Conducted Oscillator Radiation | -87 dBm , maximum |
| Antenna Input Protection | The antenna input will withstand the effects of RF power to +27 dBm and static build-up. The protection circuit automatically resets. |
| Input Impedance | 50 ohms, unbalanced, nominal |
| IF Bandwidths ( 3 dB ) | Standard: $1,4,8$ and 16 kHz |
|  | Optional: $0.5,2,6$ or 12 kHz |
| IF Shape Factor (Typical) | IF BW $\quad 50 \mathrm{~dB}: 3 \mathrm{~dB}$ |
|  | 1 kHz 5:1 |
|  | 4 kHz 3:1 |
|  | 8 kHz 3:1 |
|  | 16 kHz 2:1 |
| Detection Modes | Standard: FM, AM, CW, USB and LSB |
| Gain Control Modes | Manual, AGC |
| AGC and Manual Range | 90 dB , minimum |
| AGC Threshold | 3.0 microvolt, typical |
| AGC Attack Time | 15 ms , maximum |
| AGC Release Time | AGC: 100 ms , maximum |
| Frequency Display | 7 digit red LED |
| Frequency Resolution/Readout | $10 \mathrm{~Hz}_{-6}$ |
| Frequency Stability: with time | $2 \times 10^{-6}$ per year |
|  | $1.5 \times 10^{-6}$ |
| Synthesized BFO | $\pm 8.0 \mathrm{kHz}$ in 100 Hz steps |
| IF Rejection | Greater than 90 dB |
| Image Rejection | Greater than 90 dB |
|  |  |
| Sensitivity: $(0.2-30 \mathrm{MHz}$, see CW Sensitivity for extended |  |
| frequency range) |  |
| ( 4 kHz IF Bandwidth) | at a 400 Hz rate will produce at least a $10 \mathrm{~dB}(\mathrm{~s}+\mathrm{n}) / \mathrm{n}$ ratio at the audio output. |
| FM Sensitivity ( 16 kHz IF Bandwidth) | A 3.2 microvolt signal FM modulated at a 400 Hz rate with a 4.8 kHz peak deviation will produce at least a 17 dB $(\mathrm{s}+\mathrm{n}) / \mathrm{n}$ ratio at the audio output. |
| CW Sensitivity |  |
| $200 \mathrm{kHz}-30 \mathrm{MHz}$ |  |
|  | least $16 \mathrm{~dB}(\mathrm{~s}+\mathrm{n}) / \mathrm{n}$ ratio at the audio output. |
| $50 \mathrm{kHz}-200 \mathrm{kHz}$ | A 1.8 microvolt signal will produce at |
|  | least $16 \mathrm{~dB}(\mathrm{~s}+\mathrm{n}) / \mathrm{n}$ ratio at the audio output. |

Table 1-1. Type WJ-8770 HF Receiver Specifications (Cont'd)

| $15 \mathrm{kHz}-50 \mathrm{kHz}$ | A 7.1 microvolt signal will produce at least a $16 \mathrm{~dB}(\mathrm{~s}+\mathrm{n}) / \mathrm{n}$ ratio at the audio output. |
| :---: | :---: |
| $5 \mathrm{kHz}-15 \mathrm{kHz}$ | A 128 microvolt signal will produce a $16 \mathrm{~dB}(\mathrm{~s}+\mathrm{n}) / \mathrm{n}$ ratio, typically at the audio output. |
| USB, LSB Sensitivity | A 0.7 microvolt signal will produce a $10 \mathrm{~dB}(\mathrm{~s}+\mathrm{n}) / \mathrm{n}$ ratio at the audio output. |
| IF Output | $455 \mathrm{kHz}, 20 \mathrm{mV}$, minimum, at 3 microvolt input level. |
| Signal Monitor Output | 455 kHz , center frequency, 30 kHz bandwidth. |
| Intermodulation Distortion: Widh. |  |
| 3rd Order Input Intercept Point | +17 dBm , minimum for signals separated by 40 kHz minimum. |
| Audio Phones Amplifier Response | Within 3 dB from 250 to 4000 Hz |
| Audio Phones Power | 2.5 mW into 600 ohms |
| Record Amplifier Response | Within 3 dB from 20 Hz to 16 kHz |
| Record Output Level | 1.0 Vrms across 600 ohms |
| Audio Distortion: |  |
| Record or Phones Output | Less than 5\% total Harmonic Distortion in AGC Slow or Manual Gain Modes. |
| Ultimate Signal-to-Noise Ratio | 40 dB minimum in AM or FM |
| Meter | Signal Strength |
| Environmental Conditions: |  |
| Temperature, Operating | $-20^{\circ}$ to $+60^{\circ} \mathrm{C}$ |
| Temperature, Non-Operating | $-40^{\circ}$ to $+70^{\circ} \mathrm{C}$ |
| Altitude, Operating | 35,000 feet ( 10.67 km ) |
| Altitude, Non-Operating | 50,000 feet ( 15.24 km ) |
| Humidity | 98\% (spray proof construction) |
| Power Consumption | Approximately 0.6 amps at 28 Vde |
| Power Requirements | 22 to 32 Vdc |
| Size | 4.2 inches ( 10.82 cm ) high, |
|  | 11.38 inches ( 28.90 cm ) wide, |
|  | and 18.67 inches ( 47.42 cm ) deep |
| Weight | Approximately $20 \mathrm{lbs} .(9.07 \mathrm{~kg}$ ) |

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Figure 2-1. WJ-8770 Receiver, Critical Dimensions

## SECTION II

## INSTALLATION AND OPERATION

### 2.1 GENERAL

This section includes information on receipt inspection, unpacking, installation and operation of the WJ- 8770 HF Receiver. Also included are details of preparation for storage and shipment.

### 2.2 RECEIPT INSPECTION

Inspect the shipping container for obvious damage. If the shipping container is damaged, attempt to have the carrier's agent present while the contents of the container are unpacked, checked for completeness, and the equipment inspected for mechanical damage. If it is not feasible to have the carrier's agent present, retain the damaged shipping container and equipment padding for the carrier's inspection.

### 2.3 UNPACKING, INSPECTION AND INVENTORY

The equipment was thoroughly inspected and adjusted for optimum performance prior to packing for shipment. It should be, therefore, ready for use upon receipt. After unpacking, inventory the equipment against the packing slip. Contact Watkins-Johnson Company, Gaithersburg, Maryland, or your Watkins-Johnson representative with details of any shortage.

Visually inspect all exterior surfaces for dents and scratches. If external damage is visible, remove the receiver from its case and inspect the internal components for apparent damage. Then check the internal cables for loose connections and plug-in items such as printed wiring boards, which may have been loosened from their receptacles.

### 2.4 PREPARATION FOR RESHIPMENT AND STORAGE

If the receiver must be prepared for reshipment, the packaging materials should follow the pattern established in the original shipment. If retained, the original materials can be reused to a large extent or will at a minimum provide guidance for the repackaging effort. Conditions during storage and shipment should normally be limited as follows:

Maximum humidity: 98\%
Temperature Range: $-40^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$

## 2.5 <br> INSTALLATION

The receiver is designed with carrying handles for ease of handling and mounting. Normally, the receiver will be mounted on the WJ-8640/MT Mounting Trays or similar permanent mounting apparatus. Receiver critical dimensions are shown in Figure 2-1. If the receiver is to be mounted in the presence of other equipment, adequate clearance should be provided for cables and other ancillary items required by the receiver, Ventilation of the receiver is not normally required unless it is operated in the proximity of heat-producing equipment.


Figure 2-2. WJ-8770 Receiver, Front Panel View


Figure 2-3. WJ-8770 Receiver, Rear Panel View

Manual transportation of the receiver should not be attempted without adequate support such as carrying straps.

### 2.6 INPUT/OUTPUT CONNECTIONS

Figures 2-2 and 2-3 are photographs of the front and rear panels showing the locations of the input and output connectors. Described below are the functions and input/output parameters of each connector.

### 2.6.1 ANTENNA INPUT

This single terminal block provides the necessary electrical and mechanical connections for a direct antenna input to the receiver.

### 2.6.2 RF INPUT

This BNC connector is the RF signal input for the receiver. Nominal input impedance is $50 \Omega$. The input is protected against signals exceeding +27 dbm ( 5 Vrms ) and static build-up.

### 2.6.3 POWER INPUT

This connector provides power to the receiver from a $22-32$ Vdc power source.

IF OUTPUT
This BNC connector supplies a bandwidth-limited 455 kHz IF output signal. The level will be 20 mV , minimum, into $50 \Omega$ in AGC mode, for RF input signals greater than $3 \mu \mathrm{~V}$.

### 2.6.5 SM OUTPUT

This BNC connector provides a broad-band 455 kHz IF output signal suitable for driving a signal monitor. The signal occupies a 30 kHz bandwidth at a signal level approximately 25 dB above the receiver input level.

### 2.6.6 RECORD AUDIO OUTPUT

This connector provides wide-band, unbalanced audio at a level of 1.0 V rms across $600 \Omega$. Also available is +15 Vdc for powering ancillary equipment.

### 2.6.7 PHONE AUDIO OUTPUT

This output is intended to drive a $600 \Omega$ or greater headphone set. Narrowband audio is available at a level of 2.5 mW into $600 \Omega$.

### 2.6.8 BCD OUTPUT

This connector provides receiver tuned-frequency data in Binary-Coded-Decimal (BDC) format. Identification of data lines is shown in Table 2-1.

Table 2-1. BCD Output Lines Identification

| BCD Output Pin \# | BCD Frequency Word Output |
| :---: | :---: |
| J7-1 | $2^{0} \longrightarrow 10 \mathrm{MHz}\left(10^{7}\right)$ |
| J7-2 | $2^{1} \longrightarrow 10 \mathrm{MHz}$ |
| J7-3 | $2^{0} \square$ |
| J7-4 | $2^{1}>1 \mathrm{MHz}\left(10^{6}\right)$ |
| J7-5 | $2^{2}>1$ MHz $10{ }^{\text {a }}$ |
| J7-6 | $2^{3}$ |
| J7-7 | $2^{0}$ |
| J7-8 | $2^{1}$ |
| J7-9 | $2^{2}>100 \mathrm{kHz}\left(10^{5}\right)$ |
| J7-10 | $2^{3} \longrightarrow 100 \mathrm{KHz}(10)$ |
| J7-11 | $2^{0}$ |
| J7-12 | $2^{1}$ 10 kHz ( $10^{4}$ ) |
| J7-13 | $2^{2}>10 \mathrm{kHz}(10$ |
| J7-14 | $2^{3}$ |
| J7-15 | $2^{0} \square$ |
| J7-16 | $2^{1}$ |
| J7-17 | $2^{2}>1 \mathrm{kHz}$ |
| J7-18 | $2^{3}$ |
| J7-19 | $2^{0}$ |
| J7-20 | $2^{1}>100 \mathrm{~Hz}\left(10^{2}\right)$ |
| J7-21 | $2^{2}$ |
| J7-22 | $2^{3}$ |
| J7-23 | $2{ }^{0}$ |
| J7-24 | $2^{1}>10 \mathrm{~Hz}\left(10^{1}\right)$ |
| J7-25 | $2^{2}$ |
| J7-26 | $2^{3}$ |
| J7-27 | GND |
| J7-28 | GND |

### 2.7 OPERATION

The following paragraphs contain descriptions of the function and use of the receiver front panel controls and indicators. To provide the most rapid tuning capability to any frequency, the receiver is designed to tune itself to the center of its frequency band ( 15 MHz ) upon initial power application.
2.7.1 POWER-ON

Actuate this switch to energize the receiver. Be sure voltage of correct polarity is connected to the receiver before energizing.

### 2.7.2 SIGNAL STRENGTH

This meter contains a scale with a range of $0-100$ and provides a relative indication of receiver input signal strength.
2.7.3 RF GAIN

Rotating this control fully CW and engaging the detent places the receiver in the automatic gain mode. Rotating the control slightly CCW to disengage the detent places the receiver in the manual gain mode. Receiver gain is controlled by the setting of the RF GAIN control.

### 2.7.4 DETECTION MODE

This switch permits selection of one of the five receiver detection modes. If AM, FM or CW is selected, an IF Bandwidth position must be selected. In the USB and LSB modes, the Mode switch automatically activates the USB or LSB IF Bandwidth filter.

### 2.7.5 IF BANDWIDTH

This switch permits selection of IF Bandwidth in the AM, FM and CW Modes. Available bandwidths are: $1 \mathrm{kHz}, 4 \mathrm{kHz}, 8 \mathrm{kHz}$ and 16 kHz .

### 2.7.6 BFO OFFSET

In the ZERO position, this switch locks the BFO frequency to a fixed 455.0 kHz . In the VAR position, the BFO frequency is adjustable over a range of $\pm 8.0 \mathrm{kHz}$. Tuning of the BFO is accomplished via the TUNE knob when the TUNE RATE switch is in the BFO position.

### 2.7.7 TUNE RATE/Hz

This switch establishes the tuning rate of the receiver TUNE knob.

1. 10 kHz position. In this position, only the four most-significant digits of the readout can be varied by the TUNE knob. The
$1 \mathrm{kHz}, 100 \mathrm{kHz}$ and 10 Hz digits will be locked to the frequency indicated when the 10 kHz button was engaged.
2. $\quad 1 \mathrm{kHz}$ position. In this position, the five most-significant digits of the readout can be varied by the TUNE knob. The 100 Hz and 10 Hz digits are locked.
3. 100 Hz position. In this position, only the 10 Hz digit is locked. All other digits can be varied by the TUNE knob.
4. 10 Hz position. In this position, all digits can be varied by the TUNE knob.
5. LOCK position. In this position, the receiver is locked to the frequency displayed, and the TUNE knob is disabled.
6. BFO position. In this position, the TUNE knob is disabled from its receiver main tuning function and is available to vary the BFO offset frequency. With the BFO OFFSET switch in VAR TUNE, the TUNE knob can vary the BFO Frequency by $\pm 8.0 \mathrm{kHz}$.

### 2.7.8 TUNE

This knob varies the receiver tuned frequency when one of the four tuning rates are selected. When BFO is selected, this knob controls BFO offset frequency.

### 2.7.9 VOLUME

Rotating the VOLUME control clockwise increases the output level of the PHONES audio signals.

### 2.7.10 LEVEL

Rotating this screwdriver adjusted control clockwise increases the output level of the RECORD audio signal.

### 2.7.11 SPEAKER AMPLIFIER

The unit is supplied with an auxillary speaker housed in the front cover assembly. The speaker has its own amplifier with volume control and an affixed line cord. This cord attaches to the RECORD jack, J5, located on the front panel. This jack receives its input from the receiver audio amplifier, A9, which also feeds PHONES jack, J6.

With the speaker connected via the line cord to jack J5, clockwise rotation of the audio control knob mounted on the side of the speaker box will provide an increase in speaker volume. Use of the speaker will have no effect on the PHONES jack or its associated volume control.


Figure 3-1. WJ-8770 Receiver, Simplified Block Diagram

## SECTION III

CIRCUIT DESCRIPTION

### 3.1 GENERAL

This section describes the various circuits of the WJ-8770 HF Receiver. The receiver is divided into four functional groups: receiver, digital control, synthesizer and power supply. Discussions of each group consist of a functional description followed by detailed circuit descriptions. Functional block diagrams are included where required. This section is arranged in a functional rather than a numerical sequence to facilitate progressive reading.

### 3.1.1 OVERALL DESCRIPTION

The WJ-8770 Receiver is a triple-conversion, super-heterodyne receiver which operates in the frequency range from 5 kHz to 30 MHz . It has selected bandwidths between 1 and 16 kHz and demodulators for AM, FM, CW, USB and LSB signals. Tuning is in discrete 10 Hz steps, locked by frequency synthesizers to an internal frequency standard for accuracy and stability. The power supply sections provide regulated voltages of $+15 \mathrm{~V},-15 \mathrm{~V}$ and +5 V .

### 3.2 RECEIVER SECTION

### 3.2.1 FUNCTIONAL DESCRIPTION

Refer to the receiver simplified block diagram, Figure 3-1. Signals enter the receiver via the RF IN connector on the front panel. The Input Filter accepts signals between 5 kHz and 30 MHz . These signals are passed to the Preselector consisting of ten digitally selected sub-octave filters. The preselected input signals are then applied to the Input Converter, which includes the 1st Mixer, 1st IF Amplifier, 2nd Mixer and part of the 2nd IF Amplifier. The 10.7 MHz 2 nd IF output occupies a bandwidth of 16 kHz , fixed by erystal filters in the 1st and 2nd IF stages. In the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter, the 2nd IF signal is down converted to the 3 rd IF, 455 kHz . This signal is routed through one of the six IF filters to the IF Amplifier and the Demodulator/AGC Amplifier.

The Demodulator/AGC Amplifier provides selectable AM, FM, CW/SSB signal detection and amplification. In all detection modes, the AM detector output is processed by the AGC and used for Signal Strength Meter voltage and, in AGC mode, for RF and IF gain control.

In all modes, the AM detector is gated to the audio summing amplifier and supplies audio to the audio amplifier.

In the FM mode, the limiter and discriminator are energized. FM audio then passes through the audio summing amplifier to the audio amplifier.

In the CW/SSB mode, the CW/SSB detector is energized. The BFO signal and the 455 kHz IF are mixed and the resulting audio is passed through the audio summing amplifier to the audio amplifier.

In all modes, the detected audio from the summing amplifier is amplified by the audio amplifier and provides separate outputs for headphones and recorder.

### 3.2.2 TYPE $796123 \mathrm{DC}-30 \mathrm{MHz}$ INPUT FILTER ASSEMBLY (A1)

Refer to Figure 6-1 for schematic diagram of the $\mathrm{DC}-30 \mathrm{MHz}$ input filter. Broadband RF signals are input to the filter assembly via RF input jack J1. The input filter assembly consists of a low-pass filter with a cut-off frequency just above 30 MHz . Additional tuned elements in the filter yield a high stop-band attenuation above 40 MHz , which eliminates LO leakage and image interference.

The input filter also serves to protect the rest of the receiver from damage due to excessive signal levels in the passband. When signals greater than +15 dBm are received at RF input jack J1, diodes CR1, CR2, VR1, and VR2 conduct, shunting excessive energy away from the receiver. Signals in the passband from DC -30 MHz are output from the input filter via connector J 2 to the sub-octave preselector filters decribed in paragraph 3.2.3.

### 3.2.3 TYPE 796100 INPUT PRESELECTOR (A2)

Input Preselector Assembly A2, provides sub-octave bandpass filtering of the $0.005-30 \mathrm{MHz}$ frequency range of the receiver. A functional block diagram of the input preselector is presented in Figure 3-2. The receiver frequency tuning range is divided into ten frequency bands with each band associated with one of ten digitally selectable sub-octave filters. The selection of the correct sub-octave filter is determined by encoded frequency data from the Up/Down Counter of the Digital Control Unit. The encoded frequency data is decoded and converted into a preselector code by the preselector decoder. The preselector code is then applied to the digital control circuitry which interprets the preselector code and activates the applicable sub-octave filter. Schematic diagrams for each preselector filter and digital decoding are presented in Figures 6-2 and 6-3.

### 3.2.3.1 Type 791821-2 Digital Control

The digital control circuitry, Figure 6-8, consists of 4-line-to-10-line decoder U1 and five dual peripheral drivers U2 through U6. This circuitry provides the $\operatorname{logic}$ required to decode the 4 -bit preselector code input and activate only one sub-octave filter.

When a preselector code is input to pins 12 through 15 of decoder U1, it produces ten outputs: one being active low and the remaining nine, high. With each output line associated with a NOR circuit contained in one of the five dual peripheral drivers, the active low allows the associated filter on that line to remain active while the nine filters associated with the nine high output lines are rendered inoperative.

With a selected tuned frequency of 4.0 MHz , preselector code inputs to decoder U1 are 0110 (binary). As can be seen in Table 3-1, with a tuned frequency between $3.90-5.99 \mathrm{MHz}$ and a preselector code input of 0110 , the output from decimal 6 (pin 7) of decoder U 1 is active low and the remaining nine outputs are high. With inputs 1 B and 2 B (pins 2 and 7) tied to ground, the active low to input 1 A (pin 1) of driver U 4 results in a low output from output 1 Y (pin 3) to the $3.9-6.0 \mathrm{MHz}$ filter associated with the output allowing it to remain active. The high outputs on the remaining nine lines to their respective 1 A and 2 A inputs of drivers U2 through U6 result in a +15 Vde control voltage to the remaining nine filters, deactivating them.


Figure 3-2. Input Preselector Functional Block Diagram

Table 3-1. Tuned Frequency to U1 Output Conversion


* Designations for outputs do not correspond with IC pin numbers.


### 3.2.3.2 Sub-Octave Filters

The $0.005-0.75 \mathrm{MHz}$ filter circuit on the $0.005-0.75 / 0.75-1.1 \mathrm{MHz}$ filter board is a 5 -pole low-pass filter. The $0.75-1.1 \mathrm{MHz}$ filter circuit and the remaining eight filter circuits on the other four filter boards are 5 -pole band-pass filters which provide minimum attenuation on all frequencies in their respective passbands and maximum attenuation on all frequencies in their respective stopbands. The pole configuration of each filter circuit is shunt, series, shunt, series, shunt. The input and output impedance of each filter circuit is 50 ohms. The DC -30 MHz RF signal from the input filter assembly is applied to pin 1 of all five filter boards. Since the functional operation of all five filter boards is similar, the differences being component values, only one board is deseribed in the following paragraphs.

With a selected tuned frequency of 4.0 MHz , all of the filter circuits except the $3.9-6.0 \mathrm{MHz}$ filter circuit receive a +15 Vdc control voltage at their digital on/off control inputs, deactivating them. As described in paragraph 3.2.3.1, the active filter circuit is determined by an active low input at its digital on/off control input. With input pin 8 of the $3.9-6.0 \mathrm{MHz}$ filter circuit, Figure 6-5, at ground potential ( 0 Vdc ), diodes CR4, CR5, CR8, and CR9 are forward biased allowing the RF input at pin 1 to be processed through the filter circuit to RF output pin 18. Approximately 50 milliamperes de flow through each diode ensure that the RF currents will be small by comparison even when large signals are passing through the circuit. The 4 MHz RF signal is output to the input converter.

When the $3.9-6.0 \mathrm{MHz}$ filter circuit is active, the $2.6-3.9 \mathrm{MHz}$ filter circuit, Figure 6-5, is inactive with a +15 Vde control voltage at input pin 11, diodes CR1, CR2, CR3, CR6, CR7, and CR10 are reverse-biased prohibiting operation of the filter circuit.

### 3.2.4 TYPE 796099 INPUT CONVERTER (A3)

Input Converter Assembly A3, Figure 3-3, consists of two sub-assemblies; the 1st mixer/1st IF and the 2nd mixer/2nd IF, RF signals from Input Preselector A2, described in paragraph 3.2.3 are mixed with the 1st LO input from the 1st LO Synthesizer A5A2, deseribed in paragraph 3.6.3, and amplified by IF amplifier Q2. The 42.905 MHz 1st IF signal, is coupled through a 40 kHz band-pass filter FL1 to the 2nd mixer/2nd IF. The schematic diagram of the input converter is presented in Figure 6-9.

The 42.905 MHz 1st IF signal input to the 2 nd mixer/2nd IF is further filtered and amplified. RF AGC from Demod/AGC Amplifier A12 is provided by a PIN diode attenuator located in the signal path prior to the second mixer. The 2nd LO input from the 2nd LO Synthesizer A5A3, deseribed in paragraph 3.6.4, is input to the 2nd Mixer/2nd IF where it is filtered, amplified, and mixed with the input from the 1 st mixer/1st IF by double-balanced mixer U1. The 10.7 MHz 2nd IF signal, is then amplified by cascode amplifier Q3, Q4, filtered by the 30 kHz bandwidth, 10.7 MHz band-pass filter FL1 and output to IF Demodulator A4, described in paragraph 3.2,10.

### 3.2.4.1 $\quad 1$ st Mixer/1st IF

RF input signals to the 1st mixer/1st IF, Figure 6-9, from the input preselector, may be any frequency from 5 kHz up to 30 MHz and at any level from noise floor to +5 dBm . These RF signals, along with the 42.92 to 72.91 MHz input from the 1st LO synthesizer, are applied to input pins 3 and 1 , respectively, of double-balanced mixer U1. The double-balanced mixer produces the sum and difference frequencies of the two inputs.

The output signal from double-balanced mixer U1 is coupled through coupling capacitor C1 to IF amplifier Q2 which amplifies the signal to compensate for losses incurred in mixer U1. IF amplifier Q2 is a grounded-gate FET with a low noise figure, provides a good terminating impedance for mixer U1, and has a large signal handling capability. Transistor Q1 functions as a constant current source for amplifier Q2. Diode CR1 minimizes Q1 collector current changes due to temperature changes. A rise in temperature causes CR1 to develop a lower forward voltage drop which lowers the base bias of Q1 in the same proportion as the baseemitter voltage of Q1 maintaining a constant voltage across R4. A reduction in temperature results in a higher base bias on Q1. Transformer T1 is the output load for amplifier Q2 and is broad-tuned by C3 to provide the proper driving impedance for 43 MHz band-pass filter FL1.

Filter FL1 has a center frequency of 42.905 MHz and a 3 dB bandwidth of 40 kHz . It requires a 50 ohm source and load. Filter FL1 rejects unwanted signals passed by the input preselector and mixer U1 and, establishes the initial IF bandpass. The signals are output from filter FL1 to the 1st LO frequency trap on the 2nd mixer/2nd IF, described in the following paragraph.

### 3.2.4.2 2nd Mixer/2nd IF

The 1st IF output signal may be any frequency from 42.910 MHz to 42.900 MHz . These signals are passed through the 1st LO frequency trap, and then through a coupling

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network consisting of inductor L1 and capacitor C1 to IF amplifier Q2. IF amplifier Q2, along with its ancillary components Q1 and diode CR1, function in a similar manner as that of IF amplifier Q2, described in paragraph 3.2.4.1. PIN diode CR2, in the output circuit of Q2, functions as a voltage-controlled variable resistor with the RF AGC input as its control voltage. It provides more than $10 \mathrm{k} \Omega$ resistance at maximum AGC input down to 20 ohms with a minimum input. The variable attenuated output of Q2 is coupled to double-balanced mixer U1 by impedance matching transformer T 1 .

The 32.2100 MHz to 32.2001 MHz 2nd LO input from 2nd LO Synthesizer A5A3 is filtered by low pass filter L7, C15, and L8 which prohibits introduction of any 1st LO INPUT to the 2nd LO circuitry. The 2nd LO input is then amplified by amplifier Q5 and coupled to double-balanced mixer U1 by impedance matching transformer T3.

The 1st IF input at pins 5 and 6 of mixer U1 is mixed with the 2nd LO input at pins 1 and 2 resulting in a 10.7 MHz output from pin 3 . The 10.7 MHz output from 2 nd mixer U1 is coupled through capacitor C6 to a bi-polar cascode amplifier consisting of common emitter stage Q4 and common base stage Q3 which provide high gain with good stability and low noise contribution. The output of common base stage Q3 is coupled to 10.7 MHz band-pass filter FL1 by transformer T2. Filter FL1 has a center frequency of 10.7 MHz , a bandwidth of 16 kHz , and requires 50 ohm terminations. The 10.7 MHz signal is output to the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter A4A1.

### 3.2.5 TYPE 796120 IF MOTHERBOARD (A4)

IF Motherboard Assembly, Figure 3-4, provides the mounting provisions and electrical interface for:
$10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter A1,
Type 72463 -XX Filters, A2 through A7,
455 kHz IF Amplifier A8,
Wideband/Narrowband Filter A9 and,
Demodulator/AGC Amplifier A10.

It also provides, via its own electrical connectors, electrical interfaces from subassemblies A1 through A10 to other assemblies of the receiver, the front and rear panel connectors, and to the receiver front panel controls and indicators.

The 10.7 MHz 2nd IF signal from Input Converter A3 and the 11.155 MHz 3 rd LO signal from 3rd LO and BFO Synthesizer A5A4 are input to $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter A4A1, described in paragraph 3.2.6, which produces 3 rd IF signals centered at 455 kHz . The 455 kHz 3 rd IF signal is then output through one of the four IF bandwidth filters $(16 \mathrm{kHz}, 8 \mathrm{kHz}, 4 \mathrm{kHz}$, or 1 kHz ), operator selected via Bandwidth select switch S2, or either the LSB filter or USB filter, operator selected via Detection Mode switch S3, to 455 kHz IF Amplifier A8, described in paragraph 3.2.8.

The 455 kHz 3rd IF signal input to the 455 kHz amplifier undergoes a two-stage gain-controlled amplification and is output to Wideband/Narrowband Filter A9. The gain control input originates as either AGC or manual which is operator selected at AGC ON/OFF switch S6. The AGC or manual RF gain, with the level operator-determined via RF Gain control R1, are both input to the 455 kHz amplifier via Demodulator/AGC Amplifier A10, described in paragraph 3.2 .11 . The amplified 455 kHz 3 rd IF signal is then output to Wide Band/Narrow Band Filter A9.

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Figure 3-4. IF Motherboard, Functional Block Diagram

The 3rd IF signal input from the 455 kHz IF amplifier is applied to both the wide band and the narrow band circuits of Wide Band/Narrow Band Filter A9, described in paragraph 3.2.9. The input is passed through either the narrow band circuit which provides a 4 kHz bandwidth or the wide band circuit which provides a 35 kHz bandwidth. Circuit selection is accomplished by a switched +15 Vde input which originates from a jumpered connection on any one of the four IF bandwidth filters or either the LSB or USB filter. The 455 kHz signal is then output to Demodulator/AGC Amplifier A10.

The 455 kHz signal input from the wide band/narrow band filter to Demodulator/AGC Amplifier A10, described in paragraph 3.2.10, is, dependent upon a +5 Vde control signal via Detection Mode switch S3, switched through the AM, FM, or CW detector and amplifier circuit and output to Audio Amplifier Assembly A9.

### 3.2.6 TYPE $796101 \quad 10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter (A4A1)

A block diagram of the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ converter is presented in Figure 3-5. The 10.7 MHz 2nd IF signal from the input converter, described in paragraph 3.2 .4 and the 11.155 MHz 3rd LO signal from 3rd LO and BFO Synthesizer A5A4, are input to the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ converter which produces 3 rd IF signals centered at 455 kHz . The 455 kHz 3rd IF is then output to one of the four selectable IF filters, the LSB filter, or the USB Filter described in paragraph 3.2.7. A schematic diagram of the converter is presented in Figure 6-11.

The 2nd IF signal, at a nominal 7 db above the receiver input signal, is input to gate 3 of FET Q2, via input pin 1, 4-to-1 impedance matching transformer T1 and coupling capacitor C1. The 3rd LO signal is input at a fixed frequency of 11.155 MHz at pin A. It is passed through a filter comprised of C17 and 11.155 crystal Y1. which suppresses the 5 kHz sideband from the 3rd LO, to amplifier Q1. Amplifier Q1 provides an amplification factor of 20 resulting in a 3rd LO signal at gate 2 of FET Q2 of 1.4 Vrms. Resistor R14, in the output circuit of Q2, provides the load for the 5-pole low-pass filter comprised of C12, L3, C13, L4, and C14. Capacitor C12 in conjunction with inductor L2, acts as a 455 kHz filter. The 455 kHz signal output passes through the low-pass filter, which filters $10.7 \mathrm{MHz}, 11.155 \mathrm{MHz}$, and their sum, to amplifier Q3.

Amplifier Q3 functions as an emitter-follower for the 455 kHz IF OUT circuit via eapacitor C16 and output pin 6 . The 455 kHz output at pin 6 has an overall gain of 25 dBm . The 455 kHz output from the collector of Q3 is passed through 16 -to-1 impedance matching transformer T2 to the 455 kHz SM OUT output pin 4.

### 3.2.7 IF FILTERS

3.2.7.1 Type 72463-(XX) IF Filter (A4A2 Through A4A5)

IF Filter Assemblies A2 through A5, Figure 3-6, provide selectable bandwidth filtering of the 455 kHz IF Input from $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Assembly A1. As can be determined from the schematic Figure 6-12, the only differences between filters are types of mechanical filters used and which filter control outputs are connected into the circuits via jumpers at output pins D and E. Due to the similarity of the circuits, only one IF filter, 1 kHz Filter A4A5, is described in the following paragraphs.


Figure 3-5. $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Block Diagram


Figure 3-6. IF Filter Block Diagram

With the receiver in the FM, AM, or CW detection mode and with the 1 kHz bandwidth selected, the 455 kHz 3 rd IF from the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ converter is input to 1 kHz Filter A4A5, Figure 6-12, at input pin 6 and a +5 Vdc filter control input level is input at pin F. The +5 Vdc filter control input is via switch S 3 , in the FM , AM, or CW detection mode, IF Bandwidth switeh S2 contact 1, and input pin 18 of the IF demodulator.

The +5 Vdc filter control input, applied to the base of Q1, via input pin F, causes Q1 to turn on. With Q1 turned on, collector current flow from Q1 through the base-emitter junction of Q2 causes Q2 to saturate. With the coil of relay K1 in the collector circuit of Q2, when Q2 saturates, it causes the jumpered filter control output, pin E, to Wide Band/Narrow Band Filter A9, described in paragraph 3.2 .9 to go to +15 Vdc . It also causes relay K 1 to activate, allowing the 455 kHz input at pin 6 to be passed through the 1 kHz filter FL1 and isolation amplifier Q3 to IF output pin 1. The 455 kHz IF signal with a 1 kHz bandwidth is then output to 455 kHz IF Amplifier A8, described in paragraph 3.2.8.

### 3.2.7.2 Type 72463-17 LSB Filter (A4A6)

LSB Filter Assembly A4A6, passes lower sideband frequencies from 452.3 kHz to 454.8 kHz in a manner similar to that described for IF Filter Assemblies A2 through A5 described in paragraph $3 \cdot 2.7 .1$. As can be determined from the schematic, the only differences between the LSB filter and the IF filters are types of mechanical filters, select circuit components, and the filter control output jumpers.

With the receiver in the LSB detection mode, the 455 kHz 3 rd IF from the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ converter is input to LSB Filter A4A6, at input pin 6 and the +5 Vdc control input level is input at pin F. The +5 Vde filter control input is via switch S3, in the LSB detection mode, and input pin 9 of the IF demodulator. The LSB filter circuit functions as described for IF Filter Assemblies, paragraph 3.2.7.1, with only one exception; the jumper for the filter control output is from E1 to E3, resulting in the output at pin D.

### 3.2.7.3 Type 72463-18 USB Filter (A4A7)

USB Filter Assembly A4A7, passes upper sideband frequencies from 455.2 to 457.7 in a manner similar to that described for IF Filter Assemblies A2 through A5, paragraph 3.2.7.1. As can be determined from the schematic, the only differences between the USB filter and the IF filters are types of mechanical filters, select circuit components, and the filter control output jumpers.

With the receiver in the USB mode, the 455 kHz 3 rd IF from the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ converter is input to USB Filter A4A7, at input pin 6 and the +5 Vdc control input level is input at pin F. The +5 Vdc control input is via switch S 3 , in the USB detection mode, and input pin 5 of the IF demodulator. The USB filter circuit functions as described for IF Filter Assemblies, paragraph 3.2.7.1, with only one exception; the jumper for the filter control output is from E1 to E3, resulting in the output at pin D.

### 3.2.8 TYPE 796103455 kHz IF AMPLIFIER

A block diagram of the IF amplifiers is presented in Figure 3-7. The 455 kHz IF amplifier consists of two gain-controlled, dual-gate FETs and their ancillary circuit components. The 455 kHz IF signal is input to the assembly via pin A6, undergoes a two-stage gain-controlled amplification and is output via connector F to the wide band/narrow band IF amplifier described in paragraph 3.2.9.


Figure 3-7. 455 KHz IF and WB/NB IF Amplifier Block Diagram

Referring to the schematic diagram, Figure 6-13, Q1 and Q2 are cascaded FET amplifiers. The 455 kHz signal from the IF filter is applied through eapacitor C1 to gate 1 of Q1. The drain output of Q1 is developed across inductor L1 and applied through coupling capacitor C6 to gate 1 of Q2. The gain control signal is input through connector $C$ to gate 2 of both Q1 and Q2. Thermistors RT1 and RT2 provide temperature compensation for Q1 and Q2. As inherent temperature rise during operation causes the resistance of Q1 and Q2 to increase, RT1 and RT2 decrease in resistive value.

The drain output of Q2 is developed across inductor L2 and the IF output is taken from the arm of gain control potentiometer R16. Gate 1 bias for Q1 is developed by a voltage divider consisting of resistors R1 and R2 and gate 1 bias for Q2 is developed by resistors R9 and R10. Gate 2 of Q1 is biased at approximately 3.0 Vde by resistors R3, R5, and CR1 at 0.0 V AGC input. The bias on gate 2 of Q1 does not fall until the AGC voltage becomes sufficiently negative to reverse bias CR1, effectively removing it from the circuit. Further negative increases in AGC voltage are then reflected in a more negative bias on gate 2 of Q1, reducing the amplifier gain. The AGC input to Q2 affects it as described for Q1.

### 3.2.9 TYPE 796102 WIDE BAND/NARROW BAND IF AMPLIFIER

Referring to the schematic diagram, Figure 6-14, the wide band/narrow band IF amplifier consists of a wide band IF amplifier comprising amplifiers Q1 and Q4, filter FL1, and ancillary components and a narrow band circuit. The narrow band circuit is comprised of amplifiers Q2 and Q3, filter FL2, and ancillary components. The 455 kHz signal is input to the assembly from the 455 kHz IF amplifier, deseribed in paragraph 3.2 .8 via connector P1, pin F. Band selection is accomplished by a switched +15 Vdc source. When selected, the narrow band circuit provides a 4 kHz bandwidth at 6 dB . The wide band circuit provides a 35 kHz bandwidth at 6 dB . The selected wide band or narrow band IF output is via connector P1, pin A, to the demodulator/AGC amplifier described in paragraph 3.2.10.

The IF signal input from the 455 kHz amplifier is applied simultaneously to both the wide band and the narrow band circuits. As stated in the previous paragraph, selection of the wide or narrow band circuit is performed by application of a switched +15 Vde source to the base bias voltage dividers of the selected amplifiers, Q2 and Q3 for wide band or Q1 and Q4 for narrow band.

Assuming that the wide band circuit is activated with a +15 Vde input at connector P1, pin D, amplifiers Q2 and Q3 conduct. The IF signal is amplified by common-emitter amplifier Q2. Resistor R10 provides de-generative feedback for improved signal handling capability. Capacitor C8 couples the output from Q2 to wide-band filter FL2. Filter FL2 is a bandpass filter of a nominal 35 kHz at 6 dB , which is narrow enough to suppress any broadband noise but wide enough not to restrict the overall receiver bandwidth. The output from FL2 is coupled by capacitor C12 to emitter follower amplifier Q3 and then is output to demodulator/AGC amplifier A4A10, deseribed in paragraph 3.2.10, via connector P1, pin A. The narrow band circuit, when selected, operates in a manner similar to that just described for the wide band circuit.

## 3.2 .10 <br> TYPE 796113 DEMODULATOR/AGC AMPLIFIER (A4A10)

The demodulator/AGC amplifier, Figure 3-8, provides selectable AM, FM, CW/SSB signal detection and amplification of the 455 kHz input signal from the wide band/narrow band IF amplifier described in paragraph 3.2.9. After detection and amplification, the selected


Figure 3-8. IF Demodulator, Block Diagram
signal is output to the audio amplifier assembly, described in paragraph 3.2.11. The demodulator/AGC amplifier also provides IF AGC to the 455 kHz amplifier deseribed in paragraph 3.2.8; RF AGC to the input converter described in paragraph 3.2 .4 ; a 455 kHz IF signal to the front panel mounted IF output jack; and the output to the front panel mounted signal strength meter.

### 3.2.10.1 AM Detection Mode

In the AM detection mode, the 455 kHz 3 rd IF is input to the demodulator/AGC amplifier, Figure 6-15, via input pin B18 and coupling capacitor C1 to the base of amplifier Q1, the first IF amplifier of the two-stage IF amplifier comprising Q1 and Q2. The input signal is amplified by Q1 and applied to the base of Q2 where it is further amplified and output to the base of Q3 via AM detector CR2. Amplifier Q1 also acts as an emitter-follower, coupling the 455 kHz input through capcitor C22 to the base of IF amplifier/emitter-follower Q9.

Amplifier Q3 acts as an emitter-follower, coupling the AM signal through the AM low-pass filter comprised of inductor L3 and capacitor C11 to analog switch Q5 and to the base of amplifier Q4. With a +5 Vdc input at pin A14 from selector switch S3 in the AM detection mode, analog switch Q5 conduets, passing the AM audio signal to audio summing amplifier U2A. From U2A, the signal is output through active filter U2B and pin 10 to Audio Amplifier Assembly A9 described in paragraph 3.2.11.

In the AM detection mode, IF amplifier/emitter-follower Q9 acts strictly as an IF amplifier. The 455 kHz input at its base is amplified and output to front panel mounted IF Output jack J4 via impedance matching transformer Tl .

## 3,2,10.2 FM Detection Mode

In the FM detection mode, the 455 kHz 3 rd IF is input via pin B18 and coupling capacitor C1 to the base of amplifier Q1 where it is amplified by the Q1 and Q2 stages and coupled through to IF AGC amplifier U1A if the reciver is in the AGC mode. Amplifier Q1 also acts as an emitter-follower, coupling the 455 kHz input to the base of IF amplifier/emitterfollower Q9.

The 455 kHz input at the base of Q9 is amplified and output to IF Output jack J4 via transformer T1. In the FM detection mode, with +5 Vde input at pin A1 to current source Q11, Q9 also acts as an emitter-follower coupling the 455 kHz signal to quadrature FM detector U4. The FM output from detector U4 is filtered by the low-pass filter, comprised of inductor L6 and capacitor C42, and is input to summing amplifier U2A.

### 3.2.10.3 CW Detection Mode

In the CW detection mode, the 455 kHz 3 rd IF is input via pin B18 and coupling capacitor C1 to the base of amplifier Q1 where it is amplified by the Q1 and Q2 stages and coupled through to the IF AGC amplifier in a manner similar to that just described for the FM detection mode described above. The differences between the modes are as follows. In the CW mode or in the LSB AGC or USB AGC mode, the +5 Vdc input at pin A7 (CW mode), at pin B8 (LSB AGC mode), or at B7 (USB AGC mode) is applied to the gate of slow AGC switch Q6 causing it to conduct. Capacitor C15, in the drain circuit of Q6, and capacitor C17 both have an attack time of 15 msec , however, due to the difference in their decay times; two to four seconds for C15 and 100 msec for C17, receiver gain change as a result of gaps in the CW or SSB input signal are minimized.

As in the other detection modes, the 455 kHz input is coupled to the base of IF amplifier/emitter-follower Q9, amplified and output to IF Output jack J4. In the CW mode, Q9 acts as an emitter-follower, coupling the 455 kHz input to signal input pin 1 of CW/SSB detector U3. With BFO OFFSET switch S5 in the ZERO position, the BFO input from 3rd LO/BFO Synthesizer A5A4 at pin B12 is 455 kHz . In the VAR TUNE position, the BFO input is from 447 kHz to 463 kHz in 100 Hz steps. The BFO input is coupled through eapacitor C26 and input to carrier input pin 8 of detector U3. The output at pin 6 contains sum and difference frequency components of the 455 kHz input to pin 1 and the fundamental and odd harmonics of the BFO input at pin 8 . The output from pin 8 is passed through a CW audio pass filter, comprised of inductor L4 and capacitor C32, and input to audio summing amplifier U2A.

### 3.2.10.4 USB/LSB Detection Modes

In either the USB mode or LSB mode, the demodulator/AGC amplifier circuit operation is essentially the same as that described for the CW detection mode, the major differences being the BFO input at pin B12 is fixed at 455 kHz and the IF input frequency is as selected/tuned.

### 3.2.10.5 AGC Mode

In the AGC mode, with the front panel mounted RF GAIN switch, S 6 in the AGC position, a 0 Vdc , or electrical open, is input at pin B6 enabling -15 Vdc to be applied to the gates of source switch FETs Q7, Q8, and Q12, holding them at cut-off. Amplifier Q4 acts as an emitter-follower and outputs the AGC signal through AGC delay CR5 to IF AGC amplifier U1A. The amplified AGC signal (with a voltage swing from 0.0 to -3.0 volts, dependent upon input signal strength) is output to the 455 kHz IF amplifier, described in paragraph 3.2 .8 , via pin B3. It then passes through RF AGC delay Q13 and the RF AGC shaping circuit comprised of CR6, CR7, and R38, to RF AGC amplifier U1B. The amplified RF AFC signal (with a voltage swing from 0.0 to +4.0 Vdc , dependent on input signal strength) is output to the input converter, described in paragraph 3.2.4, via pin B1.

### 3.2.10.6 Manual Gain Mode

In the manual gain mode, with the front panel mounted RF GAIN switch S6 in the non-AGC position, a ground potential is available at pin B6 which is applied to the gates of source switch FETs Q7, Q8, and Q12 enabling them to conduct. With Q7 conducting, the ground potential is present at the juncture between AGC delay diode CR5 and resistor R23, effectively blocking the AGC circuit to IF AGC amplifier U1A. With Q12 conducting, the ground potential is also present at the juncture between voltage regulator VR1 and output pin B4, grounding the negative side of front panel mounted signal strength meter M1. With Q8 conducting, the 0.0 to -1.5 volt analog voltage input (with 0.0 volts representing maximum manual gain and -1.5 volts, minimum manual gain) is applied to IF AGC amplifier U1A. The amplified output from U1A, which ranges from 0.0 to -3.0 volts ( 0.0 to -1.5 volts manual gain input voltage), is output to the 455 kHz IF amplifier via pin B3 and, to RF AGC amplifier U1B via the RF AGC delay and RF AGC shaping circuits. The amplified output from U1B, which ranges from 0.0 to +4.0 volts ( 0.0 to -1.5 volts manual gain input voltage), is output to the input converter via pin B1.

TYPE 796116 AUDIO AMPLIFIER (A9)
Audio Amplifier Assembly A9, Figure 6-25, consists of a dual operational amplifier and ancillary circuit components. The audio output, AM, FM, CW, USB and LSB, from pin A18 of the demodulator/AGC amplifier, deseribed in paragraph 3.2.10, is input at E1 and applied to two amplifier circuits. After amplification, the two audio outputs are available at front panel mounted jacks; RECORD jack J5 and PHONES jack J6.

The audio input signal to the record circuit is fed through potentiometer R1, assembly-mounted adjustment, to OP AMP U1A. U1A provides a voltage gain of 4 to the input signal and outputs the audio signal to RECORD jack J5.

The audio input signal to the phones circuit is fed through potentiometer R5, which is mechanically linked to the front panel volume control, to OP AMP U1B. U1B provides a 3 dB roll-off at 3.8 kHz and outputs the audio signal to PHONES jack J6.

## 3.3 <br> TYPE 796106 DIGITAL CONTROL UNIT (A6)

The digital control unit, Figure $3-9$, is the interface between the front panel controls and the synthesizer section. It provides the means of converting voltages, representing operator selectable parameters, into control signal levels for use by the synthesizer section, described in paragraph 3.6, preselector assembly A2, described in paragraph 3.2.3, and display driver assembly A7, described in paragraph 3.4. Up/down counters U1 through U7 and BFO up/down counters U8 and U9 are C-MOS type 14510B presettable synchronously clocked D-type flip-flops with T-type gating structure to provide BCD count sequence. The schematic diagram of the digital control assembly is presented in Figure 6-22. A general description of this type counter is presented in the following paragraph as an aid in understanding how the digital control unit circuit functions.

The 14510 B is a presettable up/down decade counter. With a high input at up/down input pin 10, the counter will increment by one for each rising edge of the clock pulse at clock input pin 15. Conversely, with a low input at pin 10, the counter decrements by one for each rising edge of the clock pulse at pin 15. Conversely, with a low input at pin 10, the counter decrements by one for each rising edge of the clock pulse at pin 15 . With a high input at parallel enable pin 1, clocking is inhibited. Counters U1 through U7 and U8 and U9 are cascaded by tying their respective carry output pins, pin 7, to the carry input pins, pin 5 , to the following counter and by connecting the control inputs, as clock, up/down, and parallel enable, in parallel. With a high at carry input pin 5, clocking is inhibited. The carry output, normally high, goes low during a carry condition. Carry conditions occur when the counter is in a 0 state during down counting or in a 9 state during up counting. As a result, any stage in a counter chain clocks only when all preceding stages are in carry conditions.

In the digital control unit, counters U1 through U7 form a presettable, seven-digit, up/down decade counter. Their outputs drive the display driver and the synthesizer motherboard. The display driver converts the data into signals used to light appropriate segments of the frequeney word display on display assembly A8, described in paragraph 3.5 . The LO and BFO synthesizers on the synthesizer motherboard described in paragraph 3.6, use the data to establish the correct 1st through 3rd LO and BFO frequencies.

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Figure 3-9. Digital Control, Block Diagram

For the purposes of this discussion, the circuit description of the digital control unit is divided into two parts. The first part describes how the digital control unit functions in either the AM or FM detection modes in both the unlocked and locked tuning states. The second part describes only those circuit components which are unique to the CW, USB, or LSB modes (Figure 3-10).

### 3.3.1 AM, FM DETECTION MODES

In either the AM or FM detection mode with the TUNE RATE/Hz switch S4 in the 10 Hz position, tuning clock and tuning direction signals are input to direction flip-flop U22 from tuning encoder U1, described in paragraph 3.3.4, via pins 21 and 13 , respectively. After inversion by inverter U12, the input clock pulse lags the input direction pulse by 90 degrees if the receiver frequency is being up-tuned (clockwise rotation of tuning encoder U1). Conversely, when being down-tuned (counterclockwise rotation of tuning encoder U1), the input clock pulse leads the input direction pulse by 90 degrees.

When being up-tuned, the high output from pin 1 of U22 is applied to up/down input pin 10 of each up/down counter, U1 through U7, and to input pin 5 of 30 MHz limit U15. As previously stated, the enabled counter increments by one upon receipt of each rising edge of the clock pulse at pin 15 . The high at pin 5 of U 15 , at any frequency less than 30 MHz , has no effect on the low output from U15 to input pin 2 of NOR gate U13. The low at input pin 1 of U13, at any frequency other than 0 , and the low at pin 2, result in a high output from U13 to input pin 6 of U16.

The positive-going clock pulse from output pin 4 of U 12 is applied to input pin 9 of AND gate U16 and also through resistor R5 to input pin 8 of U16. Resistor R5 acts as a delay for the leading edge of the clock pulse to pin 8. The clock output from pin 10 of U 16 is passed through capacitor C24, which along with resistor R31, causes it to be of shorter duration, and when to input pin 5 of AND gate U16, along with the high input at pin 6 from NOR gate U13, a high output at pin 4 results. The positive-going clock pulse is now made available at the clock inputs, pin 15, of counters U1 through U7 and to both input pins 8 and 9 of OR gate U11. The high output from pin 10 of U11 is input to pin 5 of OR gate U11 and output to input pin 20 of PROM U10. The negative-going portion of the clock pulse at pin 20 is used to latch the outputs from counters U5 through U7 into the PROM which, effectively, uses the data at its A inputs as addresses for preselector and band switch codes.

With TUNE RATE/Hz switch S4 in the 10 k position, the +15 Vdc on the wiper arm of deck B of switeh S4 is input to the digital control unit at pin 1 of connector J2. The +15 Vde is applied to input pin 2 of X -NOR gate U14 which acts as a debounce. The high output from AND gate U19 to tune/tune inhibit switch Q1 results in a low, or ground, output from pin 5 of connector J2. The ground potential at pin 5 is applied through the wiper arm of deck A of switch S4 to input pin 19 of connector J2. With a low now at carry input pin 5 of counter U4, the clock input at pin 15 is enabled, allowing U4 to increment for each rising edge of a clock pulse. Counter U4 outputs, via its Q output pins, the operator selected frequency data to the 1st LO synthesizer and to the display driver.

When up-tuning, 30 MHz limit switch U15 prohibits frequency selection above 30.00 MHz in the following manner. With a selected frequency of 30.00 MHz , outputs Q1 and Q2, pins 6 and 11, of counter U7 are both high. The highs from pins 6 and 11 are applied to input pins 4 and 3 , respectively, of 30 MHz limit switch U15. With a high, representing the up-tuning direction, already available at pin 5 of U15, the output from pin 6 of U15 goes high.

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This high is applied to reset pins, pin 9, of counters U1, U2, and U3 and to input pin 2 of NOR gate U13. The high at pin 9 of counters U1, U2, and U3 causes these counters to be reset to zero. The high at pin 2 of NOR gate U13 and the existing low at pin 1 result in a low output from pin 3 of U13 to input pin 6 of AND gate U16. With a low at input pin 6, the output from U16 pin 4 is low which stops any further up-tuning clock pulse to counters U4, through U7.

With TUNE RATE/Hz switch S 4 in the LOCK position, the front panel mounted FREQ MHz display goes blank and the tuning encoder control is disabled. In the lock position, the wiper arm of deck B of switch S4 is at ground potential, or low. This ground potential is applied to the power input pin, pin 6, of tuning encoder U1 and to pin 1 of connector J2 of the digital control unit. The ground, or low, at pin 1 is applied to the base and emitter of frequency decimal switch Q4, shutting it off, and to input pin 12 of AND gate U19. The resultant low output from pin 11 of U19 is output from the digital control unit via pin 8 of connector P1 to the $\overline{\mathrm{BL}}$ input pins of drivers U1 through U4 and driver U7 on display driver assembly A7. With a low at the $\overline{\mathrm{BL}}$ input pins, the outputs from drivers U1 through U 4 and driver U 7 to display assembly A8 all go low resulting in a blank display. The low output from pin 11 of U 19 is also applied to the select input (SEL) pins, pin 11, of multiplexers U20 and U21. A low input at pin 11 of U20 and U21 causes the Y output lines to drivers U5 and U6 on the display driver assembly to go low resulting in displays U5 and U6 going blank.

When being down-tuned, the low output from pin 1 of U 22 is applied to up/down input pin 10 of each up/down counter, U1 through U7, and to input pin 5 of 30 MHz limit U15. With a low input at up/down pin 10, the enabled counter decrements by one for each rising edge of the clock pulse at clock pulse at clock input pin 15 . When the counter decrements to a 0 state, the level from carry output pin 7 to carry input pin 5 of the next counter goes low causing it to decrement upon receipt of each clock pulse. When the carry output from counter U7 to pin 9 of 0 -down limit U12 goes low, it results in a high input to pin 1 of NOR gate U13. The normal high output from pin 3 of U13 to pin 6 of AND gate U16 goes low resulting in a low output from pin 4 of U16 to the clock input pins of the counters.

### 3.3.2 USB, LSB DETECTION MODES - BFO ZERO

In the USB detection mode or the LSB detection mode, the digital control unit functions as described for the AM, FM detection modes, paragraph 3.3.1, with the following exception; the BFO output from the digital control unit to the synthesizer assembly is zero, resulting in a fixed 455 kHz BFO output from the BFO synthesizer to the demodulator/AGC amplifier in the USB/LSB detection modes.

With the detection mode switch in either the USB or LSB position and BFO OFFSET switch S5 in the ZERO position, the ground potential on the wiper arm of front panel mounted detection mode switch S3 is applied to either contact 10 (LSB) or contact 11 (USB). This ground, or low, is applied to input pins 2 and 8 of AND gate U15 through pin 9 of connector J2. The low output from pin 9 of U15 is input to pins $6,8,2$, and 12 of quad AND gate U18 and to input pins $6,8,2$, and 12 of quad AND gate U17. With each gate electrically located between the Q outputs of BFO up/down counters U8 and U9, the low outputs to the BFO synthesizer via pins $24,26,25,23\left(10^{2}\right)$ and pins $22,19,20,21\left(10^{3}\right)$ represent a zero BFO frequency word.

### 3.3.3 CW DETECTION MODE - BFO VARIABLE

In the CW detection mode with BFO OFFSET switch S5 in the ZERO position, the digital control unit functions as described for the USB, LSB detection modes described in paragraph 3.3.2; the BFO output from the BFO synthesizer to the demodulator/AGC amplifier is fixed at 455 kHz . With the BFO OFFSET switch in the VAR position, the BFO offset can be 8.0 kHz above or below the 455 kHz BFO output. BFO up/down counters U8 and U9 function as described in paragraph 3.3.2.

In the CW detection mode with BFO OFFSET switeh 55 in the VAR position, ground potention at wiper arm C2 of detection mode switch S3 is made available to wiper arm C1 of BFO OFFSET switch S5 via contact point 9 of switch S3. In the VAR position, this ground potential, or low, is input to the digital control unit through pin 11 of connector J2. From pin 11, it is input to pin 1 of OR gate U11. With TUNE RATE/Hz switch S4 in the BFO position, ground potential at wiper arm C1 of deck A of switch S4 is input to the digital control unit through pin 2 of connector J2. From pin 2, it is input to pins 2 and 13 of quad OR gate U11.

The lows at pins 2 and 1 of OR gate U11 result in a low output at pin 3 which is applied to pin 1 of AND gate U19 and to pin 13 of NOR gate U13. The low output from U19 is applied to pin 13 of AND gate U19, to the base of BFO decimal switch Q2 causing it to conduct, and to pin 1 of inverter U12, which produces a high to the base of frequency decimal switch Q4 causing it to shut off. The high output from Q2 is output from the digital control unit to the display driver via pin 13 of connector P1. The low at input pin 13 of U19 results in a low output at pin 11 of U19 to the select input pin, pin 1, of multiplexers U20 and U21 where, along with lows on their enable pins, pin 15, disables their B inputs and enables their A inputs. The low output from pin 11 of U19 is also applied to pin 8 of NOR gate U13 which, when tuning a BFO offset below 455 kHz , produces a high output to pin 11 of AND gate U13. This high at pin 11 along with the highs at pins 12 and 13 result in a high output from pin 10 of U13 which is inverted by NOR gate U14 and applied to the base of sign control switch Q3, causing it to conduct and produce a high at pin 25 of connector P1. This high at pin 25 is input to the display driver and output to display assembly numeric display DS-4 via pin 3 of connector P4 causing segment g of the seven-segment display to light which denotes a minus sign.

When up tuning, the high output from pin 10 of OR gate U14 is input to up/down input pin 10 of counters U8 and U9, and to pin 5 of AND gate U19. With counter U9's Q4 output low (except when producing a digital 8) applied to pin 6 of AND gate U19, a low output from pin 4 to pin 12 of NOR gate U13 results. This low, along with the low at pin 13 from pin 3 of OR gate U11, results in a high output from pin 11 of U13 to pin 12 of NOR gate U14. With input pin 13 of U14 at ground potential, U14 acts as a simple inverter producing a low input at carry input pin 5 of counter U8, enabling the clock input. The circuit from pin 2 of counter U9, just described, functions as an 8.0 kHz limiter for the BFO in the following manner.

With a BFO offset of 8.0 kHz , the Q1 through Q4 outputs of U8 and Q1 through Q3 of U9 are low. The high at the Q4 output, pin 2, of counter U9 is applied to pin 5 of AND gate U18 and to pin 6 of AND gate U19. The high at pin 5 of U18 is subsequently output from the digital control unit via pin 9 of U21 and pin 29 of connector P1 through driver U5 on the display driver assembly, deseribed in paragraph 3.4, to seven-segment display DS5 on the display assembly, described in paragraph 3.5. The high at pin 6 of U19 and the high at pin 5 of U19 result in a high output from pin 4 of U19 to pin 12 of NOR gate U13. The resultant low output from pin 11 of U13 is inverted by NOR gate U14. The high output from pin 11 of U14 is applied
to carry input pin 5 of counter U8, inhibiting the clock input, pin 15, and preventing U8 from incrementing.

When down-tuning the BFO offset in the 8 kHz to 0 kHz range, the output from pin 13 of sign flip-flop U22 remains high while the output from pin 1 of direction flip-flop U22 goes low. This places a low input at pin 9 and a high at pin 8 of NOR gate U14. The resultant low output from pin 10 of U14 is applied to up/down pin 10 of counters U8 and U9 causing U8 to decrement by one for each received clock pulse at pin 15.

When counters U8 and U9 have decremented to zero, the carry output, pin 7, from U9 changes from high to low. The low output from pin 7 of U9 is input to pins 5 and 6 of NOR gate U13 resulting in a high output at pin 4 of U13. This high is applied to input pins 1 and 12 of quad AND gate U16. The highs at pin 1 and pin 2 of U16 result in a high at reset input pin 10 of sign flip-flop U22 causing it to change state with a high output at pin 12 and a low at pin 13. The high output from pin 12 is output from the digital control unit via pin 14 of connector E1. Conversely, the low output from pin 13 to the BFO synthesizer via pin 13 of connector E1 goes low.

The low output from pin 13 of sign flip-flop U22 is applied to pin 8 of NOR gate U14 and to pin 9 of NOR gate U13. The low at pin 8 of U14, along with the low at pin 9 of U14, results in a high output from pin 10 to the up/down inputs of U8 and U9. The low at pin 9 of NOR gate U13 along with the low at pin 8 result in a high to pin 11 of AND gate U15. This high at pin 11, along with the highs at pins 12 and 13 , results in a high to input pin 5 of NOR gate U14 which acts as a simple inverter. The resultant low output from U14 causes signal control switch Q3 to turn on, placing a high at pin 25 of connector P1. This high at pin 25 is used to turn on segment $g$ of seven-segment display DS-4, indicating a minus sign.

This assembly converts tuning knob rotation to digital pulses for the Manual Tuning Up/Down Counter. When the tuning knob is turned, each of the two output lines from the encoder will swing repeatedly between approximately +5 V and 0 V . If the knob is rotated at constant speed, these two outputs will appear as trains of square waves. Due to the internal mechanics of the encoder, the transitions of these two wave trains will be staggered in time with respect to each other. When the knob is rotated clockwise to increase tuned frequency, the square wave on the direction line will appear to lead that on the clock line as in Figure 3-25. The action of the up/down counter depends on the level of its up/down input at the instant its clock line goes high. The level of the up/down input at any other time has no effect. Therefore, clockwise rotation causes the counter to count up and the tuned frequency to increase.

If the tuning knob is rotated counterclockwise, the sequence of outputs is reversed; the direction square wave lags the clock square wave. In this case, the direction line will be low when the clock line swings high, causing the counter to count down, thus reducing the tuned frequency.

The two outputs of the encoder go through approximately 120 cycles per revolution of its input shaft.

The encoder assembly uses infrared optics to accomplish its internal functions. It is not considered a repairable assembly.

### 3.3.4 Preselector Decode

The preselector decode employs a bipolar 2048 bit ROM, U10, to convert the selected digitally formatted frequency data from the Up/Down counter, into a preselector code for use by the digital control circuitry.

With a selected tuned frequency of 4.0 MHz , the inputs to ROM U3 are as follows:

| A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

With the binary inputs to ROM U3 grouped by powers of ten as follows:

|  | $10^{7}$ |  | $10^{6}$ |  |  |  | $10^{5}$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $2^{1}$ | $2^{0}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ | $2^{2}$ | $2^{2}$ | $2^{1}$ |
|  | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0, |
| an input of |  |  |  |  |  |  |  |  |  |
|  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| is, | $4 \times 10^{6}$ or, 4 MHz . |  |  |  |  |  |  |  |  |

ROM U3 converts these inputs into a 4 -bit preselector code of 0110 . The 0110 preselector code is applied to the input of the digital control circuitry.

## 3.4 <br> TYPE 796105 DISPLAY DRIVER ASSEMBLY (A7)

The display driver assembly, Figure 3-11, consists of seven BCD-to-7-segment latch decoder drivers which decode the BCD encoded frequency word data from the digital control unit, described in paragraph 3.3. The decoded data is then output from the display driver assembly to the display assembly, described in paragraph 3.5, via the seven output lines associated with each of the seven display drivers.

The frequency and BFO offset frequency data are input to the display driver assembly from the digital control unit, described in paragraph 3.3, via connector J9. When used as drivers for the frequency display, in MHz , driver U1 represents the most significant digit (MSD) and U7 represents the least significant digit (LSD). When used in the BFO offset mode, driver U5 represents the MSD and U6, the LSD.

Table 3-2 lists the relationships between inputs to, and outputs from, drivers U1 through U7, along with the various decimal numerals which may be decoded by the drivers and displayed on the display assembly. As can be determined from the table and Figures 6-23 and $6-24$, driver U1, which employs only the 1 and 2 BCD input, can only decode and display a 0,1 , 2, or be blank. In the lock mode, with TUNE RATE/Hz switch S4 in the LOCK position, or in the BFO variable mode, a low is put to the blanking ( $\overline{\mathrm{BL}}$ ) input pins of drivers U1 through U4 and U7, blanking their outputs. Blanking of drivers U5 and U6 is performed by multiplexers U20 and U21 on the digital control unit.


Figure 3-11. Display Driver, Block Diagram

Table 3-2. Display Driver Input to Output Relationships

| Inputs to U1 through U7 |  |  |  |  | Outputs from U1 through U7 |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Decimal | $\begin{gathered} \text { Pin } \\ 0 \end{gathered}$ | $\begin{gathered} \text { Pin } \\ \text { C } \end{gathered}$ | $\begin{gathered} \text { Pin } \\ \text { B } \end{gathered}$ | $\underset{\mathrm{A}}{\mathrm{Pin}}$ | $\begin{gathered} \text { Pin } \\ \mathrm{g} \end{gathered}$ | $\begin{gathered} \text { Pin } \\ \mathrm{f} \end{gathered}$ | $\begin{gathered} \text { Pin } \\ \mathrm{e} \end{gathered}$ | $\begin{gathered} \text { Pin } \\ \mathrm{d} \end{gathered}$ | $\begin{gathered} \text { Pin } \\ \mathrm{c} \end{gathered}$ | $\underset{b}{\text { Pin }}$ | $\begin{gathered} \text { Pin } \\ a \end{gathered}$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 3 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 4* | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 5* | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 6* | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 7* | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 8* | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9* | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

* Does not apply to MSD driver U1.


### 3.5 TYPE 796104 DISPLAY ASSEMBLY (A8)

The display assembly consists of seven 7-segment LED displays with each display capable of displaying a single decimal digit.

The decoded frequency and BFO offset frequency data are input to displays DS1 through DS7, from the display driver assembly, described in paragraph 3.4, via their respective 7 -pin connectors, P1 through P7. When used to display receiver tuned frequeney, in MHz, DS1 represents the MSD and DS7 represents the LSD. In this mode of operation, a decimal point is displayed on DS2. When used in the BFO offset mode, DS5 represents the MSD and DS6, the LSD. In this mode of operation, a decimal point is displayed on DS5 and displays DS1 through DS3 and DS7 are blank. When the BFO offset frequency is in the range between 455 kHz and 447 kHz , a minus sign is displayed on DS4.

Table 3-3 lists the relationships between the inputs from the display driver assembly via connectors P1 through P7 and the displayed digit.

### 3.6 SYNTHESIZER SECTION

### 3.6.1 SYNTHESIZER RELATIONSHIPS

Figure 3-1 shows the relationship of the synthesizers to the receiver signal processing. Together, three synthesizers translate all RF input signals to 455 kHz . Other stages of the receiver then demodulate this 455 kHz IF. If the receiver operates in the CW or a sideband mode, a fourth synthesizer signal beats with the 455 kHz IF to produce an audio output. The tuning process involves the 1st and 2 nd LO ; the 3 rd LO is fixed at 11.155 MHz and the BFO varies $\pm 8.0 \mathrm{kHz}$ from 455 kHz .

Table 3-3. Display Input to Segment Relationships

| Decimal/ Indication | Inputs via P1 through P7 |  |  |  |  |  |  | Display Segment Lights |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\underset{3}{\operatorname{Pin}}$ | $\mathrm{Pin}_{4}$ | $\begin{gathered} \text { Pin } \\ 2 \end{gathered}$ | $\begin{gathered} \text { Pin } \\ 1 \end{gathered}$ | $\begin{gathered} \text { Pin } \\ 5 \end{gathered}$ | $\begin{gathered} \text { Pin } \\ 6 \end{gathered}$ | $\mathrm{Pin}_{7}$ |  |  |  |  |  |  |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | - | F | E | D | C | B A |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | - | - | - | - | C | B - |
| 2 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | G | - | E | D | - | B A |
| 31 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | G | - | - | D | C | B A |
| ${ }_{1}^{1}$ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | G | F | - | - | C | B - |
| 51 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | G | F | - | D | C | - A |
| ${ }_{6}{ }_{1}$ | 1 | 1 | 1 | 1 | 1 | 0 | 0 | G | F | E | D | C | - - |
| ${ }_{7}{ }_{1}^{1}$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | $-$ | - | - | - | C | B A |
| 81 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | G | F | E | D | C | B A |
| 9 | 1 | 1 | 0 | ${ }^{0}$ | 1 | 1 | 1 | G | F | - | - | C | B A |
| Blank | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | - | - | - | - | - |
| ${ }^{2}$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | G | - | - | - | - | - |

The 1st LO tunes from 42.91 MHz to 72.90 MHz , in 10 kHz steps. This range corresponds to an RF input range of 00.00000 MHz to 29.99999 MHz . Each 10 kHz step of the 1st LO causes a different 10 kHz section of the RF spectrum to be converted to the center of the 1st IF range ( 42.90 MHz to 42.91 MHz ) by taking the difference products from the 1st Mixer. A filter follows the 1st mixer which passes signals in this 10 kHz range, plus their sidebands which extend approximately 9 kHz beyond each end of this range, for a total bandwidth of 28 kHz .

The 2 nd LO tunes from 32.21000 MHz to 32.20001 MHz , in 10 Hz steps. This range allows conversion of any signal in the 1st IF range to the center frequency of the 2nd IF $(10.7 \mathrm{MHz})$, by the 2 nd Mixer. A 16 kHz bandpass filter follows the 2nd Mixer to set the receiver's maximum IF bandwidth. As the receiver is tuned upward, the 2nd LO tunes downward across its entire range, then returns to its starting frequency as the 1st LO steps up to its next increment. This interlocking sweep action allows any 10 Hz increment of the RF range to be converted to the center of the 10.7 MHz 2 nd IF passband.

The 3rd LO provides an 11.15500 MHz signal to the 3rd Mixer. Signals centered on 10.7 MHz output from the 2 nd Mixer mix with the signal from the 3rd LO to produce signals centered at 455 kHz . The output from the 3 rd Mixer passes through another bandpass filter either to be demodulated by other stages in the receiver or mixed with the BFO output for CW or Sideband detection.

The BFO Synthesizer produces a signal ranging from 447 kHz to 463 kHz . This range centers about $455 \mathrm{kHz}( \pm 8.0 \mathrm{kHz})$ and beats with the 455 kHz signal from the 3rd Mixer to produce an audio output.

All four synthesizer circuits are synchronized by a common Time Base. Reference frequencies of $1 \mathrm{MHz}, 50 \mathrm{kHz}, 20 \mathrm{kHz}, 8 \mathrm{kHz}, 5 \mathrm{kHz}$ and 1 kHz are supplied from a 2 MHz temperature compensated erystal oscillator (TCXO).

Table 3-4 provides an example of frequency translation from the RF input to the output of the 3rd Mixer. This translation begins with an RF input signal of 00.00000 MHz (column A) and ends with a signal centered at 455 kHz . Columns B and C are tabulated for input frequencies of 00.00500 and 00.01999 MHz , respectively. In column C, notice that the 1st LO has stepped up to its second increment ( 42.92 MHz ).

The 2nd Mixer translates the signals in the 1st IF range to the 2nd IF frequency of 10.7 MHz . The 9.99 kHz range of the 2nd LO works with the increment sizes of the 1st LO to provide a translation of all 1st IF signals to 10.7 MHz . The corresponding 2 nd LO frequencies are shown in Table 3-4 along with the resultant 2 nd IF of 10.7 MHz . To determine the 1st LO and 2nd LO frequencies corresponding to a received RF frequency, refer to the examples in Table 3-5.

Table 3-4. 1st and 2nd LO Tuning Increments

|  | RF INPUT | $\begin{gathered} \text { A } \\ (0.00000 \mathrm{MHz}) \end{gathered}$ | $\begin{gathered} \text { B } \\ (0.00500 \mathrm{MHz}) \end{gathered}$ | $\begin{gathered} \mathrm{C} \\ (0.01999 \mathrm{MHz}) \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: |
| 1st | 1st LO | 42.91000 | 42.91000 | 42.92000 |
| MIXER | RF INPUT | -00.00000 | -00.00500 | -00.01999 |
|  | 1st IF | 42.91000 | 42.90500 | 42.90001 |
| 2nd | 1st IF | 42.91000 | 42.90500 | 42.90001 |
| MIXER | 2nd LO | -32.21000 | -32.20500 | -32.20001 |
|  | 2nd IF | 10.70000 | 10.70000 | 10.70000 |
| 3rd | 3 rd LO |  | 11.15500 |  |
| MIXER | 2nd IF |  | $\xrightarrow{-10.70000}$ |  |
|  | 3 rd IF |  | 0.45500 |  |
| 4th | 3 rd IF |  | AI |  |
| MIXER | BFO |  | $\pm 8.0 \mathrm{kHz}$ DE | ULATOR |
|  | AUDIO |  | $\pm 8.0 \mathrm{kHz}$ |  |

The 3rd Mixer converts the 10.7 MHz 2 nd IF to 455 kHz . A fixed 3 rd LO frequency of 11.15500 MHz provides the necessary difference frequency for this conversion. The 3rd IF resultant is shown only in column B. Demodulation of the 3rd IF takes place either in the 4th Mixer (product detector) or in the AM or FM demodulation stages of the receiver.

In the CW detection mode, the product detector combines the 455 kHz signal from the 3rd Mixer with the $455 \pm 8.0 \mathrm{kHz}$ variable BFO signal. The resultant signal is an audible tone for monitoring. For single sideband demodulation, the BFO signal is fixed at 455 kHz , and is mixed with the filtered 3rd IF sideband to produce an audio signal.

### 3.6.2 PHASE LOCK LOOPS

### 3.6.2.1 General

The phase lock loop is the method used in this receiver to provide accurate numerical control of the local oscillator frequencies. This technique allows the oscillators to be controlled by any appropriate source of BCD digital data, including remote control sources. The basic phase lock loop is composed of four circuits: a phase detector, a low-pass filter (sometimes called a lead-lag filter, integrator, or loop filter), a voltage-controlled oscillator (VCO), and a frequency divider (counter). A basic phase lock loop configuration is shown in Figure 3-12. Depending on the application, the frequency divider circuit may be fixed (to divide by a certain number), or may be programmable to divide by any number in a specific range ( 20 to 29 , for example). The frequency divider may consist of several counters cascaded together, to provide division by a large number. The operation of the basic phase lock loop requires a stable fixed frequency source, to be used as the reference frequency. This receiver contains a temperature-compensated crystal oscillator (TCXO) to provide the basic reference frequency. Both fixed and programmable loops are discussed in the following paragraphs.

Table 3-5. 1st and 2nd LO Frequencies Versus Tuned Frequency

To Obtain 1st and 2nd LO frequencies for any tuned frequency
Example: 15.75635 MHz

To obtain the 1st LO frequency, use the four most significant digits from the readout.
15.75 XXX

Add 42.91 to these digits

$$
\begin{aligned}
& 15.75 \\
+ & \frac{42.91}{58.66}
\end{aligned}=\underset{\text { frequency }}{\text { 1st }}
$$

To obtain the 2nd LO frequency, use the three least significant digits from the readout.
XX.XX635

Subtract them from 32.21000

$$
-\begin{array}{r}
32.21000 \\
-\quad 0.00635 \\
32.20365
\end{array}=\text { 2nd LO }
$$



Figure 3-12. Basic Phase Lock Loop Configuration

### 3.6.2.2 Basic Phase Lock Loop

The basic phase lock loop technique compares the frequency and phase of an incoming reference signal to the output of the voltage controlled oscillator (VCO). If the two signals differ in frequency and/or phase, an error voltage is generated by the phase detector/filter and applied to the VCO, causing it to correct in the direction required for decreasing the frequency/phase difference. The phase detector produces output pulses which are related to the frequency/phase difference. The filter circuit averages (integrates) these pulses into a proportional error correction voltage. This voltage is applied to control the capacitance of a varicap diode in the VCO circuit, and thus tune the VCO toward the correct frequency. The correction procedure continues until lock is achieved, after which the VCO will track the incoming reference signal.

Dividing a VCO output by two before applying it to the phase detector results in an error voltage that drives the VCO to twice the reference frequency. A divide-by-3 action results in an error voltage that drives the VCO to three times the reference frequency. Thus, the reference frequency is always multiplied by the divider ratio to give the VCO output frequency. From this, the following relationship can be given:

$$
\text { Fveo }=N(\text { Fref })
$$

An example of the basic phase lock loop technique, using numbers, will provide an understanding of its actual operation. Referring to Figure $3-13$, the desired frequency is obtained by programming the variable divider through selectable inputs. Assuming the VCO is locked at the desired frequency of 25 MHz , this signal enters the input of the (in this case) divide-by- 25 counter (divider). The counter emits a pulse at its output each time 25 pulses enter its input. Therefore, the 25 MHz input results in an output of 1 MHz . This 1 MHz signal is compared to the reference frequency of 1 MHz , indicating a locked situation. If the divider's output had been less than 1 MHz , the phase detector would have produced pulses to drive the VCO to a higher frequency. Similarly, if the divider's output had been greater than 1 MHz , the VCO would have been driven to a lower frequency. An important concept to be noted here is that the phase lock loop's output frequency is dependent upon the selectable inputs of the variable divider.

### 3.6.2.3 Phase Lock Loop Prescaling Technique

A variation of the basic phase lock loop, shown in Figure 3-14, is utilized in the 1st and 2nd LO Synthesizers. The divider portion consists of a two modulus prescaler and two programmable counters. The two-modulus (divider) prescaler accepts the output from the VCO and divides it by one of two numbers ( P or $\mathrm{P}+1$ ). The prescaler in the 1st LO is a divide-by$50 / 51$ counter and the 2nd LO prescaler is a divide-by-100/101 counter. The swallow counter controls the number of times the prescaler divides by $\mathrm{P}+1$. The programmable counter counts the number of pulses from the prescaler. Totally, these three components provide for coarse $(\mathrm{N})$ and fine (A) tuning of the VCO.

In operation, the prescaler divides by $\mathrm{P}+1$, A times. For every $\mathrm{P}+1$ pulse from the prescaler, both the swallow counter and programmable counter are decremented by 1 . The prescaler divides by $\mathrm{P}+1$ until the swallow counter reaches its zero state. At this point, the modulus of the prescaler changes to P and the swallow counter is disabled. The prescaler then divides by $P$ until the remaining count in the programmable counter ( $\mathrm{N}-\mathrm{A}$ ) decrements to zero. At this time the output of the programmable counter emits a pulse while the swallow and programmable counters are reset. The cycle then repeats.


Figure 3-13. Programmable Phase Lock Loop


Figure 3-14. Two-Modulus Prescaling in the Phase Lock Loop

An example of the two-modulus prescaling technique is given in Figure 3-15. For illustration, a VCO output of 153 MHz is desired. Selected into the programmable counter are the two most significant digits, 1 and 5 . Selected into the swallow counter is the least significant digit, 3. Under lock conditions, the divider has an input of 153 MHz and an output of 1 MHz .

To produce a 1 MHz signal from a 153 MHz signal requires a divide ratio of 153 . The table in Figure $3-15$ shows a count sequence with 153 input pulses resulting in one output pulse. Similarly, a 153 MHz input results in a 1 MHz output. The programmable counter emits a pulse every time it counts 15 pulses. With the swallow counter set to three, the prescaler divides-by- 11 three times and then switches to the divide-by- 10 state. At this point, the programmable counter needs 12 input pulses before emitting an output pulse. The prescaler then divides-by- 10 twelve times to finish the count sequence. With 3 counts of 11 ( $3 \times 11=33$ ), and 12 counts of $10(12 \times 10=120)$, one output pulse emits from the programmable counter every 153 input pulses ( $33+120=153$ ).

The two phase lock loop types described are used throughout the WJ-8770 synthesizer section. The 1st LO and part of the 2nd LO utilize the prescaler configuration while the 3rd LO and another part of the 2 nd LO use a fixed divide-by-N ratio. The BFO uses the two modulus prescaling technique configuration. Common to all the synthesizers in this receiver is the phase detector used. It will be described in detail below.

### 3.6.2.4 Phase Detector

The phase detector used in all of the synthesizers is actually a frequency and phase detector followed by an integrator/amplifier and low-pass filter. Table 3-6 provides some information about the phase detectors used in the synthesizers.

Table 3-6. Receiver's Phase Lock Loop Characteristics

| Synthesizer |  | Phase | Detector | Prog Divider? | VCO <br> Range | Output Freq. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Ref. Des. | Ref. Freq. |  |  |  |
| 1st LO 32 MHz |  | U1 | 20 kHz | YES | $\begin{gathered} 85.82 \underset{32 \mathrm{MHz}}{145.80 \mathrm{MHz}} \\ 3 \mathrm{MHz} \end{gathered}$ | $42.91-72.90 \mathrm{MHz}$ |
|  |  | U1 | 2 MHz | NO |  |  |
| 2nd LO | PROG | U4 | 8 kHz | YES | $168.00-160.01 \mathrm{MHz}$ |  |
|  | OUT | U16 |  | NO | $210.00-200.01 \mathrm{kHz}$ | $\begin{gathered} 32.21-32.20 \mathrm{MHz} \\ 11.155 \mathrm{MHz} \\ 447.1-462.9 \mathrm{kHz} \end{gathered}$ |
| $\begin{aligned} & \text { 3rd LO } \\ & \text { BFO } \end{aligned}$ |  | U15 | 5 kHz | NO | 11.155 MHz |  |
|  |  | U1 | 1 kHz | YES | $4.471-4.629 \mathrm{MHz}$ |  |

The phase detector receives a fixed reference frequency at one input ( R ) and a variable frequency at input (V) from the divider section. The detector responds only to differences between the two inputs and has four output states as shown in Figure 3-16. If the frequency and phase at the $V$ and $R$ inputs match exactly, outputs $U$ and $D$ remain high. If $V$ leads R in phase, U remains high and D goes low. When V and R are different in frequency, the output at V and D varies high and low at a rate proportional to the frequency difference.

| PROGRAM <br> COUNTER | SWALLOW <br> COUNTER | PRESCALER <br> COUNTS | INPUT <br> PULSES |
| :---: | :---: | :---: | :---: |
| 15 | 3 | 0 | 0 |
| 14 | 2 | 11 | 11 |
| 13 | 1 | 11 | 22 |
| 12 | 0 | 11 | 33 |
| 11 | - | 10 | 43 |
| 10 | - | 10 | 53 |
| 9 | - | 10 | 63 |
| 8 | - | 10 | 73 |
| 7 | - | 10 | 83 |
| 6 | - | 10 | 93 |
| 5 | - | 10 | 103 |
| 4 | - | 10 | 113 |
| 3 | - | 10 | 123 |
| 2 | - | 10 | 133 |
| 1 | - | 10 | 143 |
| 0 | - | 10 | 153 |
| 153 INPUT PULSES $=1$ OUTPUT PULSE |  |  |  |



Figure 3-15. Prescaler Dividing Technique


Figure 3-16. Phase Detector Timing Diagram

Under lock conditions, when $V$ and $R$ are identical in phase and frequency, the output pulses from $U$ and $D$ will be extremely narrow spikes. Large frequency differences between V and R will produce wide pulses at the U and D outputs.

The integrator/amplifier and low-pass filter convert the $U$ and $D$ output pulses into a variable voltage-level proportional to the frequency or phase difference between $V$ and $R$. This voltage output is the VCO tuning voltage which is applied to the varicap tuning diode in the VCO tank circuit, thereby controlling the VCO frequency.

### 3.6.3 TYPE 796133 1st LO SYNTHESIZER

The 1st LO Synthesizer utilizes a phase locked loop configuration with the prescaling technique previously described in paragraph 3.6.2.3. The output of the 1st LO tunes in 10 kHz steps from 42.91 MHz to 72.90 MHz . A block diagram of the 1st LO is shown in Figure 3-17.

### 3.6.3.1 Functional Description

The programmable divider, phase detector and low-pass filter of the 1st LO Synthesizer are contained on the main circuit board (Type 796115); the VCO and tuning voltage control circuits are mounted separately, but together with the main circuit board, they form a combined assembly. The phase detector and filter of the 1st LO will be discussed lightly since a detailed description of these circuits can be found in paragraph 3.6.2.4 of the phase locked loop section. Refer to Figure 3-17 for the following discussion.

A two-modulus prescaler (described in paragraph 3.6.2.3) is used at the input to the divide-by-N counter to divide down the frequency of the VCO so that it can be handled by the conventional low-power Schottky counters. The phase detector, U1, compares the 20 kHz reference frequency from the Time Base with the output frequency of the programmable counter. The difference in frequency and phase between these two signals produces a series of short pulses at the output of the phase detector. These pulses are integrated by integrator U2 and the low-pass filter to provide tuning voltage for the VCO. An octal band-switching code, generated by octal encoders U13 and U14 from the divider section, switches the VCO to one of eight tuning ranges spaced 8 MHz apart.

The VCO has 2 inputs and 2 outputs. Inputs are a tuning voltage from the phase detector and a band-switching octal code from the octal encoder. The VCO output frequency operates from 85.82 MHz to 145.80 MHz . This range is sent to the programmable divider of the phase lock loop. The VCO output frequency is also sent to a single divider which reduces the frequency range to 42.91 MHz to 72.90 MHz . This range is output from the VCO board as the 1 st LO signal.

The programmable divider has an input range from 85.82 MHz to 145.80 MHz , in 20 kHz steps, and must divide each of these frequencies down to 20 kHz . This calls for the programmable divider to have a divide ratio of 4291 ( 85.82 MHz divided-by 20 kHz ) to 7290 ( 145.82 MHz divided-by 20 kHz ).

The counters within the programmable divider, U5, U6, U7 and U8, must have a divide range from 4291 to 7290 . The nature of the counting cycle dictates that the counters be preset to 5271 for a divide ratio of 4291 , and to 8270 for a divide ratio of 7290 . The preset inputs to the counters come from the four most significant digits of the tuned frequency and range from 0000 to 2999. BCD adders U7, U8, U9 and U10 are preset to add 5271 to the tuned


Figure 3-17. 1st LO Functional Bloek Diagram
frequency inputs giving the correct preset inputs to the counters $(0000+5271=5271$; $2999+5271=8270$ ).

### 3.6.3.2 Circuit Description

### 3.6.3.2.1 Counting Cycle

The VCO output frequency, 85.82 MHz to 145.80 MHz is too high for the counters to operate properly. Therefore, a high-speed, two modulus prescaler (U4) is used to divide the VCO frequency to a frequency that can be handled by the counters. Prescaler U1 divides by either 10 or 11 .

As shown in Figure 3-17, the counter consists of two parts: a programmable counter (U5, U6 and U7) and a swallow counter (U8). Both counters receive the same clock pulse from the prescaler output. By having the swallow counter control the prescaler, the represented count will decrement by 11 when both the programmable counter and the swallow counter are counting. When the swallow counter reaches terminal count, the prescaler begins dividing by 10 and the swallow counter is disabled for the remainder of the cycle.

Figure $3-18$ depicts the 1 st counting cycle. The prescaler divides by 11 until the swallow counter reaches terminal count. This causes zero detector U3A to go high, setting the prescaler to 10 and disabling the swallow counter. The programmable counter continues to count down until U5 reaches zero. When this occurs, the U6 terminal count (TC) goes low on the next clock pulse ( 10 VCO output pulses), resetting the counters to the preset number on their inputs. Zero detector U3A is also reset, enabling the swallow counter and setting the prescaler to 11 .

Refer to the schematic diagram of the 1st LO, Figure 6-18, to aid in understanding the circuit descriptions presented below.

### 3.6.3.2.2 Prescaler, U4

The prescaler input frequency ranges from 85.82 MHz to 145.80 MHz . The prescaler divides this by 10 when its PE 1 input is high and by 11 when PE 1 is low. When the swallow counter, U3, is enabled, PE 1 is held low and the prescaler divides by 11 . When the swallow counter reaches terminal count, PE 1 goes high and the prescaler divides by 10 for the remainder of the count cycle.

### 3.6.3.2.3 BCD Adders, U9, U10, U11 and U12

The BCD adders, U9, U10, U11 and U12 serve to translate BCD data from the tuned frequency input to the values required for presetting the programmable counter. Each adder receives a BCD digit on its B input lines. BCD data permanently wired in on its A input lines is summed with the B input data. The sum, A + B, is output on the adder's S lines. Each adder has carry out and carry in lines for handling overflows from sums greater than 9 . This allows the four adders to handle four-digit decimal numbers. The A input lines on each adder are permanently wired to the following BCD digits: U9, 5; U10, 2; U11, 7; U12, 1. In this manner, the BCD adders numerically add 5271 to the four-digit number input from the tuned frequency data. The new four-digit number is applied to the preset input lines of the programmable counter.


Figure 3-18. 1st LO Counting Cycle

### 3.6.3.2.4 Programmable Counter, U5, U6 and U7

U5, U6 and U7 are wired as presettable down counters and are synchronously clocked at pin 2 from the prescaler output. The terminal count outputs of each counter are tied to the enable inputs of the following counters. U6 is decremented one count when U7 goes through a terminal count. When U6 has counted down to state zero, its terminal count output is delayed for an additional 100 clock pulses. At this point, U6's Enable T input is brought low by U7, passing U6's delayed terminal count to U5. U5 is decremented one count when it receives U6's terminal count. U5, U6 and U7 count down until U5 reaches a terminal count condition. At this point the reset line is brought low, reloading the counters to their preset values.

### 3.6.3.2.5 Swallow Counter, U8

Swallow counter, U8, is wired as a presettable down-counter and is clocked at pin 2 from the prescaler output. At the beginning of the count cycle, U8 is loaded with its preset value and begins counting down. Each clock pulse from the prescaler decrements U8 by one count. When U8 reaches its terminal count, zero detector U3A brings U8's Enable P input high. This disables the swallow counter for the remainder of the count cycle.

### 3.6.3.2.6 Count Sequence

Table 3-7 illustrates the count-down sequence of the 1st LO divider for two tuned frequency settings, $00.00 \times \mathrm{XX} \mathrm{MHz}$ and 29.99 XXX MHz . For a receiver setting of 00.00 XXX MHz , the first LO counter presets are loaded with 5271 by BCD adders U9, U10, U11 and U12. The swallow counter, U8, and the programmable counter, U5, U6 and U7, are both decremented by 1 prescaler output pulse for each 11 prescaler input pulses. When the swallow counter reaches its terminal count, it is disabled and the prescaler divide mode changes to 10. When the programmable counter reaches terminal count, the cumulative number of pulses into the prescaler equals 4291. Since the loop reference frequency equals 20 kHz , the VCO frequency is 4291 times 20 kHz , or 85.82 MHz . The VCO output to the mixer is divided by 2 , resulting in an actual LO output of 42.91 MHz . This is the 1st LO frequency corresponding to a receiver tuned frequency of 00.00 XXX MHz .

For a receiver setting of $29.99 \times \times X$, the 1 st LO counter presets are loaded with 8270 by BCD adders U9, U10, U11 and U12. Since the swallow counter, U8, is initially loaded with zero, the counting eycle begins with the swallow counter at terminal count and the prescaler divide mode at 10 . The programmable counter, U5, U6 and U7 is decremented by 1 count for each 10 prescaler input pulses. When the programmable counter reaches terminal count, the cumulative number of pulses into the prescaler equals 7290. The VCO output frequency is thus 7290 times 20 kHz or 145.80 MHz . The actual LO output is 72.90 MHz $(145.80 \mathrm{M} \mathrm{Hz}$ 2) which is the 1 st LO frequency corresponding to a receiver tuned frequency of 29.99XXX MHz.

### 3.6.4 TYPE 796107 2nd LO SYNTHESIZER

### 3.6.4.1 Functional Description

The 2nd LO tunes from 32.20001 to 32.21000 MHz in 10 Hz steps. Three phase lock loops are utilized to produce the 2nd LO output. The 2nd LO functional block diagram is shown in Figure 3-19.

Table 3-7. 1st LO Divider Countdown Cycles

| Prescaler | $\begin{array}{r} \mathrm{B} \\ \mathrm{Pr} \\ \hline \end{array}$ | qler | Prescaler Output |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | New | Cum | Pulses | U8 | U7 | U6 | U5 | COMMENTS |
| 11 | 0 | 0 | 0 | 1 | 7 | 2 | 5 | Tuned freq. $=00.00 \times \mathrm{XX} \mathrm{MHz}$ Swallow CTR Terminal Coun |
|  | 11 | 11 | 1 | 0 | 6 | 2 | 5 |  |
| 10 | 10 | 21 | 1 | 0 | 5 | 2 | 5 |  |
|  | 50 | 71 | 5 | 0 | 0 | 2 | 5 |  |
|  | 10 | 81 | 1 | 0 | 9 | 1 | 5 | U4 Terminal Count <br> U5 Terminal Count Disabled |
|  | 100 | 181 | 10 | 0 | 9 | 0 | 5 |  |
|  | 90 | 271 | 9 | 0 | 0 | 0 | 5 |  |
|  | 10 | 281 | 1 | 0 | 9 | 9 | 5 |  |
|  | 900 | 1181 | 90 | 0 | 9 | 0 | 4 | U5 Terminal Count Disabled |
|  | 90 | 1271 | 9 | 0 | 0 | 0 | 4 |  |
|  | 10 | 1281 | 1 | 0 | 9 | 9 | 3 |  |
|  | 900 | 2181 | 90 | 0 | 9 | 0 | 3 | U5 Terminal Count Disabled |
|  | 90 | 2271 | 9 | 0 | 0 | 0 | 3 |  |
|  | 10 | 2281 | 1 | 0 | 9 | 9 | 2 |  |
|  | 900 | 3181 | 90 | 0 | 9 | 0 | 2 | U5 Terminal Count Disabled |
|  | 90 | 3271 | 9 | 0 | 0 | 0 | 2 |  |
|  | 10 | 3281 | 1 | 0 | 9 | 9 | 1 |  |
|  | 900 | 4181 | 90 | 0 | 9 | 0 | 1 | U5 Terminal Count Disabled |
|  | 90 | 4271 | 9 | 0 | 0 | 0 | 1 |  |
|  | 10 | 4281 | 1 | 0 | 9 | 9 | 0 |  |
|  | 10 | 4291 | 1 | 1 | 7 | 2 | 5 | U6 Terminal Count Reload |
|  | $\stackrel{4291}{=85}$ | MHz |  |  |  |  |  |  |
| 10 | 0 | 0 | 0 | 0 | 7 | 2 | 8 | Tuned freq. $=29.99 \times \times \mathrm{XX} \mathrm{MHz}$ |
|  | 70 | 70 | 7 | 0 | 0 | 2 | 8 |  |
|  | 10 | 80 | 1 | 0 | 9 | 1 | 8 |  |
|  | 90 | 170 | 9 | 0 | 0 | 1 | 8 |  |
|  | 10 | 180 | 1 | 0 | 9 | 0 | 8 | U5 Terminal Count Disabled |
|  | 90 | 270 | 9 | 0 | 0 | 0 | 8 |  |
|  | 10 | 280 | 1 | 0 | 9 | 9 | 7 |  |
|  | 900 | 1180 | 90 | 0 | 9 | 0 | 7 | U5 Terminal Count Disabled |
|  | 90 | 1270 | 9 | 0 | 0 | 0 | 7 |  |
|  | 10 | 1280 | 1 | 0 | 9 | 9 | 6 |  |
|  | 5900 | 7180 | 590 | 0 | 9 | 0 | 1 | U5 Terminal Count Disabled |
|  | 90 | 7270 | 9 | 0 | 0 | 0 | 1 |  |
|  | 10 | 7280 | 1 | 0 | 9 | 9 | 0 |  |
|  | 10 | 7290 | 1 | 0 | 7 | 2 | 8 | U6 Terminal Count Reload |
|  | $\frac{7290}{=14}$ | $\frac{\mathrm{kHz}}{\mathrm{MHz}}$ |  |  |  |  |  |  |



Figure 3-19. 2nd LO Functional Block Diagram

The 32 MHz loop receives a 2 MHz reference signal and translates it into a 32 MHz reference signal. The programmable loop receives an 8 KHz reference signal and tuning preset data from the digital control section, producing an output frequency of 160.01 to 168.00 MHz . A divide-by- 800 divider stage reduces this output to 200.01 to 210.000 kHz . The output loop combines the 32 MHz signal and the 200.01 to 210.00 kHz signal to produce the 32.20001 to 32.21000 MHz 2nd LO output signal.

An explanation of the 2nd LO output loop operation will clarify the overall operation of this synthesizer. The phase detector, U16, will be satisfied when the mixer output is equal in phase and frequency to the divide-by -800 divider output. The phase detector achieves this condition by shifting the VCO so the difference between the 2nd LO output frequency and the 32 MHz reference frequency is equal to the divider output frequency.

### 3.6.4.2 Circuit Description

The 2nd LO will be discussed in the following order: 32 MHz loop, programmable loop and output loop. Refer to the 2nd LO schematic diagram, Figure 6-20, as an aid in understanding eircuit operation.

The 32 MHz loop uses the basic configuration shown in Figure 3-12. VCO output from Q1 is applied to buffer Q2. Output from Q2 is tapped and routed through divide-by- 16 counter U3, dividing the 32 MHz VCO output down to 2 MHz . This signal and the 2 MHz reference signal from the time base are compared in phase detector U1. The de voltage from U1 varies the capacitance of varactor diode CR1, which varies the oscillation frequency of VCO Q1. Q2 is a buffer amplifier with two isolated outputs. One output drives divider U3 as stated above. The other output is applied to mixer U15. In operation, phase detector U1 maintains the divider output frequency equal to the 2 MHz reference frequency by holding the VCO precisely at 32 MHz .

The programmable phase lock loop incorporates a two-modulus prescaler, swallow counter, phase detector, filter and VCO. The output from this loop at Q8 is applied to U6 and U9. U9 and U10 form a two-modulus prescaler with divide ratios of 100 and 101 . U10 divides by 11 when $\overline{\mathrm{PE1}}$ and $\overline{\mathrm{PE} 2}$ are both held low. This will occur only during the swallow counting sequence when $\overline{\text { PE1 }}$ is held low by U12. At the beginning of the counting sequence, $\overline{\text { PE1 }}$ is low and $\overline{\mathrm{PE} 2}$ is held high by U10. U9 divides by ten for 90 input pulses from the VCO and passes nine pulses to U10's CLK input. At this point, U10's TC output goes low for one input pulse, simultaneously bringing $\overline{\text { PE2 }}$ on U9 low. This enables U9 to divide by 11 once. Dividing by 10 nine times $(9 \times 10)$ and dividing by 11 once $(1 \times 11)$ results in a divide ratio of $101(90+11)$. This division of 101 continues until the swallow counter, U11 and U12, reaches terminal count. At this point, U12 brings $\overline{\mathrm{PE1}}$ on U9 high, and the prescaler divides by $100(9 \times 10+1 \times 10)$ for the remainder of the counting cycle.

The swallow counter consists of U11 (a decade counter) and U12 (a binary counter). The counter can be loaded with any number between 00 and 99 , inclusive. During a load pulse, U 11 and U 12 are loaded to their preset values. U12's $\mathrm{Q}_{\mathrm{B}}$ and $\mathrm{Q}_{\mathrm{D}}$ outputs both go low, bringing PEI on U9 low. This sets the prescaler to divide by 101 as described above. When U12 reaches state $1010, \mathrm{Q}_{\mathrm{B}}$ and $\mathrm{Q}_{\mathrm{D}}$ go high, bringing $\overline{\mathrm{PE}}$ on U 9 high and setting the prescaler to divide by 100. At the same time, the U11 and U12 EN $\overline{\mathrm{P}}$ inputs are brought high, disabling the swallow counter for the remainder of the count cycle. Because U11 and U12 operate in an up-counting mode, U1 will be in state 0000 when U12 is clocked to state 1010 . This sets the terminal count for the swallow counter at $100(10+0)$.

The main programmable counter consists of binary counter U13 and U14. U13 can be loaded with any value between 0 and 9 , and U14 is always loaded with 2. During a counting cycle, U13 and U14 count up synchronously until terminal count is reached at U14. At this point, U14 and U13 are at states 15 and 1 respectively. The 15 in the second digit (U14) is worth $240(15 \times 16)$ so the terminal count is 240 (U14) +1 (U13) $=241$. Each count of the programmable counter is equal to 100 counts of the overall divider chain, so the actual terminal count for the programmable counter is $241 \times 100=24100$.

Combining the terminal counts of the swallow and programmable counters will yield the overall terminal count. The swallow counter terminal count is 100 and for the programmable counter is 24100 . Terminal count for the whole chain is $24100+100=24200$. The programmable counter is always loaded with 32 plus the preset input to U13. The swallow counter is loaded with the preset inputs to U11 and U12. The overall divider chain is therefore loaded with $3200(32 \times 100)$ plus the inputs to U13, U12 and U11.

Assume 000 is loaded into the 2nd LO. The preset input is $3200+000=3200$. The divide ratio is $24200-3200=21000$. Assume 999 is loaded. The preset input is $3200+999=4199$ and the divide ratio is $24200-4199=20001$.

The output of the programmable loop VCO enters the counter at pin 16 of U9 and exits at pin 11 of U14. The VCO signal is divided by 21000 for a tuned frequency of XX.XX000 MHz and by 20001 for a frequency of XX.XX 999 MHz . The divided output goes to phase detector U4 where it is compared with the 8 kHz reference from the Time Base. The phase detector output is filtered by U5 and applied to varactor diode CR4 in the VCO circuit. In actual operation, phase detector $\mathrm{U4}$ controls the VCO frequency so the divided output frequency equals 8 kHz , the reference frequency. For a dial setting of XX.XX000 the VCO frequency is $8 \mathrm{kHz} \times 21000=168.00 \mathrm{MHz}$ and for a dial setting of XX.XX999, the VCO frequency is $8 \mathrm{kHz} \mathrm{x} \mathrm{20001}=160.01 \mathrm{MHz}$.

The VCO output goes through an additional counter composed of U6, U7 and U8. This divide-by- 800 counter divides the VCO output frequency range of $168.00-160.01 \mathrm{MHz}$ down to $210.00-200.01 \mathrm{kHz}$ and applies it to the phase detector U16 in the output loop.

The output loop consists of a phase detector, U16 and U18, a VCO, Q5, Q6 and Q7, and a mixer, U15. The VCO normally operates with an output frequency between 32.20001 MHz and 32.21000 MHz . The VCO output is tapped from the collector at Q5 and applied to mixer U15. The mixer combines the VCO signal with the 32 MHz reference signal and produces a difference frequency range of 200.010 kHz to 210.000 kHz . The phase detector, U16, receives inputs from the mixer and the programmable loop. The output from the phase detector is filtered by U18 and applied to varactor diode, CR3, in the VCO.

Operation of the output loop is as follows: With a dial setting of XX.XX000, the output from the programmable loop is 210.00 kHz . The phase detector, U16, sets the output loop VCO frequency at 32.21000 MHz . The mixer, U15, mixes this frequency with the 32 MHz reference signal, producing an output frequency of 210.00 kHz . The phase detector sees a frequency of 210.00 kHz on both inputs and holds the VCO at 32.21000 MHz . If the dial setting is changed to $\mathrm{XX} . \times \times 999 \mathrm{MHz}$, the programmable loop output frequency changes to 200.01 kHz . The phase detector changes the VCO frequency to 32.20001 MHz , which changes the mixer output to 200.01 kHz . The phase detector now sees a frequency of 200.01 kHz on both inputs and holds the VCO at 32.20001 MHz .

The VCO output signal also enters buffer amplifier, Q7, where it is amplified and output as the 2nd LO signal.

### 3.6.5 TYPE 796109 3rd LO SYNTHESIZER

The 3rd LO Synthesizer is part of the BFO/3rd LO board, 796109. The 3rd LO has an input of two reference frequencies and utilizes a phase lock loop and digital mixer to produce a fixed output frequency of 11.155 MHz .

### 3.6.5.1 Functional Description

Figure $3-20$ is a functional block diagram of the 3rd LO. The YCO is a crystal-controlled oscillator whose output frequency is slightly adjustable by varactor diode CR6. The buffered 11.155 MHz VCO output is converted to square pulses by U 16 and fed to the digital mixer. The digital mixer produces an output frequency equal to the difference between the VCO frequency ( 11.155 MHz ) and the frequency that is the nearest integral multiple of the 50 kHz reference ( $223 \times 50 \mathrm{kHz}=11.15 \mathrm{MHz}$ ). In this case, the difference is 5 kHz . The phase detector compares the digital mixer output with the 5 kHz reference and adjusts the VCO frequency as necessary to hold the digital mixer output at 5 kHz .

### 3.6.5.2 Circuit Description

A detailed description of 3rd LO operation follows. Refer to Figure 6-21, the BFO/3rd LO Schematic Diagram as an aid in understanding the operation of the 3rd LO.

The 11.155 MHz erystal, Y1, in conjunction with Q4, form a crystal-controlled oscillator. Due to the stabilizing effect of Y1, the normal frequency of oscillation of the VCO will be quite close to 11.155 MHz . The actual VCO frequency, however, is determined by the net capacitance, composed of C30, C31 and varactor CR6, in series with Y1.

The VCO output signal from Q4 is amplified by Q5, a broad-band buffer amplifier. This isolates the VCO and boosts the VCO signal level. The buffer amplifier provides two separate, isolated outputs: the signal at the collector is tapped and leaves the 3rd LO board as the 3rd LO output signal; the signal at Q5's emitter is tapped and fed to the sine-TTL converter, U16.

U16A is wired as a Schmitt-trigger inverter. The sine wave VCO signal from Q5 enters U16A and is changed to square wave pulses by virtue of the "snap-action" hysteresis of the Schmitt-trigger. U16B is wired as an inverter and serves to sharpen up the edges of the square wave output from U16A.

The digital mixer, U14A, is a D-type flip-flop. The inputs to the digital mixer are the 50 kHz reference and the square-wave 11.155 MHz VCO signal from the sine-TTL converter. The output, $\bar{Q}$, of U14A, is a square wave whose frequency is the difference between the flip-flop D-input frequency ( 11.155 MHz ) and the nearest integral multiple of the clock input frequency ( 50 kHz reference). In this case the difference is 11.155 MHz $(223 \times 50 \mathrm{kHz})=5 \mathrm{kHz}$. The 5 kHz output from the digital mixer is fed to the phase detector, U15.


Figure 3-20. 3rd LO Functional Block Diagram

The phase detector, U15, compares the 5 kHz output from the digital mixer with the 5 kHz reference signal. Any difference in frequency or phase between the two inputs is reflected as a change in the pulse output of U15. After suitable filtering, the pulse output from U15 is a de voltage which is applied to varactor diode, CR6, in the VCO circuit. By controlling the de voltage on CR6, the phase detector can vary the VCO frequency so as to maintain its frequency of oscillation at 11.155 MHz and thus keep the output of the digital mixer at 5 kHz .

### 3.6.6 TYPE 796109 BFO SYNTHESIZER

The BFO Synthesizer is part of the BFO/3rd LO board, 796109. This synthesizer utilizes the two modulus configuration shown in Figure 3-14 to produce an output of 455 kHz $\pm 8.0 \mathrm{kHz}$.

### 3.6.6.1 Functional Description

A functional block diagram of the BFO is shown in Figure 3-21. The VCO operates at a frequency of 4.470 MHz to 4.630 MHz . A presettable divider with divide ratios of 4470 to 4630 divides the VCO output frequency down to 1 kHz . The actual divide ratio is determined by the BFO preset input from the Digital Control Section. The phase detector compares the divider output with the 1 kHz reference signal and shifts the VCO frequency as necessary to maintain the divider output at 1 kHz . An output divide-by- 10 divider reduces the VCO frequency to between 447.0 kHz and 463.0 kHz as required by the product detector.

### 3.6.6.2 Circuit Description

Refer to the BFO Functional Block Diagram, Figure 3-21, and the BFO Schematic Diagram, Figure 6-21, to aid in understanding the circuit descriptions presented below.

### 3.6.6.2.1 Counting Cycle

A presettable, divide-by- N counter is used to divide the VCO frequency down to 1 kHz . The counter consists of three parts: prescaler, swallow counter and programmable counter.

U12 is a binary up-counter wired as a two-modulus prescaler with divide ratios of ten and eleven. The actual divide ratio is determined by U12's preset inputs which in turn are determined by the state of the swallow counter.

The swallow counter and the programmable counter both receive the same clock pulse for the prescaler output. When the swallow counter is in the counting mode, that is, has not reached terminal count, the prescaler is preset with 11 and operates in the divide-by- 11 mode. When the swallow counter reaches terminal count, the zero detector simultaneously disables the swallow counter and changes the prescaler count to 10 . The prescaler divides by ten for the remainder of the count cycle.

The end of cycle detector is activated when the programmable counter reaches its terminal count condition. At this point, one clock pulse is sent to the phase detector and both counters are reset to their preset values.


Figure 3-21. BFO Functional Block Diagram

### 3.6.6.2.2 Prescaler, U12

The prescaler input frequency ranges from 4.470 to 4.630 MHz . The prescaler divides this by 11 or 10 depending on the state of its preset inputs. U12 is a binary counter, wired to count down. At the beginning of the count cycle, U12's ripple count output loads it with the preset value of 11 . U12 then acts as a divide-by- 11 divider. When the swallow counter reaches terminal count, the zero detector changes U12's preset value to 10 . U12 then acts as a divide-by-10 divider.

### 3.6.6.2.3 Swallow Counter

The BFO Synthesizer swallow counter is formed by U10, a presettable binary up/down counter. U10's preset inputs can be preset from zero to nine by the BFO Offset Frequency Word. At the beginning of the count cycle, U10's "CI" input is held low by the zero detector. Under this condition, the swallow counter and the programmable counter both increment or decrement by one count for each clock pulse from the prescaler. When U10 reaches state zero, the zero detector sees this as a terminal count condition. The prescaler is then changed to divide-by-ten and U10's "CI" input is brought high, disabling the swallow counter for the remainder of the count cycle. At the completion of the count cycle, the reset pulse from the End of Cycle Detector loads U10 to its preset value. The zero detector then brings U10's "CI" input low again, readying the swallow counter for another count cycle.

### 3.6.6.2.4 Programmable Counter

The programmable counter is formed by U7, U8 and U9. U7 and U8 are preset with zero. U9 is preset from the BCD Offset Frequency Word. The three counters are cascaded with a clock input from the prescaler. U9 cascades to U8 and clocks U8 on its 1 to 0 transition when down-counting, or on its 9 to 0 transition when up-counting. U8 cascades to U7 in similar fashion.

The programmable counter counts from the preset values of U7, U8 and U9 down to a terminal count of 545 when down-counting, or up to a terminal count of 455 when up-counting. At terminal count, the End of Cyele Detector sends out a reset pulse which resets the programmable counters to their preset value.

### 3.6.6.2.5 End of Cycle Detector

The terminal counts of both the swallow counter and the programmable counters are detected by the End of Cycle Detector, U3A, U3B, U4A, U4B, U5A, U5B and U6. The End of Cycle Detector monitors the logic state outputs of the programmable counter and the output of the swallow counter zero detector. The detector has three terminal count values: for + offsets with X .0 kHz loaded, terminal count is 4550 ; for + offsets with $\mathrm{X} . \mathrm{X} \mathrm{kHz}$ loaded, terminal count is 4540 ; for all - offsets, terminal count is 5450 . Changes in the detector are programmed by the Offset Sign line.

The programmable and swallow counters begin at their preset values and count up to 4550 for + offsets; for - offsets, they begin at their preset values and count down to 5450 . When terminal count is reached, the output of U4B goes high, clocking flip-flop U3A. The output of U3A, which is the reset pulse, goes high for about one microsecond. It is then reset to zero by R18 and C49 acting on the Reset pin.

### 3.6.6.2.6 Count Sequence

The BFO Synthesizer countdown sequence will now be examined and will facilitate understanding the overall operation. Several BFO offset settings will be discussed for illustrative purposes.

First we will consider " + " offset settings. Under this condition, the Offset Sign line is low, the programmable counter is set for down counting and the End of Cycle Detector is set for a terminal count of 5450 .

Assume an offset setting of +0.0 kHz . The swallow counter will be preset with zero. Thus, at the start of the count cycle, the swallow counter will be disabled and the prescaler set for divide-by-ten. The programmable counter will start from zero and count down to 545. Total pulses from the VCO will be $0(0)+10(000-545)=4550$. VCO frequeney is $(1 \mathrm{kHz}) \times(4550)=4.550 \mathrm{MHz}$.

Assume an Offset setting of +7.9 kHz . The swallow counter will start counting from 9 and the programmable counter at 007. Total pulses from the VCO will be $11(9-0)+10((007-545)-9)=4629$. VCO frequency is $(1 \mathrm{kHz}) \times(4629)=4.629 \mathrm{MHz}$.

Next, we will consider "-" offset settings. Under this condition, the Offset Sign line is high, the programmable counter is set for up-counting and the End-of-Cycle Detector is set for a terminal count of 4550 .

Assume an offset setting of $\mathbf{- 0 . 0} \mathrm{kHz}$. The swallow counter will be preset with zero. Thus, at the start of the count cycle, the swallow counter will be disabled and the prescaler set for divide-by-10. The programmable counter will start from zero and count up to 455. Total pulses from the VCO will be $0(0)+10(455-000)=4550$. VCO frequency is $(1 \mathrm{kHz}) \times(4550)=4.550 \mathrm{MHz}$.

Assume an offset setting of -7.9 kHz . The swallow counter will start counting from 9 and the programmable counter from 007. Total pulses from the VCO will be $11(0-9)+10((454-007)-1)=4471 \mathrm{VCO}$ frequency is $(1 \mathrm{kHz}) \mathrm{x}(4471)=4.471 \mathrm{MHz}$.

The VCO signal at Q2 has a frequency range of 4.470 MHz to 4.630 MHz . U13 is a decade counter wired as a divide-by- 10 divider. The output of U13 is the BFO signal with a frequency range of 4470 kHz to 463.0 kHz .

### 3.6.7 TYPE 796111 TIME BASE GENERATOR

### 3.6.7.1 Functional Description

The heart of the Time Base is the 2 MHz temperature compensated crystal oscillator (TCXO), U1. U1 generates a highly stable signal adjustable to within $\pm 1 \mathrm{~Hz}$ of 2 MHz . The 2 MHz signal is run through a series of divide-by -N counters to reduce it to frequencies of $50 \mathrm{kHz}, 20 \mathrm{kHz}, 8 \mathrm{kHz}$ and 5 kHz as required by the various receiver synthesizers. A functional block diagram of the Time Base Generator is presented in Figure 3-22.


Figure 3-22. Time Base Functional Block Diagram

### 3.6.7.2 Circuit Description

Refer to Figure 6-17, Time Base Generator Schematic Diagram. The low-level, temperature-stable 2 MHz signal from U1 is amplified by Q1, which also serves to isolate U1 from the divider circuitry. Q1's output is split three ways: to P1-7 which feeds a 2 MHz reference signal to the 2 nd LO; to dividers U2 and U5A.

U2 is a dual divide-by-N BCD counter. It is wired to function as a divide-by- 25 divider. U2 takes the 2 MHz signal from Q1 and reduces it to 80 kHz . The 80 kHz output from U2 is then sent to U3A and U4A.

U3A is a BCD up-counter wired as a divide-by- 10 divider. It reduces the 80 kHz signal from U2 to 8 kHz . This 8 kHz signal goes to P1-6 where it is fed to the 2nd LO. The 8 kHz signal also goes to U3B which is wired as a divide-by-8 divider. It reduces the 8 kHz from U3A to 1 kHz . This 1 kHz signal goes to P1-5 where it is fed to the BFO Synthesizer.

U4A is a BCD up-counter wired as a divide-by-4 divider. It reduces the 80 kHz signal from U2 to 20 kHz . This 20 kHz signal goes to P1-8 where it is fed to the 3rd LO. The 20 kHz signal also goes to U4B which is wired as a divide-by-4 divider. It reduces the 20 kHz signal from U4A to 5 kHz . This 5 kHz signal goes to P1-4 where it is fed to the 3 rd LO.

U5A is a BCD up-counter wired as both a divide-by-2 and a divide-by-10 divider. The 2 MHz signal from U 2 is fed to the Clock input of U5A. U5A's divide-by-2 output provides a 1.0 MHz signal which goes to J 1 , the 1.0 MHz test output jack. U5A's divide-by-10 output provides a 200 kHz signal which goes to U5B.

U 5 B is a BCD up-counter wired as a divide-by-4 divider. It reduces the 200 kHz signal from U5A to 50 kHz . This 50 kHz signal goes to P1-3 where it is fed to the 3 rd LO.

### 3.6.8 TYPE 796117 SYNTHESIZER MOTHERBOARD

The Synthesizer Motherboard provides for the interconnection of the Digital Control, the three Synthesizer Boards, Time Base and LO outputs. Functionally, the Motherboard accomplishes the following:

1. Inputs Frequency Word Data, BFO Offset Data and control signals from the Digital Control.
2. Distributes Frequency Word Data to 1st and 2nd LO Synthesizers.
3. Routes BFO offset data to the BFO Synthesizer.
4. Distributes control signals to appropriate synthesizers.
5. Distributes Time Base reference signals to appropriate synthesizers.
6. Distributes LO output signals to appropriate receiver mixers.

### 3.6.8.1 Circuit Description

Refer to Figure 6-16, the Synthesizer Motherboard Schematic Diagram. Tuned frequency data enters the Motherboard on J2, pins 1-18 and 27-40. BFO Offset Frequency Data enters on J2, pins 19-26. The Tuned Frequency and BFO offset data pass through the Motherboard in a bus format and exit as BCD Output Data on J1.

The 1st LO plugs into A2P1 on the Motherboard and receives Tuned Frequency Data from J2, pins 15-18 and 27-40. The 2nd LO plugs into A3P1 and A3P2 on the Motherboard and receives Tuned Frequency Data from J2, pins 1-12. The 3rd LO/BFO plugs into A4P1 and A4P2 on the Motherboard. The BFO receives Offset Frequency Data from J2, pins 13 and 19-26.

The Time Base plugs into A1P1 on the Motherboard and distributes the following reference signals to the Synthesizers: 20 kHz to the 1 st LO; 2 MHz and 8 kHz to the 2 nd LO ; 50 kHz and 5 kHz to the $3 \mathrm{rd} \mathrm{LO} ; 1 \mathrm{kHz}$ to the BFO.

The output signals from the 1st and 2nd LO's come directly from their assemblies and do not route through the Motherboard. The BFO output goes through J8 on the Motherboard and the 3rd LO output goes through J9.

### 3.6.9 TYPE 796139 POWER SUPPLY

The Power Supply receives $+22-32$ Vdc from an external power pack and converts it to the +5 Vdc and the $\pm 15 \mathrm{Vdc}$ required by the various receiver circuits.

### 3.6.9.1 Circuit Description

Refer to Figure 6-26, Power Supply Schematic Diagram. Direct current voltage in the range of +21 to +32 Vdc is input to the receiver via J1 on the rear panel. The de voltage is applied to de-to-de converters PS1 and PS2.

PS1 is designed to operate at a nominal input voltage of +24 Vde , although it will operate satisfactorily with input voltages as low as +21 Vdc . PS1 converts the input voltage to a square wave which is fed to a step-down toroidal transformer. The transformer output is rectified and filtered by L1 and C2 to produce a ripple-free +5 Vde output.

Zener diode VR1 and transistor Q1 collectively form an input voltage regulator. For input voltages between +24 and +32 Vde, VR1 is clamped, maintaining the input voltage to PS1 at +24 Vdc . By so regulating the input voltage, the +5 Vdc output is maintained within acceptable limits.

PS2 also operates with a nominal input of +24 Vdc . PS2 converts the input voltage to a square wave which is fed to a step-up toroidal transformer with a center-tapped primary. A bridge rectifier converts the transformer output to + and - de voltages with the center tap as ground. The + and - voltages are filtered by L2 and C5, and L3 and C8, to produce ripple-free $\pm 15$ Vde outputs.

VR2 and Q2 operate as VR1 and Q1 above to form an input voltage regulator. The input to PS2 is clamped at +24 Vdc for input voltages between +24 and +32 Vdc. Regulating the input maintains the $\pm 15$ Vde outputs within acceptance limits.

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## SECTION IV

MAINTENANCE

### 4.1 GENERAL

This section contains maintenance information and procedures for the WJ-8770 HF Receiver. Included are preventive maintenance procedures, performance verification tests, troubleshooting and fault isolation procedures, repair information and alignment procedures. The troubleshooting procedures in this section are of sufficient depth to allow fault isolation to the component level.

### 4.2 TEST EQUIPMENT REQUIRED

All test equipment required to perform the maintenance procedures given in this section are listed in Table 4-1. Equivalent test equipment may be substituted for that listed.

### 4.3 TEST FACILITIES

The following items describe the minimum test facility requirements for performing maintenance of the WJ-8770 HF Receiver.

1. Power - A primary source of ac power capable of supplying 115 Vac at 5.0 amperes minimum is required to operate the test equipment. A source of de power capable of supplying 22 32 Vde at 0.6 amperes is required to operate the receiver.
2. Work Area - A test bench is required with sufficient area to support the receiver and all required test equipment.
3. Environment - Unless otherwise specified, the following environmental conditions shall be observed.
a. Temperature $-+25^{\circ} \mathrm{C} \pm 5^{\circ} \mathrm{C}\left(+77^{\circ} \mathrm{F} \pm 9^{\circ} \mathrm{F}\right)$
b. Humidity $-90 \%$ Max.
c. Altitude - Room Ambient

## 4.4 <br> PREVENTIVE MAINTENANCE

The receiver has been designed for optimum performance over extended periods of time with minimal maintenance. However, to improve the reliability of the receiver and prevent breakdowns, cleaning, visual inspections, and performance tests should be accomplished as part of a preventive maintenance routine, as outlined in Table 4-2.

Table 4-1. Test Equipment Required

| Instrument Type | Required Characteristics | Recommended Instrument |
| :---: | :---: | :---: |
| Signal Generator | AM, FM, CW, RF output, from -130 dBm to 0 dBm | HP8640B |
| Oscilloscope | de to 50 MHz | HP180C |
| RF Voltmeter | $\begin{aligned} & 1 \mathrm{mV} \text { to } 3.0 \mathrm{~V} ;-50 \mathrm{dBm} \\ & \text { to }+20 \mathrm{dBm} \end{aligned}$ | Boonton 92B |
| Power Supply | 0-40 volts, $0-1.5 \mathrm{Amp}$. | HP-6289A |
| Spectrum Analyzer | $100 \mathrm{kHz}-110 \mathrm{MHz}$ | HP-141T, 8553B, 8552B |
| Digital Counter | 0 to 500 MHz | HP5303A |
| AC Voltmeter | 1 mV to 300 V , full scale | HP-400E |
| DVM | de ranges; $1 \%$ or better | Fluke 8100 A |
| Dummy Load, $600 \Omega$ | 4-W dissipation | Two $1200 \Omega, 2-W$ resistors in parallel |
| Headphones | Mono, $600 \Omega$ impedance | Telex 820-4 |
| Tracking Generator | $100 \mathrm{kHz}-110 \mathrm{MHz}$ | HP-8443A |

Table 4-2, Periodic Maintenance Schedule

| Procedure | Interval | Comments |
| :--- | :---: | :--- |
| Cleaning | 60 days | Interval variable depending on <br> the operating environment. |
| Lubrication | 60 days | Interval variable depending <br> on equipment use. |
| Performance Tests | 180 days | Interval variable depending <br> on operating environment <br> and equipment use. |
| Interval variable depending <br> on operating environment <br> and equipment use. |  |  |
| Adjustment/Alignment | -- | Adjustment/Alignment <br> keyed to results of <br> Performance Tests. |

### 4.4.1 CLEANING

Cleaning should be performed to remove accumulated dust, grease, and other contamination, and to ensure trouble-free operation.

## CAUTION

Avoid the use of chemical cleaning agents containing benzene, toluene, zylene, acetone, or similar solvents. These chemicals may damage the plastics used in this receiver.

1. Exterior - Dust the cabinet with a soft cloth. Dust the front panel controls with a small soft-bristled paint brush. Dirt clinging to the cabinet may be removed with a clean, lint-free cloth dampened with a mild detergent and water solution. Avoid using abrasive cleaners. They will scratch the front panel.
2. Interior - Dust in the interior of the unit should be removed before it builds up enough to cause arcing and short circuits during periods of high humidity. Dust is best removed by dry, low-pressure air. Dirt elinging to surfaces may be removed with a soft-bristled paint brush or a clean, lint-free cloth dampened with a mild detergent and water solution. Use a cotton tipped applicator for cleaning in narrow spaces and on the circuit boards.

### 4.4.2 LUBRICATION

The optical encoder assembly shaft requires periodic lubrication to prevent excessive wear. The other rotating assemblies in the receiver are sealed and do not require lubrication. To lubricate the encoder assembly shaft, perform the following steps:

## CAUTION

Excessive lubrication of the encoder shaft may destroy the optical characteristics of the encoder wheel.

1. Place the receiver in a vertical position and remove the encoder knob.
2. Apply one (1) drop of SAE $5 W-20 W$ oil to the encoder shaft at the retaining ring.
3. Reassemble the encoder assembly knob and rotate the knob several times to distribute the lubricant.

### 4.4.3 INSPECTION FOR DAMAGE OR WEAR

Many potential or existing faults can be detected by making a visual inspection of the unit. For this reason, a complete visual inspection should be made on a routine basis and whenever the receiver is inoperative. At a minimum, the following items should be visually inspected.

1. Inspect the equipment covers and front panel for condition of finish and panel markings.
2. Inspect for dents, punctures, or warped areas.
3. Inspect quarter-turn fasteners and receptacles.
4. Inspect the external surfaces for loose or missing screws or washers.
5. Inspect the receptacles for conditions of pins, contacts, and mountings.
6. Inspect the internal components for signs of deterioration, discoloration, or charring. Check for melted insulation and damaged, cracked, or broken components.
7. Inspect the printed circuit boards for damaged tracks, loose connections, corrosion, or other signs of deterioration.
8. Inspect the PC connectors, interface connectors, and chassis wiring for excessive wear, looseness, misalignment, corrosion, or other signs of deterioration.

### 4.5 PERFORMANCE TESTS

4.5.1 GENERAL

The Performance Tests outlined in this Section define the Minimum Performance Standards which ensure receiver operability in all detection modes, gain modes and IF bandwidths. The given tests should be used for initial inspection, for preventive maintenance checks, to develop specific fault symptons for troubleshooting or to verify receiver performance after repairs have been made.

### 4.5.2 MINIMUM PERFORMANCE STANDARDS

Table 4-3 summarizes the parameters tested by the Performance Tests. To be acceptable for use, the receiver should meet or exceed all minimum performance standards listed.

Table 4-3. Receiver Minimum Performance Standards

| Parameter to be Tested | Performance Standard |
| :---: | :---: |
| Receiver Gain, Input to IF Out | $82 \mathrm{~dB} \pm 2 \mathrm{~dB}$ on all bandwidths |
| S/N Ratio, Input to IF Out | 10 dB with -103 dBm input level and 4 kHz bandwidth |
| AM Detection Mode, Input to Phone Out | Audibility in headphones with -97 dBm input and $50 \%$ modulation |
| Record Audio Out in AM Mode | 1.0 Vac into $600 \Omega$ with -97 dBm input and $50 \%$ modulation. |
| CW Detection Mode, Input to Phone Out | Audibility in headphone with -97 dBm unmodulated input |
| FM Detection Mode, Input to Phone Out | Audibility in headphones with -97 dBm input and 4.8 kHz deviation |
| USB, and LSB Detection Modes, Input to Phone Out | Audibility in headphones with -97 dBm unmodulated input |
| Manual Gain Control | 100 dB control range |
| AGC Performance | Control range -97 dBm to +3 dBm with 6 dB output change |
| Frequency Tuning Accuracy | $\pm 100 \mathrm{~Hz}$ at 500 kHz and 29.99999 MHz |

### 4.5.3 PROCEDURE GUIDELINES

When conducting the Peformance Tests, the technician should comply with the following guidelines:

1. Read each test procedure thoroughly before attempting to perform the test.
2. Hook up the proper test equipment as indicated in the Test Setup figure for each test.
3. Set the test equipment and receiver controls as directed for each test.
4. Allow a minimum of 30 minutes warm-up time for test equipment prior to performing any of the tests.
5. Unless otherwise specified, acceptable tolerances are $\pm 3 \mathrm{~dB}$ for signal levels and $\pm 20 \%$ for ac and de supply voltages.
6. The tests should be performed in the order given. If a malfunction is noted, refer to paragraph 4.6 for troubleshooting information.
4.5.4 POWER-UP TEST
7. Set receiver controls as follows:
a. RF Gain - Maximum CCW
b. Phone Level - Maximum CCW
c. Tuning Rate - Disable
d. Detection Mode - AM
8. Energize the receiver by lifting the POWER ON switch on the front panel.
9. Adjust the Intensity control for a comfortable display intensity. The display should indicate 15.00000 MHz .
10. Select the $10 \mathrm{~Hz}, 100 \mathrm{~Hz}, 1 \mathrm{kHz}$ and 10 kHz tuning rates in succession and, using the tuning knob, verify that the Frequency Display increments and decrements correctly for each rate selected.
11. De-energize the receiver.
4.5.5 IF GAIN TEST
12. Connect the test equipment as shown in Figure 4-1.
13. Set the Signal Generator output frequency to 15.00000 MHz and output level to -97 dBm .
14. Set the RF Voltmeter to the -10 dBm range.
15. Set the receiver controls as follows:
a. RF Gain - Maximum CW
b. IF Bandwidth $\quad 16 \mathrm{kHz}$
c. Tuning Rate -10 Hz
d. Detection Mode - AM
e. Gain Mode - Manual


Figure 4-1. IF Gain Test
5. Energize the receiver.
6. The Signal Strength meter should indicate approximately $1 / 2$ scale and the RF Voltmeter should indicate $-15 \mathrm{dBm} \pm 2 \mathrm{dBm}$.
7. Select $8 \mathrm{kHz}, 4 \mathrm{kHz}$ and 1 kHz bandwidths in succession. For each bandwidth, the RF Voltmeter should indicate -15 dBm $\pm 2 \mathrm{dBm}$.
8. Set the Signal Generator output frequency to 15.0015 MHz . Select USB mode. The RF Voltmeter should indicate -15 dBm $\pm 2 \mathrm{dBm}$.
9. Set the Signal Generator output frequency to 14.9985 MHz . Select LSB mode. The RF Voltmeter should indicate -15 dBm $\pm 2 \mathrm{dBm}$.

## NOTE

Bandwidths whose levels are slightly out of tolerance may be corrected by adjusting R12 on the IF Filter Board associated with the out of tolerance bandwidth.
10. Select AM mode and 16 kHz bandwidth.
11. Turn off the Signal Generator RF Output.
12. The RF Voltmeter should indicate a level no greater than -25 dBm .
13. Turn on the Signal Generator RF Output.
14. Tune the Signal Generator and the receiver to 500 kHz , $1.0 \mathrm{MHz}, \quad 1.5 \mathrm{MHz}, \quad 2.0 \mathrm{MHz}, \quad 3.0 \mathrm{MHz}, 5.0 \mathrm{MHz}, \quad 7.0 \mathrm{MHz}$, 11.0 MHz and 25.0 MHz in succession. At each frequency, the receiver IF output level should be within 2 dB of the level obtained in Step 6 above.
15. De-energize the receiver and disconnect the test equipment.
4.5.6 DETECTION MODE PERFORMANCE TEST

1. Connect the test equipment as shown in Figure 4-2.
2. Set the Signal Generator output frequency to 15.00000 MHz and output level to -97 dBm . Set the Generator for $50 \%$ AM modulation at 400 Hz .


Figure 4-2. Detection Mode Performance Test
3. Set the AC Voltmeter to the 3 VaC range.
4. Set the receiver controls as follows:
a. RF Gain - Maximum CW
b. Phone Level - Maximum CCW
c. IF Bandwidth -1 kHz
d. Tuning Rate -10 Hz
e. Detection Mode - AM
f. Gain Mode - Manual
5. Energize the receiver.
6. Rotate the PHONE level control until a 400 Hz tone is heard in the headphones at a comfortable listening level. The tone should be clear and free from noise, hum and other signal distortions.
7. Adjust the RECORD level control for an AC Voltmeter indication of 1.0 Vac.
8. The oscilloscope should show a clean sine wave with no evidence of clipping or distortion.
9. Turn off the Signal Generator modulation.
10. Set the receiver MODE switch to CW. Set the TUNE RATE switch to BFO and adjust the TUNE knob for a BFO offset of +0.4 kHz .
11. A clear, distinct 400 Hz tone should be heard in the headphones.
12. Set the Signal Generator output frequency to 15.00040 MHz .
13. Set the receiver MODE switch to USB. A clear, distinct 400 Hz tone should be heard in the headphones.
14. Set the Signal Generator output frequency to 14.99960 MHz .
15. Set the receiver MODE switch to LSB. A clear, distinct 400 Hz tone should be heard in the headphones.
16. Set the Signal Generator output frequency to 15.00000 MHz . Set the Generator modulation to FM, modulation frequency to 400 Hz , and deviation to 4.8 kHz .
17. Set the receiver MODE switch to FM and the BANDWIDTH switch to 16 kHz .
18. A clear, distinct 400 Hz tone should be heard in the headphones,
19. De-energize the receiver and disconnect the test equipment.

### 4.5.7 MAN/AGC PERFORMANCE TEST

1. Connect the test equipment to the receiver as shown in Figure 4-3.
2. Set the Signal Generator output frequency to 15.00000 MHz and output level to -97 dBm . Set the Generator for $50 \% \mathrm{AM}$ modulation at 400 Hz .
3. Set the receiver controls as follows:
a. RF Gain - Maximum CW
b. IF Bandwidth -1 kHz
c. Tuning Rate -10 Hz
d. Detection Mode -AM
e. Gain Mode - Manual
4. Energize the receiver.
5. Adjust the RECORD level control for an indication of 1.0 Vac on the AC Voltmeter.
6. Increase the Signal Generator output level in 10 dBm increments until +3 dBm output is reached. For each 10 dBm increase, rotate the RF Gain control counterclockwise until the RECORD AUDIO output level indicates 1.0 Vac on the AC Voltmeter.
7. Decrease the Generator output level to -97 dBm .
8. Set the receiver to the AGC Gain Mode.
9. Adjust the RECORD level control for an indication of 0.5 Vac on the AC Voltmeter.
10. Increase the Signal Generator output level to +3 dBm .
11. The AC Voltmeter should indicate no greater than 1.0 Vac.
12. De-energize the receiver and disconnect the test equipment,


Figure 4-3. MAN/AGC Performance Test

FREQUENCY TUNING PERFORMANCE TEST

1. Connect the test equipment to the receiver as shown in Figure 4-4.
2. Set the Signal Generator output frequency to 0.50000 MHz and output level to -60 dBm .
3. Set the Frequency Counter to provide 10 Hz resolution of a 1 second sample rate.
4. Set the receiver controls as follows:
a. RF Gain - Maximum CCW
b. IF Bandwidth -1 kHz
c. Tuning Rate -10 kHz
d. Detection Mode - AM
5. Energize the receiver and tune to 0.50000 MHz .
6. The Frequency Counter should indicate $455.00 \mathrm{kHz} \pm 0.10 \mathrm{kHz}$.
7. Tune the receiver and Signal Generator to 29.99000 MHz .
8. The Frequency Counter should indicate $455.00 \mathrm{kHz} \pm 0.10 \mathrm{kHz}$.
9. De-energize the receiver and disconnect the test equipment.

### 4.6 CORRECTIVE MAINTENANCE

### 4.6.1 GENERAL

Corrective Maintenance includes the testing, troubleshooting, repair and alignment necessary to return a defective receiver to a satisfactory operating condition. Information is contained in this paragraph to troubleshoot the receiver to a replaceable assembly or PC board. Individual assembly and PC board repair procedures are contained in paragraph 4.7. Receiver alignment procedures are contained in paragraph 4.8.

### 4.6.2 CORRECTIVE MAINTENANCE GUIDELINES

A receiver will require corrective maintenance as a result of failure to pass any initial inspection testing, failure to meet the minimum performance standards in Table 4-3, failure to pass any of the Performance Tests in paragraph 4.5 or operator-observed malfunctions during normal receiver operation.


Figure 4-4. Frequency Tuning Performance Test

Figure 4-5, the Troubleshooting Flowehart, is provided as an aid in localizing defective assemblies and PC boards within the receiver. To troubleshoot a defective receiver, refer to Figure 4-5 and proceed as follows:

1. Begin at START and proceed horizontally through the Chart. Perform the indicated Performance Tests until a fault (NO) is indicated.
2. Localize the fault to a defective assembly or PC board by proceeding vertically through the troubleshooting path and performing the indicated tests.
3. Replace the defective module or PC board and perform any required alignments or adjustments (see paragraph 4.8).
4. Verify receiver operation by performing the Performance Tests in paragraph 4.5. If the results are satisfactory, the receiver may be returned to service.
5. The defective assembly or PC board removed in Step 3 may be repaired by referring to the component level troubleshooting and repair procedures in paragraph 4.7 below.

### 4.7 COMPONENT LEVEL TROUBLESHOOTING AND REPAIR

### 4.7.1 GENERAL

This paragraph contains the procedures for testing and repairing defective receiver assemlbies and PC boards. Troubleshooting Tests are provided to help identify fault symptons, to localize defective components and to verify assembly or PC board performance after repair, It should be noted that the procedures in this paragraph are provided as a guide and are not intended to substitute for proper signal tracing technique by skilled personnel familiar with the receiver. In addition, the circuit descriptions in Chapter III and Schematic Diagrams in Chapter V are an essential in troubleshooting receiver assemblies and PC boards.

### 4.7.2 PROCEDURE GUIDELINES

1. Allow 20 minutes for test equipment warm-up prior to testing.
2. Read the procedure thoroughly before beginning any test.
3. Comply with all pre-test setup conditions.
4. After the repair, verify correct assembly or PC board operation by repeating the test procedure.

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## Figure 4-5. Troubleshooting Flowchart (1 of 2 )



Figure 4-5. Troubleshooting Flowchart (2 of 2 )
4-20

### 4.7.3 POWER SUPPLY TESTING AND TROUBLESHOOTING

4.7.3.1 Pre-test Setup

1. Remove the Power Supply from the receiver chassis.
2. Remove the Power Supply protective cover.
3. Connect a 24 Vdc power supply to J 1 on the receiver rear panel.
4.7.3.2 Test Procedure
4. Energize the receiver.
5. Using a de voltmeter, check the voltages of the points indicated in Table 4-4.
6. If a failure is encountered, check or replace the components indicated in Table 4-3.
7. If the failure is still present, refer to the Power Supply Circuit Description, paragraph 3.6 .9 and the Power Supply Schematic Diagram, Figure 6-26 to aid in additional signal tracing and fault isolation.
8. After the fault has been corrected, verify proper operation by rechecking the voltages in Table 4-4.

Table 4-4. Power Supply Voltage Level Cheeks

| Test Point | Voltage | Key Components |
| :--- | ---: | :--- |
| TP1 | +24 |  |
| PS1 -2 | +2 | J1; wiring |
| PS1 -3 | +5 | VR1, Q1 |
| TP2 | +5 | PS1, C2, C3 |
| PS2 -2 | +2 | L1 |
| PS2 -3 | +15 | VR2, Q2 |
| TP3 | +15 | PS2, C5, C6 |
| PS2 -5 | -15 | L2 |
| TP4 | -15 | C8, C9 |
|  |  | L3 |

4.7.4 INPUT FILTER TESTING AND TROUBLESHOOTING
4.7.4.1 Pre-Test Setup

1. Remove the Input Filter from the receiver chassis.
2. Remove the Input Filter protective cover.
3. Disconnect W1P1 from A1J1 and W5P6 from A1J2.
4. Connect the Signal Generator output to A1J1.
5. Set the Generator output frequency to 1.0 MHz and output level to 0 dBm .
6. Connect the $50 \Omega$ probe of the RF Voltmeter to A1J2. Set the Voltmeter to the 0 dBm range.

### 4.7.4.2 Test Procedure

1. Begin at 1.0 MHz and tune the Signal Generator to 5.0 MHz , $10.0 \mathrm{MHz}, \quad 15.0 \mathrm{MHz}, \quad 20.0 \mathrm{MHz}, \quad 25.0 \mathrm{MHz}$, and 30.0 MHz , successively, maintaining the output level at 0 dBm for each frequency.
2. The RF Voltmeter should indicate an output level between 0 dBm and -2 dBm for each frequency.
3. Disconnect test equipment from the Input Filter.
4. Excessive filter loss is usually caused by shorted or leaky capacitors or zener diodes. If the filter exhibits excessive loss, perform continuity checks on these components with an ohmmeter.
5. After replacing any components, verify filter performance by repeating Steps 1 and 2 above.
4.7.5 PRESELECTOR TESTING AND TROUBLESHOOTING
4.7.5.1 Pre-Test Setup
6. Remove the Preselector protective cover.
7. Disconnect W5P6 from A2J1 and W6P7 from A2J2.
8. Connect the Signal Generator output to A2J1.
9. Connect the $50 \Omega$ probe of the RF Voltmeter to A2J2.
10. Connect a 24 Vdc power supply to J 1 on the receiver rear panel.

### 4.7.5.2 Test Procedure

1. Energize the receiver.
2. Refer to Table 4-5. Tune the receiver and Signal Generator successively to each of the frequencies listed. At each frequency, set the Generator output level to 0 dBm and verify that the RF Voltmeter indicates an output level between 0 dBm and -2 dBm .

Table 4-5. Preselector Filter Parameters

| Freq. <br> (MHz) | Filter <br> No. | Filter <br> Select <br> Pin | Comments |
| :---: | :---: | :---: | :--- |$|$|  |  |
| :--- | :--- |
| 0.5 | A2A1 |
| 1.0 | A2A1 |
| 1.5 | A2A2 |
| 2.0 | A2A2 |
| 3.0 | A2A3 |
| 5.0 | A2A3 |
| 7.0 | A2A4 |
| 11.0 | A2A4 |
| 25.0 | A2A5 |

3. If excessive loss is encountered at any frequency, use a DC Voltmeter to check the Filter Select Voltage at the indicated pin.
a. If the Select Voltage is correct, check diodes CR1 - CR10 on the affected filter. Also check capacitors for shorts or leakage.
b. If the Select Voltage is not correct, refer to paragraph 3.3.3 and troubleshoot the Digital Control, A2A6.
4. If any filter components are changed, repeat Step 2 above to verify filter performance.

### 4.7.6 INPUT CONVERTER TESTING AND TROUBLESHOOTING

4.7.6.1 Pre-Test Setup

1. Remove the Input Converter from the receiver chassis.
2. Remove the Input Converter protective cover.
3. Disconnect W6P6 from A1J1.
4. Connect the Signal Generator output to A1J1.
5. Set the Generator output frequency to 15.00000 MHz and output level to -20 dBm .
6. Connect a 24 Vdc power supply to J1 on the receiver rear panel.

### 4.7.6.2 Test Procedure

1. Energize the receiver.
2. Using a high impedance RF Voltmeter, check the signal levels at the points indicated in Table 4-6. Signal frequencies, where indicated, may be verified with an oscilloscope or frequency counter.

Table 4-6. Input Converter Signal Level Checks

| Test <br> Point | Signal <br> Level | Signal Freq. | Key Components | Comments |
| :---: | :---: | :---: | :---: | :---: |
| U1-3 | 30 mV | 15.0 MHz | Input Wiring |  |
| R4 | 60 mV | 43.0 MHz | U9, Q1, Q2 | 1st IF Signal |
| E4 | 30 mV | 43.0 MHz | FL1 |  |
| T1-3 to 2 | 30 mV | 43.0 MHz | Q1, Q2 |  |
| L8-E5 | 500 mV | 32.2 MHz | Input Wiring | 2nd LO Input |
| T3-1 to 2 | 1 V | 32.2 MHz | Q5 |  |
| M9A - 3 | 20 mV | 10.7 MHz | M9A | 2nd IF Signal |
| FL1-1 | 100 mV | 10.7 MHz | Q3, Q4 |  |
| FL2-2 | 70 mV | 16.7 MHz | FL1 |  |

3. If a failure is encountered, check or replace the components indicated in Table 4-6.
4. If the failure is still present, refer to the Input Converter Circuit Description, paragraph 3.2.4 and the Input Converter Schematic Diagram, Figure 6-9 to aid in additional signal tracing and fault isolation.
5. After the fault isolation has been corrected, verify proper operation by rechecking the signal levels in Table 4-6.
4.7.7 $\quad 10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ CONVERTER TESTING AND TROUBLESHOOTING

### 4.7.7.1 Pre-test Setup

1. Disconnect W9P14 from A4J1.
2. Place the Converter board on an extender board.
3. Connect the Signal Generator output to A4J1.
4. Set the Generator output frequency to 10.7 MHz and output level to -20 dbm .
5. Connect a 24 Vdc power supply to J 1 on the receiver rear panel.

### 4.7.7.2 Test Procedure

1. Energize the receiver.
2. Using a high impedance RF Voltmeter, check the signal levels at the points indicated in Table 4-7. Signal frequencies, where indicated, may be verified with an oscilloscope or frequency counter.
3. If a failure is encountered, check or replace the components indicated in Table 4-7.

Table 4-7. $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Signal Level Checks

| Test <br> Point | Signal <br> Level | Signal <br> Freg. | Key <br> Components | Comments |
| :---: | :---: | :---: | :---: | :--- |
| Q2-2 | 2.5 V | 11.155 MHz | Q1, Y1 | 3rd LO Signal |
| Q2-3 | 20 mV | 10.7 MHz | T1 | 3rd IF Signal |
| Q3-E | 200 mV | 455 kHz | Q2 |  |
| XA1 -6 | 200 mV | 455 kHz | Q3 |  |

4. If the failure is still present, refer to the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Circuit Description, paragraph 3.2.6 and the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Schematic Diagram, Figure 6-11 to aid in additional signal tracing and fault isolation.
5. After the fault has been corrected, verify proper operation by rechecking the signal levels in Table 4-7.

## 4.7 .8

4.7.8.2

IF FILTER TESTING AND TROUBLESHOOTING

### 4.7.8.1 Pre-Test Setup

1. Remove the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter, A4A1A1.
2. Place the IF Filter (A2 - A7) to be tested on an extender board.
3. Connect the Signal Generator output to pin A4A1A1-6.
4. Set the Generator output frequency to 455 kHz for Filters A2-A5, 454.5 kHz for A6 or 456.6 for A7, and set output level to -20 dBm .
5. Connect a 24 Vdc power supply to J 1 on the receiver rear panel.

### 4.7.8.2 Test Procedure

1. Energize the receiver. Set the receiver BANDWIDTH control to correspond to the bandwidth of the IF Filter under test.
2. Using a high impedance RF Voltmeter, check the signal levels at the points indicated in Table 4-8. Signal frequencies, where indicated, may be verified with an oscilloscope or frequency counter.

Table 4-8. IF Filter Signal Level Checks

| Test <br> Point | Signal <br> Level | Signal <br> Freq. | Key <br> Components | Comments |
| :--- | :---: | :---: | :---: | :--- |
| Q2 - C | +15 Vdc | .-- | Q1, Q2 | Use DC Voltmeter |
| E1 | +15 Vdc | $-\cdots$ | CR2 |  |
| K1 $-7,8$ | 20 mV | 455 kHz | K1 |  |
| C7 | 15 mV | 455 kHz | FL1 | Adjust R12 |
| Pin 1 | 50 mV | 455 kHz | Q3 | Adju |

3. If a failure is encountered, check or replace the components indicated in Table 4-8.
4. If the failure is still present, refer to the IF Filter Circuit Description, paragraph 3.2.7 and the IF Filter Schematic Diagram, Figure $6-12$ to aid in additional signal tracing and fault isolation.
5. After the fault has been corrected, verify proper operation by rechecking the signal levels in Table 4-8.

### 4.7.9 $\quad 455 \mathrm{kHz}$ IF AMPLIFIER TESTING AND TROUBLESHOOTING

### 4.7.9.1 Pre-Test Setup

1. Place the 455 kHz amplifier A4A1A8 on an extender board.
2. Connect the Signal Generator output to pin A4A1A8 - A.
3. Set the Generator output frequency to 455 kHz and output leve] to -40 dBm .
4. Connect a 24 Vdc power supply to J1 on the receiver rear panel.
5. Set receiver for MAN Gain Mode with RF Gain Control at maximum CW.

### 4.7.9.2 Test Procedure

1. Energize the receiver.
2. Using a high impedance RF Voltmeter, check the signal levels at the points indicated in Table 4-9. Signal frequencies, where indicated, may be verified with an oscilloscope or frequency counter.

Table 4-9. 455 kHz IF Amplifier Signal Level Checks

| Test <br> Point | Signal <br> Level | Signal <br> Freg. | Key <br> Components | Comments |
| :--- | :---: | :---: | :---: | :--- |
| CR1 Anode | -2.0 Vdc | - |  | R4, CR1 |
| Q1-1 | 30 mV | 455 kHz | Q1 | Qse Voltmeter |
| Q2-1 | 300 mV | 455 kHz | Q2 |  |
| Pin F | 200 mV | 455 kHz | R16 | Adjust R16 |

3. If a failure is encountered, check or replace the components indicated in Table 4-9.
4. If the failure is still present, refer to the 455 kHz IF Amplifier Circuit Description, paragraph 3.2.8 and the 455 kHz IF Amplifier Schematic Diagram, Figure 6-13 to aid in additional signal tracing and fault isolation.
5. After the fault has been corrected, verify proper operation by rechecking the signal levels in Table 4-9.

### 4.7.10 WIDE/NARROW FILTER TESTING AND TROUBLESHOOTING

### 4.7.10.1 Pre-Test Setup

1. Remove the 455 kHz IF Amplifier, A4A1A8.
2. Place the Wide/Narrow Filter, A4A1A9, on an extender board.
3. Connect the Signal Generator output to pin A4A1A8 - F.
4. Set the Generator output frequency to 455 kHz and output level to -20 dBm .
5. Connect a 24 Vdc power supply to J 1 on the receiver rear panel.
4.7.10.2 Test Procedure
6. Energize the receiver.
7. Using a high impedance RF Voltmeter, check the signal levels at the point indicated in Table 4-10. Signal frequencies, where indicated, may be verified with an oscilloscope or frequency counter.

Table 4-10. WB/NB Filter Signal Level Checks

| Test <br> Point | Signal <br> Level | Signal <br> Freq. | Key <br> Components | Comments |
| :--- | :--- | :--- | :--- | :--- |$|$| C2-C |
| :--- |
| R14 |

3. If a failure is encountered, check or replace the components indicated in Table 4-10.
4. If the failure is still present, refer to the WB/NB Filter Circuit Description, paragraph 3.2.9 and the WB/NB Filter Schematic Diagram, Figure 6-14 to aid in additional signal tracing and fault isolation.
5. After the fault has been corrected, verify proper operation by rechecking the signal levels in Table 4-10.
4.7.1 DEMOD/AGC AMPLIFIER TESTING AND TROUBLESHOOTING
4.7.11.1 Pre-Test Setup
6. Remove WB/NB Filter A4A1A9.
7. Place the Demod/AGC Amplifier A4A1A10 on an extender board.
8. Connect the Signal Generator output to pin A4A1A9 - A.
9. Set the Generator output frequency to 455 kHz and output level to -26 dBm .
10. Connect a 24 Vdc power supply to J 1 on the receiver rear panel.
4.7.11.2 Test Procedure
11. Energize the receiver.
12. Using a high impedance RF Voltmeter, or Oscilloscope where indicated, check the signal levels at the points indicated in Table 4-11. Signal frequencies, where indicated, may be verified with an oscilloscope or frequency counter.
13. If a failure is encountered, check or replace the components indicated in Table 4-11.
14. If the failure is still present, refer to the Demod/AGC Amplifier Circuit Description, paragraph 3.2.10 and the Demod/AGC Amplifier Schematic Diagram, Figure 6-29 to aid in additional signal tracing and fault isolation.
15. After the fault has been corrected, verify proper operation by rechecking the signal levels in Table 4-11.
4.7.1 $A$ AUDIO AMPLIFIER TESTING AND TROUBLESHOOTING
4.7.12.1 Pre-Test Setup
16. Remove Demod/AGC Amplifier, A4A1A10.
17. Remove the receiver front panel to gain access to the Audio Amplifier.
18. Connect the Signal Generator output to pin A4A10-A18.
19. Set the Generator output frequency to 400 Hz and output level to 0.7 Vrms .
20. Connect a 24 Vdc power supply to J 1 on the receiver rear panel.

Table 4-11. Demod/AGC Amplifier Signal Level Checks

| Test <br> Point | Signal Level | Signal Freq. | Key Components | Comments |
| :---: | :---: | :---: | :---: | :---: |
| CR2 Anode | 100 mv | 455 KHz | Q1, Q2 | Set receiver to AM Mode |
| Pin B-12 | 70 mv | 455 KHz | Q9, T1 |  |
| TP-E1 | 2V P-P | 400 Hz | CR2, Q3 | 50\% AM at 400 Hz |
| U2A-7 | 2V P-P | 400 Hz | Q5, U2A | $50 \% \mathrm{AM}$ at 400 Hz |
| U2B-1 | 2V P-P | 400 Hz | U2B | $50 \% \mathrm{AM}$ at 400 Hz |
| U3-1 | 7 mv | 455.4 KHz | Q9 | Set Generator to 455.4 kHz no modulation, Set receiver to CW. |
| L4-C32 | .1V P-P | 400 Hz | U3, Q10, CR13 |  |
| L6-C42 | 2 V P-P | 400 Hz | U4, Q11 | Set Generator to 455 kHz , FM deviation 4.8 kHz at 400 Hz modulation. Set receiver to FM. |
| Pin B-3 | -2 VDC |  | Q4, U1 | Turn off Generator Modlation. Set receiver to AGC. |

### 4.7.12.2 Test Procedure

1. Energize the receiver.
2. Using a high impedance Oscilloscope check the signal levels at the points indicated in Table 4-12. Signal frequencies where indicated, may be verified with the oscilloscope or frequency counter.
3. If a failure is encountered, check or replace the components indicated in Table 4-12.
4. If a failure is still present, refer to the Audio Amplifier Circuit Description, paragraph 3.2.11 and the Audio Amplifier Schematic Diagram, Figure 6 - 25 to aid in additional signal tracing and fault isolation.
5. After the fault has been corrected, verify proper operation by rechecking the signal levels in Table 4-12.

Table 4-12. Audio Amplifier Signal Level Checks

| Test <br> Point | Signal <br> Level | Signal <br> Freq. | Key <br> Components | Comments |
| :--- | :---: | :--- | :--- | :--- |
| U1A-5 | $1 V \mathrm{P}-\mathrm{P}$ | 400 Hz | R1 | Set RECORD and PHONE <br> level controls to mid- <br> range. |
| U1A-7 | $8 \mathrm{~V} \mathrm{P-P}$ | 400 Hz | U1 |  |
| E4 | $8 \mathrm{~V} \mathrm{P-P}$ | 400 Hz | C3, C4 |  |
| U1B-3 | $1 \mathrm{~V} \mathrm{P}-\mathrm{P}$ | 400 Hz | R5 |  |
| U1B-1 | $10 \mathrm{~V} \mathrm{P-P}$ | 400 Hz | U1 |  |

### 4.7.13 DIGITAL CONTROL TESTING AND TROUBLESHOOTING

1. Energize the receiver. If the display does not indicate $15.00000 \mathrm{MHz}, \mathrm{C} 1$ may be defective. Momentarily bridge C1 with a jumper wire. If the display does not reset to 15.00000 MHz , check R4 and counters U1-U7.
2. Rotate the TUNE knob CW and CCW in the $10 \mathrm{~Hz}, 100 \mathrm{~Hz}$, 1 kHz and 10 kHz TUNE RATE positions. If tuning is correct for all tune Rates, proceed to Step 3. If some of the TUNE RATE positions are inoperative, check counters U1 - U7. If the display does not increment at all, proceed as follows:
a. Check the level at U22-1 with an oscilloscope. The level should be high when tuning CW and low when tuning CCW. If not, check U22 and U12.
b. Check the level at U16-4. A train of short, positive-going pulses should be observed as the TUNE KNOB is rotated. If not, check U12, U13, U15 and U16.
3. Select the BFO position on the TUNE RATE switch. Rotate the TUNE KNOB CW and CCW and observe the display tune from -8.0 to +8.0 . If not, proceed as follows:
a. Check the level at U14-10. The level should be high when tuning CW and low when tuning CCW. If not, check U13, U14, U16 and U22.
b. Check the level at U14-11. The level should be low when tuning the receiver. If not, check U11, U13, U14 and U19.
e. Check counters U8 and U9 and gates U17 and U18.
4.7.14
4.7.15

TIME BASE TESTING AND TROUBLESHOOTING

1. Place the Time Base board on an extender board.
2. Refer to Table 4-13 and use a Frequency Counter to check the indicated Test Points. When a failure is encountered, check or replace the indicated components.

Table 4-13. Time Base Parameters

| Test Point | Frequency | Key Components |
| :--- | ---: | :---: |
|  | 2 MHz |  |
| U1-1 | 2 MHz | U1 |
| Q1-C | 80 kHz | Q1, R3 |
| U2-1 | 8 kHz | U 2 |
| U3-5 | 1 kHz | U 3 |
| U3-13 | 20 kHz | U 3 |
| U4-4 | 5 kHz | U 4 |
| U4-12 | 200 kHz | U 4 |
| U5-5 | 50 kHz | U 5 |
| U5-12 | 1.0 MHz | U5 |
| J1 |  | CR1, U5 |

4.7.16 1st LO TESTING AND TROUBLESHOOTING

1. Place the 1st LO Synthesizer on an extender card.
2. Refer to Table 4-14 and cheek the VCO Band Select circuitry. If the Band Select Voltages do not agree with the Table, check U13 and U14.

Table 4-14. VCO Band Select Code

| TUNED FREQUENCY | BAND <br> E5 | SELECT <br> E4 | VOLTAGE <br> E3 |
| :---: | :---: | :---: | :---: |
| $0-3.99 \mathrm{MHz}$ | +5 | +5 | +5 |
| $4-7.99 \mathrm{MHz}$ | +5 | +5 | 0 |
| $8-11.99 \mathrm{MHz}$ | +5 | 0 | +5 |
| $12-15.99 \mathrm{MHz}$ | +5 | 0 | 0 |
| $16-19.99 \mathrm{MHz}$ | 0 | +5 | +5 |
| $20-23.99 \mathrm{MHz}$ | 0 | +5 | 0 |
| $24-27.99 \mathrm{MHz}$ | 0 | 0 | +5 |
| $28-29.99 \mathrm{MHz}$ | 0 | 0 | 0 |

3. Tune the receiver to 00.00000 MHz . Under this condition, the Divider Section has an overall divide ratio of 4291 . Use the Frequency Counter to compare the frequencies at U4-1 and U5-12 to verify the divide ratio. If not correct, proceed as follows:
a. Refer to paragraph 3.6.3.2.3 and verify the presets to U5, U6, U7 and U8 with a Voltmeter. If not correct, check U9, U10, U11 and U12.
b. Refer to paragraph 3.6.3.2.4 and check the operation of counters U4, U5, U6, U7 and U8.
4. Check the phase detector, U1. If the frequencies at U1-3 and U1-1 are close together, output at U1-5 will be narrow spikes. If the frequencies at U1-3 and U1-1 are far apart, U1-5 output will be wide pulses.
5. Check the loop filter, U2. The output at U2-6 will be negative, depending on the pulse width from U1. If the output is 0 or a very large negative or positive level, replace U2.
6. Check the VCO tuning by shorting pin E1 to ground and observing a frequency change at U4-1. If a very small or no change is noted, replace CR1.
7. If the phase lock loop on the 1st LO is working correctly, then check U1, Q3 and Q4 on the VCO assembly for failure.
4.7.17 2nd LO TESTING AND TROUBLESHOOTING
8. Determine which of the three loops is causing the problem. When the problem loop is determined, troubleshoot as described in Steps 2, 3 or 4.
a. $\quad 32 \mathrm{MHz}$ Loop - Proper operation is indicated by a 32 MHz signal at the collector of Q2. If not, proceed to Step 2.
b. Programmable Loop - Proper operation is indicated by a 200 kHz signal at U8-1 when the receiver is tuned to 15.00099 MHz and 210 kHz when the receiver is tuned to 15.00000 MHz . If not, proceed to Step 3 .
c. Output Loop - Proper operation is indicated by a frequency of 32.20 to 32.21 MHz at J1. If not, proceed to Step 4.
9. $\quad 32 \mathrm{MHz}$ Loop.
a. $\mathrm{U} 3-\mathrm{U} 3$ is a divide-by- 16 counter. Compare frequencies at pins 1 and 4 to verify the divide ratio.
b. Phase Detector - Proper operation of U1 is indicated by narrow or wide pulses at pin 5, depending on the difference in frequencies at pins 1 and 3.
c. Loop Filter - The output at U2-6 is a de voltage between -5 and +5 Vde which is proportional to the pulse width from U1.
d. VCO - If VCO oscillates, but does not lock, replace CR1. Otherwise, check Q1 and Q2.
10. Programmable Loop.
a. U6, U7, and U8 - These three counters form a divide-by800 divider. Compare frequencies at U6-1 and U8-1 to verify divide ratio.
b. Pre-Scaler - Check U9 and U10 by tuning the receiver to 15.00099 MHz . Check the frequencies at U9-1 and U10-15 to verify a divide-by-100 ratio.
c. Programmable Counter - Tune the receiver to 15.00000 MHz . This sets the programmable counter to a divide-by- 20 ratio. Check the frequencies at U13-2 and U14-15 to verify this ratio.
d. Phase Detector - Proper operation of U4 is indicated by narrow or wide pulses at pin 5 depending on the difference in frequencies at pins 3 and 6.
e. Loop Filter - The output at U5-6 is a de voltage between -5 and +5 Vde which is proportional to the pulse width from U1.
f. If the VCO oscillates, but does not lock, replace CR4. Otherwise, check Q8.
11. Output Loop.
a. Mixer U15-Check the operation of U15 by measuring frequencies of U15-8 and U15-1. The output of U15 at R20 should be the difference between these two.
b. Phase Detector - Proper operation of U16 is indicated at pin 5, depending on the difference in frequencies at pins 3 and 6.
c. Loop Filter - The output at U18 pin 5 is a de voltage between -5 and +5 Vde which is proportional to the pulse width from U16.
d. VCO - If the VCO is oscillating, but will not lock, replace $\overline{\text { CR3 }}$. Otherwise, check Q5 and Q6. If the Output Loop is locked and no output appears at J1, check Q7.
4.7.19 BFO TESTING AND TROUBLESHOOTING
12. Set the TUNE RATE switch to BFO and adjust the display to +0.0 .
13. Prescaler - The prescaler divide ratio is ten. Measure the frequencies at U12-2 and U12-11 to verify this.
14. Programmable Counters - The counter divide ratio is 455. Measure the frequencies at U12-11 and Test Point E1 to verify this. If the divide ratio is not correct, refer to paragraph 3.6.6.2 and check the counters U7 - U10, the Zero Detector, and the End of Cycle Detector.
15. Phase Detector - The output of U1-5 should consist of narrow or wide pulses, depending on the frequency difference at pins 3 and 6.
16. Loop Filter - The output at U2-6 should be a de voltage between -5 and +5 Vde which is proportional to the pulse width from U1.
17. VCO - If the VCO oscillates, but will not lock, check CR1 and $\overline{\mathrm{CR} 2}$. Otherwise check Q1 and Q2.
18. Output Divider - U13 provides a divide-by- 10 ratio. The output at U13-9 should be 455.00 kHz . If the output is dead or incorrect, replace U13.

## 4.8 <br> ALIGNMENT/ADJUSTMENT PROCEDURES

### 4.8.1

GENERAL
The following Alignment and Adjustment procedures should only be performed when indicated by the results of Performance Testing (paragraph 4.5) or after replacing PC board components. Prior to performing any Alignment or Adjustment, be sure to allow 30 minutes for Test Equipment warm-up.

### 4.8.2 INPUT CONVERTER ADJUSTMENT

1. Loosen the screws holding the Input Converter module to the chassis. Pull the module out and remove its cover. Connect Test Equipment as shown in Figure 4-6.
2. Set the receiver controls as follows:
a. RF Gain - Maximum CW
b. Detection Mode - AM
c. Gain Mode - Manual
d. Bandwidth $\quad 16 \mathrm{kHz}$
e. Tuning Rate -10 Hz
3. Energize the receiver.
4. Set the Signal Generator output frequency to 15.0000 MHz and output level to -97 dBm .
5. Adjust C3 of A3A1 and C1 of A3A2 for a maximum indication on the RF Voltmeter.
6. Deenergize the receiver and disconnect the test equipment.
7. Replace the cover on the Input Converter. Install the Input Converter in the chassis.


Figure 4-6. Input Converter Alignment

### 4.8.3 IF GAIN ADJUSTMENT

1. Remove the IF Motherboard cover plate on the right side of the receiver chassis. Connect Test Equipment as shown in Figure 4-7.
2. Set A4A1A8-R16 at approximately mid-range.
3. Set the receiver controls as follows:
a. RF Gain - Maximum CW
b. Detection Mode - AM
c. Gain Mode - Manual
d. Bandwidth $\quad-16 \mathrm{kHz}$
e. Tuning Rate -10 Hz
4. Set the Signal Generator output frequency to 15.00000 MHz and output level to -97 dBm .
5. Energize the receiver.
6. Adjust A4A1A2-R12 for a -15 dBm reading on the RF Voltmeter.
7. Switch the receiver to 8 kHz bandwidth. Adjust A4A1A3-R12 for a -15 dBm reading.
8. Switch the receiver to 4 kHz bandwidth. Adjust A4A1A4-R12 for a -15 dBm reading.
9. Switch the receiver to 1 kHz bandwidth. Adjust A4A1A5-R12 for a -15 dBm reading.
10. Switch the receiver to USB Mode. Set the Signal Generator frequency to 15.00000 MHz . Adjust $\mathrm{A} 4 \mathrm{~A} 1 \mathrm{~A} 6-\mathrm{R} 12$ for a -15 dBm reaidng.
11. Switch the receiver to LSB Mode. Set the Signal Generator frequency to 15.0000 MHz . Adjust A4A1A7-R12 for a -15 dBm reading.
12. If -15 dBm cannot be obtained at each step above, readjust A4A1A8-R16 slightly and repeat Steps 6 through 11.
13. De-energize the receiver and disconnect the Test Equipment.
14. Replace the IF Motherboard cover plate.


Figure 4-7. IF Gain Adjustment

### 4.8.4 SYNTHESIZER ALIGNMENT

### 4.8.4.1 $\quad$ 1st LO Synthesizer Alignment

The only alignment points for the 1st LO are in the 1st LO VCO which is a very sensitive circuit; care must be taken to ensure proper operation.

1. Place the 1st LO on an extender card.
2. Remove the VCO front plate.
3. Connect a Digital Voltmeter to pin A1E1.
4. Refer to Table 4-15. Beginning at Band 0, adjust the indicated components until the voltage at pin A1E1 stays within limits as the receiver is tuned through Band 0.

Table 4-15. VCO Alignment Procedures

| VCO <br> Band | Band <br> Freq. <br> Limits | Voltage <br> at Pin A1E1 <br> (Typical) | A2A1 <br> Alignment <br> Component |
| :---: | :---: | :--- | :--- |
| 0 | $0-3.99 \mathrm{MHz}$ | $<8.0$ to $<-5.0 \mathrm{Vdc}$ | C 3 |
| 1 | $4-7.99 \mathrm{MHz}$ | $<8.0$ to $<-5.0 \mathrm{Vdc}$ | L 2 |
| 2 | $8-11.99 \mathrm{MHz}$ | $<8.0$ to $<-5.0 \mathrm{Vdc}$ | L 3 |
| 3 | $12-15.99 \mathrm{MHz}$ | $<8.0$ to $<-5.0 \mathrm{Vdc}$ | $\mathrm{L} 2 \& \mathrm{~L} 3$ |
| 4 | $16-19.99 \mathrm{MHz}$ | $<8.0$ to $<-5.0 \mathrm{Vdc}$ | L 4 |
| 5 | $20-23.99 \mathrm{MHz}$ | $<8.0$ to $<-5.0 \mathrm{Vdc}$ | $\mathrm{L} 2 \& \mathrm{~L} 4$ |
| 6 | $24-27.99 \mathrm{MHz}$ | $<8.0$ to $<-5.0 \mathrm{Vdc}$ | $\mathrm{L} 3 \& \mathrm{~L} 4$ |
| 7 | $28-30 \mathrm{MHz}$ | $<8.0$ to $<-5.0 \mathrm{Vdc}$ | $\mathrm{L} 2, \mathrm{~L} 3 \& \mathrm{~L} 4$ |

5. Repeat for Bands 2 through 7. As suggested in Table 4-15, the inductors align more than one band and a compromise between bands may be necessary.
6. De-energize the receiver.
7. Disconnect the Digital Voltmeter. Replace the VCO front plate and place the 1st LO back in the receiver.

### 4.8.4.2 2nd LO Synthesizer Alignment

The 2nd LO Synthesizer Alignment consists of a 32 MHz Loop Alignment, a Programmable Loop Alignment and an Output Loop Alignment. Perform the procedure in the given sequence.

1. Preliminary Setup
a. Mount the 2nd LO Synthesizer on an extender board.
b. Energize the receiver and allow 30 minutes for warm-up.
2. 32 MHz Loop Alignment
a. Connect a Digital Voltmeter to Test Point E1.
b. Adjust C 19 until a Voltmeter reading of 7.5 Vdc is observed with the alignment tool withdrawn from the VCO shield.
3. Programmable Loop Alignment
a. Connect a Digital Voltmeter to Test Point E2.
b. Tune the receiver to $\mathbf{1 5 . 0 0 9 9 9} \mathrm{MHz}$
c. Adjust C 61 until a Voltmeter reading of -8.0 Vdc is observed with the alignment tool withdrawn from the VCO shield.
4. Output Loop Alignment
a. Connect a Digital Voltmeter to Test Point E3.
b. Tune receiver to 15.00499 MHz .
c. Adjust C44 until a Voltmeter reading of 7.5 Vdc is observed with the alignment tool withdrawn from the VCO shield.
d. Using a Frequency Counter, verify that a frequency of $32.205010 \mathrm{MHz} \pm 3 \mathrm{~Hz}$ is present at J 1 .
4.8.4.3 3rd LO Synthesizer Alignment
5. Mount the 3rd LO/BFO Synthesizer on an extender board.
6. Connect a Digital Voltmeter to Test Point E3.
7. Adjust C30 until a Voltmeter reading of 2.5 Vde is observed.
4.8.4.4 BFO Synthesizer Alignment
8. Mount the 3rd LO/BFO Synthesizer on an extender board.
9. Connect a Digital Voltmeter to Test Point E2.
10. Set receiver mode to CW, BFO offset to ZERO.
11. Adjust C8 until a Voltmeter reading of 7.5 Vde is observed.
4.8.4.5 Time Base Alignment
12. Connect a Frequency Counter to the 1 MHz Test Output test point on the Time Base.
13. Insert an adjustment tool into the access hole on the side of the TCXO on the Time Base. Adjust the TCXO trimmer until the Frequency Counter indicates $1.000000 \mathrm{MHz} \pm 1 \mathrm{~Hz}$.

## SECTION V

## REPLACEMENT PARTS LIST

### 5.1 UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations (electrical symbol numbers) has been used to identify assemblies, subassemblies (and modules) and parts. An example of the unit numbering method follows:

Subassembly Designation A1
Identify from right to left as:

## R1 Class and No. of Item

First (1) resistor ( R ) of
first (1) subassembly (A)

As shown on the main chassis schematic, components which are an integral part of the main chassis have no subassembly designation.

### 5.2 REFERENCE DESIGNATION PREFIX

Partial reference designations have been used on the equipment and on the illustrations in this manual. The partial reference designations consist of the class letter(s) and identifying item number. The complete reference designations may be obtained by placing the proper prefix before the partial reference designations. Reference Designation Prefixes are provided on drawings and illustrations in parentheses within the figure titles.

### 5.3 PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear or damage. When ordering replacement parts from Watkins-Johnson Company, specify the type and serial number of the equipment and the reference designation of each part ordered. The list of manufacturers provided in paragraph 5.5 and the manufacturer's part number for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment; however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

## NOTE

As improved semi-conductors become available, it is the policy of Watkins-Johnson to incorporate them in proprietary products. For this reason some transistors, diodes, and integrated circuits installed in the equipment may not agree with those specified in the parts list and schematic diagrams of this manual. However, the semi-conductors designated in the manual may be substituted in every case with satisfactory results.

### 5.4 ASSEMBLY REVISION LEVEL

The purpose of the Assembly Revision Level is to identify the "as built" configuration of an assembly or subassembly. The parts list and illustrations that follow, depict the revision levels of the assemblies and subassemblies at the time of preparation of the manual, which may or may not agree with the purchased equipment. However, they will serve as a guide for any necessary maintenance to be performed. Refer to Table 5-1, for the Equipment Assembly Revision Level Record, located in the rear of the parts lists section.

### 5.5 LIST OF MANUFACTURERS

The List of Manufacturers that follows is listed numerically by the manufacturer's Federal Supply Code or "Code Ident" as it appears in the parts list.
RM274 WATKINS-JOHNSON CO., GAITHERSBURG, MD. DATE 03/03/81 PAGE ..... 1
CODE NAME AND ADDRESS ..... ZIP
00779 AMP INC HARRISBURG.PENNSYLVANIA
1710501121 ALLFN-BRADLEY CO MILWAUKEE,WISCONSIN
53204
01295 TEXAS INST INC SFMICOND COMP DIV DALLAS,TEXAS ..... 7523102114 FERROXCURE CORP SAUGFRTIES,NFW YORKFERRIX02735 RCA CORP SOLIO STATE DIV SOMERVILLE, NEW JERSEY
04013 TAURUS CORP LAMBERTVILLE, NEW JERSEY

04239 GF COMPANY CHEM/METALLURTICAL VENTURES EDMORE,MICHIGAN

04239 GF COMPANY CHEM/METALLURTICAL VENTURES EDMORE,MICHIGAN ..... 08530
12477
08876
04713 MOTOROLA INC SEMICDND PROD DIV PHOENIX,ARIZONA ..... 4992806540 AMATOM ELECTRINIC HARDWARE DIV OF MITE CORP NEW HAVEN, CONNECTICUT
0651506776 ROBERTSQN-NUGENT ING ALBANY, INDIANA
07263 FAIRCHILD SEMICOND DIV MT VIEW,CALIFORNIA
12498 TELEDYNE CRYSTALONICS CAMBRIDGE,MASSACHUSETTS ..... 9404013103 THERMALLOY CO DALLAS,TEXAS
14632 WATKINS-JOHNSON CO CEI DIV GAITHERSBURG,MARYLAND ..... 75234 ..... 2076015542 MINI-CIRCUITS LABOPATORIFS BROOKLYN,NEW YORK
15818 TELENYNE SFMICONDUCTOR MT VIFW,CALIFORNIA ..... 11229 ..... 94040
17856 SILICONIX INC SANTA CLARA,CALIFURNIA
18324 SIGNETICS CORP SUNNYVALE, CALIFORNIA
1 P565 CHOMERICS INC WOBURN,MASSACHUSETTS
19505 APPLIED ENGINEERING PRODUCTS CO DERBY,CONNECTICUT
22526 BERG ELECTRONICS INC NEW CUMBERLAND, PENNSYLVANIA ..... 1707023480 ELECTRONIC HARDWARE CORP JAMAICA,NEW YORK
25088 SIEMENS AMERICA INC SOUTH ISELIN, NEW JERSEY
25330 GENFRAL CONNECTITR CORP NFWTON, MASSACHUSETTS
25350 DONALD BRUCE AND CO CHICAGO,ILLINOIS
27014 NATIONAL SEMI-CONDUC, TOR CORP SANTA CLARA,CALIFORNIA47150
0214095050
94086018010641811433
088300215860818

| BM2 74 | WATKINS-JOHNSON CO., GAITHERSBURG, MD. DATE 03/03/81 | PAGE 2 |
| :---: | :---: | :---: |
| CODE | NAME AND ADDRFSS | 2IP |
| 27735 | F-DYNE ELECTRONICS BRIDGEPORT, CONNECTICUT |  |
|  |  | 06605 |
| 27956 | RELCOM PALO ALTO, CALIFRONIA |  |
|  |  | 94304 |
| 28480 | HEWLFTT-PAGKARD CO PALO ALTO, CAL IFORNIA |  |
| 33095 | SPFCTRUM CONTROL INC FAIRVIEW, PENNSYLVANIA | 94304 |
|  |  | 16415 |
| 49956 | RAYTHEON CO LEXINGTON, MASSACHUSETTS |  |
|  |  | 02173 |
| 50829 | SEMICDNDUCTOR CIRCUITS INC HAVERHILL, MASSACHUSETS |  |
| 51406 | MURATA CORP OF AMERICA ELMSFORD,NEW YORK | 01830 |
|  |  | 10523 |
| 51642 | CENTRE ENGINEERING INC STATE COLLEGE, PENNSYLVANIA |  |
|  |  | 16801 |
| 52648 | PLESSY SEMICONDUCTORS IRVINE, CALIFORNIA |  |
| 55322 | SAMTEC INC NEW ALBANY, INDIANA | 92714 |
|  |  | 47150 |
| 56289 | SPRAGUE ELECTRIC CO NORTH ADAMS,MASSACHUSETTS |  |
|  |  | 01247 |
| 70903 | BELDEN CORP CHICAGO, ILLINOIS |  |
|  |  | 60644 |
| 71279 | CAMBRIDGE THERMIONIC CORP CAMBRIDGE, MASSACHUSETTS |  |
|  |  | 02138 |
| 71285 | CAMILLUS CUTLERY CO CAMILLUS, NEW YORK |  |
| 71400 | BUSSMAN MFG DIV OF MC GRAW-EDISON CO ST LOUIS, MISSDURI | 13031 |
|  |  | 63107 |
| 71468 | ITT CANNON ELEGTRIC SANTA ANA, CALIFORNIA |  |
|  |  | 92702 |
| 71482 | GP GLARE CO CHICAGO, ILLINOIS |  |
| 85 |  | S 60645 |
| 7278 | GINGH CONNECTOR OPERATIONS OF TRW ELK GROVE VILLAGE, ILLINOIS | 60007 |
| 72136 | ELECTRO MOTIVE MANUFACTURING CO INC WILLIAMANTIC, CONNECTICUT |  |
|  |  | 06226 |
| 72982 | ERIE TECHNOLDGICAL PRODUCTS INC ERIE,PENNSYLVANIA |  |
|  |  | 16512 |
| 73138 | BECKMAN INSTRUMENTS INC HELIPOT DIV FULLERTON, CALIFORNIA | 92634 |
| 73899 | JFD ELECTRONICS CO BROOKLYN, NEW YORK |  |
|  |  | 11219 |
| 74199 | QUAM NICHOLS CO CHICAGO, ILLINOIS |  |
| 74868 | BUNKER RAMO CORP AMPHENOL RF DIV DANBURY, CONNECTICUT | 60637 |
|  |  | 06810 |
| 75915 | LITTELFUSF INC DES PLAINES, ILLINOIS |  |
|  |  | 60016 |
| 76055 | MALLORY CONTROLS DIV OF PR MALLORY CO INC FRANKFORT, INDIANA | 46041 |
| 5-4 |  |  |

RM274 WATKINS-JOHNSON CO., GAITHERSBURG, MD. DATE 03/03/81 PAGE ..... 3
CDDE NAMF AND ADDRESS ..... ZIP
77820 BENDIX COPP ELECTRICAL COMPONENTS DIV SIDNEY,NEW YORK
80058 JOINT ELFCTRONICS TYPE DESIGNATION SYSTEM
BO131 ELECTRONIC INDUSTRIES ASSOCIATION WASHINGTON, DC
81030 INTERNATIONAL INSTRUMENTS INC DIV OF SIGMA INST INC URANGE, CONN R1073 GRAYHILL INC LA GRANGE,ILLINOIS
81349 MILTTARY SPECIFICATIONS
81350 JOINT ARMY-NAVY SPECIFICATIDNS
82389 SWITCHCRAFT INC CHICAGO, ILLINOIS
84411 TRW CAPACITORS DGALLALA, NEBRASKA
91793 JOHANSON MFG CO BOONTON,NEW JERSEY91418 RADID MATERIALS CO CHICAGD,ILLINOIS
91506 AUGAT INC ATTLEBORO, MASSACHUSETTS6064602703
92825 WHITSO INC SCHILLFR PARK, ILLINOIS
94144 RAYTHFON CO COMPONENTS DIV QUINCY, MASSACHUSETTS
95104 COLLINS RADIO CO RICHARDSON, JEXAS
95121 QUALITY COMPONENTS INC ST MARYS, PENNSYLVANIA
15857
15857
95146 ALCD ELECTRONIC PRODUCTS INC LAWRENCE,MASSACHUSETTS ..... 01842 ..... 01842
97539 APM-HEXSEAL CORP ENGLEWOOD.NEW JERSEY
99800 DELEVAN ELECTRONICS DIV AMERICAN PRECISION IND AURORA, NEW YORK
99848 WILCO CORP INDIANAPOLIS, INDIANA
96906 MILITARY STANDARDS0216975080




Figure 5-1. WJ-8770 HF Receiver, Front View, Location of Components


Figure 5-2. WJ-8770 HF Receiver, Rear View, Location of Components




Figure 5-3. WJ-8770 HF Receiver, Top View, Location of Components


| TYPE | WJ-8770-1 | 0 | A SCHEMATIC | 680035 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| title | - hF TRANSPORTABLE | EIVER |  |  |  |
| REF <br> DESIG | CESCRIPTION | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | CODE <br> IDENT | REF ASSY |
| P1 | CONN/PLUG | 7 | UG $1465 / \mathrm{U}$ | 80058 |  |
| P2 | CONN/PLUG | 7 | UG 1466 U | 80058 |  |
| P3 | S/A P2 |  |  |  |  |
| p4 | CONN/PLUG | 1 | 2-87456-6 | 00779 |  |
| P5 | S/A P1 |  |  |  |  |
| P6 | S/A P1 |  |  |  |  |
| P7 | $S / A P 1$ |  |  |  |  |
| Ps | S/A P1 |  |  |  |  |
| P9 | NOT USED |  |  |  |  |
| P10 | NOT USED |  |  |  |  |
| P11 | CONN/PLUG <br> SMC SNAP-ON RIGHT <br> ANGLF FOR RG-188 | 1 | 205/188 | 19505 |  |
| P13 | S/A PZ |  |  |  |  |
| P14 | S/A P2 |  |  |  |  |
| P15 | S/A P2 |  |  |  |  |
| P16 | $S / A P 1$ |  |  |  |  |
| P17 | S/A P1 |  |  |  |  |
| P18 | S/A P2 |  |  |  |  |
| P19 | CONN/RECEP <br> 9 POS D STYLE ACCE <br> NO. 20 CRIMP SOCKE | Is | 205203-1 | 00779 |  |
| P20 | S/A P19 |  |  |  |  |







Figure 5-4. Type 796123 Input Filter Assembly (A1), Location of Components



Figure 5-5. Type 796112 Input Filter (A1A1), Location of Components



Figure 5-6. Type 796100 Input Preselector (A2), Location of Components





Figure 5-7. Type 34936 Preselector Motherboard (A2A1), Location of Components



Figure 5-8. Type 796016 Input Filter (A2A1A1), Location of Components

BM2.72 WATKINS-JOHNSON CO.. GAITHERSBURG; MD. DATE 03/03/81 PAGE 2

| TYPE | NUMBER 796016 | REVISION | SCHEMATIC | 480020 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TITLE | - 5-750KHZ/.75-1.1 MHZ | FILTER PG | ASSV |  |  |
| RFF <br> DESIG | DESCRIPTIDN | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | $\begin{aligned} & \text { CODE } \\ & \text { IDENT } \end{aligned}$ | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| C11 | S/A C7 |  |  |  |  |
| Cl 2 | S/A 65 |  |  |  |  |
| C13 | S/A C4 |  |  |  |  |
| 614 | S/A C2 |  |  |  |  |
| C15 | S/A C2 |  | - |  | . |
| C16 | S/A Cl |  |  |  |  |
| C17 | CAP/ELEC/TANT <br> 4.7 UF 2OPCT 35 V | 1 | $1960475 \times 0035 \mathrm{JE} 3$ | 56289 |  |
| C18 | CAP/MICA/DIPPED $4300 P F$ 2PCT 500 V | 2 | CM06F0432G03 | 81349 |  |
| 019 | CAP/MICA/DIPPED $7500 P F$ 2PCT 100 V | 1 | DM 19-752G | 72136 |  |
| C20 | S/A C18 |  |  |  |  |
| C21 | S/A Cl |  |  |  |  |
| 11 | $\begin{aligned} & \text { COIL/FIXED } \\ & 4.7 \mathrm{MH} \quad 10 \mathrm{PCT} \end{aligned}$ | 4 | 553-3635-45 | 71279 |  |
| L2 | COIL/FIXED <br> 1.OMH $10 P C T$ | 3 | 553-3635-37 | 71279 |  |
| 13 | S/A LI |  |  |  |  |
| 14 | COIL VARIABLE | 2 | 34960-9 | 14632 |  |
| L5 | COIL VARIABLE | 2 | 34960-6 | 14632 |  |
| L6 | COIL VARIABLE | 1 | 34960-1 | 14632 |  |
| 17 | S/A L5 |  |  |  |  |





Figure 5-9. Type 791769 Input Filter (A2A1A2), Location of Components





Figure 5-10. Type 791770 Input Filter (A2A1A3), Location of Components







Figure 5-11. Type 791771 Input Filter (A2A1A4), Location of Components






Figure 5-12. Type 791772 Input Filter (A2A1A5), Location of Components






Figure 5-13. Type 791821-2 Digital Control (A2A1A6), Location of Components



Figure 5-14. Type 796099 Input Converter (A3), Location of Components



Figure 5-15. Type $34748-3$ 1st Mixer/1st IF (A3A1), Location of Components



| TYPE | NUMBER 796108 | REVISION | A SCHEMATIC | 480212 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TITLE | - 2ND MIXER/2ND IF PR | INTED WIRI | NG ASSEMBLY |  |  |
| REF <br> DESTG | G DESCRIPTION | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | $\begin{aligned} & \text { CODE } \\ & \text { IDENT } \end{aligned}$ | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| CRI | DIDDE | 1 | 1N4446 | 80131 |  |
| CR2 | DIDOE | 1 | 5082-3039 | 28480 |  |
| C. 1 | CAD/VAR/CERAMIC <br> 2.5-11PF 350 V N300 | 1 | 538-01182.5-11 | 72982 |  |
| C2 | CAP/CER/DISC <br> 1000PF GMV 500V | 2 | B-GP1000PFP | 91418 |  |
| C3 | S/A C2 |  |  |  |  |
| C4 | CAP/CER/DISC <br> - OLUF 2OPCT 50V | 5 | 34453-1 | 14632 |  |
| C5 | S/A C4 |  |  |  |  |
| C6 | S/A C4 |  |  |  |  |
| C. 7 | S/A C4 |  |  |  |  |
| 68 | S/A C4 |  |  |  |  |
| 59 | EAP/CER/DISC <br> . 1UF 2OPCT 50V | 1 | 34475-1 | 14632 |  |
| ClO | CAP/CER/DISC <br> 4.7PF PORM 0.25PF 100 V NPD | 1 | 8101-100-COHO-479C | 72982 |  |
| $C 11$ | CAP/MICA/DIPPED 47PF 2PCT 500V | 1 | CM05ED470G03 | 81349 |  |
| Cl 2 | CAP/CER/DISC <br> 4 TOPF 2OPCT 1000 V | 2 | B470PFM | 91418 |  |
| C13 | S/A C12 |  |  |  |  |
| C14 | C.AP/VAR/CFRAMIC 9-35PF 350 V N650 | 1 | 538-011D9-35 | 72982 |  |



Figure 5-16. Type 796108 2nd Mixer/2nd IF (A3A2), Location of Components


| B4272 | 2 WATKINS-JOHNSON | CO., GAITHERS | SBURG, MD. DATE 03 | 03/03/81 PAGE | E 3 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TYPE | NUMRER 796108 | REVISION | A SCHEMATIC | C 480212 |  |
| TITLE | - 2ND MIXER/2ND IF | PRINTED WIRI | ING ASSEMBLY |  |  |
| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | CODE <br> IDENT | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| L10 | S/A L8 |  |  |  |  |
| Q1 | TRANSISTOR | 1 | 2N2222A | 80131 |  |
| Q2 | TRANSISTOR | 1 | CD643 | 12498 |  |
| Q3 | TRANSISTOR | 3 | 2N5109 | 80131 |  |
| Q4 | S/A Q3 |  |  |  |  |
| 05 | S/A Q3 |  |  |  |  |
| RA1 | HEATSINK | 1 | 1118 C | 13103 | Q2 |
| R1 | $\begin{gathered} \text { RES/FIXED/COMPO } \\ 4.3 \mathrm{~K} \\ .25 \mathrm{~W} \end{gathered}$ | 5 PCT 1 | RCROTG432JS | 81349 |  |
| R2 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 82 \text { OHMS } \\ & .25 \mathrm{~W} \end{aligned}$ | 5PCT 1 | RCRO7G820JS | 81349 |  |
| R3 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & .25 \mathrm{~W} \quad 10 \mathrm{HMS} \\ & . \end{aligned}$ | 5PCT 3 | RCRO7G100JS | 81349 |  |
| R4 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & \text { 1.3K } \\ & .25 \mathrm{~W} \end{aligned}$ | SPCT 1 | RCR07G182JS | 81349 |  |
| R5 | $\begin{aligned} & \text { RES/F IXED/COMPO } \\ & 68 \text { OHMS } \\ & .25 \mathrm{w} \end{aligned}$ | 5PCT 2 | RCROTG680JS | 81349 |  |
| R6 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 3.3 \mathrm{~K} \\ & .25 \mathrm{~W} \end{aligned}$ | 5PCT 1 | RCRO7G332JS | 81349 |  |
| Q 7 | RES/FIXED/COMPD 2. 2 K | 5PCT | RCRO7G222JS | 81349 |  |




| TYPE NUM | BFR 796121 REV | SION | A SCHEMATIC | 580060 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TITLE - | IF/DEMODULATOR ASSEMBLY |  |  |  |  |
| $\begin{aligned} & \text { REF } \\ & \text { DFSIG } \end{aligned}$ | DESCRIPTION | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | $\begin{aligned} & \text { CODE } \\ & \text { IDENT } \end{aligned}$ | REF ASSY |
| A1 | MOTHE RBOARD PC ASSEMRLY | 1 | 796120 | 14632 |  |
| A1A1 | 10.7 MHZ/455 KHZ CONVERTER PC ASSEMBLY | 1 | 796101 | 14632 |  |
| Al 42 | 16 KHZ IF FILTER PC ASSEMBLY | 1 | 72463-22 | 14632 |  |
| A1A3 | 8 KHZ IF FILTER PC ASSEMBLY | 1 | 72463-21 | 14632 |  |
| A144 | 4 KHZ IF FILTER PC ASSEMBLY | 1 | 72463-20 | 14632 |  |
| A145 | 1 KHZ IF FILTER PC ASSEMBLY | 1 | 72463-19 | 14632 |  |
| A1A6 | LSB FILTER PC ASSEMBLY | 1 | 72463-17 | 14632 |  |
| A1AT | USB FILTER PC ASSEMBLY | 1 | 72463-18 | 14632 |  |
| $A 148$ | 455 KHZ IF AMPLIFIER PC ASSEMBLY | 1 | 795103 | 14632 |  |
| Al 49 | WB/NB FILTER PC ASSEMBLY | 1 | 796102 | 14632 |  |
| A 1410 | I)EMOD/AGC AMPLIFIER PC ASSEMBLY | 1 | 796113 | 14632 |  |



Figure 5-17. Type 796121 IF/Demodulator Assembly (A4), Location of Components



Figure 5-18. Type 796120 IF Motherboard (A4A1), Location of Components

BM272 WATKINS-JOHNSON CO., GAITHERSBURG, MD. DATE 03/03/81 PAGE 2


XA1OB S/A XA1OA



Figure 5-19. Type $79610110.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter (A4A1A1), Location of Components





Figure 5-20. Type 72463-17 through 22 IF Filter (A4A1A2 through A4A1A7), Location of Components


| BM272 | WATKINS- JOHNSON | CO., GAITHERS | BURG, MD. DATE 03 | 03/03/81 PAGE | - 2 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TVPE | NUMBER 72463-22 | RFVISION | A SCHEMATIC | C 480219 |  |
| TITLE | - IF AMPLIFIER PC | SUB-ASSEMBLY |  |  |  |
| REF <br> DESIG | DESCRIPTION | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | CODE <br> IDENT | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| KI | RELAY | 1 | PRMEIA005 | 71482 |  |
| 11 | $\begin{aligned} & \text { COIL/FFIXED } \\ & \text { 1.2MH } 10 P C T \end{aligned}$ | 1 | 553-3635-38 | 71279 |  |
| MP 1 | TRANSIPAD | 3 | 7717-44DAP | 13103 | Q1-Q3 |
| Q1 | TRANSISTOR | 1 | 2N2222A | 80131 |  |
| Q2 | TRANSISTOR | 1 | 2N2907/JAN | 81350 |  |
| Q3 | TRANSISTOR $(3 \text { N187) }$ | 1 | 841001-1 | 14632 |  |
| R1 | RFS/FIXED/COMPO 68 K 5PCT . 25 W | 1 | RCR07G683JS | 81349 |  |
| R2 | $\begin{aligned} & \text { RES/F IXFD/COMPD } \\ & \text { 22K SPCT. } 25 \mathrm{~W} \end{aligned}$ | 2 | RCRO7G223JS | 81349 |  |
| R3 | S/A R2 |  |  |  |  |
| R4 | $\begin{aligned} & \text { RES/FIXED/C TMPD } \\ & .25 \mathrm{~W} \quad 10 \text { OHMS } \end{aligned}$ | 5PCT 1 | RCRO7G100JS | 81349 |  |
| P5 | $\begin{aligned} & \text { RES/F IXED/COMPO } \\ & 750 \text { DHMS } \\ & .25 \mathrm{~W} \end{aligned}$ | 5PCT 1 | RCROIG751JS | 81349 |  |
| R6 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 1.0 \mathrm{~K} 5 \mathrm{PCT} .25 \mathrm{~W} \end{aligned}$ | 1 | RCRO7G102JS | 81349 |  |
| R7 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & .25 \mathrm{~W} \end{aligned}$ | 5 CCT 1 | RCRO7G472JS | 81349 |  |
| FB | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 470 \text { DHMS } \\ & .25 \mathrm{~W} \end{aligned}$ | 5PCT | RCRO7G471JS | 81349 |  |


| BM272 | 2 WATKINS-JOHNSON | CO., | GAITHERS | SBURG, MD. DATE 0 | 03/03/81 PAGE | 3 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TYPE | NUMBER 72463-22 |  | REVISION | A SCHEMATIC | C 480219 |  |
| TITLE | - IF AMPLIFIFR PC | SUB-A | ASSEMBLY |  |  |  |
| REF <br> DESIG | DESCRIPTION |  | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | CODE <br> IDENT | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| R9 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 58 K 5 P C T .25 \mathrm{~W} \end{aligned}$ |  | 1 | RCR076563JS | 81349 |  |
| R10 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 5.6 \mathrm{~K} \\ & .25 \mathrm{~W} \end{aligned}$ | 5 PCT | $T \quad 1$ | RCR07G562JS | 81349 |  |
| R11 | RES/FIXED/COMPO <br> 100K 5PCT . 25W |  | 1 | RCROTG104JS | 81349 |  |
| R12 | RES/TRIM/FILM 1OK LOPCT . 5 W |  | 1 | 62 PARIOK | 73138 |  |
| R13 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 12 \mathrm{~K} 5 P C T .25 \mathrm{~W} \end{aligned}$ |  | 1 | RCRO7G123JS | 81349 |  |
| R14 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 390 \text { OHMS } \\ & .25 \mathrm{~W} \end{aligned}$ | 5 PCT | 1 | RCRO7G391JS | 81349 |  |
| R15 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 47 \mathrm{~K} 5 \mathrm{PCT} .25 \mathrm{~W} \end{aligned}$ |  | 1 | RCR076473JS | 81349 |  |
| R16 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & .25 \mathrm{~W} \quad 47 \text { DHMS } \end{aligned}$ | 5PCT | 1 | RCROTG470JS | 81349 |  |
| R17 | NOT USED |  |  |  |  |  |
| R18 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 130 K 5 P C T .25 \mathrm{~W} \end{aligned}$ |  | 1 | RCRO7G134JS | 81349 |  |







| BM272 | WATKINS-JOHNSON | CO., | GA ITHE | G, MD. DATE 03 | 3/81 PAG | 3 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TYPE | NUMBER 72463-20 |  | REVISION | A SCHEMATIC | 480219 |  |
| TITLE | - IF AMPLIFIER PC | SUB-A | ASSEMBLY |  |  |  |
| REF <br> DESIG | DESCRIPTION |  | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | CODE <br> IDENT | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| R9 | RES/FIXED/COMPG 56 K 5PCT . 25 W |  | 1 | RCR07G563JS | 81349 |  |
| R10 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 5.6 K \\ & .25 \mathrm{~W} \end{aligned}$ | 5PCT | T 1 | RCRO7G562JS | 81349 |  |
| R11 | $\begin{aligned} & \text { RFS/FIXED/C OMPO } \\ & 100 K \text { SPCT } 25 \mathrm{~W} \end{aligned}$ |  | 1 | RCR07G104JS | 81349 |  |
| RI 2 | RES/TRIM/FILM 10K 10PCT .5W |  | 1 | 62PAR10K | 73138 |  |
| R13 | RES/FIXED/CDMPO <br> 12K 5PCT. 25W |  | 1 | RCROTG123JS | 81349 |  |
| R14 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 390 \text { OHMS } \\ & .25 \mathrm{~W} \end{aligned}$ | 5PCT | T 1 | RCRO7G391JS | 81349 |  |
| R15 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 47 \mathrm{~K} 5 \mathrm{PCT} .25 \mathrm{H} \end{aligned}$ |  | 1 | RCR07G473JS | 81349 |  |
| $R 16$ | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & .25 \mathrm{~W} \quad 47 \text { OHMS } \end{aligned}$ | 5PCT | 1 | RCR07G470JS | 81349 |  |
| R17 | NOT USED |  |  |  |  |  |
| R18 | RES/FIXED/COMPO <br> 130 K 5PCT. 25 W |  | 1 | RCRO7G134JS | 81349 |  |



| BM272 | WATKINS-JOHNSON | CO., | GAITHERS | G, MO. DATE O | 03/03/81 PAG | 2 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TYPE | NUMBER 72463-19 |  | REVISION | A SCHEMATIC | C 480219 |  |
| TITLF | - IF AMPLIFIER PC | SUB-A | ASSEMBLY |  |  |  |
| REF <br> DESIG | DESCRIPTIUN |  | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | CODE <br> IDENT | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| K1 | RELAY |  | 1 | PRMEIA005 | 71482 |  |
| 11 | COIL/FIXED <br> 1.2MH 1OPCT |  | 1 | 553-3635-38 | 71279 |  |
| MP1 | TRANSIPAD |  | 3 | 7717-440AP | 13103 | Q1-Q3 |
| Q1 | TRANSISTOR |  | 1 | 2N2222A | 80131 |  |
| Q2 | TRANSISTOR |  | 1 | 2N2907/JAN | 81350 |  |
| Q3 | TRANS ISTOR (3N187) |  | 1 | 841001-1 | 14632 |  |
| R1 | RES/FIXED/COMPO 68 K 5PCT . 25 W |  | 1 | RCRO7G683JS | 81349 |  |
| R2 | RES/FIXED/COMPO 22 K SPCT . 25 W |  | 2 | RCR07G223JS | 81349 |  |
| R3 | S/A R ? |  |  |  |  |  |
| R. 4 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 10 \text { OHMS } \\ & .25 \mathrm{~W} \end{aligned}$ | 5PCT | 1 | RCR07G100JS | 81349 |  |
| R.5 | $\begin{aligned} & \text { RES/FIXED/LOMPO } \\ & 750 \text { OHMS } \\ & .25 \mathrm{~W} \end{aligned}$ | SPCT | T 1 | RCR07G751JS | 81349 |  |
| R6 | $\begin{aligned} & \text { RES/FIXED/COMPD } \\ & 1.0 K 5 P C T .25 W \end{aligned}$ |  | 1 | RCR07G102JS | 81349 |  |
| P7 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 4.7 \mathrm{~K} \\ & .25 \mathrm{~W} \end{aligned}$ | 5 PCT | 1 | RCR07G472JS | 81349 |  |
| R8 | $\begin{gathered} \text { RES/FIXED/COMPO } \\ 470 \text { DHMS } \\ .25 \mathrm{~W} \end{gathered}$ | 5PCT | 1 | RCR076471JS | 81349 |  |











Figure 5-21. Type 796103455 kHz IF Amplifier (A4A1A8), Location of Components




Figure 5-22. Type $796102 \mathrm{WB} / \mathrm{NB}$ Filter (A4A1A9), Location of Components





Figure 5-23. Type 796113 Demodulator/AGC Amplifier (A4A1A10), Location of Components










| BM272 | WATKINS-JOHNSON | CO. | IT | G, MD. DATE 03 | 03/81 PAGE | 10 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TYPE N | NUMBER 796113 |  | REVISION | A SCHEMATIC | 580055 |  |
| TITLF | - DEMUDULATOR/AGC | AMPL | IFIER PRI | NTED WIRING ASSEMBLY |  |  |
| REF <br> DESIG | OESCRIPTION |  | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | $\begin{aligned} & \text { CODE } \\ & \text { IDENT } \end{aligned}$ | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| R69 | RES/FIXED/COMPO <br> 2.OK 5PCT. 25 W |  | 1 | RCR07G202JS | 81349 |  |
| $R 70$ | S/A R19 |  |  |  |  |  |
| R71 | RES/FIXED/COMPD <br> 120K 5PCT. 25W |  | 2 | RCR07G124JS | 81349 |  |
| R72 | S/A RT |  |  |  |  |  |
| R73 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & \text { 62K 5PCT } .25 \mathrm{~W} \end{aligned}$ |  | 1 | RCR076623JS | 81349 |  |
| R74 | S/A RT |  |  |  |  |  |
| R75 | 5/A R29 |  |  |  |  |  |
| R76 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 10 \text { OHMS } \\ & .25 \mathrm{~W} \quad \end{aligned}$ | 5PCT | T 4 | RCRO7G100JS | 81349 |  |
| R77 | S/A R 76 |  |  |  |  |  |
| R78 | RES/FIXED/COMPD 24 K 5PCT . 25 W |  | 2 | RCR07G243JS | 81349 |  |
| R79 | S/A R 76 |  |  |  |  |  |
| R80 | S/A R76 |  |  |  |  |  |
| R81 | S/A R78 |  |  |  |  |  |
| R82 | $\begin{aligned} & \text { RES/FIXED/COMPO } \\ & 2.7 \mathrm{~K} \\ & .25 \mathrm{~W} \end{aligned}$ | 5PCT | 1 | RCRO7G272JS | 81349 |  |
| R83 | S/A R 5 |  |  |  |  |  |
| R84 | S/A R 55 |  |  |  |  |  |
| R85 | S/A RI9 |  |  |  |  |  |




Figure 5-24. Type 796117 Synthesizer Motherboard (A5), Location of Components





Figure 5-25. Type 796111 Time Base Generator (A5A1),



Figure 5-26. Type 796133 1st LO Synthesizer (A5A2), Location of Components



Figure 5-27. Type 796115 Phase Lock Loop (A5A2A1), Location of Components







Figure 5-28. Type 796132 VCO Assembly (A5A2A2), Location of Components



Figure 5-29. Type 796131 VCO P.C. Assembly (A5A2A2A1), Location of Components





$T 3$ S/AT2



Figure 5-30. Type 796107 2nd LO Synthesizer (A5A3), Location of Components















Figure 5-31. Type $796109 \mathrm{BFO} / 3$ rd LO (A5A4), Location of Components




| BM272 | WATKINS-JOHNSON CO., | GAITHERS | , MD. DATE 03 | 03/81 PAG | PAGE |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TYPF N | NIMMER 796109 | REVISION | A SCHFMATIC | 580054 |  |
| TITLF | - BFO/3RD LO PRINTED W | IRING ASS | EMBLY |  |  |
| $\begin{aligned} & \text { REF } \\ & \text { DFSIG } \end{aligned}$ | DESCRIPTION | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | $\begin{aligned} & \text { CODE } \\ & \text { IDENT } \end{aligned}$ | REF ASSY |
| C46 | S/A C3 |  |  |  |  |
| C47 | S/A r3 |  |  |  |  |
| C48 | S/A C3 |  |  |  |  |
| C49 | CAP/CER/DISC <br> GBPF SPCT $100 V$ NPO | 1 | 8121-100-COGO-680J | 72982 |  |
| C50 | S/A C18 |  |  |  |  |
| FA1 | FERRITF BEAD | 2 | 56-590-65-4A | 02114 | C39 |
| FB2 | S/A FBI |  |  |  | C39 |
| L1 | COIL/FIXED 15UH 1OPCT | 1 | 1537-40 (14046-6) | 99800 |  |
| 12 | COIL/FIXFO 22UH 1OPCT | 1 | 1537-44 (14046-8) | 99800 |  |
| 1.3 | $\begin{aligned} & \text { COIL/FIXED/MOLD } \\ & 27, \mathrm{JH} 10 \mathrm{PCT} \end{aligned}$ | 1 | 1025-54 (75084-17) | 99800 |  |
| 14 | COIL/FIXED 12OUH $10 P C T$ | 2 | 1025-70 | 99800 |  |
| 15 | S/A L4 |  |  |  |  |
| L6 | COIL/FIXFD/MOLI | 1 | 1025-36 (75084-8) | 99800 |  |
| P1 | CONN/PLUG 20 SKT SGL ROW • 10 CTR | 2 | 65001-026 | 22526 |  |
| P2 | S/A PL |  |  |  |  |
| Q1 | TRANSISTUR <br> N-CHANNEL SILIGON JUNCTION F.F.T. | 1 | U310 | 17856 |  |
| Q2 | TRANSISTOR | 1 | 2N2222A | 80131 |  |




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PM272. WATKINS-JOHNSON CO., GAITHERSBURG, MT. DATE 03/03/8I PAGE 7
```

TYPE NUMBEF T96ID9 RFVISION A SCHFMATIC 580054
TITLF - BFT/3RD LT PRINTED WIRING ASSEMBLY
$\begin{array}{lll}\text { REF } & \text { QTY/ } & \text { CODE REF } \\ \text { DESIG } & & \text { RESCRIPTION } \\ \text { IDENT ASSY }\end{array}$
R28
QES/FIXED/COMPO
470 DHMS 5PCT
.25 W
R29 RES/FIXED/COMPO 5 5PCT
.25 H
R30 RES/FIXED/COMPO 2.7 K 5PCT
. 25 W
R31 S/A R30
R3? RES/FIXED/COMPO 1 RCR07G221JS 81349
R33 S/A R28
R34 S/A R12
R35 S/A R28
R36 S/A R28
U1 I C 2 MM74C932N 27014
PHASE DETECTOR
U2 I C
1 SA74ICN
18324
OP-AMP GENERAL
PURPOSE OPT TEMP
RANGE -40 DEG In 85
DEG C
U3 I
1 CD4013BE 02735
DUAL $D$ FLIP FLOP
I C
1 CD4082BE
02735


| BM27 | WATKI | C | E | G. MD. DATE 03 | 03/03/81 PAGE | 1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TYPE | NUMBER 796106 |  | REVISION | A SCHEMATIC | C 680036 |  |
| TItLE | - DIGITAL CONTRIL | UNIT | PRINTED | WIRING ASSEMBLY |  |  |
| REF <br> DESIG | DESCRIPTIUN |  | QTY/ EQPT | PART NUMBER | CODE <br> IDENT | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| CR 1 | NOT USED |  |  |  |  |  |
| CR2 | NOT USED |  |  |  |  |  |
| $\mathrm{CP}^{2}$ | NOT USER |  |  |  |  |  |
| CR4 | DIODE |  | 2 | $1 N 4446$ | 80131 |  |
| CR 5 | S/A CR4 |  |  |  |  |  |
| r1 | CAP/ELEC/TANT <br> 4.7 UF 2OPCT 35V |  | 2 | $1960475 \times 0035$ JE3 | 56289 |  |
| C2 | CAP/MICA/DIPPED 4709 FPCT 500 V |  | 1 | DM 15-471J | 72136 |  |
| C3 | S/A C1 |  |  |  |  |  |
| C4 | CAP/ELFC:/TANT <br> $18 U F$ LOPCT 20 V |  | 1 | $1960186 \times 9020 \mathrm{KE} 3$ | 56289 |  |
| C5 | NOT USFD |  |  |  |  |  |
| 6.6 | LAD/C.ER/DISC <br> . IUF 2OPCT 50 V |  | 18 | 34475-1 | 14632 |  |
| 67 | S/A C6 |  |  |  |  |  |
| CA | S/s 6.6 |  |  |  |  |  |
| 69 | S/A C6 |  |  |  |  |  |
| ClO | S/A C. 6 |  |  |  |  |  |
| 6.11 | S/A C6 |  |  |  |  |  |
| C12. | S/A CK |  |  |  |  |  |
| C13 | 5/A C6 |  |  |  |  |  |
| 0.14 | S/A Ch |  |  |  |  |  |



Figure 5-32. Type 796106 Digital Control (A6), Location of Components

| TYPE | NUMBER 796106 RF | RFVISION | A SCHEMATIC | 680036 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TITLE | - digital control unit pr | PRINTED | WIRING ASSEMBLY |  |  |
| REF <br> DESIG | DFSERIPTION | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | $\begin{aligned} & \text { CODE } \\ & \text { IDENT } \end{aligned}$ | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| C15 | 5/4 C6 |  |  |  |  |
| 016 | S/A C6 |  |  |  |  |
| C17 | S/A C6 |  |  |  |  |
| 0.18 | S/A CG |  |  |  |  |
| C19 | S/A C6 |  |  |  |  |
| C20 | S/A C6 |  |  |  |  |
| C21 | 5/A C6 |  |  |  |  |
| C22. | S/A [6 |  |  |  |  |
| C23 | S/A CA |  |  |  |  |
| C24 | CAP/CER/DISC <br> 2200PF 10PCT 200V | 1 | CK06B $\times 222 \mathrm{~K}$ | 81349 |  |
| F1 | CDNN/PADDLE BD 40 PIN 0.08 POST LENGTH | 1 | 88213-8 | 00779 |  |
| JI | CIJNN/ RECEP <br> 6 PIN RIGHT ANGLE HEADER ASSY DBL ROW 0.10 CTRS MOD 11 | 1 | 87382-9 | 00779 |  |
| 12 | CONN/RECEP <br> 24 PIN RIGHT ANGLE HEATFR ASSY 0.10 CTRS MOD II | $1$ | 87571-9 | 00779 |  |
| PI | CONN/PLUG <br> 40 SKT DBL ROW 0.15 CTR | 1 | 65002-026 | 22526 |  |







Figure 5-33. Type 796105 Display Driver (A7), Location of Components



| TYPE | NUMBER 796104 RF | REVISIGN | A SCHEMATIC | 480210 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TITLE | - DISPLAY PRINTED WIRING | NG ASSY |  |  |  |
| $\begin{aligned} & \text { RFF } \\ & \text { DESIG } \end{aligned}$ | DESCRTPTIUN | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER | $\begin{aligned} & \text { CODE } \\ & \text { IDENT } \end{aligned}$ | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| DS I | DISPLAY LED <br> NUMER IC 7 SEG 0.375 <br> INCH RED COM CATH RH DEC W/LENS GAP | 7 7 | FND367 | 07263 |  |
| DS 2 | S/A DS1 |  |  |  |  |
| n53 | S/A DSI |  |  |  |  |
| 054 | S/A DSI |  |  |  |  |
| OS5 | S/A DS 1 |  |  |  |  |
| OS6 | S/A OSI |  |  |  |  |
| DS 7 | S/A DSI |  |  |  |  |
| ${ }^{\text {P } 1}$ | TERMINAL STRIP <br> 7 PIN SGL ROW 0.166LG <br> $\times 0.018 R N D 0.10$ CTRS PC MT | L | TS-107-G-A1 | 55322 |  |
| P2 | S/A Pl |  |  |  |  |
| D3 | S/A P1 |  |  |  |  |
| P4 | $S / A P 1$ |  |  |  |  |
| P5 | S/A Pl |  |  |  |  |
| P6 | S/A P1 |  |  |  |  |
| P7 | $5 / A P_{1}$ |  |  |  |  |
| P8 | ```TERMINAL STRIP 3 PIN SGL ROW 0.166LG X O.OIRRND O.LOCTRS PC MOUNT``` | G 1 | TS-103-G-A | 55322 |  |
| x 051 | $\begin{aligned} & \text { SOCKFT/IC } \\ & 10 \text { PIN OIP } 0.280 \\ & \text { PROFILE } \end{aligned}$ | 7 | FNS 700 | 07263 |  |



Figure 5-34. Type 796104 Display P.C. Assembly (A8), Location of Components



Figure 5-35. Type 796116 Audio Amplifier (A9), Location of Components



Figure 5-36. Type 796139 Power Supply Assembly (A10), Location of Components




Figure 5-37. Type 796110 Power Supply P.C. Assembly (A10A1), Location of Components


BM2T2 WATKINS-JOHNSON CO., GAITHERSBURG, MD. DATE U4/09/81 PAGE 1.
TYPE NUMBER 796140 REVISION B SCHEMATIC 680035

TITLE - FRONT CUVER ASSEMBLY W/REMOVABLE SPEAKER ASSEMBLY

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{aligned} & \text { QTY/ } \\ & \text { EQPT } \end{aligned}$ | PART NUMBER |  | CODE <br> IDENT | $\begin{aligned} & \text { REF } \\ & \text { ASSY } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | REMOVABLE SPEAKER ASSEMBLY | 1 | 796134-1 (SEP | PL) | 14632 |  |



Figure 5-38. Type 796140 Front Cover Assembly with Removable Speaker Assembly (A11), Location of Components



Figure 5-39. Type 796134-1 Speaker Amplifier Assembly (A11A1), Location of Components



Figure 5-40. Type 796119-1 Speaker Amplifier P.C. Assembly (A11A1A1), Location of Components

## TABLE 5-1

Equipment Assembly Revision Level Record

| $\begin{gathered} \text { TYPE } \\ \text { NUMBER } \end{gathered}$ | $\begin{aligned} & \text { REF. } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{aligned} & \text { ASSY } \\ & \text { REV. } \\ & \text { LEVEL } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| WJ-8770 |  | HF Receiver, Main Chassis | A |
| 796123 | A1 | Input Filter Assembly | A |
| 796112 | A1A1 | Input Filter P.C. Assembly | A |
| 796100 | A2 | Input Preselector Assembly | A |
| 34936 | A2A1 | Motherboard P.C. Assembly | A |
| 796016 | A2A1A1 | Input Preselector Filter P.C. Assembly | A |
| 791769 | A2A1A2 | Input Preselector Filter P.C. Assembly | A |
| 791770 | A2A1A3 | Input Preselector Filter P.C. Assembly | A |
| 791771 | A2A1A4 | Input Preselector Filter P.C. Assembly | B |
| 791772 | A2A1A5 | Input Preselector Filter P.C. Assembly | B |
| 791821-2 | A2A1 A6 | Input Preselector Digital Control P.C. Assy | A |
| 796099 | A3 | Input Converter Assembly | A |
| 34748-3 | A3 A1 | 1st Mixer/1st IF P.C. Assembly | A |
| 796108 | A3A2 | 2nd Mixer/2nd IF P.C. Assembly | A |
| 796121 | A4 | IF/Demodulator Assembly | A |
| 796120 | A4A1 | IF Motherboard P.C. Assembly | A |
| 796101 | A4A1A1 | $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter P.C. Assembly | A |
| 72463-22 | A4A1A2 | 16 kHz IF Filter P.C. Assembly | A |
| 72463-21 | A4A1A3 | 8 kHz IF Filter P.C. Assembly | A |
| 72463-20 | A4A1A4 | 4 kHz IF Filter P.C. Assembly | A |
| 72463-19 | A4A1A5 | 1 kHz IF Filter P.C. Assembly | A |
| 72463-17 | A4A1A6 | LSB Filter P.C. Assembly | A |
| 72463-18 | A4A1A7 | USB Filter P.C. Assembly | A |
| 796103 | A4A1A8 | 455 kHz IF Amplifier P.C. Assembly | A |
| 796102 | A4A1A9 | WB/NB Filter P.C. Assembly | A |
| 796113 | A4A1A10 | Demodulator/AGC Amplifier P.C. Assembly | A |
| 796117 | A5 | Synthesizer Motherboard P.C. Assembly | A |
| 796111 | A5A1 | Time Base Generator P.C. Assembly | A |
| 796133 | A5A2 | 1st LO/Synthesizer Assembly | A |
| 796115 | A5A2A1 | Phase Lock Loop P.C. Assembly | A |
| 796132 | A5A2A2 | VCO Assembly | A |
| 796131 | A5A2A2A1 | VCO P.C. Assembly | A |
| 796107 | A5A3 | 2nd LO/Synthesizer P.C. Assembly | A |
| 796109 | A5A4 | BFO/3rd LO P.C. Assembly | A |
| 796106 | A6 | Digital Control P.C. Assembly | A |
| 796105 | A7 | Display Driver P.C. Assembly | A |
| 796104 | A8 | Display P.C. Assembly | A |
| 796116 | A9 | Audio Amplifier P.C. Assembly | A |
| 796139 | A10 | Power Supply Assembly | A |
| 796110 | A10A1 | Power Supply P.C. Assembly | A |
| 796140 | A11 | Front Cover Assy W/Removable Speaker Assy | A |
| 796134-1 | A11A1 | Speaker Amplifier Assembly | A |
| 796119-1 | A11A1A1 | Speaker Amplifier P.C. Assembly | A |

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## SECTION VI

## SCHEMATIC DIAGRAMS

Included in this section are the schematic diagrams necessary for understanding the operation of, troubleshooting problems in, and effecting repairs to the Watkins-Johnson WJ-8770 HF Transportable Receiver.


NOTES:
I. UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, $\pm 5 \%, 1 / 4 \mathrm{~W}$.
b) CAPACITANCE IS IN pF.

Figure 6-1. Type 796123 Input Filter (A1), Schematic Diagram (380217)

1. UNLESS OTHERWISE SPECIFIED a) CAPICATANCE IS IN $\mu \mathrm{F}$.


Figure 6-2. Type 796100 Input Preselector (A2), Schematic Diagram (480218)



NOTES:

1. UNLESS OTHERWISE SPECIFIED
a) RESISTANCE IS IN OHMS, $\pm 5 \%, 1 / 4 \mathrm{~W}$
b) CAPACITANCE IS pFF.

Figure 6-4. Type 791769 Input Preselector Filter (A2A1A2),
c) INDUCTANCE IS $\mu \mathrm{H}$

Schematic Diagram (43728)



NOTES
I. UNLESS OTHEWISE SPECIFIED: a) RESISTANCE IS IN OHMS; $\pm 5 \%, 1 / 4 \mathrm{~W}$ b) CAPACITANCE IS pF. c) INDUCTANCE is $\mu \mathrm{H}$.

Figure 6-6. Type 791771 Input Preselector Filter (A2A1A4) Schematic Diagram (43730)


NOTES:

1. UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, $\pm 5 \%, 1 / 4 \mathrm{~W}$
b) CAPACITANCE IS PF.
b) CAPACITANCE iS pF.
c) INDUCTANCE IS $\mu \mathrm{H}$.
b) CAPACITANCE IS IN $\mu \mathrm{FF}$.
2. ENCIRCLE NUMBERS ARE MODULE PINS.
2. DIFFERENCE BETWEEN TYPES IS SHOWN IN
DIFFEREN



Figure 6-8. Type 791821-2 Input Preselector Digital Control (A2A1A5). Schematic Diagram (43732)


Notes
UNLESS OTHERWISE SPECIFIED
a) RESISTANCE IS IN OHMS, $\pm 5 \%, 1 / 4 \mathrm{~W}$
b) CAPACITANCE IS IN pF
 Schematic Diagram (580060)



Figure 6-12. Type 72463-17 thru-22 IF Amplifier (A4A1A2 thru A4A1A7), Schematic Diagram (42710)


NOTES:
I. (UNLESS OTHERWISE SPECIFIED).
a) RESISTANCE IS IN OHMS, $\pm 5 \%, 1 / 4 \mathrm{~W}$.
b) CAPACITANCE IS IN $\mu \mathrm{F}$.
c) INDUCTANCE IS IN mH .
2. CW ON RIG INDICATES CLOCKWISE ROTATION.


NOTES
I. UNLESS OTHERWISE SPECIFIED:
a.) RESISTANCE IS IN OHMS $\pm 5 \%, 1 / 4 \mathrm{~W}$.

Figure 6-14. Type $796102 \mathrm{WB} / \mathrm{NB}$ Filter (A4A1A9).
b.) CAPACITANCE IS IN $\mu \mathrm{F}$.




Figure 6-17. Type 796111 Time Base Generator (A5A1), Schematic Diagram (480214)


Figure 6-18. Type 796133 1st LO/Synthesizer (A5A2). Schematic Diagram (580056)

## NOTES:

I. UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, $\pm 5 \%, 1 / 8 \mathrm{~W}$.
b) CAPACITANCE IS IN PFF.
c) INDUCTANCE IS IN $\mathrm{H} H$


Figure 6-19. Type 796132 VCO Assembly (A5A2A2). Schematic Diagram (480139)


Figure 6-20. Type 796107 2nd LO Synthesizer (A5A3), Schematic Diagram (680037)


Figure 6-21. Type 796109 BFO/3rd LO Synthesizer (A5A4),



Figure 6-23. Type 796105 Display Driver (A7), Schematic Diagram (480211)


SEE DISPLAY DRIVER ASSY

NOTES: UNLESS OTHERWISE SPECIFIED I. RESISTANCE IS IN OHMS $\pm 5 \%, 1 / 8 \mathrm{~W}$. 2. CAPACITANCE IS IN $\mu \mathrm{F}$.


1. UNLESS OTHERWISE SPECIFED a RESISTANCE IS IN OHMS $\pm 5 \%, 1 / 4$ W b CAPACITANCE IS IN $\mu \mathrm{F}$.




Figure 6-28. Type WJ-8770-1

