INSTRUCTION MANUAL
FOR
WJ-8718-19/FE HF RECEIVER

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WATKINS-JOHNSON COMPANY 700 QUINCE ORCHARD ROAD GAITHERSBURG, MARYLAND 20878

## WARNING

This equipment employs dangerous voltages which may be fatal if contacted. Exercise extreme caution in working with this equip ment with any of the protective covers removed.

## EQUIPMENT MALPUNCTIONS

This unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. If an apparent malfunction is encountered after installation, verify that the correct input signals are present at the proper connectors. Prior to taking any corrective maintenance action or breaking any seals, contact your Watkins-Johnson representative, or the Watkins-Johnson Company Service Department to prevent the possibility of voiding the terms of the warranty. Contact the Watkins-Johnson Company via mail, telephone, wire, or cable at:

Watkins-Johnson Company<br>Company Service Department<br>700 Quince Orchard Road<br>Gaithersburg, Maryland 20878-1794<br>Toll Call: (301) 948-7550 Ext. 7201<br>TELEX: 89-8402<br>TWX: 710-828-0546<br>TELEFAX: (301) 921-9479<br>EASYLINK: 62928185

If reshipment is necessary, follow the instructions in the following paragraph (Preparation for Reshipment or Storage). Do not return the equipment until a Return for Maintenance Authorization (RMA) number has been obtained from the Watkins-Johnson Company's Customer Service Department. See Item 10 in the General Terms and Conditions of Sale paper (WJ Form \# WJ-151-X) for more information on equipment returns.

## PREPARATION FOR RESHIPMENT OR STORAGE

If the unit must be prepared for reshipment, the packaging method should follow the pattern established in the original shipment. Use the best packaging materials available to protect the unit during reshipment or storage. When possible, use the original packing container and cushioning materials. If the original packing materials are not available, use the following procedure:

1. Wrap the unit in sturdy paper or plastic.
2. Place the wrapped unit in a strong shipping container and place a layer of shock-absorbing material ( $3 / 4$-inch minimum thickness) around all sides of the unit to provide a firm cushion and to prevent movement inside the container.
3. If shipping the unit for service, fill out all information on the $5 \times 6$ PRODUCT DISCREPANCY REPORT card (WJ Form \# WJC-QA55-0) that was provided with the original shipment. Also ensure that the Return for Maintenance Authorization (RMA) number is recorded on the card. If this card is not available, attach a tag to the unit containing the following information:
a. Return for Maintenance Authorization (RMA) number.
b. The Watkins-Johnson Type/Model number of the equipment.
c. Serial number.
d. Date received.
e. Date placed in service.
f. Date of failure.
g. Warranty adjustment requested, yes or no.
h. A brief description of the discrepant conditions.
i. Customer name and return address.
j. Original Purchase Order/Contract number.
4. Thoroughly seal the shipping container and mark it FRAGILE.
5. Ship to:

Watkins-Johnson Company
700 Quince Orchard Road
Gaithersburg, Maryland 20878-1794
U.S.A

When storing the equipment for extended periods, follow the above packing instructions to prevent damage to the equipment. The safe limits for storage environment are:

Temperature: -40 to $+70^{\circ} \mathrm{C}$
Humidity: less than $95 \%$

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## SECTION I

## GENERAL DESCRIPTION

### 1.1 ELECTRICAL CHARACTERISTICS

The WJ-8718-19/FE HF Receiver (Figure 1-1) operates over the frequency range of 5 kHz to 99.99999 MHz . The receiver can demodulate $A M, F M, C W, U S B$ and LSB signals. Receiver functions may be controlled manually through the front panel, or remotely through the rear panel remote input connectors. In the manual mode, operating parameters are selected through momentary-contact, push-button switches with LED indicators. Pushbutton access to 100 programmable memory channels is provided. RF frequency, BFO frequency and memory/scan operation parameters are entered via a keypad on the front panel. $R F$ and $B F O$ frequencies may alternately entered via a large tune wheel. Seven segment LED displays are used to display RF and BFO offset frequencies. The front panel functions are implemented through an 8bit microprocessor, and the address, storage and memory devices required to interface the front panel components with the signal processing circuits in the reaceiver.

Remote control of receiver parameters and Master/Slave operation is possible via the Asynchronous I/O port. Control format is EIA Standard RS-232. In addition, remote control can be accomplished via the Serial Synchronous I/O port.

Selectable IF bandwidths of $0.3,1.0,3.2,6$ and 50 kHz operate in conjunction with the AM, FM, or CW detection modes. When the LSB, or USB detection modes are chosen, the normal IF filters are disabled and a special 2.2 kHz BW SSB filter is enabled. RF gain is controlled manually or by Fast or Slow AGC. A dual-purpose meter indicates Signal Strength or Line Audio level.

Internal frequency tuning circuitry of the receiver includes the 1 st, 2 nd, and 3rd LO and BFO Synthesizers. The phase lock loop frequency synthesizers determine tuned frequency to a resolution of 10 Hz . The synthesized BFO tunes +/8.00 kHz from 455 kHz in $10 \mathrm{~Hz}, 100 \mathrm{~Hz}$ and 1 kHz steps. A non-volatile memory stores the tuned frequency for a minimum of 48 hours after power interruption (i.e., power failure or manually turning power off).

Rear panel features include BNC connectors for a 50 ohm RF input, a 455 kHz IF output and a 1 MHz reference input/output selected by a related slide switch. Two circular connectors provide audio outputs that include: a 600 ohm balanced line audio output and an unbalanced phone output. Line voltage selection for high and low voltage conditions may be accomplished in a few seconds by inserting the printed circuit (PC) wafer in one of four positions in the line cord assembly.

Maintenance operations are straightforward due to clean mechanical packaging and placement of nearly all components on plug-in circuit boards. These circuit boards mount on motherboards which have all pins accessible from the bottom of the receiver. Removing the top cover exposes the assemblies, which may be unplugged from their sockets or freed from the main chassis by quick disconnect plugs. The de power supplies are thermal and short circuit protected, requiring no adjustments, and are easily replaced. A printed circuit wafer, accessible on the rear panel, enables matching the power transformer to line voltages of 110 Vac ( $+/-15 \%$ ) and 220 Vac ( $+/-15 \%$ ).

### 1.2 MECHANICAL CHARACTERISTICS

The receiver is 19 inches wide and occupies one full rack width in a standard 19 -inch equipment rack. The receiver occupies 5.25 inches of vertical space, and extends 19.6 inches into the rack. The main chassis, front, rear, top, and internal compartment panels are constructed of aluminum. Side panels are 0.25 inch thick aluminum plate, the front panel is a 0.19 -inch thick aluminum plate, and the rear panel, main deck, and internal partitions are stamped aluminum. The top and bot tom covers are perforated allowing flow-through ventilation. All operating controls and indicators are on the front panel, while all input and output cables are connected to the rear panel (except for the phone jack).

The front panel is overlaid with a green bezel etched with control markings. All pushbuttons are mounted on a printed circuit card positioned behind the front panel, and extend through cutouts in the front panel. The remaining controls and line audio/signal strength meter are mounted directly on the front panel. The tuned frequency numeric display is mounted on a card positioned behind a cutout in the front panel, over which a polarized filter is installed. The audio phones jack, RF gain control and phone level controls are also mounted on the front panel.

The rear panel mounts all input, output, and accessories, except for the phones jack. BNC connectors are supplied for the RF input, IF output and 1 MHz reference input/output. The INT/EXT clock switch for selecting internal or external timebase reference is located next to the 1 MHz reference input/output. Two circular connectors supply an output for Line Audio and Phone Audio. The rectangular fuseholder has the additional functions of line filter, voltage selection and ac line cord receptacle. Also on the rear panel are two heat sinked regulators ( +15 Vdc and +5 Vdc ), and the three circular connectors for remote control.

Loosening 34 quarter-turn fasteners allows the top cover to be removed from the receiver exposing four main compartments. The four compartments are from left to right as follows: power distribution and the input converter; IF modules; digital control; and synthesizer. The use of separate compartments provides excellent mechanical support and shielding.

Removing the bottom cover via 34 quarter-turn fasteners exposes four motherboards that mount a total of 17 circuit cards and the components mounted on the front panel. All connections to the motherboard are push-on plugs so replacement of the motherboard consists of removing only 17 screws and the plugs.

### 1.3 EQUIPMENT SUPPLIED

The equipment supplied consists of the receiver and a detachable line cord.

### 1.4 EQUIPMENT REQUIRED BUT NOT SUPPLIED

Select equipment from the following general classifications to obtain full use of the receiver.

- Antenna, 50 ohm
- Audio monitoring equipment such as the following:
a )Speaker panel, 600 ohm
b) Stereo headphones, 600 ohm
c) Tape recorder
- Wideband tape recorder for 455 kHz IF amplifier predetection output.
o IF-to-tape converter for 455 kHz -to-video signal conversion.


### 1.5 OPTIONAL EQUIPMENT

The following optional equipment is available for use with the WJ-871819/FE HF Receiver. For additional information concerning these options and others, contact Watkins-Johnson Company, Gaithersburg, Maryland, or your Watkins-Johnson representative.

| $\circ$ | Frequency Shift Keying | WJ-8718/FSK |
| :--- | :--- | :--- |
| 0 | IEEE-488 Interface | WJ-8718/488 |
| 0 | Carrier Operated Relay | WJ-8718/COR |
| 0 | Dual Diversity Combiner | WJ-8718/DDC |
| 0 | Intependent Sideband | WJ-8718/ISB |
| 0 | Signal Monitor Output | WJ-8718/SMO |
| 0 | 1 Hz Tuning | WJ-8718/1 Hz |

### 1.6 WJ-8718-19/FE HF RECEIVER SPECIFICATIONS

Refer to Table 1-1 for complete receiver specifications.

## Table 1-1. WJ-8718-19/FE HF Receiver Specifications



Table 1-1. WJ-8718-19/FE HF Receiver Specifications (Continued)


## SECTION II

## INSTALLATION AND OPERATION

## 2.1 <br> UNPACKING AND INSPECTION

Examine the shipping carton for damage prior to unpacking the equipment. If the carton appears to be damaged, try to have the carrier's agent present when the equipment is unpacked. If this is not possible, retain all packaging material and shipping containers for the carrier's inspection to verify damage to the equipment after unpacking, Also verify that the equipment shipped corresponds to the packing slip. Contact the Watkins-Johnson Company, CEI Division, or your Watkins-Johnson representative for any discrepancies or shortages.

The unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. It is, therefore, ready for use upon receipt. After uncrating and checking contents against the packing slip, visually inspect all exterior surfaces for dents and scratches. If external damage is visible, remove the dust covers and inspect the internal components for apparent damage. Then check the internal cables for loose connections, and plug-in items such as printed wiring boards, which may have been loosened from their receptacles.

### 2.2 PREPARATION FOR RESHIPMENT AND STORAGE

If the receiver must be prepared for reshipment, the packaging methods should follow the pattern established in the original shipment. If retained, the original materials can be reused to a large extent or at least provide guidance for the repackaging effort. Conditions during storage and shipment should be limited as follows:

> Maximum humidity: $95 \%$ (no condensation)
> Temperature range: $-30^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$

### 2.3 INSTALLATION

Rack mounting equipment, manufactured by Watkins-Johnson Company, is designed for assembly in 19 inch racks in accordance with MIL-STD-189 or EIA Standard No. RS-310. It is recommended that chassis slides be added to the racks for ease of assembly, access to the unit, and to provide adequate for general installations. Mobile installation of the equipment should be evaluated on an individual basis.

The receiver is designed for operational temperatures between $0^{\circ} \mathrm{C}$ and $50^{\circ} \mathrm{C}\left(32^{\circ} \mathrm{F}-122^{\circ} \mathrm{F}\right)$. Installation should provide for free-flowing air circulation around and through ventilated units. Multiple stacking, in particular close adjacent stacking of electronic equipment in a standard console, can produce an appreciable increase in operating temperature for all equipment contained within the console. Forced-air ventilation may be necessary to maintain proper air circulation and temperature for efficient operation of the equipment.

### 2.3.1 INPUT/OUTPUT CONNECTORS

The receiver's input/output connectors are shown in Figure 2-1. These connectors are physically mounted on the receiver rear panel. These connectors are described individually in the following paragraphs.

### 2.3.1.1 Voltage Selector/Fuse Block and Line Cord Receptacle (FL1J1)

This assembly should be inspected before installing the receiver in a new location. With the line cord unplugged, the clear plastic window can be slid over the three male power receptacle prongs. This exposes the line fuse and a hinged, plastic FUSE PULL lever.

Swinging of the FUSE PULL lever to the left ejects the fuse from the holder and frees a line-voltage-select PC wafer found at the bottom of the assembly. Looking down on the PC wafer at a slight angle on the left side shows the selected line voltage for the receiver, either $100,120,220$, or 240 Vac . If the voltage shown does not match the available line voltage, remove the PC wafer and reinstall it so that the line voltage visible with the PC wafer in position most closely matches the line voltage used. Then install the fuse suitable for the line voltage: 1 A , slow-blow for 100 Vac and 120 Vac , or $1 / 2 \mathrm{~A}$, slow-blow for 220 Vac and 240 Vac . Install the other fuse in the alternate fuseholder.

Slide the clzar plastic window back over the fuse and PC wafer portion of the assembly holder and insert the line cord in the receptacle.

### 2.3.1.2 RF Input (A2J1)

This BNC connector is the RF signal input for the receiver. Nominal input impedance is 50 ohms. The input is protected against signals exceeding +15 dBm ( 1.25 V rms ) and static build-up.

### 2.3.1.3 Line/Phone Audio Out (J16)

This 9 -pin circular connector provides line audio and phone audio outputs. The line audio output drives a balanced 600 ohm load. Output level is from 0 vac to a maximum of $24.5 \mathrm{Vac}(+30 \mathrm{dBm})$ as determined by the setting of the rear panel LINE AUDIO LEVEL potentiometer. The phone audio output drives an unbalanced 600 ohm load. Output level is from a minimum of 0 Vac to a maximum of 4.2 Vac ( +15 dBm ) as determined by the setting of the front panel PHONE LEVEL potentiometer. The pin assignments are as follows:


1. Line Cord Receptacle (FL1J1)
2. RF Input (A2J1)
3. Line/Phone Audio (J16)
4. Sync Serial I/O (J14)
5. Clock Switch (S2)
6. 1 MHZ REF (J11)
7. Remote Input (232J1)
8. Monitor Out (232J2)
9. IF Output (J12)
10. ISB/FM Audio (J15)
11. Line Audio Level (R1)

Figure 2-1. Receiver Rear Panel Input/Output Connectors

### 2.3.1.4 Synchronous Serial I/O (J14)

This 19-pin circular connector is the interface point between the receiver and remote control equipment. The pin assignments are as follows:

| $A-D F R$ GND | $G-D 3(8)$ |
| :--- | :--- |
| $B-D F R$ | $K-T F R$ |
| $C-G N D$ | $V-G N D$ |
| $D-D 0(1)$ | $R-T C$ GND |
| $E=D 1(2)$ | $U-T C$ |
| $F-D 2(4)$ |  |

### 2.3.1.5 Clock Switch (S2)

Setting this switch to the INT position selects the internal time base for the receiver and provides the internal 1 MHz reference output at J11. Setting this switch to the EXT position deactivates the internal reference so that an external signal may be applied to J11.

### 2.3.1.6 $1 \mathrm{MHZ} \mathrm{REF} \mathrm{(J11)}$

When the CLOCK switch is in the INT position, this BNC connector provides a $1 \mathrm{MHz}, 100 \mathrm{mV}$ rms output into 50 ohms. When the switch is set in the EXT position, a 1 MHz reference signal of at least 50 mV rms into 50 ohms must be applied to J11 to provide a time base for the receiver.
2.3.1.7 Remote Input (232J1)

This 10 -pin circular connector is the interface point between the receiver and remote control equipment. The pin assignments are as follows:

| A - PROT GND | F - DSR |
| :--- | :--- |
| B - TXD | G - SIG GND |
| C RXD | H - SYNC TXC |
| D - RTS | J - SYNC RXC |
| E - CTS | K - DTR |

### 2.3.1.8 Monitor Output (232J2)

This 10 -pin circular connector is the interface point for connecting the next receiver is the series chain for remote control. The pin assignments are as follows:

| A - PROT GND | F - DSR |
| :--- | :--- |
| B - TXD | G - SIG GND |
| C RXD | H - SYNC TXC |
| D - RTS | J - SYNC RXC |
| E CTS | K - DTR |

### 2.3.1.9 IF Output (J12)

This BNC connector supplies a 455 kHz IF output. The level will be 20 mV , minimum, into 50 ohms in AGC mode, for RF input signals greater than 3 V .

### 2.3.1.10 ISB/FM Audio (J15)

This 6-pin circular connector provides ISB audio (N.U.) and FM audio outputs. The FM audio output drives a high impedance load. The output level is approximately 1 V p-p for FM signal deviation equal to $30 \%$ of selected IF bandwidth. Pin assignments are as follows:

$$
\begin{aligned}
& \text { A - FM AUDIO HI } \quad \text { D - ISB AUDIO LO } \\
& \text { B - ISB CTR TAP } \\
& \text { C }- \text { N/C } \\
& \text { ISB AUDIO HI F }- \text { FM AUDIO LO }
\end{aligned}
$$

### 2.3.1.11 Line Audio Level (R1)

This potentiometer adjusts the level of audio signals on the LINE AUDIO pins of connector J16. The front panel meter monitors this output when the related LINE AUDIO switch is engaged. Rotating this control fully clockwise provides a 50 mw audio output ( $24.5 \mathrm{~V} \mathrm{rms} /+30 \mathrm{dBm}$ ) into 600 ohms.

### 2.4 OPERATION

The following paragraphs are an operator's guide to familiarize the operator with the different operating modes available with the receiver. The function and use of the front panel controls and indicators are explained and detailed receiver operating instructions are provided.

### 2.4.1 INTRODUCTION

The WJ-8718-19/FE Receiver incorporates the following operational features:

- Local receiver control through momentary contact keypad switches and a tuning knob on the front panel.
- Ninety-nine discretely addressed and one implicitly addressed memory channels. The channels are utilized to store front panel data. They may be accessed individually or scanned.
- A memory scan mode in which the receiver scans a selected group of channels.
- Remote control capability through an RS-232 link to an external controller.


### 2.4.2 FRONT PANEL CONTROLS AND INDICATORS

Refer to Figure 2-2 for each of the following front panel controls and indicators.

### 2.4.2.1 Push On/Off Power (S1)

Press this button in to energize the receiver. During initial installation, be sure the line-voltage-select PC wafer on the rear panel matches the available line voltage before energizing the receiver. Refer to paragraph 2.3.1 for the voltage selection procedure.

### 2.4.2.2 Meter (M1)

The meter contains two scales of which one is a signal strength scale with a relative scale range of 0 to 110 . This signal strength scale contains a MAN SET mark on the scale to indicate proper signal strength in the MAN gain mode. The other scale on the meter indicates the audio level of the LINE AUDIO output in dB above 1 mW , referenced to 600 ohms.

### 2.4.2.3 Meter Switch

The LINE AUDIO and SIGNAL STR switches are utilized to select the operational mode of the front panel meter (M1).

### 2.4.2.4 Scanner Mode Switches

The Scanner Mode switches are used in various memory operations. The EXAM switch is used to display parameters stored in memory. The AUTOSCAN switch is used to initiate a sequential scan of memory channels. The LOCKOUT switch is used to lock out channels from a memory scan. The THRS switch switch is used for entering a threshold level to be subsequently compared to a received signal strength. The DWELL switch is used during AUTO SCAN mode when a dwell time must selected.

### 2.4.2.5 Detection Mode Switches

These switches are used to select the desired detection mode. Available detection modes are AM, FM, USB, LSB, CWV (variable BFO) and MA (Master/Slave). ISB mode is not available in the WJ-8718-9/FE Receiver.

### 2.4.2.6 Gain Mode Switches

These switches are used to select the desired gain mode. Available gain modes are MGC (manual), SLOW (AGC) and FAST (AGC).


1. Push On/Off Power (S1)
2. Meter (ml)
3. Meter Switch
4. Scanner Mode Switches
5. Detection Mode Switches
6. Gain Mode Switches
7. BFO OFS/THRS LVL Display
8. Fault Indicators
9. Tuned Frequency Readout
10. Tune Switches
11. Tune Knob
12. General Purpose Keypad
13. Nemory Operation Switches
14. MEM ADRS Display
15. Bandwidth Select Switches
16. REMOTE/LOCAL Switches
17. RF GAIN Control
18. PHONE LEVEL Control
19. PHONES Jack

Figure 2-2. Receiver Front Panel Controls and Indicators

### 2.4.2.7 BFO OFS/THRS LVL Display

This display is used to display the BFO. offset frequency in kHz when in CW mode. This display is also used to display threshold level and dwell time.

### 2.4.2.8 Fault Indicators

The DATA fault indicator illuminates when incorrect data is transferred during remote operation. The ENTRY fault indicator illuminates when an invalid entry is attempted. The RCVR fault indicator illuminates when a receiver power supply or LO fault is detected.

### 2.4.2.9 Tuned Frequency Readout

This seven-digit readout displays the tuned frequency of the receiver. Each digit is a seven-segment LED. The least-significant digit, at the far right, indicates 10 's of Hz . Tuned frequency is displayed for both local and remote control of the receiver.

### 2.4.2.10 Tune Switches

The TUNE switches in conjunction with the TUNE knob (see paragraph 2.4.2.11) are used to adjust the receiver tuned frequency. Tuning steps of $1 \mathrm{kHz}, 100$ Hz or 10 Hz are selected with the FAST, MED and SLOW switches.

### 2.4.2.11 Tune Knob

Rotating the knob clockwise increases tuned frequency; counterclockwise rotation decreases tuned frequency. Continuing to tune past the end of the range causes the receiver to step to the opposite end of the band and to continue tuning in the same increasing or decreasing frequency direction. The receiver tunes from 00.00000 MHz to 99.99999 MHz , usable above 5 kHz .

### 2.4.2.12 General Purpose Keypad

The general purpose keypad permits direct entry of RF Frequency, BFO Offset Frequency and numerical data input required during other control operations.

### 2.4.2.13 Memory Operations Switches

These switches are used during storage or recall of data stored in the 100 memory channels.

### 2.4.2.14 MEM ADRS Display

This display indicates the channel address currently in used for storage or recall of stored data.

### 2.4.2.15 Bandwidth Select Switches

These switches are used to select the desired IF bandwidth in AM, FM or CW modes. The switches are not operative in USB, LSB or DF modes. Available bandwidths are: $0.3,1.0,3.2,6.0$ and 50 kHz .

### 2.4.2.16 REMOTE/LOCAL Switches

These two switches are used to select remote or local control modes.

### 2.4.2.17 RF GAIN Control

The RF GAIN control is used to manually adjust the receiver gain level when MGC gain mode is selected.

### 2.4.2.18 PHONE LEVEL Control

The PHONE LEVEL control is a dual-concentric potentiometer. Rotating the outer ring of the control varies the level at the tip contact of the PHONES jack. Rotating the inner shaft varies the level at the ring contact of the PHONES jack.

### 2.4.2.19 PHONES Jack

The PHONES jack permits monitoring audio from the receiver via 600 ohm stereo or mono headphones.

### 2.4.3 LOCAL CONTROL MODE

Local control of the receiver is accomplished through momentary-contact pushbutton switches arranged in functional blocks on the front panel. Some control operations require only a single keystroke. Others require entry of specific data on the general purpose keypad.

### 2.4.3.1 Local/Remote Switches

Pressing the LOCAL switch places the receiver in local control mode. Pressing the REMOTE switch places the receiver in remote control mode. The LOCAL and REMOTE LED indicators display the present receiver control mode.

Applying power to the receiver automatically places it under local control. After power-up, remote control mode may be selected manually at the front panel, or by an I/O instruction from the remote control device. If the LOCAL switch is depressed after power, the receiver will ignore instructions from the remote controller until remote control operation is selected by pressing the remote switch.

### 2.4.3.2 General Purpose Keypad

The general purpose keypad is the l6-button switch block located to the left of the tuning wheel. The multi-function, numerical selection buttons labeled 0 through 9 are utilized to enter RF and BFO frequencies, signal threshold level, BFO offset, dwell time and memory address. A special function key (*) is used to place the receiver in the BITE mode and to clear the numbered memory channels.

### 2.4.3.2.1 Terminator Functions

The software structure of the microprocessor in the receiver control block is such than an accepted numerical keypad entry is not acted upon until a termination switch is activated. The terminator informs the microprocessor how the number is to be used. Table 2-1 lists the termination switches and their associated function.

Table 2-1. Termination Switches

| Switch | Function |
| :--- | :--- |
| MHz | RF frequency |
| kHz | BFO or RF frequency |
| RECALL | Memory address |
| STORE | Memory address |
| AUTO SCAN | Initiate scan mode |
| EXAM | Memory address |
| DWELL | Scan pause, in seconds |
| THRS | Signal level threshold |
| LOCK OUT | Memory address |
| Special Function (*) | See paragraph 2.4.7 |
| CLEAR | Terminate BITE, Receiver |
|  | BITE Tests and EXAM escape. |

### 2.4.3.2.2 CLEAR Keypad Switch

The CLEAR key will remove an unterminated numerical entry from the receiver's internal circuits. Once the terminator is entered, the CLEAR switch does nothing. The CLEAR switch is also used to release the EXAM mode. See paragraph 2.4.4.4 for explanation of EXAM mode.

### 2.4.3.2.3 Special Function Switch

The (*) key is a special function keys used to access the BITE program mode, to access the receiver BITE tests, and to clear all numbered memory channels. The (*) key also turns on or off the special master mode. Refer to paragraph 2.4.7 for details on using the special function switch.

### 2.4.3.3 Receiver Operating Parameters

Receiver operating parameters are entered on the front panel switches and transferred to the receiver automatically. Parameters can be stored in a memory using the STORE switch (see paragraph 2.4.4). Selectable parameters are detection mode, IF bandwidth, RF Gain Control level, Gain Mode, RF frequency and BFO offset frequency.

### 2.4.3.3.1 Detection Mode

Detection mode is selected by pressing one of the seven available detection mode switches. When a mode is selected, the LED associated with that mode switch will illuminate and the previous mode selection is disabled. The available modes and associated criteria are as follows:
a. AM Mode - Amplitude Modulation

1. Press the $A M$ detection mode key switch.
2. Select the desired IF bandwidth by pressing the appropriate IF bandwidth key-switch (see paragraph 2.4.3.3.2).
3. Select the desired gain control by pressing the appropriate gain control mode key-switch (see paragraph 2.4.3.3.3).
4. Demodulated audio is available at the rear panel Line Audio and front panel Phones Audio outputs.
b. FM Mode - Frequency Modulation
5. Press the FM detection mode key switch.
6. Select the desired IF bandwidth by pressing the appropriate IF bandwidth key-switch (see paragraph 2.4.3.3.2).
7. Select the desired gain control by pressing the appropriate gain control mode key-switch (see paragraph 2.4.3.3.3).
8. Demodulated audio is available at the rear panel Line Audio and front panel Phones Audio outputs.
c. CW Mode - Continuous Wave
9. Press the CWV detection mode key switch.
10. Select the desired $I F$ bandwidth by pressing the appropriate IF bandwidth key-switch (see paragraph 2.4.3.3.2).
11. Select the desired gain control by pressing the appropriate gain control mode key-switch (see paragraph 2.4.3.3.3).
12. Select the desired BFO offset frequency (see paragraph 2.4.3.3.6).
13. Demodulated audio is available at the rear panel Line Audio and front panel Phones Audio outputs.
d. USB Mode - Upper Sideband
14. Press the USB detection mode key switch.
15. In USB mode, the bandwidth selection switches are inoperative. The receiver automatically selects the USB IF filter ( 2.2 kHz bandwidth).
16. Select the desired gain control by pressing the appropriate gain control mode key-switch (see paragraph 2.4.3.3.3).
17. Demodulated audio is available at the rear panel Line Audio and front panel Phones Audio outputs.
e. LSB Mode - Lower Sideband
18. Press the USB detection mode key switch.
19. In LSB mode, the bandwidth selection switches are inoperative. The receiver automatically selects the USB IF filter ( 2.2 kHz bandwidth).
20. Select the desired gain control by pressing the appropriate gain control mode key-switch (see paragraph 2.4.3.3.3).
21. Demodulated audio is available at the rear panel Line Audio and front panel Phones Audio outputs.
f. DF Mode - Direction Finder
22. Press the DF detection mode key switch.
23. In DF mode, the bandwidth selection switches are inoperative. The receiver automatically selects the DF IF filter ( 2.2 kHz bandwidth).
24. Select the desired gain control by pressing the appropriate gain control mode key-switch (see paragraph 2.4.3.3.3).
25. Demodulated audio is available at the rear panel Line Audio and front panel Phones Audio outputs.

### 2.4.3.3.2 IF Bandwidth Selection

IF Bandwidth is selected by pressing one of the five available detection mode switches. When a bandwidth is selected, the LED associated with that bandwidth switch will illuminate and the previous bandwidth selection is disabled. The available bandwidths and associated criteria are as follows:

- IF Bandwidth Selection
a. Ensure that $A M, F M$ or $C W$ mode is selected (see paragraph 2.4.3.3.1). The bandwidth switches are inoperative in USB, LSB and DF modes.
b. The available IF bandwidth selections are $0.3,1.0,3.2$, 6.0 , and 50 kHz . Depress the desired IF bandwidth switch.


### 2.4.3.3.3 Gain Control Selection

Gain control mode is selected by pressing one of the three available gain control mode switches. When a mode is selected, the LED associated with that mode switch will illuminate and the previous mode selection is disabled. The available modes and associated criteria are as follows:
a. Manual Gain Control

1. Press the SIGNAL STRENGTH meter switch.
2. Press the MGC gain control switch.
3. Rotate the RF Gain control until the SIGNAL STRENGTH meter pointer indicates MAN SET.
b. Automatic Gain Control
4. Select the desired AGC time constant by pressing either the FAST or SLOW key switches.
5. FAST AGC gives a 15 ms response time constant useful for $A M$ and $F M$ signals.
6. SLOW AGC a 15 ms attack time and 2 sec decay time suitable for CW, PULSE, and SSB signals.

### 2.4.3.3.4 RF Frequency: Tuning Wheel Entry

Adjusting the receiver tuned frequency is accomplished either by utilization of the tuning wheel and TUNE switches or by entering the desired tuned frequency on the general purpose keypad. The RF tuned frequency is displayed in the FREQUENCY/MHz display window.

When the tuning wheel is utilized to tune the receiver, turning the wheel clockwise or counterclockwise causes the receiver's tuned frequency to increase or decrease respectively. Selection of tuning step size is accomplished by pressing one of the TUNE switches. In standard MFP-equipped receivers, the selectable tuning step sizes are as follows: FAST (1 kHz steps), MED ( 100 Hz steps), SLOW ( 10 Hz steps).

### 2.4.3.3.5 RF Frequency: Keypad Entry

The RF-tuned frequency can also be adjusted by entering the desired frequency, in kHz or MHz , on the general purpose keypad. The following procedure enters an RF-tuned frequency. Examples 1 and 2 show two typical RF tuned frequency commands.

- RF Tuned Frequency - Procedure

1) Enter numerical frequency data on keypad.
2) Terminate command by pressing MHz or kHz termination switch.

Example 1: Tune the receiver to 5.5 MHz
[5] [o] [5] (1)
(1) Data entry; " 5 c5" displayed in FREQUENCY/MHZ display window.
[MHZ]
(2) Termination command; receiver tuned frequency set to 5.5 MHz ; "05.50000" displayed in FREQUENCY/MHZ display window.

Example 2: Tune the receiver to 5.5 MHz (alternate method)
[5] [5] [0] [0]
[KHZ]
(1) Data entry; "5500" displayed in FREQUENCY/MHZ display window.
(2) Termination command; receiver tuned frequency set to 5.5 MHz ; "05.50000" displayed in FREQUENCY/MHZ display window.

### 2.4.3.3.6 BFO Frequency: Tuning Wheel Entry

The one-finger tuning wheel can be used to dial a BFO frequency if the BFO and CWV switches are engaged. Selecting a tuning resolution via the TUNE switch block to the right of the wheel disengages the LOCK switch and allows the tuning wheel to dial a BFO frequency. The only effective tuning resolution for BFO tuning is the 100 Hz rate in the FAST, MED and SLOW positions. Rotating the wheel clockwise will increment the displayed frequency from a negative offset, through zero, to the upper limit of the range. Rotating the wheel counterclockwise will decrement the displayed frequency from a positive offset, through zero, to the lowest limit of the range.

### 2.4.3.3.7 BFO Frequency: Keypad Entry

The BFO offset can also be adjusted by entering the desired offset in kHz on the general purpose keypad. When CWV detection mode is selected, the following procedure is used to enter a BFO offset. Example 3 shows a typical BFO offset entry for changing the offset frequency while leaving the direction, with respect to zero offset, unchanged. Example 4 shows a typical BFO offset entry for changing the offset frequency and direction.

- BFO Offset Frequency - Procedure

1) Press BFO +/- keypad switch.
2) Repeat step (1) if direction change is desired.
3) Enter numerical BFO offset data.
4) Terminate command by pressing $k H z$ termination switch.

Example 3: Change BFO offset from 1.00 kHz to 2.50 kHz
[BFO]
[2] [o] [5]
[ KHZ ]
(1) Identifies following data entry as BFO offset data.
(2) Data entry.
(3) Termination command; BFO offset set to 2.50 kHz ; " 2.50 " displayed in BFO OFS/THRS LVL display window.

## Example 4: Change BFO Offset from +2.50 kHz to -3.60 kHz

[ BFO ]
[BFO]
[3] [.] [6]
[ KHz ]
(1) Identifies following data entry as BFO offset data.
(2) Changes direction of BFO offset; "-2.50" displayed in BFO OFS/THRS LVL display window.
(3) Data entry; "3c6" displayed in FREQUENCY/MHz display window.
(4) Termination command; BFO offset set to -3.6 kHz ; " $-3.60^{\text {" }}$ displayed in BFO OFS/THRS LVL display window.

### 2.4.4 MEMORY STORAGE \& RECALL OPERATIONS

### 2.4.4.1 General

There are 100 available memory locations ( 99 discrete and one implicitly addressed) for storage of receiver parameter data. Each memory channel is utilized to store one set of receiver parameters. Storable parameters are RF tuned frequency, detection mode, gain mode, IF bandwidth, BFO offset and threshold level. Nonstorable parameters are tuning resolution, front panel meter mode and dwell time.

### 2.4.4.2 Quick Access Memory Channel

The implicitly addressed memory channel is a quick access memory location. Pressing the STORE switch without entering data beforehand loads the present receiver parameters into the quick access channel. Pressing the RECALL switch without entering data beforehand sets the receiver to the parameters stored in the quick access channel. In either case, the MEM ADRS display goes blank to indicate the quick access channel.

### 2.4.4.3 Accessing Numbered Memory Channels

The following procedure loads the present receive parameters into one of the numbered memory channels. Example 5 shows a typical memory loading command.

- Loading Numbered Memory - Procedure

1) Enter destination channel number on keypad
2) Terminate command by pressing STO termination switch.

Example 5: Store present receiver parameters in memory channel 15.
[1] [5]
[STO]
(1) Data. entry; "15" displayed in FREQUENCYOMHZ display window.
(2) Termination command; present receiver parameters stored in channel 15; " 15 " displayed in MEM ADRS display window.

The following procedure recalls the parameters stored in one of the numbered memory channels and sets the receiver to those parameters. Example 6 shows a typical memory recall commandn

- Recall Memory - Procedure

1) Enter designated channel number on keypad.
2) Terminate command by pressing RCL termination switch.

Example 6: Set receiver to the parameters stored in memory channel 49.
[4] [9]
[RCL]
(1) Data entry; "49" displayed in FREQUENCYoMHZ display window.
(2) Termination command; receiver parameters set to those stored in memory channel 49; front panel indicators and displays reflect updated parameters; "49" displayed in MEM ADRS display window.

The following procedure updates one or more individual parameters in a designated numbered memory channel. Example 7 shows a typical memory update command sequence.

- Update Memory - Procedure

1) Enter designated channel number on keypad.
2) Terminate recall command by pressing RECALL termination switch.
3) Update desired individual parameters.
4) Enter designated channel number on keypad.
5) Terminate command by pressing STORE termination switch.

Example 7: Change IF bandwidth stored in memory 55 from 50 kHz to 6 kHz .
[5] [5]
[RCL]
(1) Data. entry; "55" displayed in FREQUENCY/MHZ display window.
(2) Termination command; receiver parameters set to those stored in memory channel 55 ; front panel indicators and displays reflect channel 55 parameters; "55" displayed in MEM ADRS display window.
[6]
[5] [5]
[STO]
(3) 6 kHz IF bandwidth selected.
(4) Data entry; "55" displayed in FREQUENCY/MHZ display window.
(5) Termination command; updated parameters stored in memory channel 55; " 55 " displayed in MEM ADRS display window.

### 2.4.4.4 Memory Examination

The memory EXAM switch displays the parameters stored in memory without disturbing the operating parameters of the receiver. Pressing the EXAM switch without entering data beforehand causes the front panel indicators and displays to display the stored parameters of the next sequential memory channel after the one displayed in the MEM ADRS display window. For example, if "15" is displayed in the MEM ADRS display window, pressing EXAM results in a flashing " 16 " in the MEM ADRS display window, indicating that the parameters displayed on the front panel indicators and displays are those stored in memory channel 16. Pressing EXAM again causes channel 17 's parameters to be displayed, and so on until channel 99 is reached. At that time, pressing EXAM displays channel 1 's parameters. Pressing the CLEAR switch, located in the lower right-hand corner of the keypad, terminates the memory examination mode and causes the front panel displays and indicators to reflect the present receiver operating parameters. The address of the last channel examined will be displayed in the MEM ADRS display window.

- Memory Examination (Specific Channel) - Procedure

1) Enter designated channel number on keypad.
2) Terminate examination command by pressing EXAM termination switch.
3) Terminate memory examination mode by pressing CLEAR keypad switch.

## Example 8: Examine the contents of memory channel 15.

## [1] [5]

[EXAM]
[CLEAR]
(1) Data. entry; "15" displayed in FREQUENCY/MHZ display window.
(2) Termination command; flashing b15" displayed in MEM ADRS window; front panel indicators and displays reflect parameters reflect parameters stored in memory channel 15.
(3) Termination command; "15" displayed in MEM ADRS display window; front panel reflects receiver operating parameters.

The following procedure examines the contents of a sequential group of memory channels. Example 9 shows a typical sequential channel memory examination command.

- Memory Examination (Sequential Group) - Procedure

1) Enter first channel number on keypad.
2) Terminate examination command by pressing EXAM termination switch.
3) Press EXAM switch again for each channel to be examined.
4) Terminate memory examination mode by pressing CLEAR keypad switch.

Example 9: Examine the contents of memory channels 35 and 36.
[3] [5]
[EXAM]
[EXAM]
[CLEAR]
(1) Data entry; "35" displayed in FREQUENCY/MHZ display window.
(2) Termination command; flashing "35" displayed in MEM ADRS display window; front panel indicators and displays reflect parameters stored in memory channel 35.
(3) Termination command; flashing "36" displayed in MEM ADRS display window; front panel indicators and displays reflect parameters stored in memory channel 36.
(4) Termination command; "36" displayed in MEM ADRS display window; front panel indicators and displays reflect receiver operating parameters stored.

### 2.4.5 MEMORY SCAN OPERATIONS

### 2.4.5.1 General

The MFP memory scan capability allows the receiver to sequentially scan a selected group of memory channels. During scan operation the stored parameters of each memory channel are automatically recalled and transferred to the receiver. As each channel is recalled, the received signal strength is compared to a selected threshold level stored in that channel. When a channel is located where signal strength equals or exceeds the threshold level, the scanning operation stops for a selected dwell time, and then restarts automatically.

### 2.4.5.2 Special Purpose Memory Channels

Numbered memory channels 17 through 29 are utilized to store sector scan data. These special purpose channels are passed over during memory channel scanning operations. They can be accessed individually as described in paragraph 2.3. Paragraph 2.5 describes how memory channels 17 through 29 are utilized during sector scan operations.

### 2.4.5.3 Threshold Level

During all MFP scan operations, the received signal strength is compared to a selected threshold level. The threshold levels are entered as single digit codes which are stored, along with the receiver parameters, in the memory channels. Table 2-2 lists the single digit threshold level codes and their corresponding signal strength levels in dBm .

Table 2-2. Threshold Data Codes

| Keypad Entry <br> Code | Threshold <br> Level |
| :--- | :--- |
| 0 | *See Note 1 |
| 1 | -110 dBm |
| 2 | -100 dBm |
| 3 | -90 dBm |
| 4 | -80 dBm |
| 5 | -70 dBm |
| 6 | -60 dBm |
| 7 | -50 dBm |
| 8 | -30 dBm |
| 9 | *See Note 2 |

* NOTE: 1. An entered threshold data code of 0 causes the SCAN to stop, regardless of signal strength, at the channel where the 0 is stored.

2. An entered threshold data code of 9 causes the SCAN to continue regardless of signal strength.

The following procedure loads threshold data, along with the present receiver operating parameters, into a memory channel. Example 10 shows a typical threshold command.

- Threshold Entry - Procedure

1) Enter desired threshold code on keypad.
2) Terminate threshold command by pressing THRS termination switch.
3) Enter designated channel number on keypad.
4) Terminate command by pressing STORE termination switch.

Example 10: Store present receiver parameters and threshold of 5 in memory channel 62.
[THRS]
[6] [2]
[STORE]
(1) Threshold data entry; "5" displayed in FREQUENCY/MHZ display window.
(2) Termination command; "5" displayed in BFO OFS/THRS LVL display window.
(3) Channel number data entry; "62" displayed in FREQUENCY/MHZ display window.
(4) Termination command; "62" displayed in MEM ADRS display window; all front panel data stored in memory channel 62.

Threshold level display: Pressing THRS, without entering keypad data beforehand, causes the threshold data to be displayed in the BFO OFS/THRS LVL display window. Pressing THRS, without entering keypad data beforehand, during AUTO SCAN or EXAM operations, causes the stored threshold level for each channel accessed to be displayed.

### 2.4.5.4 Dwell Time

When AUTO SCAN mode is utilized, a dwell time must be selected. The dwell time is used when signal strength exceeds threshold. Entering a dwell time of " 0 " selects 0.1 seconds. Entering a dwell time of " 1 " through " 8 " selects 1 through 8 seconds respectively. If a dwell time of "9" is entered the scan stops until restarted by pressing aUTO SCANn

The following procedure enters a desired dwell time. Example 11 shows a typical dwell time command.

- Dwell Time - Procedure

1) Enter desired dwell time code on keypad.
2) Terminate command by pressing DWL termination switch.

## Example 11: Establish a dwell time of 3 seconds.

[DWL]
(1) Desir.ed data entry; "3" displayed in FREQUENCY/MHZ display window.
(2) Termination command; dwell time established at 3 seconds; DWELL LED illuminated; "3" displayed in BFO OFS/THRS LVL display window.

Dwell Time Display Mode: Pressing DWELL, without entering keypad data beforehand, causes the present dwell time code to be displayed in the BFO OFS/THRS LVL display window.

### 2.4.5.5 Memory Scan Control

Pressing AUTO SCAN initiates a sequential scan of the memory channels. If none of the memory channels are locked out of the scan, the receiver will scan through all channels.

Once started, the scan will continue until stopped by again pressing the AUTO SCAN switch. The AUTO SCAN LED indicator illuminates whenever the receiver is scanning.

The following procedure locks out an individual channel. Example 12 shows a typical single channel lockout command.

- Single Channel Lockout - Procedure

1) Enter designated channel number on keypad.
2) Terminate command by pressing LOCK OUT termination switch.

Example 12: Lockout memory channel 3.
(1) Data entry; "3" displayed in FREQUENCY/MHZ display window.
[LOCKOUT]
(2) Termination command; channel 3 locked out of sean; LOCK OUT LED indicator illuminates.

## NOTE

When the LOCK OUT switch is pressed, the LOCK OUT LED indicator illuminates. Pressing LOCK OUT again, without entering keypad data beforehand, causes the previously locked out channel or group of channels to be returned to the scan.

The following procedure locks out a sequential group of memory channels. Example 13 shows a typical channel group lockout command.

- Channel Group Lockout - Procedure

1) Enter first and last channel numbers of the group on the keypad, separated by a decimal point.
2) Terminate command by pressing LOCK OUT termination switch.

Example 13: Lock out channels 2 through 4.
[2] [0] [4]
(1) Data entry; "14" displayed in FREQUENCY/MHZ display window
[LOCK OUT]
(2) Termination command; channels 2 , 3 and 4 locked out of scan.

The following procedure adds or returns a channel or group of channels to the scan. The procedure is similar to the previously discussed lockout commands. Examples 14 and 15 show typical commands for adding channels to the scan.

- Add Memory Channel(s) to Scan - Procedure

1) Enter designated channel or group of channels on keypad.
2) Terminate command by pressing LOCK OUT termination switch twice.

Example 14: Add channel 14 to previously established scan of channels 1 to 3.
[1] [4]
[LOCKOUT][LOCKOUT]
(1) Data. entry; "14" displayed in FREQUENCY/MHZ display window.
(2) Termination command; pressing AUTO SCAN results in receiver scanning channels $1,2,3$ and 14 .

Example 15: Add channels 4 to 9 to previously established scan of channels 1 to 3.
[4] [.] [9]
[LOCKOUT][LOCKOUT]
(1) Data entry; "4c9" displayed in FREQUENCY/MHZ display window.
(2) Termination command; pressing AUTO SCAN results in receiver scanning channels 1 to 9 .

The following procedure returns all locked out channels to the scan.

- All Channel Scan - Procedure

1) Enter 0 on keypad.
2) Terminate command by pressing LOCK OUT termination switch twice.

Example 16 shows how the above procedure can be utilized to establish a scan of all but a few memory channels.

Example 16: Establish scan of all memory channels except 5 and 6.
[0]
(1) Data entry; "0" displayed in FREQUENCY/MHZ display window.
[LOCKOUT][LOCKOUT]
[5] [.] [6]
[LOCKOUT]
(2) Termination command; all locked out channels are returned to the scan.
(3) Data entry; "5c6" displayed in FREQUENCY/MHZ display window.
(4) Termination command\{ channels 5 and 6 are locked out of scan.

## 2.4 .6

## SECTOR SCAN OPERATION

The MFP sector scan feature allows the operator to establish two scan sectors. Memory channels 17 through 29 are reserved for storage of sector scan data. The tuned frequency data stored in these channels, as shown in Table 2-3, represents the start and stop frequencies ( $f 1$, to $f_{2}$ ) for the two programmable sectors, the frequency step size (Sector B only), and designated lockout frequencies (four per sector).

The receiver can be commanded to scan Sector A or Sector B individually or to scan both sectors. During a Sector A scan the receiver scans from $f_{1}$ to $f_{2}$ in steps equal to one-half of the selected IF bandwidth. During a Sector $B^{1}$ scan the receiver scans from $f_{1}$ to $f_{2}$ in steps equal to the tuned frequency data stored in memory channel 21.

Table 2-3. Sector Scan Frequency Data Storage


### 2.4.6.1 Sector Scan Frequency Data

The RF tuned frequency data stored in channel 17 represents the start frequency ( $f_{1}$; of the first sector (Sector A). The RF tuned frequency data stored in channel 18 represents the stop frequency $\left(f_{2}\right)$ of Sector A. During a Sector A scan the receiver scans between $f_{1}$ and $f_{2}$. The frequency step size during a Sector $A$ scan is equal to one-half the selected IF bandwidth.

The RF tuned frequency data stored in channel 19 represents the start frequency ( $f$ ) of the second sector (Sector B). The RF tuned frequency data stored in channel 20 represents the stop frequency ( $f_{2}$ ) of Sector B. During a Sector B scan the receiver scans between $f_{1}$ and $f_{2}$. The frequency step size during a Sector $B$ scan will be equal to the RF tuned frequency stored in channel 21 . If an $R F$ tuned frequency of 00.00000 MHz is stored in channel 21 the step size will be equal to onehalf the selected IF bandwidth.
o Sector A Frequency Data Entry - Procedure

1) Tune receiver to desired $f_{1}$. .
2) Store $\mathrm{f}_{1}$ data in channel 17 by entering "17" on keypad and pressing STO termination switch.
3) Tune receiver to desired $f_{2}$.
4) Store $\mathrm{f}_{2}$ data in channel 18 by entering "18" on keypad and pressing STORE termination switch.
Example 17: Establish a Sector A scan between 5 MHz and 10 MHz
[5] [MHz]
(1) Receiver tuned to 5.00000 MHz
[17] [STO]
(2) 5.00000 MHz (f1) stored in channel 17; "17" displayed in MEM ADRS display window.
[1] [0] [MHz]
(3) Receiver tuned to 10.00000 MHz .
[1] [8] [STO]
(4) 10.00000 MHz (f2) stored in channel 18; " 18 " displayed in MEM ADRS display window.
o Sector B Frequency Data Entry - Procedure
5) Tune receiver to desired $f_{1}$.
6) Store $\mathrm{f}_{1}$ data in channel 19 by entering "19" on keypad and pressing STO termination switch.
7) Tune receiver to desired $f_{2}$.
8) Store $\mathrm{f}_{2}$ data in channel 20 by entering "20" on keypad and pressing STO termination switch.
9) Tune receiver to desired scan step size.
10) Store step size data in channel 21 by entering " 21 " on keypad and pressing STO termination switch.

Example 18: Establish Sector B scan between 3.5 MHz and 3.9 MHz in 10 kHz steps.

| [3] | [.] | [5] [MHz] | (1) | Receiver tuned to 3.50000 MHz . |
| :---: | :---: | :---: | :---: | :---: |
| [1] | [9] | [STO] | (2) | 3.50000 MHz (f1) stored in channel 19; "19" displayed in MEM ADRS display window. |
| [3] | [.] | [9] | (3) | Receiver tuned to 3.90000 MHz . |
| [2] | [0] | [STO] | (4) | 3.90000 MHz (f2) stored in channel 20 ; " 20 " displayed in MEM ADRS display window. |
| [1] | [0] | [ KHz ] | (5) | Receiver tuned to 10 kHz . |
| [2] | [1] | [STO] | (6) | 10.00 kHz (step size) stored in channel 21; "21" displayed in MEM ADRS display window. |

### 2.4.6.2 Sector Lockout

When a single sector scan is desired, the undesired sector must be locked out. The following procedure locks out a sector to establish a single sector scann Example 19 shows a typical sector lockout command.

- Sector Lockout - Procedure

1) Enter designated sector channel number on keypad (17 or 18 to lockout Sector A, 19 or 20 to lockout Sector B).
2) Terminate command by pressing LOCK OUT termination switch.

Example 19: Lockout Sector B (establish single sector scan of Sector A).
[1] [9]
[LOCKOUT]
(1) Data entry; "19" displayed in FREQUENCY/MHZ display window.
(2) Termination command \{channels 19 and 20 will display a lockout attribute when accessed\{ Sector B locked out.

The following procedure restores a previously locked out sector to establish a two sector scan. Example 20 shows a typical sean sector restoration command.

- Return Previously Locked Out Sector - Procedure

1) Enter designated sector channel number on keypad (17 or 18 for Sector A, 19 or 20 for Sector B).
2) Terminate command by pressing LOCK OUT termination switch twice.

Example 20: Return previously locked out Sector B.
[2] [0]
(1) Data entry; "20" displayed in FREQUENCY/MHZ display window.
[LOCKOUT][LOCKOUT]
(2) Termination command; Sector $B$ returned to the scan.

Sector lockout and sector return commands may be made at any time. If a sector lockout command is made while the receiver is scanning the designated lockout sector, the scan will continue until the sector's $\mathrm{f}_{2}$ frequency is reached. At that time, the lockout command will take effect.

### 2.4.6.3 Sector Scan Receiver Register Data

The receiver register parameters (except for RF tuned frequency) should be set prior to initiating a sector scan. This may be done manually, or by recalling receiver register data previously stored in any of the 99 memory channels. The procedures in the following paragraphs can be used to initially a single sector scan or a two sector scan. If the microprocessor receives a sector scan command and the other sector is not locked out, the receiver first scans the desired sector and then scans the other sector.

### 2.4.6.3.1 Sector Scan/Receiver Register Data Source - Manual

The following procedure manually sets the receiver register parameters, and then initiates a sector scan. Example 21 shows a typical sector scan command sequence.

- Sector Scan Command - Procedure 1

1) Set receiver register parameters as desired.
2) Enter designated channel number ( 17 for Sector A, 19 for Sector B) on keypad.
3) Terminate command by pressing AUTO sCAN termination switch.

Example 21: Initiate a Sector $B$ scan with the receiver parameters set as follows: AM mode, FAST AGC, 6 kHz IF bandwidth, Threshold level of 5 .
[AM] [FAST] [6]
[5] [THRS]
[1] [9]
[AUTOSCAN]
(1) Desired receiver parameter entry.
(2) Threshold level set to 5. "5" displayed in BFO OFS/THRS LVL display window.
(3) Data entry; "19" displayed in FREQUENCYoMHZ display window.
(4) Termination command; receiver scans Sector B; "19" displayed in MEM ADRS display window

### 2.4.6.3.2 Sector Scan/Receiver Register Data Source - F1 or F2 Channel

The receiver register data stored with each sector's $f_{1}$ and $f_{2}$ frequencies can be utilized to set the receiver parameters prior to initiating a sector scan. This feature provides the capability to store two sets of receiver register data for each scan sectorn

The following procedure recalls receiver register data from a sector $f_{1}$ or $f_{2}$ frequency storage channel and initiates a sector scan in that sector. Examples 22
and 23 show typical command sequencesn

- Sector Scan Command Sequence - Procedure 2

1) Enter designated channel number (17 or 18 for Sector A, 19 or 20 for Sector B).
2) Terminate recall command by pressing RCL termination switch.
3) Terminate command sequences by pressing AUTO SCAN termination switch.
"0

Example 22: Initiate a Sector A scan utilizing the receiver register parameters stored with the sector's f1 frequency in memory channel 17.
[1] [7]
[RCL]
[AUTO SCAN]
(1) Data entry; "17" displayed in FREQUENCY/MHZ display window.
(2) Termination command; receiver parameters set to those stored in channel 17; "17" displayed in MEM ADRS display window.
(3) Termination command; receiver scans Sector A; "17" remains displayed in MEM ADRS display window.

Example 23: Initiate a Sector A scan utilizing the receiver register parameters stored with the sector's f2 frequency in memory channel 18.
[1] [8]
[RCL]
[AUTO SCAN]
(1) Data entry; "18" displayed in FREQUENCY/MHZ display window.
(2) Termination command; receiver parameters set to those stored in channel 18; "18" displayed in MEM ADRS display window.
(3) Termination command; receiver scans Sector A; "18" displayed in MEM ADRS display.

Comments: In either of the above examples, it is not necessary to enter "17" on the keypad before pressing AUTO SCAN. Pressing AUTO SCAN without entering keypad data beforehand, and with " 17 " or "18" displayed in the MEM ADRS display window, automatically initiates a Sector A scan. Likewise, pressing AUTO SCAN, with a " 19 " or " 20 " displayed automatically initiates a Sector B scan.

### 2.4.6.3.3 Sector Scan/Receiver Register Data Source - Memory Channel

The receiver register data stored in any of the 100 memory channels may be utilized to set the receiver parameters prior to initiating a sector scan. The following procedure recalls receiver register data from any memory channel and initiates a sector scan. Example 24 shows a typical command sequence.

- Sector Scan Command Sequence - Procedure 3

1) Enter receiver register data location (channel number) on keypad.
2) Terminate recall command by pressing RCL termination switch.
3) Enter sector channel number ( 17 for Sector A, 19 for Sector B) on keypad.
4) Terminate command sequence by pressing AUTO SCAN termination switch.

## Example 24: Initiate a Sector $B$ scan utilizing receiver register parameters stored in memory channel 45.

| [4] [5] | (1)Data entry; "45" displayed in <br> FREQUENCY/MHZ display windown |
| :--- | :--- |
| [RCL] | (2)Termination command; receiver <br> parameters set to those stored in <br> channel 45; "45" displayed in MEM |
| [1] [9] | (3DRS display window.Data entry; "19" displayed in <br> FREQUENCY/MHZ display windown |
| [AUTO SCAN] | (4)Termination command; receiver <br> scans Sector B; "19" displayed in |
|  |  |

### 2.4.6.3.4 Frequency Lockout

The frequency lockout feature of the MFP allows up to four frequencies per sector to be locked out of the scan. A desired tuned frequency is locked out by storing it in one of eight designated scan frequency lockout channels. Sector A lockout frequencies must be stored in memory channels 22 through 25 . Sector B lockout frequencies must be stored in memory channels 26 through 29.

When a specific frequency is locked out of a sector scan, all active channels within a certain frequency band surrounding that frequency are ignored during the scan operation. The width of the locked out frequency band is determined y the IF bandwidth selected for use during the sector scan, and is approximately equal to the 60 dB bandwidth of the selected IF filter.

The following procedure locks out a specific tuned frequency. Example 25 shows a typical tuned frequency lockout command.

- Tuned Frequency Lockout - Procedure

1) Tune receiver to desired lockout frequency.
2) Enter designated lockout channel number (22 through 25 for Sector A, 26 through 29 for Sector B).
3) Terminate command sequence by pressing STO termination switch.

## Example 25: Lockout 1.30000 Mhz from a previously Sector A scan.

[1] [.] [3] [MHz]
(1) Tuned frequency data entry and termination command; receiver tuned to 1.30000 MHz ; " 1.30000 " displayed in FREQUENCY/MHZ display window.
[2] [2]
[STO]
(2) Data entry; "22" displayed in FREQUENCY/MHZ display window.
(3) Termination command; "22" displayed in MEM ADRS display window; LOCK OUT indicator illuminates indicates that channel 22 contains a lockout attribute.

### 2.4.7 SPECIAL FUNCTION TERMINATION SWITCH (*)

### 2.4.7.1 General

The special function key located in the lower left hand corner of the general purpose keypad is utilized to access MF P special functions. The following paragraphs define the MFP special functions. The special access commands for each function are shown in parenthesis in the paragraph headings.

### 2.4.7.2 Built-In Test Equipment

Entering ${ }^{*} 17$ on the keypad accesses the MFP's Built-In Test Equipment (BITE) program. Accessing the BITE program has the following initial effects on the front panel LED displays and indicators:

- Illumination of all front panel LED indicators.
- Display of a zero in all front panel seven segment displays.

After the BITE program is accessed, it may be utilized to verify proper operation of the front panel switches. As each switch is pressed, a corresponding two-digit code appears at one of two designated locations on the front panel.

The front panel switches are divided into two groups. Group 1 switches are on the right side of the front panel and Group 2 switches are on the left. Pressing a Group 1 switch causes its corresponding two-digit code to be displayed in the 100 Hz and 10 Hz digits of the FREQUENCY/MHz display window. Pressing a Group 2 switch causes its two-digit code to be displayed in the MEM ADRS display window. Group 1 and Group 2 display codes are listed in Tables 2-4 and 2-5 respectively. To take the receiver out of the BITE mode, press the CLEAR key.

Table 2-4. Group 1 Switch Codes

| Switch | Code | Switch | Code |
| :---: | :---: | :---: | :---: |
| 0 | 00 | - | 22 |
| 1 | 01 | CLEAR | Clears Bite |
| 2 | 02 | BFO +/- | 60 |
| 3 | 03 | MHz | $6 \quad 1$ |
| 4 | 10 | kHz | $6 \quad 2$ |
| 5 | 11 | Special Function (*) | 63 |
| 6 | 12 | LCK | 70 |
| 7 | 13 | SLO | 71 |
| 8 | 20 | MED | 72 |
| 9 | 21 | FAST | 73 |

Table 2-5. Group 2 Switch Codes

| Switch | Code | Switch | Code |
| :---: | :---: | :---: | :---: |
| A.M | 00 | 6 | 24 |
| FM | 01 | 50 | 23 |
| USB | 02 | LOCAL | 31 |
| LSB | 03 | RECALL | 35 |
| DF | 04 | REMOTE | 41 |
| CWV | 05 | STORE | 45 |
| MA | 06 | LINE AUDIO | 50 |
| MGC | 10 | SIGNAL STR | 51 |
| SLOW | 11 | EXAM | 60 |
| FAST | 12 | HAND OFF |  |
| BFO (TUNE) | 15 | AUTO SCAN | $6 \quad 2$ |
| . 3 | 20 | LOCK OUT | 65 |
| 1 | 21 | THRS | 66 |
| 3.2 | 22 | DWELL |  |

### 2.4.7.3 Special Master Mode

Figure 2-3 shows a typical master/slave setup. In a master/slave system, only one receiver may be designated as the master, while the other receiver must designated as the slave. This is a hard-wired option with the following special master mode connections in the A-model.

FUNCTION

PROT GND
TXD
RXD
CTS
DRT
SIG GND

232J1 NB1 MASTER RX

Pin A
Pin $B$

Pin E

Pin G

232J1 NB2
SLAVE RX
Pin A
Pin C

Pin K

-     - 

Pin G


[^0]Figure 2-3. Master/Slave Setup
(THIS PAGE DELIBERATELY LEFT BLANK)

### 2.4.7.4 Special Function Display

Pressing the special function (*) key, without entering data beforehand, initiates the special function display mode. During the special function display mode, the two least significant digits in the FREQUENCY/MHz window will display (in sequential order) the receiver address and the entry code number of any active MFP special functions.

### 2.4.7.5 Erase Memory

Entering 10* on the keypad erases the contents of all memory channels, including the quick access channel, and then performs a RESET sequence. The RESET sequence leaves the receiver in local mode.

### 2.4.8 REMOTE OPERATION VIA RS-232 SERIAL INTERFACE

The RS-232 Option permits full control of receiver parameters by an external controller. To establish remote operation, the operator must depress the front panel REMOTE keypad.

### 2.4.8.1 Preparation For Operation

Prior to remote operation via RS-232, the receiver must be place in the remote operating mode and remote operating parameters must be established in the I/O board and switches.

### 2.4.8.1.1 Remote Operating Mode

A receiver to be addressed as a listener must be placed in the remote operating mode by depressing the front panel REMOTE keypad. The receiver can be addressed to talk regardless of the receiver operating mode. Local or remote operating mode cannot be established by remote command.

### 2.4.8.1.2 Baud Rate

The baud rate is established by precoded entries to the S1 switch assembly on the Asynchronous I/O Board (A6A3). An open switch denotes binary 1 and a closed switch denotes binary 0 . Table 2-6 lists the baud rate codes.

Table 2-6. Baud Rate Codes

| Baud Rate | $\frac{\mathrm{S} 1-4}{}$ | $\frac{\mathrm{~S} 1-3}{}$ | $\frac{\mathrm{~S} 1-2}{}$ | $\frac{\mathrm{~S} 1-1}{2}$ |
| :---: | :---: | :---: | :---: | :---: |
| 50 | 0 | 0 | 0 | 0 |
| 75 | 0 | 0 | 0 | 1 |
| 110 | 0 | 0 | 1 | 0 |
| 134.5 | 0 | 0 | 1 | 1 |
| 150 | 0 | $\vdots$ | 0 | 0 |
| 300 | 0 | 1 | 0 | 1 |
| 600 | 0 | 1 | 1 | 0 |
| 1200 | 0 | 1 | 1 | 1 |
| 1800 | 1 | 0 | 0 | 0 |
| 2000 | 1 | 0 | 0 | 1 |
| 2400 | 1 | 0 | 1 | 0 |
| 4800 | 1 | 0 | 1 | 1 |
| 7200 | 1 | 1 | 0 | 0 |
| 9600 | 1 | 1 | 1 | 1 |
| 19200 | 1 | 1 | 1 | 1 |

### 2.4.8.1.3 Receiver Address, Parity and Master/Slave

Up to 15 properly addressed receivers can be controlled by one controller. The receivers are series connected or "daisy-chained". The MON OUT of the first receiver is connected to the REM IN connector of the next receiver in the chain. Only one receiver is interfaced directly to the controller. The serial data stream from the remote controller is actively repeated to all receivers in the chain, but only the addressed receiver "recognizes" its address and accepts the data.

Receiver address is established by four switch settings in the S2 assembly on the I/O board. Table 2-7 lists the functions of the S2 switch assembly. A closed switch denotes a binary 1 and an open switch denotes a binary 0 . Switch 8 is always open for the receiver to be a slave and closed for the receiver to be a master. As a slave, the receiver can be commanded and monitored by a master receiver. Switches 6 and 7 are used if the remote control equipment provides a parity bit. Switch 6 is closed for even parity and open for odd parity. Valid receiver addresses are binary coded from 0 to 30 in Table 2-8.

Table 2-7. Switch Assembly (S2) Functions

| S2-8 | S2-7 | S2-6 | S2-4 | S2-3 | S2-2 | S2-1 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Master/ <br> Slave <br> Enable | Parity <br> Enable | Even <br> Parity <br> Bit | 8 | 4 | 2 | 1 |

Table 2-8. Receiver Address Codes

| Receiver Address | S2-5 | S2-4 | S2-3 | S2-2 | S2-1 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 |
| 12 | 0 | 1 | 1 | 0 | 0 |
| 13 | 0 | 1 | 1 | 0 | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 |
| 15 | 0 | 1 | 1 | 1 | 1 |

### 2.4.8.2 Operation Via RS-232 Interface Bus

The receiver is ready to be interfaced with a remote control device compatible with the RS-232 EIA standard interface bus. The option uses nine of the available interchange channels provided by the bus: one for ground, two for data output, two for data input and four for handshake protocol. The interface point between receiver and remote control equipment is the connector at the REM IN port located at the receiver's rear panel. A connector located at the receiver's rear panel MON OUT port is the interface point for connecting the next receiver in the series chain. Up to $15 \mathrm{WJ}-8718-19 / \mathrm{FE}$ receivers configured as slaves can be controlled by one remote control device, as shown in Figure 2-5.


Figure 2-4. Daisy Chain Configuration

Table 2-9 lists the RS-232 connection pin numbers with the respective interchange signals and functions. The connection between receivers will be pin for pin compatible if each receiver is connected as shown in Figure 2-4. If one receiver is configured as a master and the remainder are slaves, it is necessary to use reverse cable (modem bypass).

Table 2-9. RS-232 Connector Pin Assignments

| Pin Number | Signal | Description |
| :---: | :--- | :--- |
| A | P-GND | Protective Ground |
| B | TxD | Transmitted Data |
| C | RxD | Received Data |
| D | RTS | Request To Send |
| E | CTS | Clear To Send |
| F | DSR | Data Set Ready |
| G | S-GND | Signal Ground |
| H | SYNC - TxC | Transmit Timing Signal |
| J | DTR - RxC | Receive Timing Signal |
| K |  | Data Terminal Ready |

### 2.4.8.2.1 Byte Structure

The I/O software structure of the WJ-87.18/232 Option consists of a series of 11 -bit binary code words (if parity is used), presented in a pre-determined sequence. Each byte is composed of a start bit, eight data bits, a parity bit (if parity is enabled), and a stop bit. Figure 2-5 illustrates the byte structure. Binary coded logic levels are high ( -6 V ) or low ( +6 V ).


Figure 2-5. Byte Structure

### 2.4.8.2.2 Data Format: Tier 1

Full Status parameter data of a standard $W J-8718$ HF Receiver equipped with the WJ-8718/232 Option is contained in seven bytes; these seven bytes, plus address and data definition bytes and a byte for Tier 2 access, comprise Tier 1 of the I/O software structure. Tier 2 is discussed in paragraph 2.4.8.2.6. Tier 1 is structured as follows:

1. Byte 1: Receiver Address Byte.
2. Byte 2: Data Information Definition Byte (DID).
s. Bytes 3 through 9 (10): In monitor mode, Byte 3 is the address byte returned from the receiver to controller and Bytes 4 through 10 are data. In command mode, Bytes 3 through 9 are parameter data (controller to receiver).
3. Byte 10 or 11: Tier 2 Access Byte.

### 2.4.8.2.3 Receiver Address Byte

The data bits in the first byte (controller to receiver) determine which receiver is to be referenced. Up to 15 receivers can be controlled and monitored by one controller (such as the WJ-9644A Asynchronous Controller) via the WJ-8718/232 Option. As shown in Table 2-10 five bits of the receiver address byte allow for 15 unique binary-coded addresses from 0 through 15. The three most significant bits of the address are a binary code (110) that uniquely identifies the function (receiver address) of the byte.

In the monitor mode, the receiver address byte is returned to the controller by the receiver prior to the transmission of data (receiver to controller).

Table 2-10. Receiver Address Byte

| $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 0 |  |  |  |  |  |  |
|  | Address <br> Byte Code |  | Receiver Address: |  |  |  |  |  |

### 2.4.8.2.4 Data Information Definition

Byte 2 is the Data Information Definition (DID) Byte, as shown in Table 2-11. The three most significant bits of the DID byte are a binary code (111) which uniquely defines Byte 2 as a DID byte. The 2 bit of the DID byte is the command/monitor bit, which defines the function of the data bytes to follow Byte 2 . If the $2^{4}$ bit is logic 1 , the controller desires to command the receiver and will transmit receiver parameter data in the byte or bytes to follow Byte 2. If the 2 bit is logic 0, the controller desires to monitor the receiver; the receiver will transmit the address byte (paragraph 1.5.2.3), and the byte or bytes that follow will contain the current status of the addressed receiver (transmitted by the receiver).

Table 2-11. DID Byte

| $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 1 | 1 |  |  |  |  |  |
|  | $\mathrm{Co}$ |  | C/M | S/A | 00 | $\begin{aligned} & \text { ter } \\ & 11 \end{aligned}$ |  |

$C / M=$ Command (1) or Monitor (0)
$\mathrm{S} / \mathrm{A}=$ Single (1) or All (0) Bytes

The $2^{3}$ bit of the DID defines the number of data bytes to succeed Byte 2 ; a logic 1 indicates a single byte and a logic 0 indicates all bytes.

The remaining three bits of the DID byte contain a binary coded register address. All receiver parameters are stored in seven 8 -bit registers, addressed in binary code from 0 through 7. If all parameter data are to be transmitted, the logic levels of the three register address bits are irrelevant; however, if one word of receiver parameter data is to be transmitted, the 3-bit binary code for the desired register must be established in the $2^{0}, 2^{1}$, and $2^{2}$ bits of the DID byte (paragraph 2.4.8.2.4).

### 2.4.8.2.5 Data Bytes

If all receiver parameters are to be controlled, the bytes following the DID Byte will contain data transmitted from receiver to controller or from controller to receiver, as listed in Table 2-12. If all receiver parameters are to be monitored, Byte 3 will be the address return byte followed by data, Bytes 4 through 10. Transmission of less than complete parameter data requires that the register associated with a articular byte of data be addressed in the DID byte. The selected data will then be transmitted as Byte 3 or 4. Paragraphs 2.4.8.2.7 and 2.4.8.2.8 contain examples of data formats for full and partial status transmissions, in monitor and command modes.

### 2.4.8.2.6 Tier 2 Access Byte

A second tier containing four pages of eight bytes each is available and is accessed by the byte shown in Table $2-13$. The 3 most significant bits of the byte are the DID code (111), the $2^{4}$ and $2^{3}$ bits are a page code, and the remaining three bits are the address code for the second tier.

Tier 2 contains four pages of eight bytes each. At this point in time, the four most significant bits of the 000 register byte on page 1 are the only bits of Tier 2 with an assigned function. These four bits contain the 100 digit (in BCD form) of tuned frequency if the WJ-8718 HF Receiver is equipped with both the WJ-8718/232 and the WJ-8718/1 Hz Options. The remaining bytes in Tier 2 are available for future expansion. Table 2-14 is the data format for Byte 1 on Page 1 of Tier 2. This byte must be preceded by a receiver address byte, a Tier 2 access byte, and a DID byte containing the register address 000. See paragraph 2.4.8.2.9 for an example of data format requiring access to Tier 2.

### 2.4.8.2.7 Monitor Format Example

Table 2-16 contains examples of data format for full status monitor operations of a WJ-8718A HF Receiver, equipped with the $W J-8718 \mathrm{~A} / 232 \mathrm{M}$ and MFP Options. Table 2-17 contains examples of data format for partial status monitor operations. Operating parameters of the receiver to be monitored (at address 15) are given in Table 2-18.

### 2.4.8.2.8 Command Format Example

In the example in Table 2-19 the receiver at address 4 is commanded to establish the listed parametersn Table 2-20 lists the data format for full status command and Table 2-21 is the data for commanding only the BFO frequency.

### 2.4.8.2.9 Access Tier Format

In this example, shown in Table 2-22, it is assumed that the receiver is equipped with 1 Hz tuning and the controller desires to monitor the status of the 1 Hz digit of tuned frequency. The receiver is at address 20 and the 1 Hz digit is 6 .

Table 2-12. Register Parameter Data


* COMMAND: AGC DUMP, MONITOR: FAULT (for future expansion)

NOTE: BFO and TUNED frequencies in BCD ( Hz )

Function Codes


Table 2-13. Tier 2 Access Byte


Table 2-14. Tier 2, Page 1, Byte 1

| $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |  |  |  |  |
| $10^{0}$ |  | TUNED FREQ. | UNUSED |  |  |  |  |

Table 2-15. Tier 2, Page 1, Byte 2

| $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |
| :--- | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
| COR | X | X | X | COR THRESHOLD |  |  |  |
| FLAG |  |  |  |  |  |  |  |

Table 2-16. Full Status Monitor

| Byte Number | Binary Code |  |
| :---: | :---: | :---: |
| 1 | 11001111 | Controller to Receiver |
| 2 | $11100 \times \times$ | Controller to Receiver |
| 3 | 11001111 |  |
| 4 | $\mathrm{x} \times \mathrm{x} \times 0001$ |  |
| 5 | 00100011 |  |
| 6 | 01000101 | Receiver to Controller |
| 7 | $\begin{array}{llllllll}0 & 1 & 1 & 0 & 1 & 1\end{array}$ |  |
| 8 | 01000000 |  |
| 9 | 001100000 |  |
| 10 | 0 x 11111111 |  |

Table 2-17. Bandwidth/Gain Mode/Detection Mode Monitor

| Byte Number | Binary Code |  |
| :---: | :---: | :---: |
| 1 | 11001111 | Controller to Receiver |
| 2 | 11101100 |  |
| 3 | 1100011111 | Receiver to Controller |
| 4 | 01000000 |  |

Table 2-18. Address 15 Receiver Parameters

| Tuned Frequency | 12.34567 MHz |
| :--- | :--- |
| BFO Frequency | -3.0 kHz |
| Operating Mode | Local |
| Bandwidth | 3.2 kHz |
| Gain Mode | Fast AGC |
| Detection Mode | AM |
| Signal Strength | Maximum |

Table 2-19. Command Parameters to Address 4 Receiver

| Tuned Frequency | 23.45678 MHz |
| :--- | :--- |
| BFO Frequency | +6.0 kHz |
| Operating Mode | Remote |
| Bandwidth | 50 kHz |
| Gain Mode | Manual |
| Detection Mode | CW |
| RF Gain | Maximum |

Table 2-20. Full Status Command

| Byte Number | Binary Code |  |
| :---: | :---: | :---: |
| 1 | 11000100 |  |
| 2 | $11110 \times x$ |  |
| 3 | $\mathrm{x} \times \mathrm{x} \times \mathrm{x} \times 110$ |  |
| 4 | 00110100 |  |
| 5 | 011010110 | Controller to Receiver |
| 6 | 011111000 | Controller to Receiver |
| 7 | 00001010 |  |
| 8 | 01100000 |  |
| 9 | $0 \times 000000$ |  |

Table 2-21. Command BFO Frequency

| Byte Number | Binary Code |  |
| :---: | :---: | :---: |
| 1 | 11000100 |  |
| 2 | 11111000 |  |
| 3 | x $\mathrm{x} \times \mathrm{x} \times \mathrm{x} 1110$ |  |
| 1 | 11000100 | Controller to Receiver |
| 2 | $\begin{array}{llllllllll}1 & 1 & 1 & 1 & 1 & 1 & 0 & 1\end{array}$ |  |
| 3 | 011000000 |  |

Table 2-22. Tier 2 Access Format

| Byte Number | Binary Code |  |
| :---: | :---: | :---: |
| 1 | 11010100 |  |
| 2 | 11101111 | Controller to Receiver |
| 3 | 11010100 |  |
| 4 | 11100000 | Receiver to Controller |
| 5 | $0110 \times \mathrm{xx}$ |  |

### 2.4.9 REMOTE OPERATION VIA SYNCHRONOUS SERIAL I/O

The Synchronous Serial I/O Option .permits full control of receiver parameters by an external controller. To establish remote operation, the operator must depress the front panel REMOTE keypad.

The Synchronous Serial I/O (SS I/O) allows the following six interface operations:

1. Transfer To Receiver (TTR)
2. Transfer From Receiver (TFR)
3. SIGNAL SEEK: SLEW UP
4. SIGNAL SEEK: SLEW DOWN
5. COUNT PULSES: SLEW UP
6. COUNT PULSES: SLEW DOWN

TFR is the only interface operation that can be performed with the receiver in REMOTE or LOCAL mode. The other interface operations are performed only when the receiver is in REMOTE mode.

The SS I/O has two status outputs. The Receiver Remote Vode (RRM) output is active high whenever the receiver is in REMOTE mode. The SQUELCH OUT output is active high whenever the strength of the received signal is equal to or greater than the operator programmed threshold during a SLEW interface operation.

### 2.4.9.1 Transfer to Receiver (TTR) and Transfer from Receiver (TFR)

Data format and the timing necessary for TTR and TFR operations are shown in Figures 2-6 through 2-8. Note that parity is always odd for the 32 bit message and that the receiver must be in REMOTE mode (RRM active high) for the TTR operation.

### 2.4.9.2 Signal Seek: Slew Up and Signal Seek: Slew Down

The SIGNAL SEEK: SLEW UP or SIGNAL SEEK: SLEW DOWN operations cause the receiver to step up or down in frequency steps equal to the current IF bandwidth, and at a rate of 100 msec . per step. At each step the signal strength is compared to the current threshold. If it is equal to or greater than the threshold the SQUELCH OUT line is made active high. The remote controller then has 2 msec . to lower either the SLEW UP or SLEW DOWN line before the receiver slews to the current frequency plus or minus the IF bandwidth.

Once the receiver tuned frequency reaches 99.99999 MHz or 00.00000 MHz , the operation will stop. There is no "wrap-around" in any of the remote SLEW modes. Figure $2-9$ shows the timing relationships for the SIGNAL SEEK: SLEW UP operation.

### 2.4.9.3 Count Pulses: Slew Up and Count Pulses: Slew Down

The COUNT PULSES: SLEW UP or COUNT PULSES: SLEW DOWN operation causes the receiver's tuned frequency to step up or down in frequency steps equal to the current IF bandwidth at a rate equal to the COUNT PULSES rate. The operation is subject to the limitation that the COUNT PULSES can not change at a rate faster than once every 100 msec . If COUNT PULSES are bursted the receiver cannot change at a rate faster than once every 100 msec .

The state of the SQUELCH OUT line during the COUNT PULSES: SLEW UP or COUNT PULSES: SLEW DOWN operation will be the same as previously described in Paragraph 2.4.9.2, as are the frequency end point limitations. Figure 2-10 shows the timing relationship for the remote COUNT PULSES: SLEW DOWN operation.

EXAMPLE: $23.6581 \mathrm{MHz}, \mathrm{CW}, 3.2 \mathrm{kHz}$ IF BW

| 32 | 31)30\|29 | 28 | 27\|26|25 | 24/23\|22 | 212 | 0 19 18 17 |  | 1514 | 13 | 12 | 11110 | 9 |  | 8 | 6 | 5 | 4 |  | 3 | 1 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | $\begin{aligned} & 100 \\ & \text { IF } \\ & \text { BAND } \end{aligned}$ |  | $\begin{array}{lll} \hline 0 \text { I } & 0 \\ \text { MHZ } \\ \text { TENS } \end{array}$ | O O M Hz UNITS |  | $\begin{aligned} & \hline 01110 \\ & k H z \\ & \text { HUNDREDS } \end{aligned}$ |  | 1 $H 2$ ENS |  |  | 0 Hz NITS |  |  | $\mathrm{O}_{\mathrm{O}}^{\mathrm{Hz}}$ |  |  |  |  | $\begin{array}{ll} 1 & 0 \\ D E T . \end{array}$ <br> MODE |  |  |
| 㝘 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | S |  |  |  |

NOTE I: SHIFT RIGHT FOR BOTH TTR \& TFR

| DETECTION |  |  |  |
| :---: | :--- | :--- | :--- |
| MODE | BITS |  |  |
| CW | 0 | 2 | 1 |
| AM | 0 | 0 | 1 |
| FM | 0 | 1 | 0 |
| USB | 0 | 1 | 1 |
| LSB | 1 | 0 | 0 |
| CW | 1 | 0 | 1 |
| CW | 1 | 1 | 0 |
| CW | 1 | 1 | 1 |


| IF BW | BITS |  |  |
| :--- | :--- | :--- | :--- |
| $(k H z)$ | 31 | 30 | 29 |
| 50 | 0 | 0 | 0 |
| 0.3 | 0 | 0 | 1 |
| 1.0 | 0 | 1 | 0 |
| 2.2 (DF) | 0 | 1 | 1 |
| 3.2 | 1 | 0 | 0 |
| 6.0 | 1 | 0 | 1 |
| 50 | 1 | 1 | 0 |
| 50 | 1 | 1 | 1 |

NOTE 2: PARITY IS ALWAYS ODD FOR THE 32 BIT MESSAGE.

NOTE 3: RECEIVER MUST BE IN REMOTE MODE (RRM ACTIVE HIGH) FOR TTR.

Figure 2-6. DTR and DFR Format


Figure 2-7. TTR Timing


Figure 2-8. TRF Timing


Figure 2-9. SIGNAL SEEK: SLEW UP Timing


Figure 2-10. COUNT PULSES: SLEW DOWN Timing

## SECTION III

## CIRCUIT DESCRIPTION

### 3.1 INTRODUCTION

This section describes the theory of operation of the receiver. A receiver simplified block diagram is provided to show overall functional partitioning of the receiver. Functional block diagrams are provided for each of the receiver's major sections to show functional signal flow through the receiver. The functional descriptions are followed by individual circuit descriptions of each receiver module.

## GENERAL DESCRIPTION

Figure $3-1$ is a simplified block diagram of the receiver. The receive functions have been grouped into the following seven sections:

1. Input RF Switching Section
2. Frequency Extender Section
3. RF/IF Conversion Section
4. IF/Demodulator Section
5. Synthesizer Section
6. Digital Control Section
7. Power Supply Section

A general discussion of each of these sections follows.

### 3.2.1 INPUT RF SWITCHING SECTION

A general discussion of the Input RF Switching Section functions and signal interfaces is provided in the following paragraphs.

### 3.2.1.1 Input RF Switching Functions

The Input RF Switching Section performs the following functions:
a. Signal Routing - HF signals (. 005 to 29.99999 MHz ) signals are routed directly to the Input Conversion Section and VHF signals ( 30 to 100 MHz ) are routed through the Frequency Extender Section to the Input Conversion Section.
b. Band Limiting - Signal output from the Input Switching Section to the Input Conversion Section are bandlimited to 30 MHz maximum.


Figure 3-1. Receiver Overall Block Diagram.

### 3.2.1.2 Input RF Switching Signal Interfaces

The following input/out signals interface with the Input RF Switching Section:
a. RF Input - Rear panel connector FE-A2J1 feeds broadband 0 to 100 MHz signals from an antenna or similar source at a 50 ohm impedance.
b. VHF Out - The VHF output is a wideband signal from 30 to 100 MHz and is sent to the Frequency Extender Section.
c. IF In - The IF input signals is $29.5 \mathrm{MHz}+/-1 \mathrm{MHz}$ signal received from the Frequency Extender Section.
d. RF Out - The RF output is a wideband signal from 0.005 to 30 MHz signal and is sent to the Input Conversion Section.
e. Switch Control - The Switch Control is a single control line from the Digital Control Section and controls the routing of RF signals within the Input Switching Section.

## 3.2 .2

FREQUENCY EXTENDER SECTION
A general description of the Frequency Extender Section functions and signal interfaces is provided in the following paragraphs.
3.2.2.1 Frequency Extender Section Functions

The Frequency Extender Section performs the following functions:
a. Frequency Translation - VHF signals in the range of 30-100 MHz are down converted to 29.5 MHz (2nd IF) by a double conversion process with a 1 st IF center frequency of 159.5 MHz .
b. Bandlimiting - The bandwidth of the 29.5 MHz 2 nd IF output is limited to 1 MHz .
c. Gain Control - Under high RF input signal conditions, the overall gain of the Frequency Extender Section is reduced to prevent overloading or saturation of succeeding receiver stages.

### 3.2.2.2 Input/Output Signal Interfaces

The following input/output signals interface with the Frequency Extender Section:
a. VHF Input - The VHF input is a broadband $30-100 \mathrm{MHz}$ RF signal sent from the Input Switching Section.
b. IF Output - The IF output is a 29.5 MHz IF signal sent to the Input Switching Section.
d. 1 MHz Ref. - The Synthesizer Section sends a 1 MHz square time base signal to the Frequency Extender Section.
e. Tuning Data - Tuning Data is sent from the Digital Control Section and consists of a 7-bit tuning word, 2-bit band select word, RF switch control and an analog tuning voltage.

### 3.2.3 RF/IF CONVERSION SECTION

A general description of the RF/IF Conversion Section functions and signal interfaces is provided in the following paragraphs.

### 3.2.3.1 RF/IF Conversion Section Functions

The RF/IF Conversion Section performs the following functions:
a. Frequency Translation - The incoming $0.005-100 \mathrm{MHz}$ spectrum is converted to 10.7 MHz (2nd IF) by a double conversion process with a 1 st IF center frequency of 42.905 MHz .
b. Bandlimiting - The bandwidth of the 10.7 MHz 2nd IF output is limited to 50 kHz and is characterized by low in-band ripple and group delay.
c. Gain Control - Under high RF input signal conditions, the overall gain of the RF/IF Conversion Section is reduced to prevent overloading or saturation of succeeding receiver stages.

### 3.2.3.2 Input/Output Signal Interfaces

The following input/output signals interface with the RF/IF Conversion Section:
a. RF Input - Rear panel FE-A2J1 feeds broadband $0.005-100 \mathrm{MHz}$ RF signals from an antenna or similar source into the receiver at a 50 ohm impedance.
b. 1st LO - The Synthesizer section sends the 1st LO signal, $42.91-72.90 \mathrm{MHz}$ to operate the 1st mixer.
c. 2nd LO - The Synthesizer Section sends the 2nd LO signal, $32.31000-21.20001 \mathrm{MHz}$, to operate the second mixer.
d. 2nd IF Output - The 10.7 MHz 2nd IF output is provided as an input to the IF/Demodulator Section. This output is 50 ohms at 50 kHz bandwidth and is nominally 15 dB above the RF input level.

### 3.2.4 IF/ DEMODULATOR SECTION

A general discussion of the IF/Demodulator Section functions and signal interfaces is provided in the following paragraphs.

### 3.2.4.1 IF/Demodulator Section Functions

The IF/Demodulator Section performs the following functions:
a. Frequency Translation - The 10.7 MHz 2nd IF is converted to 455 kHz (3rd IF) by a single conversion process.
b. Bandlimiting - The 3rd IF signal is routed through one of five selectable IF bandpass filters. Filter bandwidths are 0.3 kHz , $1.0 \mathrm{kHz}, 3.2 \mathrm{kHz}, 6.0 \mathrm{kHz}, 50 \mathrm{kHz}$ and 2.2 kHz USB/LSB.
c. IF Amplification - A two-stage, high gain, 3rd IF amplifier provides the major portion of overall receiver gain.
d. Gain Control - An AGC detector provides primary gain control to the 3rd amplifier under normal signal conditions, and secondary gain control to the RF/IF Conversion under high input signal conditions.
e. Signal Demodulation - Three signal demodulators provide demodulated AM, FM and CW/SSB audio outputs.

### 3.2.4.2 Input/Output Signal Interfaces

The following input/output signals interface with the IF/Demodulator Section:
a. 2nd IF Input - The RF/IF Conversion Section sends the 10.7 MHz 2nd IF input signal. Signal bandwidth is 100 kHz and input impedance is 50 ohms.
b. 3rd LO - The Synthesizer Section sends the 3rd LO signal, 11.155 MHz , to operate the 3rd Mixer.
c. BFO - The Synthesizer sends the BFO signal, $447.1-463.9 \mathrm{kHz}$, to operate the CW/SSB detector.
d. BW Select - The Digital Control Section sends a 5-bit data word to select each of the five 3rd IF filters.
e. Mode Select - The Digital Control sends a 5-bit data word to select AM, FM or CW/SSB modes.
f. Gain Select - The Digital Control Section sends a 2-bit data word to select SLOW, FST or MAN gain modes. In MAN mode, the Digital Control Section also sends a MAN GAIN analog control voltage to vary the gain of the 3rd IF amplifier.
g. IF Out - A high level, 3rd IF signal is provided as a rear panel receiver output at J12. This output is 50 ohms, bandwidth limited by the 3 rd IF filter, and is nominally 67 dB above the 2nd IF input signal.
h. Line Audio Out - A demodulated AM, FM or CW/SSB audio signal is provided as a rear panel receiver output at $\mathrm{J} 15 / 16$. This output is 26 Vac into 600 ohms ( +30 dBm ).
i. RF Gain Control - This de voltage is supplied to the RF/IF Conversion Section. This level is nominally 0 Vde under normal signal conditions, increasing to -4 Vde under maximum; signal conditions.
j. Status - Two de outputs are send to the Digital Control Section and represent the relative signal strength and line audio output level.
k. Combined Audio - This low level audio is sent to the Digital Control for distribution to the front panel headphone amplifier.

### 3.2.5 SYNTHESIZER SECTION

A general discussion of the Synthesizer Section functions and signal interfaces is provided in the following paragraphs.
3.2.5.1 Synthesizer Section Functions

The Synthesizer Section performs the following functions:
a. LO Signal Generation - The Synthesizer Section translates digital tuning data from the Digital Control Section into the 1st, 2nd, 3rd and BFO signals required for operation of the mixers in the RF/IF Conversion and IF/Demodulator Sections.
b. External Reference Locking - Internal phase locked loops the accuracy of the four LO signals to an external frequency reference source for high tuning accuracy.

### 3.2.5.2 Input/Output Signal Interfaces

The following input/output signals interface with the Synthesizer Section:
a. $\quad 1 \mathrm{MHz}$ REF IN - Rear panel Jll provides the input for a high stability 1 MHz reference signal. Signal must be square wave and TTL-compatible.
b. Tuning Data - BCD encoded data words are sent from the Digital Control Section to program the output frequencies of the 1 st , 2 nd , 3 rd and BFO synthesizers.
c. 1st LO - The 1st LO output is provided as an input to the RF/IF Conversion Section. Frequency range is $42.91-72.90 \mathrm{MHz}$ and level is +20 dBm nominal into 50 ohms.
d. 2nd LO - The 2nd LO output is provided as an input to the RF/IF Conversion Section. Frequency range is $32.21000-$ 32.20001 MHz and level is 0 dBm nominal into 50 ohms.
e. 3rd LO - The 3rd LO output is provided as an input to the IF/Demodulator Section. Frequency is fixed as 11.155 MHz and level is -6 dBm nominal into 50 ohms.
f. BFO - The BFO output signal is provided as an input to the IF/Demodulator Section. Frequency range is $447.1-463.9 \mathrm{kHz}$ and level is 40 mV rms (high impedance).

### 3.2.6

digital Control section
A General Discussion of the Digital Control Section functions and signal interfaces is provided in the following paragraphs.

### 3.2.6.1 Digital Control Section Functions

The Digital Control Section performs the following functions:
a. Receiver Control - The Digital Control Section generates the digital control words necessary to operate the RF/IF Conversion, IF/Demodulator, and Synthesizer Sections.
b. Front Panel Interface - Operator selected parameter inputs are interfaced from the front panel to the digital circuitry to generate receiver digital control words. Receiver status is also input and displayed on the front panel displays and indicators for monitoring purposes.
c. Remote Controller Interface - External controller commands are interfaced to the digital circuitry to generate receiver digital control words.

### 3.2.6.2 Input/Output Signal Interfaces

The following input/output signals interface with the Digital Control
Section:
a. Front Panel Control/Display Data - Front panel bandwidth, mode, gain and frequency data is recei ved from the front panel. Also, receiver tuned frequency data and signal strength/line audio status data is sent to the front panel for display.
b. Tuning Data - BCD encoded data words are sent from the Digital Control Section to program the output irequencies of the 1st, 2nd, 3rd and BFO synthesizers.
c. BW Select - A 5-bit BW select data word is sent to the IF/Demodulator Section to select each of the five 3rd IF filters.
d. Mode Select - A 5-bit mode select data word is sent to the IF/Demodulator Section to select AM, FM or CW/SSB modes.
e. Gain Select - A 2-bit mode select data word is sent to the IF/Demodulator Section select SLOW, FST or MAN gain modes. In MAN mode, a MAN GAIN analog control voltage is sent to the IF/Demodulator Section to vary the gain of the 3rd IF amplifier.
f. RF Gain Control - This de voltage is supplied to the RF/IF Conversion Section. This level is nominally 0 Vde under normal signal conditions, increasing to -4 Vdc under maximum; signal conditions.
g. Status - Two de outputs are received from the IF/Demodulator Section and represent the relative signal strength and line audio output level.
h. Combined Audio - This low level audio is received from the IF/Demodulator Section for distribution to the front panel headphone amplifier.

### 3.2.7 POWER SUPPLY SECTION

The Power Supply Section received 115 or 230 Vac input from the AC line and converts it to de levels required by the receiver circuits. There are two main groups of regulator assemblies: three are mounted on the main chassis, three are mounted on the Synthesizer Motherboard, A5.

Main Chassis Regulator Outputs:

U1: +15 Vdc
U2: -15 Vde
U3: $\quad+5 \mathrm{Vdc}$

Main Chassis Motherboard Outputs:

U1: +5 Vdc
U2: $\quad+5 \mathrm{Vde}$
U3: $\quad+12 \mathrm{Vdc}$

## 3.3. <br> FUNCTIONAL THEORY OF OPERATION

### 3.3.1 INPUT RF SWITCHING SECTION

Figure $3-2$ is a block diagram of the Input RF Switching Section. As shown in Figure 3-2, it consists of two major assemblies: Input Switch FE-A2, and RF Filter, A2.

### 3.3.1.1 Input Switch FE-A2 (794276)

Input RF signals from $0-100 \mathrm{MHz}$ enter the switch via J 1 . When the Switch Control line from Digital Control is low (receiver tuning from 0 to 29.9999 MHz ), the signals pass through FE-A2 to J 2 ; from J 2 to J 4 ; through FE-A2 to J 5 ; from J5 to RF Filter, A2. When the Switch control line from Digital Control is high (receiver tuning from 30 to 99.99999 MHz ), the signals pass through FE-A2 to J3; from J3 to A1A1 of the Input Converter/2nd LO, FE-A1A1.

### 3.3.1.2 RF Filter (A2) (791616)

The RF Filter (A2) is a 15 -pole low pass filter with a 50 ohm characteristic impedance and a 3 dB nominal loss. RF input signals from the Input RF Switching Section are band-limited to 5 kHz to 30 MHz by the RF Filter and are applied to the Input Converter (A3).

Serial Numbers 1 Thru 20


Serial Numbers 21 Thru 38
Figure 3-2. Input RF Switching Section Block Diagram

### 3.3.2 FREQUENCY EXTENDER (FE-A1) (794278)

Figure $3-3$ is a block diagram of the Frequency Extender, FE-A1. As shown in Figure 3-3, it consists of two major assemblies: VHF Preselector/lst LO, FE-A1A1; Input Converter/2nd LO, FE-A1A2.


Figure 3-3. Frequency Extender Section Block Diagram

### 3.3.2.1 VHF Preselector/1st LO (FE-A1A1) (794315)

VHF signals from the Input RF Switching Section drives the input to the Preselector. The Preselector is a narrow band tunable filter. Tuning is organized into two bands, $30-54$ and $54-100 \mathrm{MHz}$ by the Band Switch lines from Digital Control. The Tuning Voltage from Digital Control forces the Preselector to track the receiver tuned frequency. Preselector output drives the 1 st Converter input in FE-A1A2.

The 1 MHz Reference and the Tuning Data word drive the Synthesizer input. The band switch signals and tuning voltage generated in the Synthesizer force the VCO to oscillate from 190 to 260 MHz in two tuning bands. The VCO output is fed back to the Synthesizer to achieve a "lock" condition in the Synthesizer loop. The VCO output (1st LO) drives the 1st Converter input in FE-A1A2.

### 3.3.2.2 Input Converter/2nd LO (FE-A1A2) (794316)

VHF signals ( $30-100 \mathrm{MHz}$ ) from FE-A1A1 drive the 1 st Converter Input. These signals are mixed with the 1 st $L O(190-260 \mathrm{MHz})$ from FE-A1A1 to produce a $159.5 \mathrm{MHz}+/-0.5 \mathrm{MHz}$ 1st IF output. The 1 st IF output drives the 2 nd converter.

The 1 MHz Reference signal from FE-A1A1 drives the 2nd LO. The 2nd LO is a fixed synthesizer producing a 2 nd LO output of 189 MHz .

The 2nd converter mixes the 1st IF of 159.5 MHz and the 2 nd of 189 MHz to produce the 2 nd IF of $29.5 \mathrm{MHz}+/-0.5 \mathrm{MHz}$. The 2 nd IF output is sent to the Input RF Switching Section where it is routed to the RF/IF Conversion Section.

### 3.3.3 RF/IF CONVERSION SECTION

Figure $3-4$ is a block diagram of the RF/IF Conversion Section. As shown in Figure 3-4, it consists of one major module: Input Converter, A3.


Figure 3-4. RF/IF Conversion Section Block Diagram

### 3.3.3.2 Input Converter (A3) (791592)

As shown in Figure 3-4, the Input Converter consists of two major subassemblies: 1st Mixer A3A1 and 2nd Mixer A3A2.

### 3.3.3.2.1 1st Mixer (A3A1) (370611-6)

The 1st Mixer receives RF Input signals ( $0.005-30 \mathrm{MHz}$ ) from the RF Filter (A1) and the LO Signal ( $42.91-72.90 \mathrm{MHz}$ ) from the 1 st LO Synthesizer (A5A1). The 1st LO and RF Input signals are mixed by the 1st mixer to produce a first IF in the range of 42.90001 to 42.910 MHz . The 1st IF signal is amplified and filtered by a 150 kHz bandwidth band-pass filter with a center frequency of 42.905 MHz .

### 3.3.3.2.2 2nd Mixer (A3A2) (370646-6)

The 2nd Mixer receives the 1st IF signal ( 42.905 MHz ) from the 1st Mixer and the 2nd LO signal ( $32.21000-32.20001 \mathrm{MHz}$ ) from the 2nd LO Synthesizer (A5A2). The 2nd LO and 1st IF are mixed by the 2 nd Mixer to produce a 2 nd IF of 10.70 MHz The 2nd IF signal is amplified and filtered by a 50 kHz bandwidth band-pass filter with a 10.7 MHz center frequency and drives the 50 ohm input of the 10.7 MHz Filter Switch, A4A1.

### 3.3.4 IF/DEMODULATOR SECTION

Figure 3-5 is a block diagram of the IF/Demodulator Section. The IF/Demodulator Section is mounted on the IF Motherboard P.W. Assembly A4. As shown in Figure 3-5, the IF/Demodulator Section consists of the following major modules: 10.7 MHz Filter Switch, A4A1; $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter, A4A2; 455 kHz Filter Switch, A4A3; AGC, A4A6; 455 kHz Amplifier/A.V1 Detector, A4A7; FM/CW/SSB Detector, A4A9; Audio Amplifier, A4A10.

### 3.3.4.1 $\quad 10.7 \mathrm{MHz}$ Filter Switch (A4A1) (791594)

The 2nd IF output from A3 drives the 50 ohm input of the 10.7 MHz Filter Switch, A4A1-13. The signal is routed through one of three voltage-selectable circuit paths within A4A1. The wideband path, selected by +5 Vdc at pin 15 , passes the full 50 kHz bandwidth from A3 through A4A1. The other two circuit paths, selected by +5 Vdc at pin 17 or 19, restricts the bandpass to 6.0 or 3.2 kHz respectively (see Table 3-1 for summary of 2 nd and 3 rd IF bandwidth selection). The amplified, band-limited output at A4A1-57 drives the 50 ohm input of the 3 rd Mixer, A4A2-57.


Figure 3-5. IF/Demodulator Section Block Diagram

Table 3-1. 2nd and 3rd IF Bandwidth Selection

| BW Filter |  | BW Switch Selection (AM, FN, CW Mode) |  |  | SSB Modes |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Select Pin |  |  |  |  |  |  |

Table 3-2. Detection Mode Selection.

| Node <br> Select Pin | Detection Mode Switch Selection |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A4A10-47 | (AM SEL) | +5 | 0 | 0 | 0 | 0 |
| A4A9-41 | (FM) | 0 | +5 | 0 | 0 | 0 |
| A4 A9-43 | (CW/SSB) | 0 | 0 | +5 | +5+ | 5 |
| A5 A3-43 | ( OFFSETEN | 0 | 0 | +5 | 0 | 0 |
| A5 A3-57 | (BFO INH) | +5 | +5 | 0 | 0 | 0 |

### 3.3.4.2 $\quad 10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter (A4A2) (794254)

The amplified 2nd IF output from A4A1-57 drives the 50 ohm input of the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter, or the 3 rd Mixer A4A2-57. The 3 rd Mixer also receives the LO signal from the 3rd LO Synthesizer, A5A1, which is fixed at a frequency of 11.155 MHz . In DF mode, the internal bandwidth of A 4 A 2 is set at 2.2 kHz by a bandpass filter. The 3 rd LO and 2nd IF are mixed by the 3 rd Mixer to produce a 3 rd IF of 455 kHz . The 3 rd IF output, A4A2-19, of the 3 rd Mixer is stepped up to an impedance of 1000 ohms and drives the input of the 455 kHz Filter Switch, A4A3.

455 kHz Filter Switch (A4A3) (791595)
The 3rd IF output from A4A2-19 drives the high-impedance input of the 455 kHz Filter Switch, A4A3-13. When AM, FM or CW Mode is selected, the signal is routed through one of three voltage-selectable circuit paths within A4A3. The wideband path, selected by +5 Vdc of pin 15 , passes the full bandwidth, determined by A3 and A4A1, through A4A3. The other two circuit paths, selected by +5 Vdc at pin 17 or 19, narrow the bandpass from that determined by A3 and A4A1 down to 1.0 kHz or 0.3 kHz respectively (see Table $3-1$ for summary of 2nd and 3 rd IF bandwidth selection). The amplified, band-limited output from A4A3-57 drives the high-impedance input of the 455 kHz IF Amplifier/Demodulator, A4A7-57.

### 3.3.4.4 AGC (A4A6) (796175)

The AM Audio output from A4A7-51 drives the input of the AGC, A4A6-51. In AGC mode, selected by 0 Vdc at pin 13, the detected DC level from A4A7-51 is amplified to become the IF GC Voltage at A4A6-47. This voltage adjusts the gain of the IF Amplifier, A4A7. Under strong input signal conditions, a gate circuit transfers the IF GC voltage to pin 19, RF GC, reducing Input Converter gain. A4A6-41, AGC Signal Strength, is a DC sample of the IF GC voltage that drives the front panel meter in Signal Strength Mode. In MAN mode, selected by +5 Vdc at pin 13, the IF and RF GC outputs respond to the MAN GAIN, A4A6-17, signal from the front panel RF GAIN control. A4A6-12, MAN Signal Strength, is a DC sample of the IF GC voltage that drives the front panel meter in the Signal Strength Mode.

### 3.3.4.5 $\quad 455 \mathrm{kHz}$ Amplifier/AM Detector (A4A7) (726002-2)

The amplified 3rd IF output from A4A3-57, A4A4-57 or A4A5-57 drives the high impedance input of the 455 kHz IF Ampl/Detector, A4A7-57. The signal is amplified by a two-stage gain-controlled (for AGC purposes) amplifier. The amplifier is untuned to give the required 50 kHz bandpass characteristic. Following this, the IF signal is split to provide three outputs: the input to the AM Detector, the third IF output at A4A7-13 which drives the input to the $\mathrm{FM} / \mathrm{CW} / \mathrm{SSB}$ Detector and the 3rd IF output at A4A7-17 which drives the rear panel IF Output jack J2. The AM Audio output from the AM Detector at A4A7-51 contains a DC level proportional to RF Input signal strength and audio resulting from modulation detection by the AM Detector. This AM Audio output drives the parallel-connected inputs of the AGC, A4A6-51, and the Audio Amplifier, A4A10-51.

### 3.3.4.6 FM/CW/SSB Detector (A4A9) (791599-4)

The amplified 3rd IF output from A4A7-13 drives the high-impedance input of the FM/CW/SSB Detector, A4A9-13. In the FM Mode, selected by +5 Vdc at pin 41 (see Table $3-2$ for a summary of detection mode selection), the signal is amplified, limited and drives an FM discriminator. The audio from the discriminator as FM Audio at A4A9-57. In the CW or any of the sideband modes, selected by +5 Vdc at pin 43 (see Table 3-2), the signal is applied to a product detector. The BFO Synthesizer is also enabled and supplies, a fixed (SSB mode) or variable (CW mode) $j 5 \mathrm{kHz}$ BFO signal to A4A9-17. This BFO signal mixes with the 3rd IF signal in the product detector. The audio from the product detector appears as CW/SSB Audio at A4A9-57. Audio from A4A9-57 drives the input of the Audio Amplifier, A4A10-57.

### 3.3.4.7 Audio Amplifier (A4A10) (7459)

The AM Audio output from A4A7-51 drives the input to the Audio Amplifier, A4A10-51, and the FM/CW/SSB Audio output from A4A9-57 drives the input to the Audio Amplifier, A4A10-57. In AM mode, selected by +5 Vdc at pin 47 (see Table 3-2 for a summary of detection mode selection), the AM Audio at pin 51 is gated through a summing amplifier at unity gain and appears at pin 55. In FM, CW or SSB Modes, pin 47 is 0 Vdc , and the FM/CW/SSB Audio at pin 57 is gated through the summing amplifier and appears at pin 55. Combined Audio at pin 55 is routed through the front panel Audio Level control to the high level Line Audio Amplifier via pin 17. The Line Audio amplifier amplifies the signal and outputs it through A4A10-13 to rear panel J16. A rectifier samples the output of the Line Audio amplifier and supplies the front panel meter in the LINE AUDIO setting. A low level audio signal from the from the front panel headphone amplifier drives the Auxiliary Phone amplifier. The Auxiliary Phone out signal at A4A10-19 appears at the rear panel J16.

## 3.3 .5 <br> SYNTHESIZER SECTION

Figure 3-6 is a block diagram of the Synthesizer Section. The Synthesizer Section is mounted on the Synthesizer Motherboard P. W. Assembly A4. As shown in Figure 3-6, the Synthesizer Section consists of three major modules: 1st and 3rd LO/Time Base, A5A1; 2nd LO Synthesizer, A5A2; BFO Synthesizer, A5A3.


Figure 3-6. Synthesizer Section Block Diagram

### 3.3.5.1 1st L.O. Synthesizer (A5A1) (791630)

The 1st LO receives $B C D$ tuned frequency command data from the four MSDs of the receiver tuned frequency readout. The $B C D$ numbers range in value of 0000 to 2999 corresponding to receiver tuned frequencies of 00.00 XXX MHz to 29.99 XXX MHz . The output of the 1 st LO tunes from 42.91 MHz to 72.90 MHz in 10 kHz steps in accordance with the BCD tuned frequency data. A stable 40 kHz time base signal provides a precise reference for the 1st LO phase lock loop control circuits.

### 3.3.5.2 2nd L.O. Synthesizer (A5A2) (791601)

The 2nd LO receives $B C D$ tuned frequency command data from the three LSD's of the receiver tuned frequency readout. The BCD numbers range in value from 000 to 999 corresponding to receiver tuned frequencies of $\mathrm{XX} . \mathrm{XX} 000 \mathrm{MHz}$ to XX. XX999 MHz . The output of the 2 nd LO tunes down from 32.21000 MHz to 32.20001 MHz as the $B C D$ data increments from 000 to 999 . Stable 10 kHz and 1 MHz time base signals provide precise references for the 2nd LO phase lock loop control circuits.

### 3.3.5.3 3rd L.O. Synthesizer (P/O A5A1) (791629)

The 3rd LO Synthesizer produces a fixed frequency output of 11.155 MHz . Basic frequency control is obtained by an 11.155 MHz crystal oscillator. The exact frequency of oscillation is precisely locked to 10 kHz and 50 kHz time base reference signals by a phase locked loop.

### 3.3.5.5 BFO Synthesizer (A5A3) (791576)

The BFO Synthesizer receives BCD offset frequency command data from the MSD and LSD of the BFO offset switch, A9. The BCD numbers range in value from 00 to 89 corresponding to offset frequencies of 0.0 kHz to 8.9 kHz . Offset control data from the " $+, 0,-"$ switch section of A9 programs the direction of BFO offset. The output of the BFO tunes from $446.1 \mathrm{kHz}(455 \mathrm{kHz}-8.9 \mathrm{kHz})$ to 463.9 kHz $(455 \mathrm{kHz}+8.9 \mathrm{kHz})$. In the AM and FM modes, BFO INH, A4A8-57, is high, shutting off the BFO output at A5-P15, even though the BFO itself is oscillating. In SSB modes, OFFSET ENABLE, A4A8-43 is low, fixing the BFO output at 455.000 kHz . A stable 1 kHz time base signal provides a precise reference for the BFO phase lock loop control circuits.

### 3.3.5.6 Time Base (P/O A5A1) (791600)

All four synthesizer circuits are synchronized by a common Time Base. Reference frequencies of $1 \mathrm{MHz}, 50 \mathrm{kHz}, 40 \mathrm{kHz}, 10 \mathrm{kHz}$, and 1 kHz are supplied from a 2 MHz temperature compensated crystal oscillator or from a 1 MHz external source input at rear panel jack J11. The rear panel INT/EXT clock switch S2 allows selection at the internal and external reference. When in the internal mode, the 1 MHz internal -eference is output from rear panel jack J11.

### 3.3.6 DIGITAL CONTROL SECTION

Figure 3-7 is a block diagram of the Digital Control Section. The Digital Control Section is mounted on the I/O Motherboard P.W. Assembly A6. As shown in Figure 3-7, the Digital Control Section consists of six major modules: Synthesizer Interface/Memory, A6A1; IF Interface, A6A2; Asynchronous I/O, A6A3; Serial I/O Buffer, A6A4; Sync Serial Input/Output, A6A5; Front Panel Switch/Encoder, MFP-A1.

### 3.3.6.1 Synthesizer Interface/Memory (A6A1) (794275)

The Synthesizer Interface contains a microprocessor and memory which serves as the control element for the Digital Control Section. The microprocessor is interfaced to A6A2 and A6A3 via an address/data bus. Front panel commands are processed by the microprocessor via the address/data bus and receiver control commands are sent back out over the bus. Tuned frequency and BFO frequency latehes transfer tuning data from the microprocessor to the Synthesizer Section.

### 3.3.6.2 IF Interface (A6A2) (796032)

The IF Interface connects to the Digital Control Section microprocessor on A6A1 via the address/data bus. The IF Interface receives control commands from the Front Panel components and sends them to the microprocessor on A6A1. Receiver control commands to select gain mode, bandwidth, detection mode and RF gain control are passed from the microprocessor to the IF/Demodulator Section via latches on the IF Interface.

### 3.3.6.3 Asynchronous I/O (A6A3) (796037)

The Asynchronous I/O interfaces the microprocessor on A6A1 with remote control equipment. The I/O connects to the Digital Control address/data bus and communicates with remote equipment via RS422 serial format. The Asynchronous I/O will accept commands from the remote equipment and will transfer receiver parameters to the remote equipment. Two external ports are provided. One connects to the external controller. The other connects to a second receiver. A maximum of 15 receivers can be connected in this "serial" fashion to be controlled by the remote equipment.

### 3.3.6.4 Serial I/O Buffer, (A6A4) (794300)

The Serial I/O Buffer performs two functions. First it interfaces the microprocessor on A6A1 with the Frequency Extender. Data lines from the address/data bus pass directly to the Frequency Extender to transfer frequency tuning data words. An analog digital converter develops the analog tuning voltage to tune the Preselector in the Frequency Extender. Second, the Serial I/O buffer functions as a buffer/interface between the Sync Serial I/O and external remote control equipment.


Figure 3-7. Digital Control Section Block Diagram

### 3.3.6.5 <br> Sync Serial Input/Output, A6A5 (794255)

The Sync Serial I/O interfaces the microprocessor on A6A1 with external remote control equipment via A6A4. This permits the remote equipment to direct the receiver to perform frequency scans and stop when a signal exceeds threshold. Scan signals (Slew/Seek) from the remote equipment is interfaced to the address/data bus and then to the microprocessor.

### 3.3.6.6 Front Panel Switch/Encoder, MFP-A1 (796013-5)

The Front Panel Switch/Encoder interfaces all front panel functions with the Microprocessor on A6A1 via the address/data bus. Two major subassemblies are mounted on the Front Panel Switch/Encoder: The Front Panel Switchboard, MFPA1A1 and the Front Panel Encoder, MFPA1A2.

### 3.3.6.6.1 Front Panel Switchboard (MFPA1A1A2) (796057-5)

The Front Panel Switchboard contains switch matrices and all front panel LED displays and indicators. A programmable interface transfers switch matrix information to the Front Panel Encoder and decodes display information sent from the Front Panel Encoder for display purposes.

### 3.3.6.6.2 Front Panel Encoder (MFPA1A1) (796056)

The Front Panel Encoder receives switch matrix information from the Front Panel Switchboard, encodes it and transfers it to the microprocessor on A6A1 via the address/data bus. Also, the Encoder receives display data from A6A1 via the address/data bus, decodes to a format suitable for display and transfers it to the Front Panel Switchboard for display.

### 3.3.7 POWER SUPPLY SECTION

See Figure 3-8 for the power supply block diagram. The receiver may be operated from either $110 \mathrm{Vac}, 120 \mathrm{Vac}, 220 \mathrm{Vac}$ or 240 Vac . This voltage feeds Filter Assembly FL1 which contains the input voltage selector. It then passes through fuses F1 and F2 and through the main power switch, S1. From the switch, current is routed through the Voltage Selector and into Transformer T1. The Transformer has a dual primary and center-tapped secondaries and produces outputs of 34 and 16 Vac . The 34 Vac is rectified and filtered and sent to Main Chassis regulators U1 and U2 and to U3 on Motherboard A5. U1 and U2 on the back of the chassis provide regulated +15 Vdc and -15 Vdc , respectively. These two voltages are supplied to most
of the circuits in the receiver. The 16 Vac is rectified by two diodes located on the rear panel and filtered to become the +10 V unregulated supply. The unregulated 10 Vdc , with its unregulated ground, connects to U3, a +5 Vde regulator. U3 supplies +5 Vde to the Synthesizer and Digital Control Sections. The unregulated 10 Vde also connects through two +5 Vdc regulators on $A 5$ and provide two separate +5 Vde voltages to the 1 st and 3rd LO Synthesizers.


Figure 3-8. Power Supply Section Functional Block Diagram.

## 3.4

## CIRCUIT DESCRIPTIONS

This paragraph provides detailed circuit descriptions of the subassemblies and modules contained in the WJ-8718-19-FE HF Receiver. All significant components are identified and supplementary block diagrams are employed to aid in understanding circuit operation.

### 3.4.1 RF FILTER (A2) (791616)

The RF Filter is a modular assembly which mounts one subassembly, Input
Filter A2A1.

### 3.4.1.1 <br> Input Filter (A2A1) (280093)

Refer to Figure 6-1, Input Filter Schematic Diagram, as an aid in understanding the following description. The Input Filter is a 15 -pole, elliptic function low-pass RF filter, with an insertion loss of less than 3.5 dB over normal input range of 5 kHz to 30 MHz . Above 30 MHz , the attenuation increases rapidly. This attenuation improves the image rejection and reduces the conducted LO leakage of the receiver. Over the range of $L O$ and image frequencies, the attenuation of the input filter exceeds 80 dB . Resistor R1 provides a dc path to ground to bleed off any accumulated static charge at the RF input. Diodes CR1 through CR4 use the Zener breakdown potential to protect the rest of the receiver from input signals in excess of +15 dBm . C12 and L1 provide a high frequency trap to prevent radiation of harmonies of the 1st LO. The nominal input impedance of the filter is 50 ohms.

### 3.4.2

1ST LO SYNTHESIZER (FE-A1A1A1) (370689)

The 1st LO Synthesizer mounts on the Frequency Extender, FE-A1, Assembly (see paragraph 3.3.2). Figure 3-9 is a detailed block diagram of the 1 st LO Synthesizer which should be referred to in the following circuit description. Figure 64, 1st LO Synthesizer Schematic Diagram, may be referred to for greater component level detail, if desired.

Tuning data (D0-D6) from the Digital Control and the 1 MHz reference signal drive the input to synthesizer chip Ul. The VCO sample (1st LO signal) from FE-A1A1A2 is divided by $40 / 44$ (dual modulus divider) and drives the Fin terminal of U1. U1 further divides the VCO signal (actual divide ratio determined by DO-D6) and compares it with the 1 MHz reference. The OR and OV outputs from Ul are typically short spikes ( +5 V peak) when the error between VCO frequency and 1 MHz reference is small (synthesizer loop locked).

The short spike outputs from U1 are integrated by U2 to give an average de level. The U2 output varies from +1 to +4 Vde depending where in the tuning range of 190 to 260 MHz the VCO is operating. U2 output goes through a sharp notch filter to the tuning voltage input of the VCO, FE-A1A1A2.

Four bits of data (D0-D3) are latched through U7, then through US and U6 to give three bits of bandswitch tuning data for the VCO. This organizes the VCO tuning into 7 separate bands, each 10 MHz wide, as follows:


Figure 3-9. 1st LO Synthesizer, FE-A1A1A1, Block Diagram

| VCO FREQUENCY (MHZ) | E2 | E3 | E4 |
| :---: | :--- | :--- | :--- |
| 190 to 200 | 0 | 0 | 0 |
| 200 to 210 | 1 | 0 | 0 |
| 210 to 220 | 0 | 1 | 0 |
| 220 to 230 | 1 | 1 | 0 |
| 230 to 240 | 0 | 0 | 1 |
| 240 to 250 | 1 | 0 | 1 |
| 250 to 260 | 0 | 1 | 1 |

$$
\text { NOTE: } 0=0 \mathrm{Vdc} ; 1=+5 \mathrm{Vdc}
$$

### 3.4.3 $\quad V C O$ (FE-A1A1A2) (370960)

The VCO mounts on the Frequency Extender, FE-A1, Assembly (see paragraph 3.3.2). Figure $3-10$ is a detailed block diagram of the VCO which should be referred to in the following circuit description. Figure 6-5, VCO Schematic Diagram, may be referred to for greater component level detail, if desired.

The VCO consists of oscillator transistor Q1. The oscillation frequency of Q1 is controlled by C6/C7/CR4, T3 and L2/CR1, L3/CR2, L4/CR3. Inductors L2, 13, 14 are tapped across $T 3$ and are controlled by bandswitch data from the 1st LO through CR1-CR3. By switching CR1-CR3 high or low, L2-L4 may be switch in or out of the tuning circuit allowing the tuning range of Q1 to increment in 10 MHz steps between 190 and 260 MHz .

Diode CR4 is a varactor that swings the frequency of Q1 over a 10 sweep as the tuning voltage goes from +1 to +4 Vdc . The tuning data going into the lst LO Synthesizer sets the tuning voltage at the correct level to lock the Q1 oscillation frequency at the desired frequency.

Q1 output is amplified by buffers Q2 and Q3. Each buffer has broad band tapped down transformers in the collectors for stability and impedance matching. The output from Q2 is the VCO sample sent back to the 1st LO. The output from Q3 is the 1st output which is sent to Input Converter/2nd LO, FE-A2.


Figure 3-10. VCO, FE-A1A1A2, Block Diagram

### 3.4.4

PRESELECTOR (FE-A1A1A3) (794274)
The Preselector mounts on the Frequency Extender, FE-A1, Assembly (see paragraph 3.3.2). Figure 3-11 is a detailed block diagram of the Preselector which should be referred to in the following circuit description. Figure 6-6, Preselector Schematic Diagram, may be referred to for greater component level detail, if desired.

The preselector consists of two narrow band voltage-tuneable bandpass filters, the first tuning from $30-54 \mathrm{MHz}$, the second tuning from $54-100 \mathrm{MHz}$. Filter 1 $(30-54 \mathrm{MHz})$ consists of varactor diodes CR3-CR9, and inductorsT1, T2, L4, L8. Filter $2(54-100 \mathrm{MHz})$ consists of varactor diodes CR10-CR16, and inductors T3, T4, L5, L9. The tuning voltage from the Digital Control is impressed on the varactor diodes and tunes each filter from its low end (tuning voltage low) to its high end (tuning voltage high).

Switching between the filters is accomplished by PIN diodes CR1, CR2, CR17 and CR18. The diodes are controlled by the band switch data through U3. When band $1(30-54 \mathrm{MHz})$ is selected, E5 is high, U3-3 is 0 Vdc and U3-5 is +15 Vde . This forward biases CR1 and CR17 and reverse biases CR2 and CR18. A low loss path is created through filter 1, while filter 2 is cutoff. When band $2(54-100 \mathrm{MHz}$ is selected, E6 is high, U3-3 is +15 Vdc and U3-5 is 0 Vdc . This forward biases CR2 and CR18 and reverse biases CR1 and CR17. A low loss path is created through filter 2 while filter 1 is cutoff.


Figure 3-11. Preselector, FE-A1A1A3, Block Diagram

The Preselector mounts on the Frequency Extender, FE-A1, Assembly (see paragraph 3.3.2). Figure $3-12$ is a detailed block diagram of the 2nd LO Synthesizer which should be referred to in the following circuit description. Figure 6-8, 2nd LO Synthesizer Schematic Diagram, may be referred to for greater component level detail, if desired.

The 2nd LO consists of a VCO and a Synthesizer. Q1 is the VCO oscillator. Frequency of oscillation is controlled by CR1, C15, C19 and L2. Actual oscillating frequency is set by the tuning voltage from the Synthesizer portion which drives varactor CR1. Q1 output is amplified by buffer Q2. The drain output is the 2nd LO output which drives the 2nd converters. The source output is the VCO sample which drives the Synthesizer portion.

The Synthesizer portion consists of synthesizer chip Ul which is hard wired for a fixed internal divide ratio. The VCO sample from Q2 is divided by dualmodulus divider $U 2$ and drives the U1-Fin input. U1 compares the Fin input with the 1 MHz reference input. The U1 OR and OV outputs consists short spikes ( +5 Vde peak) when the synthesizer is locked. The U1 output is integrated by U3 to an average de level (typically +3 Vde when locked) and then sends it to CR1 as tuning voltage.

Q1 typically oscillates at approximately 189 MHz . The tuning voltage from U3 adjusts the frequency Q 1 until it oscillates at exactly 189 MHz .


Figure 3-12. 2nd LO Synthesizer, FE-A1A2A1, Block Diagram

## 3.4 .6

2ND CONVERTER (FE-A1A2A2) (270907)
The 2nd Converter mounts on the Frequency Extender, FE-A1, Assembly (see paragraph 3.3.2). Figure 3-13 is a detailed block diagram of the 2nd Converter which should be referred to in the following circuit description. Figure 6-9, 2nd Converter Schematic Diagram, may be referred to for greater component level detail, if desired.

The 159.5 MHz 1st IF signal from the 1 st Converter is applied through an impedance matching network to the input of mixer U3. The 189 MHz LO signal from the 2nd LO Synthesizer is amplified to a level of +15 dBm by buffer U2 and applied to mixer U3. U3 mixes these two signals to give a 2 nd IF output of 29.5 MHz . U2 output is amplified by 15 dB by buffer U1 and is sent as the FE IF output to RF switch FE-A2.


Figure 3-13. 2nd Converter, FE-A1A2A2, Block Diagram

### 3.4.7

1ST CONVERTER (FE-A1A2A3) (270901)
The 1st Converter mounts on the Frequency Extender, FE-A1, Assembly (see paragraph 3.3.2). Figure $3-14$ is a detailed block diagram of the 1 st Converter which should be referred to in the following circuit description. Figure 6-10, 1st Converter Schematic Diagram, may be referred to for greater component level detail, if desired.

VHF signals ( $30-100 \mathrm{MHz}$ ) from the Preselector, FE-A1A1A3, are routed through bandpass filter FL1 to the input of U1. FL1 has a 50 ohm characteristics and filters output signals above 100 MHz and below 30 MHz with an overall loss of -2 dB . U1 amplifies the signals by +15 dB and sends the signals to voltage controlled attenuator U2. U2 has a nominal loss of -2 dB when the de voltage at its control input is $>+7 \mathrm{Vdc}$ and a loss of $>-40 \mathrm{~dB}$ when the control input voltage is 0 Vdc . U2 output drives the input to mixer U5.

The 1st LO signal, $190-260 \mathrm{MHz}$, from the VCO, FE-A1A1A2, is amplified by +15 dB by buffer U3 and drives mixer U5. U5 mixes the 1st LO with the VHF RF signals and produces the 29.5 MHz 2 nd IF output. The 2 nd IF output is routed to RF Switch, FE-A2.

AGC control voltage from the IF/Demodulator Section is applied to level changer U6. Under no signal input conditions, the AGC voltage is 0 Vdc , and the U6 output which drives the control input of U 2 is +7.5 Vdc . This gives an overall loss in U2 of -2 dB . Under maximum signal input conditions, the AGC voltage is +4 Vde , and the U6 output is +1.5 Vde. This gives an overall loss in U2 of -32 dB .


Figure 3-14. 1st Converter, FE-A1A2A3, Block Diagram

RF INPUT SWITCH (FE-A2) (794276)
The RF Input Switch is a modular assembly which mounts one P.W. subassembly, RF Input Switch, FE-A2A1.

### 3.4.8.1 RF Input Switch (FE-A2A1) (270935)

Refer to Figure 6-11, RF Input Switch Schematic Diagram, as an aid in understanding the following circuit description.

The RF Input Switch consists of two solid RF switches, U1 and U2. Pin 11, the control pin, of each switch is connected together and routed to the control input line from the Digital Control. When the control input is low, U1-7 is connected internally to U1-4, making an RF signal path from J1 to J2. At the same time, U2-7 is connected internally to U2-4, making an RF signal path from J4 to J5.

When the control input is high, U1-1 is connected internally to U1-4, making an $R F$ signal path from J 1 to J 3 . At the same time, U2-1 is connected internally to U2-4, making an RF signal path from J6 to J5.

## 3.4 .9

1 MHZ FILTER (FE-A3) (794327)
Refer to Figure $6-12,1 \mathrm{MHz}$ Filter Schematic Diagram, as an aid in understanding the following circuit description.

The 1 MHz Filter is a 5 -pole elliptic low pass filter with a cutoff frequency of 1 MHz . It exhibits a 50 ohm characteristic impedance and a nominal loss of < -3 dB . Above 1 Mhz , the loss increases rapidly, being typically > -40 dB for frequencies above 2 MHz .

### 3.4.10 INPUT CONVERTER (A3) (791592-7)

The Input Converter is a modular assembly which mounts two P.W. subassemblies, First Mixer, A3A1, and 2nd Mixer, A3A2. Figure 3-15 is a detailed functional block diagram of the Input Converter which should be referred to in the following circuit description. Figure 6-13, Input Converter Schematic Diagram, may be referred to for greater component level detail, if desired.

### 3.4.10.1 First Mixer (A3A1) (370611)

RF input signals enter the 1st Mixer, A1U1, in the frequency from 5 kHz to 30 Mhz . The Mixer, AlU1, is also driven by the 1 st LO signal, 42.91-72.90 MHz at a level of +20 dBm . AlU1 converts the RF input signals to the lst IF frequency of 42.905 MHz . The conversion loss of the 1st Mixer is approximately 6 dB . Therefore, the 1 st Mixer is followed by amplifier A1U2 to overcome the loss. A1U2 is a broadband hybrid integrated amplifier with a low noise figure, a good terminating impedance for the mixer, and a large signal handling ability. The output load of 11 U 2 is 50 ohms, which properly terminates the 1 st IF crystal filter A1FL1. This filter requires a 50 ohms source and load and has a center frequency of 42.905 MHz and a 3 dB bandwidth of 16 kHz .


Figure 3-15. Input Converter Functional Block Diagram.

### 3.4.10.2 Second Mixer (A3A2) (370646)

Signals passed by A1FL1 are coupled to a second amplifier, A2Q2, through a coupling network. This amplifier is biased by constant current source A2Q1 biasing network. Its output circuit is a broadly tuned transformer, but is shunted by gain control diode A2CR2. As the current through the diode increases, its $R F$ impedance decreases and the net gain of A2Q2 is decreased. Current to A2CR2 is supplied by the RF Gain portion of the AGC, A4A6. As the current varies from zero to maximum, there is approximately 30 dB of gain reduction.

The output signal of A2Q2 is down converted by the 2nd Mixer, A2U1. The 2nd LO signal enters the Input Converter via A2J1 at a level of approximately 0 dBm . Common emitter amplifiers, A2Q5 and A2Q6, provide enough gain to bring the 2nd LO signal to a nominal level of +17 dBm . Each of these stages is broadly tuned transformer-coupled and each has some unbypassed emitter resistance to preserve a relatively low harmonic content in the 2nd LO signal.

The 2nd Mixer is followed by a bipolar cascode amplifier. It consists of common emitter stage A2Q4 and common base stage A2Q3. These provide relatively high gain with good stability and low noise contribution. The 2nd IF signal is coupled from the collector of A2Q3 through Matching Network Z1. Z1 consists of a single pole bandpass filter $\mathrm{C} 1, \mathrm{C} 2, \mathrm{C} 1$ and C 2 , and has a center frequency of 10.7 MHz . The output of $\mathrm{Z1}$ passes through A2J3 to rear panel WB OUT J16. Transformer A2T2 couples the 2nd IF output of A2Q3 to crystal filter A2FL1. This filter has a center frequency of 10.7 MHz , a bandwidth of 50 kHz , and requires 50 ohm terminations.

The amplified, bandlimited 2 nd IF output from A3 drives the 50 ohm input to the 10.7 MHz Filter Switch, A4A1.

### 3.4.11 $\quad 10.7 \mathrm{MHz}$ FILTER SWITCH (A4A1) (791594)

The 10.7 MHz Filter Switch mounts on the IF Motherboard, A4, (see paragraph 3.3.4). Figure $3-16$ is a detailed functional block diagram of the 10.7 MHz Filter Switch which should be referred to in the following circuit description. Figure $6-15,10.7 \mathrm{MHz}$ Filter Switch Schematic Diagram, may be referred to for greater component level detail, if desired.

The 10.7 MHz Filter Switch receives the 10.7 MHz IF signal output from the Input Converter, A3. At this point, the IF bandwidth has been set at 100 kHz by a filter in the Input Converter. The 10.7 MHz Filter Switch contains bandpass filters of 6.0 kHz and 3.2 kHz bandwidth. The purpose of this circuit is to route the IF signal through one of these filters, or through a wideband path which allows the full 50 kHz bandwidth to pass. The selection of the filter path is made by application of a logic high level to one of the three control terminals.

In any IF bandwidth, a logic high is applied to one of three control lines from the I/O Motherboard, at pin 15, 17, or 19. These lines are connected to the non-inverting inputs of U1A, U1B, and U2A. The inverting inputs are held at approximately 0.8 V by voltage divider R52-R53. The output voltage of the selected op-amp swings positive, turning on one pair of common-emitter IF amplifier stages. or example, if U1A is selected, Q1 and Q4 are turned on.


Figure 3-16. 10.7 MHz Filter Switch Functional Block Diagram.

The 10.7 MHz IF signal is input at pin 13 and coupled through C 1 to the base circuits of Q1, Q2, and Q3. If Q1 is on, the signal is amplified and coupled to FL1. This filter has a 200 ohm input impedance and a 3 dB bandwidth of 3.2 kHz . The filtered IF signal is applied to amplifier Q4 through level-adjust potentiometer R26. The amplified IF signal is output at pin 57 . If 6.0 kHz bandwidth is selected, the IF signal is routed through Q2, FL2, and Q5. If any other bandwidth is selected, the IF signal is routed through Q3, attenuator R22, R23, R24, and Q6. The gain of the three signal paths is equalized by $R 26, \mathrm{R} 28$, and R 30 to approximately 14 dB . The circuit has nominal input and output impedances of 50 ohms.

### 3.4.12

$10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ CONVERTER (A4A2) (794254)
The $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter mounts on the IF Motherboard, A4, (see paragraph 3.3.4). Figure 3-17 is a detailed functional block diagram of the 10.7 MHz/455 kHz Converter which should be referred to in the following circuit description. Figure $6-16,10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Schematic Diagram, may be referred to for greater component level detail, if desired.
10.7 MHz IF signals from A4A1 drive the input to A4A2. In all modes but DF, the DF select pin 45 is low, causing U2-1 to be low and U2-7 to be high. The IF signals then pass through Q2 and Q4 to the input of mixer U1. In DF mode, pin 45 is high, causing U2-1 to be high and U2-7 to be low. The IF signals then pass through Q1, filter FL1 and Q3 to the input of mixer U1. FL1 restricts the bandpass to 2.2 kHz .

Mixer U1 converts the 10.7 MHz IF signals to 455 kHz . The 3 rd LO signal is input at the fixed frequency of 11.155 MHz and a level of approximately -6 dBm , and is amplified by transistor Q 1 and its associated circuitry to +7 dBm before entering the mixer. The amplifier operates as a common emitter stage with some unbypassed emitter resistance to stabilize its gain and reduce distortion. The pi-network, C7-L2-C8, serves as an impedance transformer and low-pass filter, further reducing distortion of the LO signal.

Low-pass filter C9, L3, C10, L4, and C11 filters out undesired components above 500 kHz from the mixer output and matches impedances between the mixer and the following circuits. The nominal input impedance of the 3rd Mixer is 50 ohms and the output impedance is 1000 ohms.


Figure $3-17$. $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Functional Block Diagram.

The 455 kHz Filter Switch mounts on the IF Motherboard, A4, (see paragraph 3.3.4). Figure $3-18$ is a detailed functional block diagram of the 455 kHz Filter Switch which should be referred to in the following circuit description. Figure $6-17,455 \mathrm{kHz}$ Filter Switch Schematic Diagram, may be referred to for greater component level detail, if desired.

The 455 kHz Filter Switch receives the 455 kHz IF signal output from the $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter, A4A2. The 455 kHz Filter Switch routes the IF signal through one of two bandpass filters of 1.0 kHz and 0.3 kHz bandwidth, or through a wideband path which allows the full bandwidth from A3, A4A1 and A4A2 to pass. The selection of the filter path is made by application of a logic high level to one of the three control terminals.

The input signal at pin 13 connects in parallel to Q1, Q3, and Q5. When Q1 is biased on, the signal passes through Q1 and is fed through the 0.3 kHz crystal filter (FL1). The biasing of Q1 and Q2 is controlled by the voltage on pin 19. When this voltage is high ( +5 V ), the output of U1D will be +12 V , thus biasing Q1 and Q2. When this voltage is low ( 0 V ), the output of U1D will be -12 V which will cause an approximate 1 V reverse bias to the bases of Q 1 and Q 2 , and thus they are turned off.

When the 1.0 kHz bandwidth is selected, module pin 17 is high, and U1A turns on Q3 and Q4. When the $3.2 \mathrm{kHz}, 6 \mathrm{kHz}$ or 50 kHz bandwidths are selected, module pin 15 is high and U1B turns on Q5 and Q6. When ISB, LSB, or USB are selected, all three control lines to this card are low and all three signal paths are inhibited.

All transistors, Q1 through Q6, are operated as common emitter amplifiers with unbypassed emitter resistors to control their gain. Through any of the three signal paths there is a net voltage gain of approximately 9 dB from the input to the output of the module. OPAMP section U1C is not used and is as shown in the schematic connected in an inoperative condition.

## 3.4 .14

AGC AMPLIFIER (A4A6) (791675)
The AGC Amplifier mounts on the IF Motherboard, A4, (see paragraph 3.3.4). Figure $3-19$ is a detailed functional block diagram of the AGC Amplifier which should be referred to in the following circuit description. Figure 6-18, AGC Amplifier Schematic Diagram, may be referred to for greater component level detail, if desired.

In the AGC module, the direct coupled output of the AM detector is filtered by R5 and C3 to limit the speed of response of the Fast AGC. In the Fast AGC Mode, Q7 is biased off, disconnecting C4, so Q1 operates simply as an emitter
follower. Q7 is biased on when Slow AGC is selected, grounding the negative end of C4. Q1 continues to be off until C4 is discharged by R3. This action gives the fast attack response and slow decay response of the Slow AGC mode. Zener diode CR2 acts as a limiter to prevent short bursts of signal from overcharging C 4 (which might cut off the amplifiers for many seconds).


Figure 3-18. 455 kHz Filter Switch Block Diagram


Figure 3-19. AGC Block Diagram

Buffer amplifier U1A isolates C4 from the following circuits. Q2 is a threshold blocking AGC action for weak signals. The base of Q2 is biased to approximately +0.2 V . If the emitter of Q 2 is lower than about +0.8 V , Q2 will be turned off and no AGC action can occur. When the output of U1A is greater than $+0.8 \mathrm{~V}, \mathrm{Q} 2$ conducts and a gain control voltage appears across R13. When the Manual gain mode is selected, Q3 and Q6 will be turned on and will clamp the voltage on R13 to ground, and +5 V will be applied to the RF Gain potentiometer on the front panel. Inverting summing amplifier U2B combines the voltage at R13 (which will be zero in Manual gain mode) and the voltage on the RF GAIN control (which will be zero in Fast or Slow AGC modes).

The output of summing amplifier U2B is buffered by OP AMP U1D and fed to the 455 kHz amplifier on A4A7. Zero volts from U1D allows the 455 kHz amplifier to operate at maximum gain while a negative output from U1D causes the gain of the IF amp to be reduced.

A sample of the IF gain control voltage from U2B is also applied to RF AGC threshold detector Q5. This threshold detector causes the gain reduction to occur only in the 3rd IF amplifier, unless the signal at the RF input of the receiver and in the early stages of the receiver is great enough to ensure a good signal-to-noise ratio even in the early stages. The operation of the threshold detector is the same as that of Q2, except with polarities reversed to allow for the inversion which occurs in U2B. The base of $Q 5$ is biased around -2.7 V so the IF gain control voltage must be more negative than -3.3 V for Q 5 to conduct.

To achieve the desired relationship between AM Detector output and RF gain reduction requires that the control diode current rise slowly at first, then more rapidly as the received signal strength increases further (exponentially). This current/voltage relationship is obtained through a shaping network comprised of U2D, R47, R48, CR5, and R31. The actual current for the control diode is supplied by buffer U2A. In the Manual gain mode, this voltage is proportional to the RF input signal voltage. Its polarity is inverted by OP AMP U1C and it is applied through R49 and front panel switches A10A1S1B and S2C to the meter. This allows the receiver to act as a tuned voltmeter whose calibration depends on the setting of the RF GAIN control.

In the AGC modes, the voltage out of U1A increases approximately linearly with signal voltage up to the AGC threshold level of 3 V (RF input). Above this level the U1A output is compressed by AGC action to be nearly proportional to the logarithm of the RF input voltage. By using a shaping network composed of R41, R50, R51, CR6, CR7, and CR8 to suitably compress the output of U1C at low signal levels, the signal strength meter is made to be approximately linear in dB over a greater than 100 dB range. Resistors R 50 and R51 control the amount of compression and the exact fit of the meter scale with signal strength. If an accurate source of variable signal level is available, these fixed resistors may be replaced with variable ones which may be adjusted for best tracking of the meter. The variable resistors may then be removed, measured and replaced with fixed resistors of the same value.

The 455 kHz Amplifier/AM Detector mounts on the IF Motherboard, A4, (see paragraph 3.3.4). Figure $3-21$ is a detailed functional block diagram of the 455 kHz Amplifier/AM Detector which should be referred to in the following circuit description. Figure $6-19,455 \mathrm{kHz}$ Amplifier/AM Detector Schematic Diagram, may be referred to for greater component level detail, if desired.

The IF input signal is first amplified by two-stage gain controlled amplifier, The signal is then split to provide three outputs: the IF sample which operates the FM/CW/SSB Demodulator, the IF output for the rear panel, and the input to the AM Detector. The AM Detector, which operates at a relatively high level for good linearity, has its output directly coupled to the AGC module and the Audio Amplifier.

FET's Q1 and Q2 operate as common. source amplifiers with their gains controlled by a variable voltage applied to gate 2 of each transistor. Inductors L1 and L2 broadly tune the outputs of Q1 and Q2 by cancelling any stray capacitance. The net overall bandwidth of the Q1/Q1 amplifier exceeds 50 kHz . Potentiometer R7 between the first and second amplifiers adjusts the maximum gain of the amplifiers and hence of the whole receiver. Q2 drives emitter follower amplifier Q7. The low impedance emitter output of Q7 passes through bandpass filter L3, L8, L9, C11 and C34-C36. This filter establishes the bandpass of A4A7 at approximately 100 kHz . The filter is terminated by the low impedance base input of Q3.

Transistor Q3 serves as a buffer between the 455 kHz amplifier and its chree outputs. For signals fed to the FM/CW/SSB Detector (pin 13), Q3 acts as an emitter-follower stage. For the rear panel IF Output, Q3 feeds the signal to Q4, which acts as a power amplifier. Transformer T1 supplies a 50 ohm IF output to the rear panel, providing a nominal 20 mV IF output for RF inputs greater than 3 V . For the AM detector, Q3 and Q5 both act as common-emitter amplifiers to raise the IF signal to a level of several volts which will permit the detector diode, CR3, to perform linearly. Diodes CR4 and CR5 provide a de-bias to operate the AM Detector and emitter-follower (Q6) above ground to establish the proper de level for the AGC circuit. The low-pass filter of L7 and C31 suppresses any residual IF signal.

## 3.4 .16

FM/CW/SSB DETECTOR (A4A9) (791599)
The FM/CW/SSB Detector mounts on the IF Motherboard, A4, (see paragraph 3.3.4). Figure 3-22 is a detailed functional block diagram of the FiM/CW/SSB Detector which should be referred to in the following circuit description. Figure 6-20, FM/CW/SSB Detector Schematic Diagram, may be referred to for greater component level detail, if desired.

For FM reception, this module contains a limiter and discriminator. Power for these circuits is supplied when the FM detection mode is selected. For CW or SSB reception, there is a product detector which has its power applied when the CW, USB or LSB detection modes are selected. Also, when the product detector is energized, the BFO Synthesizer is enabled and its output is applied to the product detector.


Figure 3-21. 455 kHz Amplifier/AM Detector Functional BlockDiagram.


Figure 3-22. FM/CW/SSB Detector Functional Block Diagram.

The IF output sample of approximately 10 mV from the 455 kHz amplifier of A4A7 is the input signal for this module. It is applied to both demodulators although only one is actuated at a time. When FM is selected, the control input at pin 41 is high ( +5 V ) and Q 2 and Q 1 are turned on. This applies approximately +9 V to limiter U1. The input signal is amplified and clipped by cascaded stages within U1, so its output is free of any amplitude variations. The extent to which the amplitude variations are removed contributes to the AM rejection of the receiver when receiving FM. The output of the limiter drives the Foster-Seeley discriminator. Diodes CR1 and CR2 rectify the composite signals fed to them by C7 and T1. When the signal from the limiter is at exactly $455 \mathrm{kHz}, \mathrm{T} 1$ is tuned so that equal and opposite voltages are produced across load resistors R6 and R7, giving a net output of zero to buffer U3A. For inputs slightly off 455 kHz , the voltages of R6 and R7 do not cancel causing a positive output for inputs above 455 kHz and a negative for those below 455 kHz . (Note that these polarities are reversed by U3C, so the output of the module will go negative when the signal frequency increases.) Proper adjustment of L1 will make the output voltage vary linearly with input frequency over $\$ 8 \mathrm{kHz}$ from 455 kHz . At the output of U3A, a low-pass filter, L3 and C11, reduces higher frequency noise components which are present in the discriminator output. When the CW mode or any of the sideband modes is selected, the control input on pin 43 is high $(+5 \mathrm{~V})$. This turns on Q4 and Q3, applying +9 V to balanced modulator U2. The BFO is also applied to U2 (approximately a 40 mV level). This allows U 2 to act as the 4 th mixer in the signal path as described in the Synthesizer Relationships section. Its action may be considered to down-convert IF signals to the audio frequency range. For sideband signals, proper tuning of the receiver places the center of the IF signal at the frequency corresponding to the carrier frequency of the received signal. This causes the audio components out of $U 2$ to reconstruct those of the original signal transmitted. For CW signals, the BFO is of fset from the signal either by use of the BFO offset control on the front panel to cause an audible tone at the audio output when a signal is present.

The output of U2 goes through low-pass filter L2 and C17, which reject higher frequency noise components, to buffer U3B. OP AMP U3C acts as a summing amplifier for the outputs of the FM discriminator or product detector when either is present. It gives different amplifications to these two signals to bring them up to approximately equal levels. The audio output of this module goes to the Audio Amplifier.

### 3.4.17 AUDIO AMPLIFIER (A4A10)

The Audio Amplifier mounts on the IF Motherboard, A4, (see paragraph 3.3.4). Figure $3-23$ is a detailed functional block diagram of the Audio Amplifier which should be referred to in the following circuit description. Figure 6-21, Audio Amplifier Schematic Diagram, may be referred to for greater component level detail, if desired.

The Audio Amplifier combines the audio outputs of the AM detector and FiM/CW/SSB Detector and feeds them to the LINE AUDIO LEVEL control on the front panel and the PHONE LEVEL control on the front panel. The signal returned from the wiper of the LINE AUDIO LEVEL potentiometer drives the line audio amplifier. The signal returned from the PHONE LEVEL control drives the auxiliary phone amplifier which feeds the PHONE AUDIO terminals on rear panel J16. A rectifier which samples the output of the line audio amplifiers supplies de to operate the front panel meter in the LINE AUDIO setting.


Figure 3-23. Audio Amplifier Functional Block Diagram.

When the AM detection mode is selected, the control input to pin 47 is high ( +5 V ). The output of U1A is +14 V , which reverse biases CR1. The gate of FET Q1 will then assume the same potential as its source and Q1 will be on, acting as a closed switch for AM audio. Both demodulators of the FM/CW/SSB Detector will be off so the output of U1D will be AM audio only. When any other detection mode is selected, the control input to pin 47 will be low ( 0 V ) and the output of UlA will be approximately -14 V . This will tend to forward bias CR1 and will cause gate of Q1 to be similarly negative, cutting off all signal flow through Q1. The audio signal from the FM/CW/SSB Detector will appear at the output of U1D.

The signal into line audio amplifier U2 is the output of U1D attenuated by the LINE AUDIO LEVEL control, R1. The two sections of $U 2$ act as a push-pull bridge amplifier, driving output transformer T2 located on the inside of the rear panel. The amplifier U2 uses a supply voltage of +24 Vde from A1-J35. Transistor Q2 is biased as a current limiter to protect U2 in case of short circuit on any of U2's outputs. A circuit within U2 provides a bias voltage at pin 1 which is equal to one-half the supply voltage. This is connected to the non-inverting inputs of both amplifier sections of U2. Both amplifiers use unity feedback at dc, that is, the only de path to the inverting inputs is from the outputs, so there is very little de difference between their outputs at pins 2 and 13 .

The input signal is applied to the non-inverting input of U2B, pin 9. Although pins 6 and 9 are at the same de potential, pin 6 is bypassed so no ac signal appears there. The operation of amplifier U2B will be clear if pin 7, the inverting input of U2A, is considered to be at ac ground. With this assumption, U2B simply appears as a non-inverting amplifier with a closed-loop ac gain of 50 . Its ac gain is determined by the ratio of feedback resistors R20 and R19. On the other hand, U2A may then be viewed as an inverting amplifier with an ac gain of nearly one. Its input is the full output of U2B and its gain is determined by R20 and R19 acting as input resistors and R21 as feedback resistor. As with inverting OP AMPs, extremely little signal voltage appears at the amplifier inverting input terminal, thus satisfying the assumption made to explain the behavior of U2B. The net gain of the combined amplifier is 100 and its outputs are balanced with respect to ground. Due to the high current U2 can pass, it is grounded separately from the other circuits on the Audio Amplifier module to prevent ground current coupling which might lead to instability and parasitic oscillations.

The output signal of U2A is rectified and filtered to indicate LINE AUDIO level on the panel meter. The rectifier is a voltage doubler consisting of CR2, CR3, C 12 , and C13. It responds to peak-to-peak input voltage and is calibrated by resistors R22, R23, and R24 to indicate the RMS value of a sine-wave at the LINE AUDIO terminals of J16 on the rear panel. Its calibration is therefore most accurate for sine-wave voltages.

The auxiliary phone amplifier U1B and U1C is a low power bridge amplifier and is therefore similar to U2. It operates from both +15 V and -15 V supplies and has its inputs biased at ground. Comparing its circuit with that of $U 2$ it should be apparent that it also uses unity de feedback and has a closed loop gain of 100 for ac signals. The phone amplifier output is transformer coupled to the rear panel terminal J16. Output level is 100 mW nominal across 600 ohms.

1ST AND 3RD LO SYNTHESIZER/TIME BASE (A5A1) (791630)
The 1 st and 3rd LO Synthesizer/Time Base Assembly mounts on the A5 Motherboard (see paragraph 3.3.5), and consists of two subassemblies: VCO, A5A1A1, and 1 st \& 3rd LO/Time Base, A5A1A2.

### 3.4.18.1 $\quad \mathrm{VCO}$ (A5A1A1) (791629)

Refer to Figure 3-23, 1st LO Synthesizer Block Diagram, and Figure 6-24, 1st LO/VCO Assembly Schematic Diagram, as aids in understanding the following description. The VCO has two inputs and two outputs. The inputs to the VCO are a tuning voltage and a band-switching code. The VCO operates at a frequency four times the desired 1st LO frequency. The band select code and the tuning voltage combine to tune the oscillator from 171.64 MHz to 291.60 MHz in 40 kHz steps.

Octal encoder U13 accepts BCD inputs from the two MSD's of the 1st LO frequency word from the Digital Control Section. U13 output consists of a binary coded word Y2, Y3 and Y4. The levels for each bit are -12 V for logic 0 and +15 V for logic 1. Applying a negative-true-code voltage to the BAND SELECT inputs tunes the oscillator to one of eight different frequency bands. When the BAND SELECT inputs are all positive, CR1 through CR3 are off, and L2 through L4 are effectively out of the circuit. This allows the inductance of T 1 to be maximum. When any or all of the BAND SELECT inputs are negative, the corresponding diode will conduct and the inductance of T1 will be reduced by the shunting effect of the inductor (L2, L3, or 4).

Varactor diode CR4 fine tunes the oscillator in response to the tuning voltage input. Common-emitter amplifier Q2 keeps load changes at the input of power divider R9 and R10 from being reflected back to the output of oscillator Q1. T2 matches the output of the amplifier to the input of the power divider. The signal is coupled to buffer amplifier Q3, which drives the prescaler of the synthesizer. R9 and C15 couple the signal from Q2 to the input of the divide-by-4 circuit U1. MECL divider U1 divides the signal frequency by four and amplifier Q5 isolates its output from load changes. Voltage regulator Q4 provides U1 and Q5 with a -7.0 V power input from the -12 V power supply input to the assembly. Amplifiers Q 5 and Q 7 provide the relatively high currents needed to drive the input of the lst Mixer.

### 3.4.18.2 1 st and 3rd LO/Time Base (A5A1A2) (791600)

Refer to Figure 3-23, 1st LO Synthesizer Block Diagram, Figure 3-24, 3rd LO Block Diagram, and Figure 3-25, Time Base Block Diagram, as aids in understanding the following description. Figure 6-23, 1st and 3rd LO Synthesizer/Time Base Schematic Diagram, Figure 6-24, 1st LO/VCO Schematic Diagram, and Figure 6-25, 1st and 3rd Synthesizer Schematic Diagram, may be referred to for greater component level detail, if desired. The 1 st and 3 rd LO/Time Base consists of the following major circuit areas:


Figure 3-23. 1st LO Synthesizer Block Diagram


Figure 3-24. 3rd LO Functional Block Diagram.


Figure 3-25. Time Base Circuits Functional Block Diagram

- 1st LO Prescaler
- 1st LO Main Programmable Divider .
- 1st LO Terminal Count Detector
- 1st LO Phase Detector
- 3rd LO Synthesizer
- Time Base


### 3.4.18.2.1 1st LO Prescaler

A two-modulus prescaler, U1/U2A, is used at the input to the divide-by-N counter to divide down the frequency from the VCO so that it can be handled by conventional low-power Schottky counters.
The prescaler input frequency ranges from 171.64 MHz to 291.60 MHz . The prescaler divides this by 50 or 51 , depending on the states of the E inputs of U1. U1 is a divide-by-10/11 counter and U2A is a divide-by-5 counter. The prescaler divides by 51 when E4 is low and when E5 pulses low once for every five pulses from U2A. E5 is low for only one count out of five so the complete count cycle of U1 and U2A takes 51 counts ( $4 \times 10+1 \times 11$ ). Control of the prescaler via E4 comes from the swallow portion of the programmable divider (see paragraph 3.4.18.2.2). The prescaler output rives the clock input to the programmable divider and the terminal count detector.

### 3.4.18.2.2 1st LO Programmable Divider

The programmable divider consists of swallow counter U8/U9 and main counter U9, U10, U11 and U12A. The counters within the programmable divider have a divide range from 4291 to 7290. The inputs of the counters are always preset from the $B C D$ equivalents of the four most significant digits of the tuned frequency. This range is from 0000 to 2999.

The 1st LO swallow counter is formed by decade counter U8 and the divide-by-5 part of bi-quinary counter U9. Cascaded, they form a divide-by-50 counter which controls the divide mode of prescaler U1. The programmable counter is formed by U11, U10, and part of U9. U11 and U10 count down and U9 counts up. U10 is a divide-by-10 counter (BCD). U11 is a divide-by-10 counter (BCD). With the D input of U11 tied high (to Vec 3), the counter is always preset with at least 8 (1000). The divide-by-2 counter within bi-quinary counter $U 9$ is part of the programmable counter, using preset input $A$ and output QA .

Since U11 is wired to automatically add 8 to its preset, the programmable divider has a preset input range of $8000(0000+8000)$ to $10999(2999+8000)$. The terminal count detector (see paragraph 3.4.18.2.3) stops the programmable divider when a terminal count of 3709 is reached. Since the counters are wired to count down, the overall divide range needed from the counters is obtained; the divide range is from (291 (8000-3709) to 7290 (10999-3709).

### 3.4.18.2.3 1st LO Terminal Count Detector

The terminal counts of both the swallow counter and the programmable counter are detected by the terminal count control IC, U3. The prescaler mode is controlled by the swallow counter logic outputs applied to the Z inputs of U3. The terminal count for the swallow counter occurs at 09. The terminal count of the programmable (main) counter is obtained when the correct logic levels are applied to the $P$ and $B$ inputs of U3. As previously stated, the terminal count occurs at 370 .

When the terminal count logic conditions are satisfied (at the $P$ and $B$ inputs) U3 counts one clock pulse, then drops the $F_{0}$ output line low. This resets the flip-flops and presets (loads) the counters. At the end of the second clock pulse, the $\mathrm{F}_{0}$ output goes high, starting the count cycle and clocking the VCO phase detector, U5. The Fo output pulse to the phase detector is approximately 40 kHz .

### 3.4.18.2.4 1st LO Phase Detector

Phase detector $U 5$ receives a fixed 40 kHz reference frequency at the $R$ input and a variable frequency at the $V$ input from the programmable divider. The output of U5 consists of narrow pulses, whose average de level is proportional to the frequency difference between the $V$ and $R$ inputs.

When properly locked, the output pulses from U5 will be extremely narrow. For large differences in frequency, the U5 output consists of wide pulses. These pulses are integrated and amplified by the charge pump, U6C, and the loop filter, U7. The resulting dc level is the VCO tuning voltage which drives the VCO frequency determining network, thus controlling the VCO frequency.

### 3.4.18.2.4 3rd LO Synthesizer

The 3rd LO is part of the 1 st and 3rd LO/Time Base board. The 3rd LO has an input of two reference frequencies from the Time Base and a fixed output frequency of 11.155 MHz .

VCXO (voltage-controlled crystal oscillator) for this synthesizer is formed by Q8, Y1, CR7, and their associat ed components. The oscillator is crystal-controlled to 11.155 MHz , with actual oscillating frequency determined by the de tuning voltage applied to CR7. The oscillator signal is buffered by follower Q9 and is split into two signal paths. One path is to board pin A55, the 3rd LO output. The other path is through sine-to-TTL converter Q10 to flip-flop U21B, which acts as a digital mixer. The 3rd LO signal is compared to a 50 kHz reference at pin 11 of U 21 B , to produce a 5 kHz output, when the 3 rd LO is locked. The 5 kHz output is the difference between the VCO frequency ( 11.155 MHz ) and the frequency that is the nearest integral multiple of the clock frequency ( $223 \times 50 \mathrm{kHz}=11.15 \mathrm{MHz}$ ). This 5 kHz signal from the mixer is compared to a 5 kHz signal from the time base, via divide- by- 2 U 21 A , in the phase detector, U22A. The charge pump U22B converts the differences in phase and/or frequency into positive and negative going de levels. These levels pass through filter U22C and bias varactor diode CR7. The 11.155 MHz crystal oscillator is then driven in the direction to achieve lock. The 3rd LO frequency then passes through buffer amplifier Q9 and TTL driver Q10 to complete the loop.

### 3.4.18.2.6 Time Base

The Time Base can be controlled internally with a 2 MHz temperature compensated crystal oscillator, U14, and divide-by-2 frequency divider, U15A, or with a 1 MHz external source. Tri-state buffers controlled by rear panel INT/EXT switch accomplish the switching of internal and external reference sources.

When operating with an external source of reference, the external select (EXT SEL) line is grounded and the internal select (INT SEL) is pulled high by R84, and the externally supplied 1 MHz reference is seen at module pin A17, EXT/INT STD. The internal 1 MHz reference is inhibited when it reaches tri-state buffer U23B. The external 1 MHz signal passes to transformer T 1 . T1 and C 23 resonate at 1 MHz while the voltage divider of R 34 and R 35 shifts the 1 MHz signal to a 2.5 Vdc level. This signal enters U16 which converts the sine wave to TTL levels. The output of U16 passes through tri-state buffer U23A and on to the rest of the Time Base circuits.

Operation with the internal source grounds the internal select (INT SEL) line and allows the external select line to be pulled up by R85. Tri-state buffer U23 allows the 2 MHz signal that is divided to 1 MHz to be passed on to the rest of the circuitry. The 1 MHz reference splits to two parts of the circuit. In one direction, the reference signal passes through U23C and out the EXT/INT STD connection. The signal does continue to pass through U16 but is inhibited at U23A. In the other direction, the reference signal passes to pin 3 of U23A (EXT) or pin 11 of U23B (INT), and on to the rest of the time base circuitry.

For either source of reference, a 1 MHz TTL signal is present at the input of Q6 and U15B. This signal is divided by 25 , through U15B and U17, to become a 40 kHz reference for the 1 st LO . The 1 MHz signal also passes through an isolation amplifier Q6 to board pin A9 to be used as a reference for the 2nd LO. The 1 MHz signal also passes through another isolation amplifier, Q7, to be divided down to three more reference frequencies.

U18A and U19A form a divide-by-4 network whose input is 1 MHz and whose output is 250 kHz . This 250 kHz divides down to 50 kHz through divider U19B and is sent to U21B, the digital mixer of the 3rd LO. The output of U19B also enters U18B, whose output is a 10 kHz signal. This signal leaves the board to be used as a reference for the 2nd LO, and is divided to 5 kHz by U21A to act as a reference for the 3 rd LO circuit. The 10 kHz signal also passes through a divide-by- 10 network, consisting of U20A and U20B, for an output reference signal of 1 kHz .

### 3.4.19 2ND LO SYNTHESIZER (A5A2) (791601)

The 2nd LO Synthesizer Assembly mounts on the A5 Motherboard (see paragraph 3.3.5). The 2nd LO Synthesizer tunes in 100 Hz steps from 32.21000 MHz to 32.20001 MHz . Refer to Figure 3-26, 2nd LO Synthesizer Block Diagram, as an aid in understanding the following description. Figure 6-26, 2nd LO Synthesizer Schematic Diagram, may be referred to for greater component level detail, if desired. The 2nd LO consists of three separate phase locked loops as follows:


Figure 3-26. 2nd LO Synthesizer Block Diagram

# - 32 MHz Fixed Loop <br> - Programmable Loop <br> - Output Loop 

### 3.4.19.1 32 MHz Fixed Loop

The 32 MHz loop consists of VCO Q5 operating at approximately 32 MHz . The frequency of Q5 is determined by varactor diode CR3. The Q5 output is amplified by buffer Q1 and drives a divide-by- 32 counter U2/U3A. The resulting 1 MHz output from the counter drives the $V$ input of phase detector $U 1$. The $R$ input of $U 1$ is driven by a 1 MHz reference signal from A5A1. The $R$ and $V$ inputs are compared by U1A and the resulting de output from loop filter U1B drives varactor diode CR3. The de voltage applied to CR3 locks the oscillating frequency of Q5 at exactly 32 MHz . The 32 MHz output from buffer Q1 passes through filter C9/L9 and drives the input to mixer U4.

### 3.4.19.2 Programmable Loop

The programmable loop consists of a prescaler, main programmable counter, phase detector, filter and VCO. The VCO, Q7, oscillates at approximately $200-210$ MHz . The frequency of Q7 is determined by varactor diode CR5. The output of Q5 frives the prescaler U14/U15. The prescaler has divide ratios of $100 / 101$ and is under the control of the swallow counter portion (U7/U8) of the main programmable counter. The purpose of the prescaler is to divide the 200 MHz VCO frequency down to a frequency which can be handled by the main counter.

The main programmable counter consists of swallow counter, UT/U8, and main counter, U9/U10. U11A,B,C,D is wired as a terminal count detector the swallow counter and the main counter. The terminal count detector resets the main programmable counter with a reset pulse when a terminal count of 24200 is reached. The swallow counter is preset with BCD digits from 00 to 99 and the main counter is preset with BCD digits from 0 to 9 from the Digital Control Section. Counter U10 is always wired to add binary 32 to the main counter preset, so the overall chain is preset with the range of $3200(3200+000)$ to $4199(3200+999)$.

Suppose 000 is loaded into the 2nd LO. The input to the counters is 3200 $+000=3200$. The terminal count is 24200 , so the divide ratio is $24200-3200=$ 21000. Suppose 999 is loaded. The input is $3200+999=4199$. The divide ratio is $24200-4199=20001$. Suppose 500 is loaded. The input is $3200+500=3700$. The divide ratio is $24200-3700=20500$.

The result pulse from U11 is approximately 10 kHz and drives the V input of phase detector U12. The $R$ input of U12 is driven by the 10 kHz reference signal from A5A1. U12A compares the $R$ and $V$ inputs and the resulting de level is filtered and amplified by loop filter U12B. The de tuning voltage from U12B is applied to varactor CR5. This tuning voltage locks the frequency of VCO Q7 to 200.01 MHz ( 999 oreset inputs or divide ratio $=20001$ ) to $210.00 \mathrm{MHz}(000$ preset inputs or divide ratio 21000). The VCO output passes through the divide-by-1000 counter U16, U17 and U19. The resulting output of 210.00 kHz to 200.01 kHz drives phase detector U6A.

### 3.4.19.3 Output Loop

The output loop consists of VCO Q6, phase detector U6 and mixer U4. VCO Q6 oscillates at approximately 32.2 MHz . The oscillating frequency of $Q 6$ is determined by varactor diode CR4. The 2nd LO VCO output of approximately 32.2 MHz is routed to mixer U4, where it is mixed with the fixed-frequency phase lock loop output of 32 MHz . This mixer produces the difference of its two input frequencies, resulting in an output within the 200 to 210 kHz range. This output is amplified and level translated for TTL compatibility. Mixer output and divide-by- 1000 output signals are compared in frequency and phase by U6A, whose output characterizes the difference between its two inputs. Filter U6B integrates the phase detector output into a varying de voltage which drives the VCO.

When the divide-by-1000 output is 200.01 kHz ( 999 preset inputs), U6 locks VCO Q6 at 32.20001 MHz . When the divide-by- 1000 output is 210.00 kHz ( 000 preset inputs), U6 locks VCO Q6 at 32.21000 MHz . The VCO output is amplified by buffer Q3 and is coupled through matching network C22/C23 to become the 2nd LO output.
3.4 .20

BFO SYNTHESIZER (A5A3) (791576)
The BFO Synthesizer mounts on the A5 Motherboard (see paragraph 3.3.5)The BFO Synthesizer produces a $455 \mathrm{kHz}+/-8.9 \mathrm{kHz}$ signal. The BFO therefore tunes from 446.1 to 463.9 kHz , in 100 Hz steps. Refer to Figure 3-27, BFO LO Synthesizer Block Diagram, as an aid in understanding the following description. Figure 6-27, BFO LO Synthesizer Schematic Diagram, may be referred to for greater component level detail, if desired. The BFO Synthesizer consists of a VCO, a main programmable divider, an end of cycle detector and a phase detector.

Emitter-coupled oscillator Q1 with its external tank circuit comprises the VCO. Varactor diode CR1 receives a control voltage from the active filter and adjusts the tank circuit's frequency of oscillation to establish lock. The VCO operates from 4.461 to 4.639 MHz . Resistors R8, R9, and R10 form the de bias network, and feedback capacitor C7 sustains oscillation along with tuned circuit C8 and L1. R11 and C9 form a low-pass filter for +15 V isolation, and the VCO 's output is coupled to the next stage by C10.

The VCO output drives the clock inputs of the programmable divider. The divider consists of divide-by-10 counters U1-U4. U1 and U2 are preset with BCD digits 0 to 9 from the BFO switch, A9. U3 is preset with + or - from A9. The programmable divider must produce an output of 1 kHz for any input signal in the range of 4.461 to 4.639 MHz . Therefore, the divide ratio of the programmable counter must be from $4461(4.461 \mathrm{MHz} 1 \mathrm{kHz})$ to $4639(4.639 \cdot \mathrm{MHz} 1 \mathrm{kHz})$. The count outputs of U1-U4 drive the input of the end-of-cycle detector to terminate the count sequence. The end-of-cycle detector, consisting of U5A, U5B, U6A, U6B, U6C, U7A, and U7B terminates the counting of U4, U3, U2, and U1 at 5450 . When this number is detected, a pulse is sent to the phase detector (U9) and the counters are reset.

Assume that counters U4, U3, U2, and U1 are all loaded with 0000. This corresponds to a BFO frequency of 455 kHz , a $V C O$ frequency of 4.55 MHz , and a BFO thumbwheel setting of 0.0 kHz . A ${ }^{n+"}$ thumbwheel setting initiates down counting. Therefore, counting from 0000 down to 5450 results in a divide ratio of 4550. A negative "-" setting enters a 1001 (BCD 9) in U3, making the count start from 0900. With an input of 0900 counting up to 5450 results in the divide ratio of 4550 .


Figure 3-27. BFO Functional Block Diagram

Assume a BFO frequency of 460.4 kHz is needed. This corresponds to a thumb wheel selection of +5.4 kHz , and a VCO frequency of 4.604 MHz . From the thumbwheel selection, a "+" presets U3 with a 0000 ; a " 5 " presets U2 with a 0101 , and a "4" presets Ul with a 0100 . Therefore, counting from 0054 down to 5450 results in a divide ratio of 4604. With a divide ratio of 4604 , the end-of-cycle detector will produce a 1 kHz reset pulse output for an input frequency of 4.604 MHz .

The phase detector, U9A, receives a fixed 1 kHz frequency at its reference input, pin 1 , and a signal from the divider at its variable input, pin 3. These two signals produce an output that characterizes their differences in frequency and phase. The charge pump, U9B receives this pulsed waveform from the phase detector outputs and translates them to fixed positive and negative-going amplitude levels (centered about 1.5 V ).
These levels are filtered and integrated by the loop filter, Q4 and U9C, providing the tuning voltage to lock the VCO at the correct frequency.

The VCO output drives buffer amplifier Q2. Q2 and its surrounding components form a tuned amplifier for the incoming VCO output frequency. This VCO sine-wave frequency is then coupled to a sine-wave to TTL converter, Q3. From here, the digital signal returns as the clock input of the programmable divider, and is divided by 10 in U10 and provided as the BFO output signal.

### 3.4.21 SYNTHESIZER INTERFACE/MEMORY (A6A1) (794275)

The Synthesizer Interface/Memory mounts on the A6 Motherboard (see paragraph 3.3.6). The Synthesizer Interface/Memory interfaces the Digital Control microprocessor with the LO and BFO synthesizers with data latches. Refer to Figure 3-28, Synthesizer Interface/Memory Block Diagram, as an aid in understanding the following description. Figure 6-29, Synthesizer Interface/Memory Schematic Diagram, may be referred to for greater component level detail, if desired. The Synthesizer Interface/Memory consists of the following major circuit areas:
o Microprocessor

- Bi-directional Bus Transceiver
- Address Latch
- Address Decoder
- Memory
o Frequency Registers


### 3.4.21.1 Microprocessor

The microprocessor, U18, is an 8-bit general purpose microprocessor. It contains eight addressable 8-bit general purpose registers and two 16 -bit nonaddressable registers. A multiplexed data bus allows the microprocessor to communicate with external devices. The address is divided between the high order bits address bus A8A15 and the low order address/data bus AD0-AD7. The eight low order address bits are latched into external devices by the ALE signal.


Figure 3-28. Synthesizer Interface/Memory Block Diagram

The microprocessor provides RD, WR and ALE outputs for bus control and RST inputs for interrupts. Clock generator U11 drives the microprocessor at 2 MHz . During power up, U11A and U11F provide a time-delayed reset function which holds the microprocessor from initializing until the power supply circuits have stabilized.

### 3.4.21.2 Bi-Directional Bus Transceiver

Transceiver U4 consists of 16 high speed buffer drivers, eight of which are enabled at a time. The direction of data flow is controlled by the DIR and is connected to the RD line. When RD is low, data flows through U4 to the microprocessor. When RD is high, data flows through U4 from the microprocessor to the bus.

### 3.4.21.3 Address Latch

Address latch U5/U6 are octal flip-flops. Data inputs to U5 and U6 are the low and high order address lines from U18. When ALE is low, indicating a valid address on the bus, the clock inputs to $U 5$ and $U 6$ are strobed. The address bits on the $D$ inputs of $U 5$ and $U 6$ are clocked to the $Q$ outputs. These outputs remain latched onto the address bus until the next ALE cycle.

### 3.4.21.4 Address Decoder

Address decoders U7 and U8 are 3-to-8 octal decoders. When addressed by applying a high input to G1 and a low to inputs G2A and G2B, these decoders provide a logic low output on one of eight Y outputs. U7 is addressed by bits A12-A15 and its Y0-Y4 outputs are enabled for ROM 1, U8-G2B, RAM and ROM 2. U8 is addressed by bits A0-A2, A4 and A5, and its Y0-Y5 outputs are clock strobes used to latch bus data into the frequency registers.

### 3.4.21.5 Memory

Memory consists of RAM, U3, and ROM, U1 and U2. The RAM is a $2 K$ by 8 CMOS integrated circuit. RAM stores data and current receiver status. RAM is enabled by the CE input from decoder U7. When selected, CE goes low, selecting the RAM chip. RAM read and write inputs are connected to the RD and WR outputs from the microprocessor. RD is low when reading data from the RAM to the bus. WR is low when writing data from the bus to the RAM.

The ROM consists of two 8 K by 8 CMOS EPROM's. The ROM contains the operating software for the receiver Digital Control Section. U1 and U2 are selected by CE inputs from decoder U7. The OE inputs are tied to the RD line from the microprocessor. During a ROM read cycle, CE and OE inputs are both pulled low.

### 3.4.21.6 Frequency Registers

Frequency registers U12 through U17 are octal D-type flip-flops. These registers latch bus data to the synthesizer circuits. The clock input of each register is tied to a Y output from U8. When addressed by the microprocessor, one of the U8 Y outputs goes low, clocking its respective frequency register. This causes the data present on the bus to be clocked through the $D$ input of the register to its $Q$ output.

## 3.4 .22 <br> IF INTERFACE (A6A2)

The IF Interface mounts on the I/O Motherboard, A6 (see paragraph 3.3.6). The IF Interface interfaces the Digital Control microprocessor with the IF Demodulator Section to select detection mode, bandwidth and gain. Refer to Figure 3-29, IF Interface Block Diagram, as an aid in understanding the following description. Figure $6-30$, IF Interface Schematic Diagram, may be referred to for greater component level detail, if desired. The IF Interface consists of the following major circuit areas:

- Bus Transceiver
o Address Latch
- Address Decoder
- RF Gain D/A
- A/D Converter
- Mode Latches
- Audio Switching


### 3.4.22.1 Bus Transceiver

Transceiver U20 consists of 16 high speed buffer drivers, eight of which are enabled at a time. The direction of data flow is controlled by the DIR and is connected to the RD line. When RD is low, data flows through U20 to the microprocessor. When RD is high, data flows through U20 from the microprocessor to the bus.

### 3.4.22.2 Address Latch

Address latch U8 is an octal flip-flop. Data inputs to $U 8$ are the low address lines from U18. When ALE is low, indicating a valid address on the bus, the clock inputs to $U 8$ are strobed. The address bits on the $D$ inputs of $U 8$ are clocked to the $Q$ outputs. These outputs remain latched onto the address bus until the next ALE cycle.


Figure 3-29. IF Interface Block Diagram

### 3.4.22.3 <br> Address Decoder

Address decoder U11 is a $3-t o-8$ octal decoder. When addressed by applying a high input to G1 and a low to inputs G2A and G2B, this decoder provides a logic low output on one of eight Y outputs. U11 is addressed by bits A0-A2 and its Y outputs are tied to enable inputs of read only and write only devices on the board.

### 3.4.22.4 RF Gain D/A

D/A converter $U 23$ is used when the receiver is under remote control. An 8 -bit binary coded RF gain word is latched into its inputs when the WR1 input is pulsed low during a WR cycle from the Y3 output of U11. U23 provides a current output which is converted to positive voltage by U23. Each binary input bit corresponds to 0.019 Vdc at the output of U23.

### 3.4.22.5 A/D Converter

A/D converter U25 consists of an eight channel multiplexed analog switch, an 8-bit A/D converter, address decoder and tri-state output buffer. Seven of the eight channel inputs to the multiplexer are connected to receiver signals and are monitored during receiver operation. Channel inputs are selected by a 3-bit binary address on the $A, B$ and $C$ inputs. Converted data is read from the output buffer via the Y4 output of U11 which enables the output buffer of U25.

U25 is a successive approximation converter with an input voltage range of 0 to +5 Vdc . Each output bit from the buffer corresponds to an input of 0.019 Vdc .

### 3.4.22.6 Mode Latches

Three registers (U5, U9, U21) serve as storage devices for control of the IF Demodulator Section. Each register latches the data on its $D$ inputs to the $Q$ outputs on a positive-going transition of its clock pulse. The registers are selected by the Y0-Y4 outputs of U11. U5 controls bandwidth selection, U9 controls gain/detection mode selection and U21 controls local/remote selection.

### 3.4.23 ASYNCHRONOUS I/O (A6A3) (796037)

The Asynchronous I/O mounts on the I/O Motherboard, A6 (see paragraph 3.3.6). The Asynchronous I/O interfaces the Digital Control microprocessor with the IF Demodulator Section to select detection mode, bandwidth and gain. Refer to Figure 3-30, Asynchronous I/O Block Diagram, as an aid in understanding the following description. Figure 6-31, Asynchronous I/O Schematic Diagram, may be referred to for greater component level detail, if desired. The Asynchronous $I / O$ consists of the following major circuit areas:


Figure 3-30. Asynchronous I/O Block Diagram

- UART
- RS-232 Drivers
- Address Latch
o Address Decoder
Switch Latch


### 3.4.23.1 UART

The UART, U1, contains a transmit and a receive section. The receiver converts the incoming RXD serial stream into 8 -bit parallel words and places them on the Digital Control data bus, AD0-AD7. The transmitter converts parallel words on the data bus to a serial TXD data stream. Timing and control of receive and transmit functions is coordinated by the address latch and decoder. The UART is initialized by the RESET line from the CPU. When received data is present in the UART, the UART sets the RxRDY line low to interrupt the CPU. A clock generator, U5, is switch settable, and drives the UART at 16 times the baud rate of the serial data stream.

### 3.4.23.2

## RS-232 Drivers

Drivers U7-U10 convert TTL level signals to bipolar RS-232 levels. U7 interfaces RTS, TXD and DSR signals from U1 to the remote controller. U8 interfaces DTR, CTS and RXD signals from U1 to the remote controller. U9 interfaces DSR, CTS and RXD signals from the remote controller to U1. U10 interfaces RTS, DTR and TXD signals from the remote controller to $U 1$.

### 3.4.23.3 Address Latch

The address latch, U 2 , is an 8 -bit latch which captures and holds an address present on the AD0-AD7 bus. When a valid address is present at the input of the latch, the CPU brings the ALE line momentarily low, transferring the address to the $Q$ outputs of the latch. The Q0 output selects transmit or receive in the UART. Q1-Q7 drive the address and enable inputs to the decoder.

### 3.4.23.4 Address Decoder

The address decoder, $\mathrm{U4}$, is a 3- to 8 -line decoder. Its address bits are driven from the Q1-Q3 outputs of the address latch. Its enable inputs driven from Q4 and Q5 of the latch and the A12 from the address bus. The Y0 output enables the UART, while the Y1 output enables the switch latch.

## Switch Latch

The switch latch, U3, is an 8-bit latch which reads the status of the programming switch, S2. The setting of the 8 switch in S2 is latched through the switch latch by the Y1 decoder output. The switch latch output is placed on the data bus, AD0-AD7, and is read by the CPU.

SERIAL I/O BUFFER (A6A4) (794300-1)
The Serial I/O Buffer mounts on the A6 Motherboard (see paragraph 3.3.6). Refer to Figure 3-31, Serial I/O Buffer Block Diagram, as an aid in understanding the following description. Figure 6-32, Serial I/O Buffer Schematic Diagram, may be referred to for greater component level detail, if desired. The Serial I/O Buffer consists of the following major circuit areas:

- D/A Converter, U6, U7, U8
- Address Decoder, U5
- Sync Serial I/O Buffers, U1-U3
3.4.24.1 D/A Converter, U6, U7, U8

U8 is a fixed voltage regulator producing a fixed +5 Vdc output from the +15 Vdc supply input. The +5 Vdc is buffered by U7A and supplied to D/A reference input at U6-2.

U6 is an 8-bit digital to analog converter. It takes an 8-bit digital input from the address/data bus (equivalent analog range from 0 to 255 ) and converts it to an analog voltage output with a range of 0 to 1.2 ma (full scale). The D/A is enabled from decoder U5 via pin U6-2. U7B converts the current output of U6 to a voltage range of 0 to +5 Vdc. The U7B output is sent to the Frequency Extender as the preselector tuning voltage.

### 3.4.24.2 Address Decoder, U5

U5 is a 3-8 decoder driven by 2 bits on the address/bus. Outputs Y2, Y3 and Y 4 are enabled by the input bits as follows:

INPUT BITS
A0 A1

H L
L H
H H
U5 is not clock enabled. input of U5 are immediately decoded.

OUTPUT BITS

## Y2 Y3 Y4

L H H
H L H
H $\mathrm{H} \quad \mathrm{L}$
Thus, any bits appearing on the A0 and AI


Figure 3-31. Serial I/O Buffer Block Diagram

### 3.4.24.3 <br> Serial Sync I/O Buffers, U1-U3

Buffers U1-U3 are used only when the Sync Serial I/O remote control mode is operational. I/O data signals appear from connector Jl and drive the inputs of each buffer, U1A, U2A and U3A. These are inverted and passed to U1B, U2B and U3B respectively. They are once again inverted and passed on to the remote connector on the rear panel. The buffer outputs are low impedance and can source or sink considerable current over long distance lines.

## 3.4 .25 <br> SYNC SERIAL INPUT/OUTPUT (A6A5)

The Sync Serial I/O mounts on the A6 Motherboard (see paragraph 3.3.6). Refer to Figure 3-32, Sync Serial I/O Block Diagram, as an aid in understanding the following description. Figure 6-23, Sync Serial I/O Schematic Diagram, may be referred to for greater component level detail, if desired. The Asynchronous $1 / O$ consists of the following major circuit areas:

- Address Latch ,U9
- Address Decoders, U7 and U10
- Serial to Parallel Converters, U3-U6


### 3.4.25.1 Address Latch, U9

The address latch is an 8-bit latch which captures and holds an address from the address/data bus while a specific operation is being performed. The latch outputs are used to address the inputs of the address decoders. The microprocessor on A6A1 outputs an address on the bus and follows by bring the ALE line momentarily low. This transfers the address on the bus to the $Q$ outputs of $U 9$.

### 3.4.25.2 Address Decoders, U7 and U10

Decoder U7 is used to select multiplexers U1 and U2. U7 is a $3-$ to-8 line decoder. The input is addressed by the address latch. When a valid address is present at the decoder input, bit A12 on the bus is brought high, activating the addressed decoder output. When U7-1 is addressed high, the U7-Y0 output is low, selecting U1. When U7-2 is addressed high, the U7-Y1 output is low, selecting U2.

### 3.4.25.3 Serial to Parallel Converters, U3 to U6

U3 to U6 form a 64-bit shift register. In typical operation, serial data pulses (DTR from the controller) are clocked into the SR (pin 11) and out of the Q7 (pin 17) terminals of each shift register. When all 64 bits have clocked in, the registers U3-U6 signal the microprocessor via U10 and the address/data bus that they
are full. The 64 bits are then clocked are full. The 64 bits are then clocked through multiplexers U1 and U2 (8 bits at a time) until all 64 bits are transferred to the microprocessor.


Figure 3-32. Sync Serial Input/Output

### 3.4.25.4 Multiplexers U1 and U2

U1 and U2 are three-port multiplexers. . Each port can pass 8 bits to the output port. The ports are selected by two address bits driving the multiplexer. Address 00 selects Port A; address 01 selects Port B; address 10 selects Port C.

Each multiplexer can read, that is transfer from any port to the output, or it can write, that is transfer from the output to any port. The multiplexers are selected by the CS inputs from decoder U7. When not selected by U7, the multiplexer outputs are tri-stated to not interfered with other output ports on the bus.

### 3.4.26 FRONT PANEL SWITCH/ENCODER (MFP-A1) (796013-5)

The Front Panel Switch/Encoder is a P.W. Assembly that mounts two subassemblies: Front Panel Switch Board, MFP-A1A1, and Front Panel Encoder Board, MFP-A1A2. Refer to Figure 3-33, Front Panel Switch/Encoder Block Diagram, Figure 6-34, Front Panel Switch/Encoder Schematic Diagram, Figure 6-35, Front Panel Encoder Board Schematic Diagram, and Figure 6-36, Front Panel Switch Board Schematic Diagram, as aids in understanding the following descriptions.

### 3.4.26.1 Front Panel Encoder Board (MFP-A1A1) (796056-1)

The Front Panel Encoder Board consists of the following major circuit
areas:

- Address Latch, U18
- Address Decoder, U19
- Programmable Keyboard/Display Interface, U1,U2
- Switch Decoders, U11,U12


### 3.4.26.1.1 Address Latch, U18

U18 is an octal flip-flip used as an 8-bit latch. The $D$ inputs are driven from the address/data bus. The microprocessor outputs an address on the bus, followed by bringing ALE low. This transfers the address to the U18 Q outputs.

### 3.4.26.1.2 Address Decoder, U19

U19 is a 3-to-8 line decoder. The address inputs of U19 are driven by the Q outputs of U18 and bit A12. The Y outputs enable the following functions:

```
Y0 -- Tune wheel encoder
Y1 -- Interface U1
Y2 -- Interface U2
Y3 -- Audio Multiplexer Latch U20
Y4 -- Tune Wheel Encoder
```



Figure 3-32. Front Panel Switch/Encoder Block Diagram

## SECTION IV

MAINTENANCE .

### 4.1 GENERAL

This section provides detailed procedures to perform preventive and corrective maintenance on the WJ-8718-19/FE HF Receiver. Preventive maintenance helps prevent malfunctions or breakdowns. Corrective maintenance includes procedures for returning a malfunctioning receiver to operating condition.

### 4.3 MODULE ACCESS

The receiver is a highly compact unit consisting of small printed circuit assemblies, interconnecting cabling and chassis mounted components. Physical access to all receiver assemblies is obtained by removing the top cover. Access to front panel components is obtained by removing the front panel which is secured to the receiver side panels.

### 4.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of visual inspection, cleaning and lubrication. Although the WJ-8718-19/FE HF Receiver is designed for extended operation with little or no routine servicing, optimum long-term performance can only be achieved by a periodic preventive maintenance schedule. Table 4-1 is a recommended schedule for performing preventive procedures.

Table 4-1. Preventive Maintenance Schedule

| PROCEDURE | INTERVAL |
| :--- | :--- |
| Cleaning | $\begin{array}{c}\text { COMMENTS }\end{array}$ |
| Inspection for damage | 60 days |
| Interval variable |  |
| depending on the |  |
| operating environment. |  |$\}$| Interval variable |
| :--- |
| depending on |
| operating environment |
| and equipment use. |

### 4.2.1 VISUAL INSPECTION

A visual inspection of the receiver should be performed every 1200 hours of operation or less. The inspection should be performed thoroughly to uncover existing or potential component malfunctions. At a minimum, the following items should be checked.

1. Inspect the equipment covers and front panel for condition of finish and panel markings.
2. Inspect for dents, punctures, or warped areas.
3. Inspect quarter-turn fasteners and receptacles.
4. Inspect the external surfaces for loose or missing serews or washers.
5. Inspect the receptacles for conditions of pins, contacts, and mountings.
6. Inspect the internal components for signs of deterioration, discoloration, or charring. Check for melted insulation and damaged, cracked, or broken components.
7. Inspect the printed circuit boards for damaged tracks, loose connections, corrosion, or other signs of deterioration.
8. Inspect the PC connectors, interface connectors, and chassis wiring for excessive wear, looseness, misalignment, corrosion, or other signs of deterioration.

### 4.2.2 CLEANING

Complete removal of dust, grease and other contamination is of prime importance in maintaining the reliability and useful life of the receiver.

## CAUTION

Avoid the use of chemical cleaning agents containing benzene, toluene, xylene, acetone, or similar solvents. These chemicals may damage the plastics used in this receiver.

1. Exterior - Dust the cabinet off with a soft cloth. Dust the front panel controls with a small soft-bristled paint brush. Dirt clinging to the cabinet may be removed with a clean, lint-free cloth dampened with a mild detergent and water solution. Avoid using abrasive cleaners. They will scratch the front panel.
2. Interior - Dust in the interior of the unit should be removed before it builds up enough to cause arcing and short circuits during periods of high humidity. D.ust is best removed by dry, low-pressure air. Dirt clinging to surfaces may be removed with a soft-bristled paint brush or a clean, lint-free cloth dampened with a mild detergent and water solution. Use a cotton-tipped applicator for cleaning in narrow spaces and on the circuit boards.
3. Switch Contacts - When maintenance is necessary due to accumulated dirt and dust on the contacts, observe the following precautions: Clean the switch contacts with isopropyl alcohol or a mild detergent solution. Avoid cleaning solutions containing benzene, acetone, or similar solvents.

### 4.2.3 LUBRICATION

The optical encoder assembly shaft requires lubrication every 720 hours of operation to prevent excessive wear. The other rotating assemblies in the receiver are sealed and do not require lubrication. To lubricate the encoder assembly shaft, perform the following steps:

## CAUTION

Excessive lubrication of the encoder shaft may destroy the optical characteristics of the en coder wheel.

1. Place the receiver in a vertical position and remove the encoder knob.
2. Apply one (1) drop of SAE $5 \mathrm{~W}-20 \mathrm{~W}$ oil to the encoder shaft at the retaining ring.
3. Reassemble the encoder assembly knob and rotate the knob several times to distribute the lubricant.

### 4.3 RECEIVER CHECKOUT PROCEDURE

### 4.3.1 GENERAL

The checkout procedure outlined in this paragraph defines the minimum performance standards which ensure adequate receiver functioning all detection modes, gain modes and IF bandwidths. The tests should be used for initial receiver inspection, for preventive maintenance checks, for troubleshooting or to verify receiver performance after repairs have been made.

### 4.3.2 TEST EQUIPMENT REQUIRED

Table 4-2 lists the test equipment required for corrective maintenance of the WJ-8718-19/FE HF Receiver. Equivalent equipment may be used.

Table 4-2. Test Equipment Required

| Instrument Type | Required Characteristics | Recommended Instrument |
| :---: | :---: | :---: |
| Signal Generator | AM, FM, CW, RF output, from -111 dBm to 0 dBm | HP8640B |
| Oscilloscope | de to 50 MHz | HP180C |
| RF Voltmeter | $\begin{aligned} & 1 \mathrm{mV} \text { to } 3.0 \mathrm{~V} ;-50 \mathrm{dBm} \\ & \text { to }+20 \mathrm{dBm} \end{aligned}$ | Boonton 92B |
| Digital Counter | 0 to 500 MHz | HP5303A |
| AC Voltmeter | 1 mV to 300 V , full scale | HP-400E |
| Digital Voltmeter | dc ranges; $1 \%$ or better | Fluke 8100A |
| Dummy load, 600 ohm | 1/2-W dissipation | Two 1200 ohm, $1 / 4-W$ or $1 / 2-W$ resistors in parallel |
| Headphones | Stereo, 600 ohm impedance, or Mono | Telex 325-02 or Telex 820-4 |
| Sweep Generator | 100 kHz to 11.0 MHz | HP8601A |

### 4.3.3 RECEIVER CHECKOUT PROCEDURE GUIDELINES

 procedure:Observe the following guidelines to perform the receiver checkout

1. With the receiver deenergized, connect the test equipment as shown in Figure 4-1. Remove receiver top and bottom covers.
2. Set the receiver input voltage selector to match the available AC line voltage.
3. Energize the receiver and test equipment. Allow 30 minutes for warm-up before proceeding.
4. Set the receiver to $A M$ Detection Mode, 50 kHz Bandwidth and MAN Gain Mode. Rotate the PHONE LEVEL, RF GAIN and LINE AUDIO controls fully CCW.
5. Refer to Table 4-3. Beginning with step 1 , perform each of the checkout procedures.
6. If a malfunction is encountered, refer to the IF INDICATION IS ABNORMAL column. This column refers to a corresponding step in Table 4-4, Troubleshooting Procedures, listing the probable cause and additional tests steps necessary to locate a defective receiver module.
7. Perform any tests steps or corrective action indicated in Table 4-4. Replace any receiver modules indicated in the CORRECTIVE ACTION column.
8. Verify corrective action by repeating the Checkout Procedure in Table 4-3 that identified the malfunction.
9. Proceed to the next Checkout Procedure step in Table 4-3 only after obtaining the required response as indicated in the NORMAL INDICATION column.
10. Defective receiver modules removed in Step 7 may be repaired by referring to the appropriate module checkout and troubleshooting procedure in paragraph 4.3.4.


Figure 4-1. Receiver Checkout Procedure, Test Setup.

Table 4-3. WJ-8718-19/FE HF Receiver Checkout Procedure.

| Step | Test Equipment | Control Settings and Instructions | Normal Indication | IF Indication is Abnormal |
| :---: | :---: | :---: | :---: | :---: |
| 1. Preliminary | Fluke 8100A | a. After power-up in Par. 4.3.3, perform BITE tests (refer to paragraph 2.4.7.2). <br> b. Exercise all front controls and observe that all displays and indicators respond properly. |  | Refer to Table 4-4, Steps 1a, 1 b . <br> Refer to Table 4-4, Steps 1c, 1d, 1 e. |
| 2. Power Supply |  | a. Measure Power Supply Test Points listed below: <br> b. E1. | $\begin{aligned} & +15 \mathrm{Vdc} \\ & +/-0.75 \end{aligned}$ | Refer to Table-4-4, step 2a |
|  |  | c. E2. | $\begin{aligned} & -15 \mathrm{Vdc} \\ & +/-0.75 \end{aligned}$ | Refer to Table 4-4, step 2b |
|  |  | d. E3. | $+10 \mathrm{Vde}$ (minimum) | Refer to Table 4-4, step 2c |
|  |  | e. C8 (feedthru) | $+22 \mathrm{Vdc}$ (minimum) | Refer to Table 4-4, step 2d. |
| 3. IF Gain | HP8640B <br> Boonton 92B | a. Set Sig. Gen. to $15.00500 \mathrm{MHz},-97 \mathrm{dBm}$, Set RF Voltmeter to -10 dBm range. |  |  |
|  |  | b. Adjust receiver RF Gain for -15 dBm on RF Voltmeter. | $-15 \mathrm{dBm}$ | Refer to Table 4-4, step 3a, 3b, 3c |
|  |  | c. Select 50 kHz , <br> $6 \mathrm{kHz}, 3.2 \mathrm{kHz}, 1.0 \mathrm{kHz}$ and 0.3 kHz BW's. Read RF V.M. level at each B.W. | $\begin{aligned} & -15 \mathrm{dBm} \\ & +/-4 \mathrm{dBm} \end{aligned}$ | Refer to Table 4-4, step 3a, 3b, 3c |
|  |  | d. Increase Sig. Gen <br> to 15.00650 MHz . <br> Select USB Mode. <br> Read RF V.M. level. | $\begin{aligned} & -15 \mathrm{dBm} \\ & +/-4 \mathrm{dBm} \end{aligned}$ | Refer to Table 4-4, step 3d |

Table 4-3. WJ-8718-19/FE HF Receiver Checkout Procedure. (Cont'd)

| Step | Test <br> Equipment | Control Settings and Instructions | Normal Indication | IF Indication is Abnormal |
| :---: | :---: | :---: | :---: | :---: |
| 3. IF Gain (Cont'd) <br> 4. Detection Mode | HP8640B <br> HP400-EL <br> HP180C <br> Boonton 92B | e. Decrease Sig. Gen. to 15.00350 MHz . Select LSB Mode. Read RF V.M. level. <br> f. Increase Sig. Gen. to 42.0000 MHz . Select AM mode and 6.0 kHz bandwidth. <br> g. Increase Sig. Gen. to 76.5 MHz . <br> a. Set Sig. Gen. to $15.00500 \mathrm{MHz},-97 \mathrm{dBm}$, $30 \% \mathrm{AM}$ at 400 Hz . Set receiver to AM Mode, 6.0 kHz BW. Set AC V.M.to 50 Vac range. Set HP180C A-input to $20 \mathrm{~V} / \mathrm{cm}, \mathrm{B}$-input to $5 \mathrm{~V} / \mathrm{cm}$, time base to 1 msec . Set RF Gain for -15 dBm on RF V.M. <br> b. Rotate PHONE LEVEL control until 400 Hz is heard in headphones. <br> c. Rotate LINE AUDIO LEVEL control until AC V.M. indicates 0.707 <br> Vrms ( 0 dBm ). <br> d. Depress A-Input switch on oscilloscope and observe Line Audio waveform. <br> e. Turn off Sig. Gen. modulation. Set receiver to CW mode, $6.0 \mathrm{kHz} \mathrm{BW},-0.4 \mathrm{kHz}$ BFO Offset. Monitor Headphone. |  | Refer to Table $4-4$, step 3 e. <br> Refer to Table 4-4, step $3 f$. <br> Refer to Table $4-4$, step 3 g . <br> Refer to Table 4-4, step 4a. <br> Refer to Table $4-4$, step 4 b . <br> Refer to Table 4-4, step 4c. <br> Refer to Table 4-4, step 4d. |

Table 4-3. WJ-8718-19/FE HF Receiver Checkout Procedure. (Cont'd)


Table 4-3. WJ-8718-19/FE HF Receiver Checkout Procedure. (Cont'd)


Table 4-4. WJ-8718-19/FE HF Receiver Troubleshooting Procedures.


Table 4-4. WJ-8718-19/FE HF Receiver Troubleshooting Procedures. (Cont'd)

| Step | Fault | Probable Cause | Additional Test | Corrective Action |
| :---: | :---: | :---: | :---: | :---: |
| (cont) | IF output dead on all bandwidths. | Faulty LO <br> signals | Check 2nd LO at A2J1: 32.20500 MHz at 0 dBm . | Check BCD presets to A5A2. If correct replace A5A2. If no replace A6A1. |
|  |  |  | Check 3rd LO at A4A2-13: 11.155 MHz at -6 dBm . | If incorrect replace A5A1. |
|  |  |  | Check A4A7-47 for 0 Vde. | If correct, replace A4A7, repeat step 3b Table 4-3. If not, check or replace A4 A6. |
|  |  | Faulty A4A2 |  | Replace A4A2. Repeat step 3b, Table 4-3. |
|  |  | Faulty A3 | Cheek A 3 Cl for 0 Vdc. | If correct, replace A3, repeat step 3b Table 4-3. If not, check or replace A4 A6. |
| b. | If output dead on 1 or more BWs. | Faulty Filter Switch A4A1 or A4 A3. | Check BW Select voltages, pins $15,17,19$ or A4A1 and A4A3: +3 Vdc for selected BW. | If correct, replace A4A1 or A4A3, repeat Step 3b, 3c, Table 4-3. If not, check or replace A6A1 then A6A2. |
| c. | IF output level out of limits on 1 or more BWs. | Incorrect Alignment. |  | Perform A4A1 <br> Alignment, Para. <br> 4.3.6.3.2 and A4A7 <br> Alignment, Para. <br> 4.3.6.3.4. |
| d. | Incorrect USB IF output in JSB Mode. | Faulty A4A2 | Check DF Select voltege at A4A2-45: +3 Vdc in USB Mode. | If correct, replace A4A2, repeat step 3d, Table 4-3. If not, check or replace A6A1 then A6A2. |

Table 4-4. WJ-8718-19/FE HF Receiver Troubleshooting Procedures. (Cont'd)

| Step | Fault | Probable Cause | Additional Test | Corrective Action |
| :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & 3 \mathrm{~d} . \\ & \text { ( cont) } \end{aligned}$ <br> e. | Incorrect USB IF output in USB mode. | Faulty A4A3 | Check W1 select at A4A2-15 for +3 Vdc . | Replace A4A2 if OK. If not, then replace A6A1,A6A2. |
|  | Incorrect LSB IF output in LSB Mode. | Digital Control is faulty. |  | Replace A6A2. |
|  | No IF output at 42.00000 MHz | Fault Freq. Extender | Verify RF switch. | Check RF switch for loss. Replace if bad. |
|  |  |  | Check lst LO output at FE-A1A1-J5: $232 \mathrm{MHz} /-2 \mathrm{dBm}$ | Replace FE-A1A1A1 then $\mathrm{FE}-\mathrm{A} 1 \mathrm{~A} 1 \mathrm{~A} 2$ if if not good. |
|  |  |  | Check RF output at FE-A1A1-J3 | Replace FE-A1A1A3 if not good. |
|  |  |  | Check 2nd LO output at FE-A1A2-J2: $189 \mathrm{MHz} /-2 \mathrm{dBm}$ | Replace FE-A1A2A1 if not good. |
|  |  |  | Check IF output at FE-A1A2-3: $29.5 \mathrm{MHz} /+10 \mathrm{~dB}$ gain from input. | Replace FE-A1A2A3 then $\mathrm{FE}-\mathrm{A} 1 \mathrm{~A} 2 \mathrm{~A} 2$ if not good. |
| g . | IF output dead at 76.50000 MHz . |  |  | Replace FE-A1A1A3. |
| 4. $\begin{aligned} & \text { a. } \\ & \\ & \\ & \\ & \text { b. }\end{aligned}$ | No 400 Hz tone in earphone (AM Mode) | Faulty A4A10 | Check signal at A4A10-51: 0.7 Vrms at 400 Hz . | If incorrect, replace A4A7. If correct, perform next test. |
|  |  |  | Check signal at A4A10-55: 0.7 Vrms at 400 Hz . | If incorrect replace A4A10. If correct, check Headphone Amp. A10A2U1. |
|  | No Line Audio Output (AM Mode) | Faulty A4A10 | Check signal at A4A1013 with R1 at max CW: 3 Vrms at 400 Hz | If incorrect, replace A4A10. If correct, replace C11. |

Table 4-4. WJ-8718-19/FE HF Receiver Troubleshooting Procedures. (Cont'd)

| Step | Fault | Probable Cause | Additional Test | Corrective Action |
| :---: | :---: | :---: | :---: | :---: |
| c. | Line Audio Output distorted. <br> (AM Mode) | Faulty A4A10 |  | Replace A4A10. If problem not corrected, check +24 V at J1-5. |
|  | No 400 Hz tone in earphone (CW Mode) | Faulty A4A9 | Check Audio Signal at A4A9-57. 0.7 Vrms at 400 Hz . | If correct, replace A4A10. If incorrect, perform next test. |
|  |  |  | Check BFO Signal at A4A9-17: 454.600 kHz at 40 mV . | If incorrect, check or replace A5A3. If incorrect, perform next test. |
|  |  |  | Check CW/SSB Select voltage, A4A9-43: <br> 3 Vde in CW mode. | If incorrect, check or replace A6A1 then A6A2. If correct, replace A4A9. |
| e. | $\begin{aligned} & \text { No } 400 \mathrm{~Hz} \\ & \text { tone in } \\ & \text { earphone } \\ & \text { (USB) } \end{aligned}$ | Faulty A6A2 | Check USB Select Voltages at A4A2-45 (DF), A4A9-43 (SSB): +3 Vde in selected modes. | If incorrect, check or replace A6A2. If correct, perform next test. |
|  |  | Faulty A5A3 | Check BFO Signal at A4A9-17: 455.000 kHz at 40 mV . | If incorrect, check or replace A5A3. If correct, check A4 A9. |
| f. | No 400 Hz tone in earphone, (LSB Mode) | Faulty A6A2 |  | Check or replace A6A1 then A6A2. |
| g. | No Phone Audio Output. | Faulty A4A10 |  | Check or replace A4 A10. |
| 5. a . | Low SNR. | Faulty RF Filter |  | Check or replace RF Filter. |
|  |  | quilty A3 | Check 1st and 2nd LO signals for adequate levels: <br> 1st LO: +20 dBm <br> end LO: 0 dBm | If incorrect, replace A5A1 or A5A2 If correct, replace A3 and repeat Step 5, Table 4-3. |

Table 4-4. WJ-8718-19/FE BF Receiver Troubleshooting Procedures. (Cont'd)


### 4.3.4 <br> MODULE TROUBLESHOOTING PROCEDURES

Module troubleshooting procedures consist of checkout, fault-isolation and repair information necessary to restore a malfunctioning module to normal operation. Troubleshooting information provided in this paragraphs consists of the following categories:

1. Module checkout procedures to verify module fault symptoms.
2. Fault isolation tables to help isolate defective components on the modules. Semiconductor voltage tables are also provided to help locate defective transistors and integrated circuits.
3. A Parts Replacement Guide, Paragraph 4.3.5, to assist in repairing a defective module.

In addition to using the information provided in this paragraph, reference to the Circuit Description in Section III and Schematic Diagrams in Section VI is essential for efficient module troubleshooting.

### 4.3.4.1 Procedure Guidelines

To properly check-out and troubleshoot a defective module, the following guide lines should be utilized:

1. Allow the test equipment a 30 minute warm-up before any check out.
2. Refer to the Testing and Troubleshooting paragraph for the desired module. Configure the receiver and test equipment as stated in the Checkout Procedure for the desired module.
3. Perform the Checkout Procedure in the sequence given. If any desired result is not obtained, refer to the Fault Isolation Table for the module to locate the defective component.
4. Refer to the Parts Replacement Guide, Paragraph 4.3.5, to assist in replacing any components found to be defective. Following component replacement, re-perform the Module Checkout Procedure. If the module still fails, additional troubleshooting using the Circuit Descriptions in Section III and Schematic Diagrams in Section VI is necessary.

### 4.3.4.2 RF Filter Testing And Troubleshooting

RF Filter Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator, an RF Voltmeter, and a Digital Voltmeter (see Table 4-1) are required to perform the tests outlined below.

### 4.3.4.2.1 RF Filter Checkout Procedure

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to paragraph 4.3.4.2.2 for fault isolation.

1. Disconnect A2P1 from A3A1J1 on the Input Converter.
2. Connect an RF Voltmeter and 50 ohm adapter to A2P1.
3. Connect the output of a Signal Generator to A2J1 on the rear panel of the receiver.
4. Set the RF Voltmeter to the 0 dBm range.
5. Set the Signal Generator output frequency to 1.0 MHz and output level to 0 dBm .
6. The RF Voltmeter should indicate a level between 0 dBm and -1.0 dBm .
7. Tune the Signal Generator to 10 MHz and 20 MHz , and 30 MHz successively, maintaining the output level at 0 dBm for each frequency. The filter output level should not be less than -3.0 dBm for each frequency.
8. Disconnect the test equipment from the receiver.
9. Reconnect A2P1 to A3A1J1.

### 4.3.4.2.2 RF Filter Fault Isolation

1. Remove the filter from the receiver and remove the filter's protective cover.
2. Check all capacitors and the two Zener diodes for leakage to ground.
3. Check all inductors for continuity.
4. Field realignment of the filter is not practical.

### 4.3.4.4

## 1 st LO Synthesizer, FE-A1A1A1, (370689) Testing and Troubleshooting

1st LO Synthesizer Testing and Traubleshooting includes a checkout procedure and fault isolation information. An oscilloscope (see Table 4-1) is required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-5 for fault isolationn

1. Deenergize the receiver.
2. Obtain access to module FE-A1A1A1. Connect the oscilloscope to terminal E10n
3. Set the receiver front panel controls as follows:
a. Gain Mode- Manual
b. RF Gain - Maximum Clockwise
4. Energize the receiver and tune to 42.0000 MHz .
5. The oscilloscope should display a level of +3 Vdc .
6. IF the signal in step 5 is incorrect, check the Test Points given in Table 4-5 with an oscilloscope and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-4, 1st LO Synthesizer Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
7. When the 1st LO Synthesizer has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-5. 1st LO Synthesizer Fault Isolation Chart

| Test Point | Normal Signal | Key Components | Comments |
| :---: | :---: | :---: | :---: |
| E12 | 1 MHz clock, TTL |  | Time Base |
| E11 | Pulse train when tuning with wheel | A6A1 | Check or replace A6A1 |
| U1-3 | Approx. 5.73 MHz | U3, U4 | Prescaler |
| U1-16,17 | Short, 5 V spikes | U1 | Synthesizer |
| E5 | +3 Vde | U2 | Tuning Voltage |
| E2 | 0 Vde | U5-U7 |  |
| E3 | +5 Vde | " |  |
| E4 | 0 Vdc | " |  |
| E2 | +5 Vde | " | Tune receiver to 76.5 MHz |
| E3 | 0 Vde | " |  |
| E4 | +5 Vde | " |  |

### 4.3.4.5 VCO, FE-A1A1A2, (370690) Testing and Troubleshooting

VCO Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Frequency Counter and an RF Voltmeter (see Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-6 for fault isolation.

1. Deenergize the receiver.
2. Disconnect W 2 P 2 from $\mathrm{FE}-\mathrm{A} 2 \mathrm{~J} 2$. Connect P 2 to the frequency counter.
3. Set the receiver front panel controls as follows:
a. Gain Mode- Manual
b. RF Gain - Maximum Clockwise
4. Energize the receiver and tune to 30.00000 MHz .
5. The frequency counter should indicate 190.0000 MHz .
6. Tune the receiver in 10 MHz increments to 90.0000 MHz . The frequency counter indication should increment in 10 MHz steps to 260.0000 MHz .
7. Remove the frequency counter and connect the RF voltmeter. The RF Voltmeter should display a level of2 dBm .
8. If the signal in steps $5-7$ is incorrect, check the Test Points given in Table 4-6 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-5, VCO Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
9. When the VCO has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-6. VCO Fault Isolation Chart

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| E15 | +3 Vdc | Synthesizer | Receiver tuned to 42 or 76.5 <br> MHz. |
| Q1-D | 100 mV sine | Q1 | VCO |
| E11 | 100 mV sine | Q2,Q3 | Dig. Control <br> E12,E13,E14 <br> 0 or +5 Vdc |
|  |  | Refer to paragraph 3.4 .2 and <br> verify the TP's while tuning <br> from $30-100 \mathrm{MHz}$. |  |

Preselector Testing and Troubleshooting includes a checkout procedure and fault isolation information．A Signal Generator and an RF Voltmeter（see Table 4－1）are required to perform the tests outlined below．

Perform the following procedure in the sequence given．If any specified result is not obtained，refer to Table 4－7 for fault isolation．

1．Deenergize the receiver．
2．Connect the signal generator to the rear panel RF input jack．Set the generator for -20 dBm output at 42.0000 MHz ．

3．Energize the receiver．Set the receiver front panel controls as follows：
a．Gain Mode－Manual
b．RF Gain－Maximum Clockwise
c．Freq．－ 42.0000 MHz
4．Obtain access to module FE－A1A1A3．Connect the RF Voltmeter to terminal E1 using a high impedance probe．

7．The RF Voltmeter should display a level $>-18 \mathrm{dBm}$ ．
8．Change the receiver and the generator to 76.5 MHz ． The RF Voltmeter should display a level $>-18 \mathrm{dBm}$ ．

9．IF the signal in steps 7 and 8 is incorrect，check the Test Points given in Table 4－6 with an RF Voltmeter and high impedance probe．When a faulty signal is encountered，replace the key components indicated and repeat the Checkout Procedure．Figure 6－6，Preselector Schematic Diagram should be referred to if additional signal tracing／fault isolation is necessary．

9．When the Preselector has been repaired and is operating satisfactorily，deenergize the receiver and disconnect test equipment，if no further tests are to be performed．

Table 4-7. Preselector Fault Isolation Chart

| Test Point | Normal Signal | Key Components | Comments |
| :---: | :---: | :---: | :---: |
| E5 | +5 Vde | Dig. Control | Tune revr to 42 MHz |
| E3 | $+3 \mathrm{~V}$ | " " | Tune voltage |
| U3-3 | 0 Vdc | U3 |  |
| CR10 anode | 200 Mv | CR2 | Tune gen to 42 MHz |
| CR15 anode | 100 Mv | CR10-CR16 | Check all diodes with ohmmeter. |
| E1 | 100 mV | CR18 |  |
| E4 | +5 | Dig. Control | Tune revr to 76.5 MHz |
| E3 | +3 Vde | " " | Tune voltage |
| U3-5 | 0 Vde | U3 |  |
| CR3 anode | 200 mV | CR1 | Tune gen to 76.5 MHz |
| CR8 anode | 100 mV | CR3-CR9 | Check all diodes with ohmmeter. |
| E1 | 100 Mv | CR17 |  |

### 4.3.4.7 2nd LO Synthesizer, FE-A1A2A1, (794270) Testing and Troubleshooting

2nd LO Synthesizer Testing and Troubleshooting includes a checkout procedure and fault isolation information. An oscilloscope, frequency counter and an RF Voltmeter (see Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-8 for fault isolation.

1. Deenergize the receiver.
2. Connect the frequency counter to FE-A1A2-J5.
3. Energize the receiver. Set the receiver front panel controls as follows:
a. Gain Mode- Manual
b. RF Gain - Maximum Clockwise
4. The frequency counter should indicate 189.0000 MHz .
5. Disconnect the frequency counter and connect the RF voltmeter. The voltmeter should indicate -2 dBm .
6. If the signal in step 4 and 5 is incorrect, check the Test Points given in Table 4-7 with an RF Voltmeter and oscilloscope. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-8, 2nd LO Synthesizer Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
7. When the 2nd LO Synthesizer has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-8. 2nd LO Synthesizer Fault Isolation Chart

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| U1-3 | +9 Vdc | U4 | DC Supply |
| E1 | 1 MHz clock, TTL |  | Time Base |
| U1-1 | Approx. 4.66 MHz | U2 | Prescaler |
| U1-7,8 | Short, 5 V spikes | U1 | Synthesizer |
| U3-6 | +3 Vdc | U2 | Tuning Voltage |
| Q1-D | 100 mV sine | Q1,CR1 | VCO |
| E3 | 100 mV sine | Q2 |  |

### 4.3.4.8 2nd Converter, FE-A1A2A2, (270907) Testing and Troubleshooting

2nd Converter Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and an RF Voltmeter (see Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-9 for fault isolation.

1. Deenergize the receiver.
2. Connect the signal generator to FE-A1A2-J2. Connect the RF voltmeter to FE-A1A2-J3.
3. Set the generator to -20 dBm at 42.0000 MHz .
4. Energize the receiver. Set the receiver front panel controls as follows:

| a. | Gain Mode | - | Manual |
| :--- | :--- | :--- | :--- |
| b. | RF Gain | - | Maximum Clockwise |
| c. | Freq. | - | 42.0000 MHz |

6. The RF Voltmeter should display a level $>0 \mathrm{dBm}$.
7. IF the signal in step 6 is incorrect, check the Test Points given in Table 4-9 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-9, 2nd Converter Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
8. When the 2nd Converter has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-9. 2nd Converter Fault Isolation Chart

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| E3 | -6 dBm | 1st Converter |  |
| U2-4 | +15 dBm | U2 | 2nd LO Signal |
| U3-1 | -15 dBm | U3 | 2nd IF Signal |
| E1 | 0 dBm | U1 |  |

### 4.3.4.9 1st Converter, FE-A1A2A3, (270901) Testing and Troubleshooting

1st Converter Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and an RF Voltmeter (see Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-10 for fault isolation.

1. Deenergize the receiver.
2. Connect the signal generator to FE-A1A2-J2. Connect the RF voltmeter to FE-A1A2-J3.
3. Set the generator to -20 dBm at 42.0000 MHz .
4. Energize the receiver. Set the receiver front panel controls as follows:
a. Gain Mode- Manual
b. RF Gain - Maximum Clockwise
c. Freq. - 42.0000 MHz
5. The RF Voltmeter should display a level of 0 dBm .
6. IF the signal in step 6 is incorrect, check the Test Points given in Table 4-10 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-10, 1st Converter Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
7. When the 1 st Converter has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-10. 1st Converter Fault Isolation Chart

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| E1 | -20 dBm | Input cabling |  |
| U1-4 | -8 dBm | FL1, U1 |  |
| E6 | 0 Vdc | Digital control | AGC voltage |
| U6-6 | +7 Vdc | U6 |  |
| U2-4 | -10 dBm | U 2 | 1st LO Signal |
| U3-2 | -15 dBm | U3 | 1st IF Signal |
| U5-4 | -15 dBm | U5 |  |
| E3 | -6 dBm | U4 |  |

### 4.3.4.10

## RF Input Switch, FE-A2, (794276) Testing and Troubleshooting

RF Input Switch Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and an RF Voltmeter (see Table 4-1) are required to perform the tests outlined below. Perform the following procedure in the sequence given. Refer to Figure 6-11, RF Input Switch Schematic Diagram as an aid in performing the procedure.

1. Deenergize the receiver.
2. Connect the signal generator to FE-A2-J1.
3. Set the generator to 0 dBm at 42.0000 MHz .
4. Energize the receiver. Set the receiver front panel controls as follows:
$\begin{array}{lll}\text { a. Gain Mode- } & \text { Manual } \\ \text { b. RF Gain - } & \text { Maximum Clockwise } \\ \text { c. Freq. } & \text { - } & 42.0000 \mathrm{MHz}\end{array}$
5. Use the oscilloscope to verify that terminal E3 is low.
6. Use the $R F$ voltmeter to verify a 0 dBm output signal at $\mathrm{FE}-\mathrm{A} 2 \mathrm{~J} 2$. If no signal is found, RF switch A1U1 is defective.
7. Use the $R F$ voltmeter to verify a 0 dBm output signal at FE-A2J5. If no signal is found, RF switch A1U2 or cable FE-W10 is defective.
8. Change the receiver frequency to 76.5 MHz .
9. Use the RF voltmeter to verify a 0 dBm output signal at FE-A2J3. If no signal is found, RF switch A1U1 is defective.
10. Connect the generator to FE-A2J6.
11. Use the RF voltmeter to verify a 0 dBm output signal at FE-A2J5. If no signal is found, RF switch A1U2 is defective.
12. When the RF Switch has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

### 4.3.4.11 1 MHz Filter, FE-A3, (794327) Testing and Troubleshooting

1 MHz Filter Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator, an RF Voltmeter, and a Digital Voltmeter (see Table 4-1) are required to perform the tests outlined below. Perform the procedure below in the sequence given. Refer to Figure 6-12, 1 MHz Filter Schematic Diagram, as an aid in performing the sequence.

1. Disconnect P2 from A1J2 on the Frequency Extender.
2. Connect an RF Voltmeter and 50 ohm adapter to P 2 .
3. Connect the output of a Signal Generator to J 1 on the 1 MHz filter.
4. Set the RF Voltmeter to the 0 dBm range.
5. Set the Signal Generator output frequency to 1.0 MHz and output level to 0 dBm .
6. The RF Voltmeter should indicate a level between 0 dBm and -3.0 dBm .
7. If the signal in step is incorrect, check all capacitors and the two Zener diodes for leakage to ground. Check all inductors for continuity. Field realignment of the filter is not practical.
8. When the 1 MHz Filter has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed. Reconnect all cables removed during testing.
4.3.4.12

Input Converter, A3, (791592) Testing And Troubleshooting
Input Converter Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and an RF Voltmeter (see Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-11 for fault isolation.

1. Deenergize the receiver.
2. Disconnect A2P1 from A3A1J1 and P28 from A3A2J2. Terminate A3A2J2 with 50 ohms.
3. Set the receiver front panel controls as follows:
a. Gain Mode- Manual
b. RF Gain - Maximum Clockwise
4. Connect the RF Voltmeter to connector A3A2J2 using a short coaxial cable (a "TEE" connector should be used to maintain 50 ohm termination).
5. Connect the Signal Generator to connector A3A1J1 using a short coaxial cable. Set the Generator output frequency to 15.00500 MHz and output level to -7 dBm .
6. Energize the receiver and tune to 15.00500 MHz .
7. The RF Voltmeter should display a level of 350 mV .
8. IF the signal in step is incorrect, check the Test Points given in Table 4-11 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repest the Checkout Procedure. Figure 6-13, Input Converter Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
9. When the Input Converter has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-11. Input Converter Fault Isolation Chart

| Test Point | Normal | Signal | Key Components | Comments |
| :---: | :---: | :---: | :---: | :---: |
| A1J2 | 1.8 V at | 57.91 MHz | Cheek 1st LO | 1st LO Signal |
| U1-8 | 74 mV at | 42.905 MHz | U1 | 1st IF |
| FL1-IN | 200 mV at | 42.905 MHz | U2 |  |
| FL1-OUT | 80 mV at | 42.905 MHz | FL1 |  |
| A2Q2-S | 40 mV at | 42.905 MHz | Input Matching Network |  |
| A2Q2-D | 500 mV at | 42.905 MHz | A2Q2, T1, C16, CR2 |  |
| A 2 J 1 | 260 mV at | 32.205 MHz | Check 2nd LO | 2nd LO Signal |
| A2Q6-B | 500 mV at | 32.205 MHz | A2Q5 |  |
| A2Q6-C | 1.3 V at | 32.205 MHz | A2Q6 |  |
| A201-3 | 130 mV at | 10.7 MHz | A2U1 | 2nd IF |
| A2Q3-C | 1.3 V at | 10.7 MHz | Q3, Q4, T2 |  |
| A252 | 350 mV at | 10.7 MHz | FL1 |  |

### 4.3.4.13 <br> 10.7 MHz Filter, A4A1, (791594) Switch Testing and Troubleshooting

10.7 MHz Filter Switch Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and an RF Voltmeter (Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-12 for fault isolation.

1. Deenergize the receiver.
2. Disconnect connector P19 from A4XA1.
3. Place PC board A4A1 in an extender.
4. Select the 3.2 kHz BW position.
5. Connect the RF Voltmeter to A4XAl pin 57 using a short coaxial cable with clip leads on one end.
6. Connect the Signal Generator to A4XA1 pin 13 using a short coaxial cable with clip leads on one end. Set the Generator output frequency to 10.7 MHz and output level to -27 dBm .
7. Energize the receiver. The RF Voltmeter should display a level of 50 mV .
8. Select the 6 kHz BW and then the 50 kHz BW positions. The RF Voltmeter should display a level of 50 mV in both BW position.
9. Check the Test Points given in Table 4-12 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure $6-15,10.7 \mathrm{MHz}$ Filter Switch Schematic Diagram, should be referred to if additional signal tracing/fault isolation is necessary.
10. When the 10.7 MHz Filter Switch has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-12. $\quad 10.7 \mathrm{MHz}$ Filter Switch Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| C1/L1 | 33 mV at 10.7 MHz | $\mathrm{C} 1, \mathrm{~L} 1$ | All BW positions |
| Q1-C | 110 mV at 10.7 MHz | Q1 | Select 3.2 kHz |
| BW |  |  |  |
| FL1-OUT | 65 mV at 10.7 MHz | FL1 |  |
| Q4-B | 12 mV at 10.7 MHz | R26, Q4 |  |
| Q2-C | 120 mV at 10.7 MHz | Q2 |  |
| FL2-OUT | 65 mV at 10.7 MHz | FL2 |  |
| Q5-B | 10 mV at 10.7 MHz | R28, Q5 |  |
| Q3-C | 90 mV | at 10.7 MHz | Q3 |
| Q6-B | 10 mV at 10.7 MHz | R30, Q6 |  |
| A1-57 | 50 mV at 10.7 MHz | Q4, Q5, Q6, U1, U2 | All BW positions |

4.3.4.14
$10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter, A4A2, (794254) Testing and Troubleshooting
$10 \mathrm{n} 7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and an RF Voltmeter (Table 4-1) are required to perform the tests outlined below.

Perform the following in the sequence given. If any specified result is not obtained, refer to Table 4-13 for fault isolation.

1. Deenergize the receiver.
2. Place PC board A4A2 on an extender. Remove PC board A4A1.
3. Connect the RF Voltmeter to A4XA2 pin 19 using a short coaxial cable with clip leads on one end. Connect cable shield to the IF Motherboard ground plane.
4. Connect the Signal Generator RF output to A4XA2 pin 57 using a short coaxial cable with clip leads on one end. Connect cable shield to the IF Motherboard ground plane. Set the Generator output frequency to 10.7 MHz and output level to -27 dBm .
5. Energize the receiver. The Oscilloscope should display a level of 22 mV .
6. Check the Test Points given in Table 4-13 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-16, $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
7. When the Converter has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-13. $\quad 10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter Fault Isolation Chart.

| Test Point | Normal Signal |  | Key Components |
| :--- | :--- | :--- | :--- |
| A4A2-13 | 150 mV at 11.155 MHz | Check 3rd LO | Comments |
| Q1-C | 2.5 V at 11.155 MHz | Q1 |  |
| U1-2 | 350 mV at 11.155 MHz | L2, C6, C7, C8 |  |
| U1-4 | 5 mV at 455 kHz | U1 |  |
| A4A2-19 | 22 mV at 455 kHz | L3, L4, C9, C10, C11 |  |

### 4.3.4.15 $\quad 455 \mathrm{kHz}$ Filter Switch, A4A3, (791595) Testing and Troubleshooting

455 kHz Filter Switch Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and an RF Voltmeter (Table 4-1) are required to perform the following tests.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-14 for fault isolation.

1. Deenergize the receiver.
2. Remove PC board A4A2. Place PC board A4A3 on an extender.
3. Select the 3.2 kHz BW position.
4. Connect the RF Voltmeter input to A4XA3 pin 57 using a short coaxial cable with clip leads on one end. Connect cable shield to the IF Motherboard ground plane.
5. Connect the Signal Generator $R F$ output to A4XA3 pin 13 using a short coaxial cable with clip leads on one end. Terminate the generator with a 50 ohm load. Connect cable shield to the IF Motherboard ground plane. Set the Generator output frequency to 455 kHz and output level to -27 dBm .
6. Energize the receiver. The RF Voltmeter should display a level of 25 mV .
7. Select the 1.0 kHz BW and then the $0.3 \mathrm{kHz} B W$ positions. The RF Voltmeter should display no less than 20 mV in both BW positions.
8. Check the Test Points given in Table 4-14 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-17, 455 kHz Filter Switch Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
9. When the 455 kHz Filter Switch has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-14. 455 kHz Filter Switch Fault Isolation Chart.

| Test Point | Normal Signal |  | Key Components | Comments |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Q5-C | 23 mV | at | 455 kHz | Q5 | Select 3.2 kHz BW |
| Q3-C | 27 mV | at | 455 kHz | Q3 | Select 1.0 kHz BW |
| Q4-B | 17 mV | at | 455 kHz | FL2, Q4 |  |
| Q1-C | 19 mV | at | 455 kHz | Q1 | Select 0.3 kHz BW |
| Q2-B | 17 mV | at | 455 kHz | F11, Q2 |  |
| A4A3-57 | 25 mV | at | 455 kHz | Q2, Q4, Q6 | 3.2 kHz BW |
| A4A3-57 | 20 mV | at | 455 kHz | Q2, Q4, Q6 | $1.0,0.3 \mathrm{kHz} \mathrm{BW}$ |

AGC Amplifier, A4A6, (796175) Testing and Troubleshooting
AGC Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and a Digital Voltmeter (Table 4-1) are required to perform the tests outlined belown

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-15 for fault isolation.

1. Deenergize the receiver.
2. Remove PC boards A4A3, and A4A10.
3. Set the receiver Gain Mode to Fast $A G C$ and Meter switch to Line Audio.
4. Connect the Digital Voltmeter input to A4XA6 pin 47 using a short cable with clip leads on one end. Connect the common lead to the IF Motherboard ground plane. Set the Digital Voltmeter to the 20 Vdc range.
5. Connect the Signal Generator output to A4XA7 pin 57 using a short coaxial cable with clip leads on one end Connect cable shield to the IF Motherboard ground plane. Set the Generator output frequency to 455 kHz and output level to -40 dBm .
6. Energize the receiver. The Digital Voltmeter should indicate -3.5 Vdc.
7. If the signal in step 5 is incorrect, check the test points given in Table 4-15 with an oscilloscope and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-18, AGC Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
8. Select the receiver MAN Gain Mode. Adjust the RF Gain control until the Digital Voltmeter indicates the same level indicated in step 7.
9. Select the Fast AGC Mode.
10. Connect the Digital Voltmeter clip lead to A4XA6 pin 19. The Voltmeter should indicate +0.7 Vden
11. Connect the Digital Voltmeter clip lead to A4XA6 pin 41. The Voltmeter should indicate -3.0 Vdc .
12. If the signal in step 5 is incorrect, check the test points given in Table 4-15 with an oscilloscope and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-18, AGC Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
13. When the AGC has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-15. AGC Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| A4A6-51 | +3.2 Vdc | Check A4A7 | AGC Mode |
| Q1-E | +2.7 Vdc | Q1 |  |
| U1-1 | +2.7 Vdc | U1 |  |
| Q2-C | +0.13 Vdc | CR9, Q2, Q6 |  |
| U2-7 | -6.6 Vdc | U2 |  |
| U1-14 | -3.5 Vdc | U1 |  |
| U2-10 | -0.06 Vdc | Q5 |  |
| U2-8 | -0.32 Vdc | U 2 |  |
| U2-1 | +1.07 Vdc | U 2 |  |

### 4.3.4.17

455 kHz Amp ./AM Detector, A4A7, (726002) Testing and Troubleshooting
455 kHz AmplifieroAM Detector Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator, an RF Voltmeter and Oscilloscope (Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-16 for fault isolation.

1. Deenergize the receiver.
2. Remove PC board A4A3. Place PC board A4A7 on an extender.
3. Connect the RF Voltmeter Input to A4XA7 pin 17 using [a short coaxial cable with clip leads on one end. Connect cable shield to the IF Motherboard ground plane.
4. Connect the Signal Generator RF output to A4XA7 pin 57 using a short coaxial cable with clip leads on one end. Connect cable shield to the IF Motherboard ground plane. Terminate the generator with a 50 ohm load. Set the Generator output frequency to 455 kHz and output level to -47 dBm .
5. Energize the receiver. The Oscilloscope should display a level of 90 mV .
6. Move the RF Voltmeter clip lead to A4XA7 pin 13. The Oscilloscope should display a level of 20 mV .
7. Turn on the Signal Generator AM Modulation and set it for $50 \%$ modulation at 400 Hz .
8. Connect the Oscilloscope vertical input to A4XA7 pin 51 using a coaxial with clip leads on one end. The Oscilloscope should display a level of 1.0 V p-p at 400 Hz superimposed on a de level of +3.8 Vdc .
9. If the signal in steps 4 and 8 is incorrect, check the test points given in Table 4-16 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-19, 455 kHz Amplifier/AM Detector Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
10. When the 455 kHz Amplifier/AM Detector has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-16. Amplifier/AM Detector Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :---: | :---: | :---: | :---: |
| Q1-1 | 12 mV at 455 kHz | Q1, CR1, L1 | No Modulation |
| Q2-1 | 19 mV at 455 kHz | Q2, CR2, L2, R7 |  |
| Q3-E | 20 mV at 455 kHz | Q3, L3 |  |
| Q4-C | 300 mV at 455 kHz | Q4, T1 |  |
| A4 A7-17 | 90 mV at 455 kHz | T1 |  |
| Q5-B | 1 V at 455 kHz | Q5 |  |
| CR3/L6 | 3.1 V at 455 kHz | Q5, L5 |  |
| Q6-B | 4.6 Vdc/1 Vpp - 400 Hz | CR3, Q6 | Turn on Modulation. Use oscilloscope. |
| A4A7-51 | $3.8 \mathrm{Vdc} / 1 \mathrm{Vpp}-400 \mathrm{~Hz}$ | Q6, L7 | Turn on Modulation. Use oscilloscope. |

### 4.3.4.18 <br> FM/CW/SSB Detector, A4A9, (791599) Testing and Troubleshooting

FM/CW/SSB Detector Testing and Troubleshooting includes a CW/SSB Detector Checkout procedure, an FM Detector Checkout Procedure and fault isolation information. A Signal Generator, RF Voltmeter and an Oscilloscope (Table 4-1) are required to perform the tests outlined below.

### 4.3.4.18.1 CW/SSB Detector Checkout Procedure

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-17 for fault isolation.

1. Deenergize the receiver.
2. Remove PC board A4A7. Place PC board A4A9 on an extender.
3. Connect the Oscilloscope Vertical Input to A4XA9 pin 57 using a short coaxial cable with clip leads on one end. Connect cable shield to the IF Motherboard ground plane.
4. Connect the Signal Generator RF output to A4XA9 pin 13 using a short coaxial cable with clip leads on one end. Connect cable shield to the ground plane. Terminate the generator with a 50 ohm load. Set the Generator output frequency to 455.4 MHz and output level to -33 dBm .
5. Energize the receiver and select the USB Mode. The Oscilloscope should display a level of 0.5 V p-p at 400 Hz . The waveform should be a clean sine save.
6. If the signal in step 5 is incorrect, check the test points given in Table 4-17 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-20, FM/CW/SSB Detector Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
7. When the Input Converter has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

### 4.3.4.18.2 FM Detector Checkout Procedure

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-17 for fault isolation.

1. Deenergize the receiver.
2. Remove PC board A4A7. Place PC board A4A9 on an extender.
3. Connect the Oscilloscope Vertical Input to A4XA9 pin 57 using a short coaxial cable with clip leads on one end. Connect cable shield to the IF Motherboard ground planen
4. Connect the Signal Generator RF output to A4XA9 pin 13 using a short coaxial cable with clip leads on one end. Connect cable shield to the IF Motherboard ground plane. Terminate the generator with a 50 ohm load. Set the generator output frequency to 455 kHz and output level to -33 dBm . Set the Generator for FM Modulation at 400 Hz and 4.8 kHz deviation.
5. Energize the receiver and select the FM Mode. The Oscilloscope should display a level of $>1 \mathrm{~V}$ p-p at 400 Hz . The waveform should be a clean sine wave.
6. If the signal in step 5 is incorrect, check the test points given in Table 4-20 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-20, FM/CW/SSB Detector. Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
7. When the FM/CW/SSB Detector has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-17. FM/CW/SSB Detector Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :---: | :---: | :---: | :---: |
| U2-8 | 200 mV at 455 kHz | Cheek BFO | Select CW Mode |
| U3-5 | 4 Vpp at 400 Hz | U2, Q3, Q4 | Select CW Mode Use oscilloscope |
| A4 A9-57 | 0.5 Vpp at 400 Hz | U3 | Select CW Mode Use oscilloscope |
| U1-5 | 2 V at 455 kHz | U1, Q1, Q2 | Select FM Mode |
| U3-3 | 4 Vpp at 400 Hz | CR1, CR2, T1 | Turn on FM Modulation. Use Oscilloscope. |
| A4 A9-57 | 1 Vpp at 400 Hz | U3 | Turn on FM Modulation. Use Oscilloscope. |

### 4.3.4.19

## Audio Amplifier, A4A10, (7459) Testing and Troubleshooting

Audio Amplifier Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Signal Generator and an Oscilloscope (Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-18 for fault isolationn

1. Deenergize the receiver.
2. Remove PC boards A4A6, A4A7, and A4A9. Place PC board A4A10 on an extender.
3. Set the receiver Line Audio Level control to Maximum Clockwise and the Phone Level control to mid-range.
4. Connect the Oscilloscope Vertical Input to A4XA10 pin 55 using a short coaxial cable with clip leads on one end. Connect shield to IF Motherboard ground plane.
5. Connect the Signal Generator AM output to A4XA10 pin 51 using a short coaxial cable with clip leads on one end. Connect cable shield to IF Motherboard ground plane. Set the Signal Generator Modulation Frequency to 400 Hz , set Audio Output Level to 0.2 V rms and set AM switeh to INT.
6. Energize the receiver and select the AM Mode. The Oscilloscope should display a level of 0.3 V p-p at 400 Hz . The waveform should be a clean sine wave.
7. Use the Oscilloscope lead to probe A4XA10 pin 13 and A4XA10 pin 11. The Oscilloscope should display a level of $15 \mathrm{~V} \mathrm{p-p}$ at 400 Hz on each pin.
8. Connect the Oscilloscope clip lead to A4XA10 pin 41. The Oscilloscope should indicate a level of -10.8 Vdc .
9. Move the Oscilloscope clip lead to A4XA10 pin 19. The Oscilloscope should show a level of $7 \mathrm{~V} p-\mathrm{p}$ at 400 Hz .
10. If the signals in steps $6-9$ are incorrect, check the test points given in Table 4-18 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-21, Audio Amplifier Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
11. When the Audio Amplifier has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-18. Audio Amplifier Fault Isolation Chart.

| Test Point | Normal Signal |  | Key Components | Comments |
| :--- | :--- | :--- | :--- | :--- |
| Q1-D | 0.45 Vpp at 400 Hz | Q1, U1, CR1 | Select AV1 Mode |  |
| U1-14 | 0.3 Vpp at 400 Hz | U1 |  |  |
| C8, R18 | 300 mVpp at | 400 Hz | Line Audio Control |  |
| U2-2, 13 | 15 Vpp | at | 400 Hz | U2 |
| R7, R8 | 20 mVpp | at | 400 Hz | Phone Level Control |

### 4.3.4.20

1st LO Synthesizer, A5A1, (p/o 791630) Testing and Troubleshooting
1st LO Synthesizer Testing and Troubleshooting includes a checkout procedure and fault isolation. A Frequency Counter, wideband Oscilloscope and RF Voltmeter (Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Tables $4-19,4-20$ and $4-21$ for fault isolation.

1. Deenergize the receiver.
2. Disconnect connector from A1J2.
3. Connect the Frequency Counter to AlJl.
4. Energize the receiver and tune it to 00.00000 MHz . The Frequency Counter should indicate 42.91 MHz .
5. Rotate the tuning knob counterclockwise and tune receiver to 29.99999 MHz . The Frequency Counter should indicate 72.90 MHz .
6. Disconnect the Frequency Counter and connect the RF Volt meter and 50 ohm Probe to A1Jl. The Voltmeter should indicate $+20 \mathrm{dBm}+/-2 \mathrm{dBm}$.
7. If the signals in steps $4-6$ are correct, you may deenergize the receiver and remove all test equipment unless further testing is desired.
8. If the signals in steps $4-6$ are incorrect, the following tables may be used as fault isolating aids for troubleshooting and repairing the 1st LO.
9. VCO Band Select Circuitry - Table 4-19 below checks for proper operation of U13, diodes CR8 through CR10, and Q1 through Q3, while dialing different frequencies on the front panel.

Table 4-19. VCO Band Select Code

| TUNED FREQUENCY |  |  |  | BAND SELECT OUTPUT (Vdc) |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | E3 | E2 | E1 |  |
| 0.00 | - | 3.99 MHz | +15 | +15 |  |
| 4.00 | - | 7.99 MHz | +15 | +15 |  |
| 8.00 | - | 11.99 MHz | +15 | -12 |  |
| 12.00 | - | 15.99 MHz | +15 | -12 |  |
| 16.00 | - | 19.99 MHz | -12 | +15 |  |
| 20.00 | - | 23.99 MHz | -12 | +15 |  |
| 24.00 | - | 27.99 MHz | -12 | -12 |  |
| 28.00 | - | 29.99 MHz | -12 | -12 |  |

10. Divider Section - With a tuned frequency of 00.00000 MHz , or a 1 st LO input to J 1 of 171.64 MHz , the following frequencies in Table 4-20 should be found at the corresponding IC pins using a Digital Counter.

Table 4-20. 1st LO Frequency Chart

| IC | PIN | FREQUENCY | IC | PIN | FREQUENCY |
| :--- | :--- | :--- | :--- | :---: | :---: |
| U1 | 7 | 17 MHz | U9 | 5 | 1.68 MHz |
| U1 | 9 | 3.4 MHz | U9 | 9 | 80 kHz |
| U1 | 10 | 40 kHz | U9 | 2 | 40 kHz |
| U2 | 12 | 3.4 MHz | U10 | 3 | 840 kHz |
| U3 | 7 | 40 kHz | U10 | 7 | 200 kHz |
| U3 | 9 | 40 kHz | U11 | 6 | 40 kHz |
| U5 | 3 | 40 kHz | U11 | 7 | 40 kHz |
| U8 | 7 | 200 kHz | U12 | 5 | 40 kHz |
| U24 | 1 | 40 kHz | U12 | 9 | 40 kHz |

12. Phase Detector U5 - Check for 40 kHz signal at input pin 3 of U5. If signal is not present, troubleshoot Time Base Circuits. Check for 40 kHz signal at pin 1 of U5. If not present, troubleshoot 1 st LO counter circuits. With a tuned frequency of 00.00000 MHz , the Phase Detector output at U7-6 should be approximately -8 Vde. If not good, check U5, U6, U7, CR1 and CR2.
13. 1st LO VCO - The 1st LO VCO is located on the 1st and 3rd LO PC board. Table 4-21 below checks for proper operation of the VCO and buffer amplifiers. Set the receiver to a tuned frequency of 29.99999 MHz and use an oscilloscope with low capacitance probe to check the tests points indicated. Diodes CR1-CR3 should be checked with an ohmmeter for continuity.

Table 4-21. 1st LO/VCO Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| Q1-2 | $1 \mathrm{Vpp} @ 291.60 \mathrm{MHz}$ | Q1, CR4, CR1-CR3 | CR1-CR3 conduct |
| Q2-C | 2 Vpp | Q2 |  |
| Q3-C | 10 Vpp | Q3 | Divide by 4 |
| U1-3 | $5 \mathrm{Vpp} @ 72.90 \mathrm{MHz}$ | U1, Q4 | 1st LO output |
| E1 | 6 Vpp | Q5, Q7 |  |

14. When the 1st LO has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.
4.3.4.21

2nd LO Synthesizer, A5A2, (791601) Testing and Troubleshooting
2nd LO Synthesizer Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Frequency Counter, wideband Oscilloscope, and $R F$ Voltmeter (Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Tables $4-22,4-23$ and $4-24$ for fault isolation.

1. Deenergize the receiver.
2. Disconnect connector P13 from A5A2XB15/16.
3. Connect the Frequency Counter to TP13.
4. Energize the receiver and tune to 00.00000 MHz . The Frequency Counter should indicate 32.21 MHz .
5. Tune the receiver to 00.00999 MHz . The Frequency Counter should indicate 32.20001 MHz .
6. Disconnect the Frequency Counter and connect the RF Volt meter and 50 ohm probe to W4P4. The Voltmeter should indicate $0 \mathrm{dBm}+/-2 \mathrm{dBm}$,
7. If the signal in step 5 is incorrect, check the test points given in Tables 4-22 through 4-24 with an RF Voltmeter and oscilloscope. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-26, 2nd LO Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
8. When the 2nd LO has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-22. 32 MHz Loop Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| Q5-B | 2 Vpp | Q5, CR3 | VCO circuit |
| Q1-E | 2 Vpp | Q1 |  |
| U1-1 | 1 MHz | Time Base | Reference Signal |
| U1-3 | 1 MHz | U2, U3 |  |
| U3-3 | 32 MHz | VCO circuits | Divide by 32 |
| U1-8 | +3 Vdc | U1 | Phase Detector |

Table 4-23. Programmable Loop Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
|  | $316-15$ | 3 Vpp @ 210 MHz | Q1, CR5 |
| U14-11 | 3 V peak @ 2.09 MHz | U14, U15 | VCO circuit |
| U12-3 | 3 V peak @ 10 kHz | U7-U11, U20 | Counter output |
| U12-1 | 3 V peak @ 10 kHz | Time Base |  |
| U12-8 | +6.2 Vdc | U12 | Phase Detector |

Table 4-24. Output Loop Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| Q6-B | $2 \mathrm{Vpp} @ 32 \mathrm{MHz}$ <br> Q3-1 <br> $\mathrm{U} 6-3$ <br> U6-8 | $5 \mathrm{Vpp@} 32 \mathrm{MHz}$ <br> $5 \mathrm{Vpp@} 200 \mathrm{kHz}$ <br> +3 Vdc | Q6, CR4 <br> Q3 |

### 4.3.4.22 3rd LO Synthesizer, p/o A5A1, ( $p / 0$ 791630) Testing and Troubleshooting

3rd LO Synthesizer Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Frequency Counter, wideband Oscilloscope, and RF Voltmeter (Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-25 for fault isolation.

1. Deenergize the receiver.
2. Disconnect connector W6P10 from J7.
3. Connect the Frequency Counter to W6P10.
4. Energize the receiver. The Frequency Counter should indicate 11.155 MHz .
5. Disconnect the Frequency Counter and connect the RF Volt meter and 50 ohm probe to W6P10. The Voltmeter should indicate $-6 \mathrm{dBm}+/-2 \mathrm{dBm}$.
6. If the signal in step 5 is incorrect, check the test points given in Table 4-25 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-25, 1st \& 3rd LO Synthesizer Schematic Diagram should ve referred to if additional signal tracing/fault isolation is necessary.
7. When the 3rd LO has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-25. 3rd LO Fault Isolation Chart.

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| Q8-E | 2 Vpp @ 11.155 MHz | Q8, CR7 | VCO Circuit |
| U21-12 | 3 V peak | Q9, Q10 |  |
| U21-11 | 3 V peak @ 50 kHz | Time Base |  |
| U22-11 | 3 V peak @ 5 kHz | U21, Time Base | Divide by 2 |
| U22-8 | +3 Vdc | U21, U22 |  |

### 4.3.4.23 BFO Synthesizer, A5A3, (791576) Testing and Troubleshooting

BFO Synthesizer Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Frequency Counter and wideband Oscilloscope (Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-26 for fault isolation.

1. Deenergize the receiver.
2. Disconnect connector A4Wl3P18 from A4XA8-17/19.
3. Connect the Frequency Counter to W13P18.
4. Energize the receiver and select CW Mode. Set the BFO of fset to +0.0 kHz . The Frequency Counter should read 455.000 kHz .
5. Set the BFO Offset first to +8.0 kHz and then to -8.0 kHz . The Frequency Counter should read 463.999 kHz and 446.999 kHz respectively.
6. Disconnect the Frequency Counter and reconnect A4W13P18 to A4XA8-17/19.
7. Connect the Oscilloscope input to A4TP15 using a shielded cable with clip leads on one end. Connect cable shield to the IF Motherboard ground plane. The Oscilloscope should display a level of $>120 \mathrm{mV}$ p-p at
446.999 kHz .
8. If the signal in step 5 is incorrect, check the test points given in Table 4-26 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-27, BFO Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
9. When the BFO has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-26. BFO Fault Isolation Chart.
BFO OFFSET $=\phi$

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
|  | +3 Vdc |  |  |
| U9-8 | 2 Vpp @ 4.55 MHz | Q9 | Phase Detector |
| Q1-C | 3 V peak @ 4.55 MHz | Q2, Q3 | VCO Circuit |
| U10-1 | 3 V peak @ 455 kHz | U1 |  |
| U1-13 | 3 V peak @ 46 kHz | U2 |  |
| U2-13 | 3 V peak @ 5 kHz | U3 |  |
| U3-13 | 3 V peak @ 1 kHz | U4 |  |
| U9-3 | 3 V peak @ 1 kHz | U5-U9 |  |
| U9-1 | 3 V peak @ 1 kHz | Time Base |  |

4.3.4.24 Time Base, p/o A5A1, ( $\mathrm{p} / \mathrm{o} 791630$ ) Testing and Troubleshooting

Time Base Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Frequency Counter and a wideband Oscilloscope (Table 4-1) are required to perform the tests outlined below.

Perform the following procedure in the sequence given. If any specified result is not obtained, refer to Table 4-27 for Fault Isolation.

1. Deenergize the receiver.
2. Connect the Frequency Counter input to A5XA1 pin A9 using a short coaxial cable with clip leads on one end. Connect cable shield to Motherboard ground plane.
3. Energize the receiver. The Frequency Counter should read $1.000000 \mathrm{MHz}+/-3 \mathrm{~Hz}$.
4. Move the Frequency Counter clip lead to A5XA1 pin A47. The Frequency Counter should read 10.000 kHz $+/-1 \mathrm{~Hz}$.
5. Move the Frequency Counter clip lead to A5XA1 pin A53. The Frequency Counter should read $1.000 \mathrm{kHz}+/-$ 1 Hz .
6. Move the Frequency Counter clip lead to test point A5A1A2 pin E6. The Frequency counter should read $40.000 \mathrm{kHz}+/-1 \mathrm{~Hz}$.
7. If the signal in step 5 is incorrect, check the test points given in Table 4-27 with an RF Voltmeter and high impedance probe. When a faulty signal is encountered, replace the key components indicated and repeat the Checkout Procedure. Figure 6-25, 1st \& 3rd LO Synthesizer Schematic Diagram should be referred to if additional signal tracing/fault isolation is necessary.
8. When the Time Base has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Table 4-27. Time Base Frequency Chart

| IC | PIN | FREQUENCY | IC | PIN | FREQUENCY |
| :--- | :--- | ---: | ---: | :--- | :--- |
| U15 | 5 | 1 MHz | U 18 | 12 | 10 kHz |
| U15 | 6 | 1 MHz | U 19 | 5 | 250 kHz |
| U15 | 8 | 2 MHz | U 19 | 12 | 50 kHz |
| U15 | 12 | 200 kHz | U 20 | 5 | 5 kHz |
| U17 | 12 | 40 kHz | U 20 | 12 | 1 kHz |
| U18 | 5 | 500 kHz | U 23 | 8 | 1 MHz |
| U18 | 8 | 1 MHz | U 23 | 11 | 1 MHz |

Synthesizer Interface/Memory Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Digital Voltmeter and a wideband Oscilloscope (Table 4-1) are required to perform the tests outlined below.

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Deenergize the receiver.
2. Remove the receiver top cover.
3. Place module A6A1 on an extender card.
4. Set the receiver to the following parameters:
a. Tuned Frequency -- $\quad 15.00500 \mathrm{MHz}$
b. Bandwidth -- 50 kHz
c. Gain Mode -- AGC FAST
d. Detection Mode -- AM
e. Tuning Rate -- 10 Hz
5. Using the oscilloscope, verify the external input signals to the microcontroller, U18, using the following table.

Table 4-28. Microcontroller Input Signal Check

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| U18-X1 | Clock signal, <br> 2.078 MHz | U11, U18 |  |
| U18-36 | +5 Vdc | U11,R6,C9 | Powerup Reset |
| U18-35 | +5 Vdc | R7 |  |
| U18-7 | 637 kHz | U11,C10,R10 |  |

6. Using the oscilloscope, verify microcontroller Ul data bus and control signal activity using the following table.

Table 4-29. Microcontroller Bus Activity Check

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :---: | :---: |
| U18 pin 21-28 | Pulse train, <br> less than 1 us <br> prr. | U18, U4, U5,U6, U7, <br> U8 pin 12-19 | Pulse train, <br> less than 1 us <br> prr. |
| U18-31,32 | Pulse train, <br> less than 1 us <br> prr. <br> Uulse train, <br> 0.4 us prr | $"$ |  |

7. Using the oscilloscope, verify $I / O$ signal activity using the following table.

Table 4-30. CPU I/O Signal Check

| Test Point | Normal Signal | Key Components | Comments |
| :---: | :---: | :---: | :---: |
| U6 pin 2-19 | Pulse train, less than 1 us prr. | U6 | Address Latch |
| U4 pin 2-9 | Pulse train, less than 1 us prr. | U4 | Data/Address Latch |
| $\text { U7 pin } \begin{array}{r} 11,13, \\ 14,15 \end{array}$ | Square wave, 1 ms prr. | U7 | Address Decoder |
| U8 pin 10-15 | Square wave, 1 ms prr. | U8,U9 | Address Decoder |

8. Using the oscilloscope, verify the RF Frequency and BFO Frequency outputs using the following table. If any faulty signals are encountered, replace the integrated circuit associated with that signal as indicated in the table.

Table 4-31. Synthesizer Interface Frequency Outputs

| Component | Pin No. | Level |
| :---: | :---: | :---: |
| U13 | 16 | L |
|  | 19 | H |
| U14 | 2 | L |
|  | 5 | H |
|  | 6 | L |
|  | 9 | H |
|  | 12 | L |
|  | 15 | L |
|  | 16 | L |
|  | 19 | L |
| U15 | 2 | L |
|  | 5 | L |
|  | 6 | L |
|  | 9 | L |
|  | 12 | L |
|  | 15 | H |
|  | 16 | L |
|  | 19 | H |
| U16 | 2 | L |
|  | 5 | L |
|  | 6 | L |
|  | 9 | L |
|  | 12 | L |
|  | 15 | L |
|  | 16 | L |
|  | 19 | L |
| U12 | 2 | L |
|  | 5 | L |
|  | 6 | L |
|  | 9 | L |
|  | 12 | L |
|  | 15 | L |
|  | 16 | L |
|  | 19 | L |

9. When the Synthesizer Interface has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

### 4.3.4.26 IF Interface, A6A2, (796032) Testing and Troubleshooting

IF Interface Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Digital Voltmeter and a wideband Oscilloscope (Table 4-1) are required to perform the tests outlined below.

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Deenergize the receiver.
2. Remove the receiver top cover.
3. Place module A6A2 on an extender card.
4. Set the receiver to the following parameters:
a. Tuned Frequency -- $\quad 15.00500 \mathrm{MHz}$
b. Bandwidth -- 50 kHz
c. Gain Mode -- AGC FAST
d. Detection Mode -- AM
e. Tuning Rate --10 Hz
5. Using the oscilloscope, verify control signal/data activity indicated in the following table.

Table 4-32. IF Interface Control Signal/Data Activity Check

| Test Point | Normal Signal | Key Components | Comments |
| :---: | :---: | :---: | :---: |
| XUl Pins 12-19 | Pulse train, less than $l$ us prr. | $\begin{aligned} & \text { U9,U14 } \\ & 794275 \text { PCB } \end{aligned}$ | Addr/Data Bus |
| $\begin{array}{r} \mathrm{U} 13 \begin{array}{l} \mathrm{Q} 0-\mathrm{Q} 2, \\ \mathrm{Q} 4, \mathrm{Q} 5 \end{array} \end{array}$ | Square wave, 1 msec PW. | U13,44 | Address Latch |
| U7 Y0-Y6 | Pulse train, less than 1 msec PW . | U4, U21, U13 | Address Decoder |
| U17-10 | $+5 \mathrm{Vdc}$ | U19, U17 | RF Gain Voltage RF Gain Control at max cw. |

6．Using the Digital Voltmeter or oscilloscope，the IF Interface select outputs using the following table．The levels on the pins are to be observed when the detection mode or bandwidth is selected as indicated in the table．If a faulty signal is encountered，replace the IC associated with that function as indicated in the table．

Table 4－33．IF Interface Voltage Table

| Pin No | I．C． | AM | CW | FM | USB | LSB |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A6A2－B5 | U11，U15 | LO | LO | LO | LO | HI |  |
| A6A2－B3 | U11，U15 | LO | LO | LO | HI | LO |  |
| A6A2－B1 | U11，U15 | LO | LO | LO | LO | LO |  |
| A6A2－B18 | Ull | LO | HI | LO | HI | HI |  |
| A6A2－B16 | Ull | LO | LO | HI | LO | LO |  |
| A6A2－B48 | Ull | HI | LO | LO | LO | LO |  |
| A6A2－B60 | U10 | HI | LO | HI | LO | LO |  |
| Pin no | I．C． | 50 kHz | 6 kHz | 3． 2 kHz | 1.0 kHz | 0.3 kHz | USB／LSB |
| A6A2－B49 | U10 | HI | HI | HI | LO | LO | LO |
| A6A2－B51 | U10，U15 | HI | LO | LO | HI | HI | HI |
| A6A2－B53 | U10，U15 | LO | HI | LO | LO | LO | LO |
| A6A2－B55 | U10，U15 | LO | LO | HI | LO | LO | LO |
| A6A2－B47 | U10，U15 | LO | LO | LO | HI | LO | LO |
| A6A2－B45 | U10，U15 | LO | LO | LO | LO | HI | LO |

7．When the IF Interface has been repaired and is operating satisfactorily，deenergize the receiver and disconnect test equipment，if no further tests are to be performed．

Asynchronous I/O, A6A3, (796037) Testing and Troubleshooting
Asynchronous I/O Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Digital Voltmeter and a wideband Oscilloscope (Table 4-1) are required to perform the tests outlined below.

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Deenergize the receiver.
2. Remove the receiver top cover.
3. Place module A6A3 on an extender card.
4. Connect a remote controller to rear panel REM IN connector, J14.
5. Set the receiver to the following parameters:
a. Tuned Frequency -- 15.00500 MHz
b. Bandwidth -- 50 kHz
c. Gain Mode -- AGC FAST
d. Detection Mode -- AM
e. Tuning Rate -- Disable
6. Using the oscilloscope, verify the UART and $I / O$ signal/data activity using Tables 4-34 and 4-35. Activity should be checked in conjunction with sending commands from a remote terminal.

Table 4-34. UART Control Signal/Data Activity Check

| Test Point | Normal Signal | Key Component | Comments |
| :--- | :--- | :--- | :--- |
| U1-3 | Square wave <br> pulse train | U9 | Send command from <br> terminal to revr |
| U1-19 | High pulse when <br> data is sent | U9 | " |
| Square wave <br> pulse train | U1 | Present when revr <br> transmits to terminal |  |

Table 4-35. I/O Signal Activity Check

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| U2-Q1 to Q7 | Pulse train <br> 1 msec PW | U7 | Address Latch |
| U4-Y0,Y1 | Pulse train <br> 1 msec PW <br> 5 MHz Clock | U4,Y1 | Address Decoder |

7. When the Asynchronous $I / O$ has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

### 4.3.4.28 <br> Serial I/O Buffer, A6A4, (794300) Testing and Troubleshooting

Serial I/O Buffer Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Digital Voltmeter and a wideband Oscilloscope (Table 4-1) are required to perform the tests outlined below.

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered,
replace the key components indicated in the table.

1. Deenergize the receiver.
2. Remove the receiver top cover.
3. Place module A6A4 on an extender card.
4. Set the receiver to the following parameters:
a. Tuned Frequency -- 42.0000 MHz
b. Bandwidth -- 50 kHz
c. Gain Mode -- AGC FAST
d. Detection Mode -- AM
e. Tuning Rate -- Fast
5. Using the oscilloscope, verify the data signals using Table 4-36. Activity should be checked in conjunction with rotating the tuning wheel slightly from side to side.

Table 4-36. Data Signal Activity Check

| Test Point | Normal Signal | Key Components | Comments |
| :--- | :--- | :--- | :--- |
| $\mathrm{U} 5-5$ | Sharp, negative | U 5 | Read/Write from A6Al |
| $\mathrm{U} 5-6$ | $"$ | $"$ | $"$ |
| $\mathrm{U} 5-7$ | $"$ | $"$ | $"$ |
| $\mathrm{U} 6-8$ | -10 Vdc | $\mathrm{UB}, \mathrm{U7}$ |  |
| $\mathrm{U} 7-7$ | +7 Vdc | $\mathrm{U}, \mathrm{U} 7$ | A/C reference |
| $\mathrm{J} 2-4,5$ | Clock pulse | $\mathrm{U4}$ | Tuning Voltage |
| $\mathrm{J} 2-2$ | High | $\mathrm{U4}$ | Band Select |

7. When the Serial I/O buffer has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

### 4.2.4.29

Sync Serial I/O, A6A5, (794255) Testing and Troubleshooting
Sync Serial I/O Testing and Troubleshooting includes a checkout procedure and fault isolation information. A Digital Voltmeter and a wideband Oscilloscope (Table 4-1) are required to perform the tests outlined below.

The testing and troubleshooting information in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given. When a faulty signal is encountered, replace the key components indicated in the table.

1. Deenergize the receiver.
2. Remove the receiver top cover.
3. Place module A6A5 on an extender card.
4. Connect a remote controller to rear panel REM connector, J14.
5. Set the receiver to the following parameters:
a. Tuned Frequency -- $\quad 15.00500 \mathrm{MHz}$
b. Bandwidth -- 50 kHz
c. Gain Niode -- AGC FAST
d. Detection Mode -- AiM
e. Tuning Rate -- Disable
f. LCL/REM -- REM
6. Connect the receiver to a remote control unit such as the WJ-9195C. Place the receiver in remote mode and verify data transfer from the controller to the receiver.
7. Using the oscilloscope, verify the signal/data activity using Table 4-37. Activity should be checked when sending commands from a remote terminal.

Table 4-37. Signal/Data Activity Check

| Test Point | Normal Signal | Key Component | Comments |
| :---: | :---: | :---: | :---: |
| $\begin{gathered} \mathrm{J} 1-3,4,5 \\ 9,11 \end{gathered}$ | Rapidly changing logic levels | Remote Controller | Ensure that controller is is working properly. |
| J1-15 | Clock pulse | " " | " |
| Pin 17 on U3-U6 | Changing logic | U3-U6 |  |
| U9-11 | Clock pulse | U8 |  |
| U9-Q0 to Q5 | Sharp, negative going pulses | U9 | Data latch output |
| Pin 6 of U1, U2 | Negative going pulses | U7, U8, U12 | Address decoder |
| U10-7,9 | Negative going pulses | U8, U11, U10 | Address decoder |
| PA, PB, PC inputs of U1, U2 | Rapidly changing logic levels | U3-U6 |  |

7. When the Sync Serial I/O has been repaired and is operating satisfactorily, deenergize the receiver and disconnect test equipment, if no further tests are to be performed.

Front Panel Encoder Bd., MF P-A1A1, (796056) Testing and Troubleshooting
Front Panel Encoder Board Testing and Troubleshooting includes a checkout procedure and fault isolation information. An Oscilloscope (Table 4-1) are required to perform the tests outlined below.

The testing and troubleshooting information in this paragraph is keyed to following guidelines used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given.

1. Deenergize the receiver. Select any detection mode.
2. Remove the front panel and gently pull it out several inches from the receiver main chassis, being careful not to place any strain on the interconnecting cables.
3. Access and execute the BITE program as described in Section II.
4. If a single switch does not respond to BITE, check the switch for continuity and replace if bad.
5. If all switches and displays appear defective, check the clock inputs to pin 3 of U1 and U2 of the Front Panel Encode board. Replace U13 if not present.
6. If all group 1 switches and LEDs are defective, replace U1 and any associated chips. If all group 2 switches and LEDs are defective, replace U2 and any associated chips.
7. If the problem is associated with a particular row or column, replace chips associated with the row or column.
8. If all LEDs in Group 1 are defective, replace U3 on the Encode Board. If all LED's in Group 2 are defective, replace U7 on the Encode Board.
9. Check the $\overline{R D}, \overline{W R}$ and RESET inputs to $U 1$ and $U 2$. If defective, replace U19, U18 and U15.
10. If the tuning wheel does not increment the display, replace U17 and U21.
11. When the Encoder/Switch Board has been repaired and is operating satisfactorily, deenergize the receiver and remove all test equipment, unless further testing is desired.

### 4.3.4.31 Front Panel Audio Circuits, ( $\mathrm{p} / \mathrm{o}$ 796013) Testing and Troubleshooting

Front Panel Interconnect Testing and Troubleshooting includes a checkout procedure and fault isolation information. An Oscilloscope (Table 4-1) and Signal Generator are required to perform the tests outlined below.

The testing and troubleshooting information in this paragraph is keyed to the following testing procedure used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedure in the sequence given.

1. Deenergize the receiver. Remove PCB A4A7.
2. Remove the front panel and gently pull it out several inches from the receiver main chassis, being careful not to place any strain on the interconnecting cables.
3. Connect the Oscilloscope Vertical input to connector J41 using a short coaxial cable with clip leads on one end. Connect cable shield to ground. Plug in headset or a test speaker (optional).
4. Connect the Signal Generator AM Output to terminal A1-B57 using a short coaxial cable with clip leads on one end. Connect cable shield to terminal ground. Set the Signal Generator Modulation Frequency to 400 Hz , set Audio Output Level to 70 mV .
5. Energize the receiver. Select any detection mode and rotate the Phone Level control fully clockwise. The Oscilloscope should display a level of $>20 \mathrm{~V} p-\mathrm{p}$. The waveform should be a clean sine wave.
6. Move the Oscilloscope input lead to connector J4-2. The Oscilloscope should display a level of $>20 \mathrm{~V}$ p-p. The waveform should be a clean sine wave.
7. If the signals are defective, replace $U 1$, then $R 7$.
8. Deenergize the receiver and disconnect test equipment.

### 4.3.5 PARTS REPLACEMENT GUIDELINES

This paragraph provides techniques to assist the Technician in replacing components on PC boards.

## WARNING

To prevent electrical shock or damage to the receiver, always disconnect the receiver from the ac power source before soldering or replacing components.

### 4.3.5.1 Soldering Techniques

When removing components from a printed circuit board for inspection or replacement, be especially careful not to damage the track. The soldering iron power should be no larger than 40 W , and a solder sipper or wicking procedure should be employed when removing solder. Non-corrosive soldering flux should be used when removing solder by wicking. In returning components to the board, make sure that holes are clear and that leads do not catch the edge of the track and lift it from the board. A good grade of rosin core $60 / 40$ solder should be used. Heat no longer than is necessary to achieve a good joint. A heat sink should be used where possible.

### 4.3.5.2

Component Replacement
Guidelines for replacing the various kinds of components are as follows.

1. When soldering or unsoldering diodes or resistors, solder quickly to allow as little heat conduction as possible. When wiring permits, use a heat sink between the soldering iron and the part.
2. When soldering or unsoldering transistors, use a low wattage iron and a heat sink. Solder as quickly as possible. The use of a circular soldering tip to heat all three or four joints simultaneously is recommended.
3. When soldering or unsoldering glass or ceramic capacitors, use a heat sink between the capacitor and the iron. Excessive heat will crack the capacitor body.
4. When any electronic part is removed, note the position of the part and its leads, and replace it the same way.

### 4.3.5.3 Realignment

Replacement of semiconductors or tuned circuit components may affect the alignment of the PC board being repaired. Realignment may be necessary to return .he PC board to normal operation.

## 4.3 .6

## ADJUSTMENT/ALIGNMENT PROCEDURES

### 4.3.6.1

## General

The following Adjustment and Alignment Procedures should not be performed on a routine basis, but instead, should be used as aids in troubleshooting and post-repair testing. Before alignment is attempted, the technician should first perform the relevant procedures to determine which module needs alignment.

### 4.3.6.2 Synthesizer Alignment

4.3.6.2.1 1st LO Synthesizer, A5A1, (791630) Alignment

The only alignment for the 1st LO Synthesizer is the 1st LO VCO (A5A1A1). The VCO is a very sensitive circuit should only be adjusted when a definite alignment is needed.

1. Mount the 1 st and 3 rd $L O$ on an extender card and remove the VCO front plate to gain access to alignment components.
2. Connect a Digital Voltmeter to module pin B1.
3. Refer to Table 4-38. Tune receiver to the middle of band 0 . Adjust the components indicated until the voltage at Bl is within stated limits as the receiver is tuned throughout the range of band 0 . The voltage at B1 should be verified with the VCO front plate in place.
4. Repeat step 3 for bands 1 through 7.
5. 1st LO frequency band can be verified by connecting a counter at test point A5A1A1-P2.

Table 4-38. VCO Alignment Parameters

| VCO BAND |  | 1ST LO FREQ | PIN B1 VOLTAGE(DC) |  | COMPONENT |  |
| :--- | ---: | :--- | :--- | :--- | :--- | :--- |
| 0 | $(0-3.99)$ | $42.91-46.90$ | -8.5 | to | 6.0 | C6*, L1 |
| 1 | $(4-7.99)$ | $46.91-50.90$ | -7.5 | to | 4.1 | L2 |
| 2 | $(8-11.99)$ | $50.91-54.90$ | -7.2 | to | 2.8 | L3 |
| 3 | $(12-15.99)$ | $54.91-58.90$ | -5.3 | to | 3.9 | L2, L3 |
| 4 (16-19.99) | $58.91-62.90$ | -6.6 | to | 2.7 | L4 |  |
| 5 (20-23.99) | $62.91-66.90$ | -6.0 | to | 2.2 | L4, L2 |  |
| $6(24-27.99)$ | $66.91-70.90$ | -6.2 | to | 0.4 | L3, L4 |  |
| 7 | $(28-29.99)$ | $70.91-72.90$ | -5.7 | to | -3.0 | L4, L3, L2 |

4.3.6.2.2 2nd LO Synthesizer, A5A2, (791601) Alignment

The 2nd LO Synthesizer procedure consists of a 32 MHz Loop Alignment, a Programmable Loop Alignment, and an Output Loop Alignment. Perform the procedure in the given sequence.

## CAUTION

For optimum results, the 2nd LO Synthesizer Alignment should be performed in an ambient temperature of $+25^{\circ} \mathrm{C}+/-50 \mathrm{C}$.

1. Preliminary Setup
a. Remove the top protective cover from the receiver.
b. Mount the 2nd LO Synthesizer board (A5A2) on an extender card.
c. Energize the receiver and allow 30 minutes warm-up time.
d. Using a Digital Voltmeter, verify that $+15 \mathrm{Vdc}+/-$ 0.25 Vdc is present at pins B5, B41, and A59, and that $+5 \mathrm{Vdc}+/-0.25 \mathrm{Vdc}$ is present at pins $\mathrm{A} 1, \mathrm{~B} 1$, and B45.
e. Using a Frequency Counter, verify that the 1 MHz reference frequency at pin B 49 is 1.000000 MHz and that the 10 kHz reference frequency at pin A57 is 10.000 kHz .

NOTE
If the two reference frequencies are not correct, perform the Time Base Adjustment Procedure before proceeding with the 2nd LO Synthesizer Alignment.
2. 32 MHz Loop Alignment
a. Connect the Digital Voltmeter to test point E1.
b. Adjust capacitor C51 until a Voltmeter reading of +3.0 Vdc is observed with the alignment tool withdrawn from the VCO shield.
3. Programmable Loop Alignment
a. Connect the Digital Voltmeter to test point E3.
b. Tune the receiver to 00.00499 MHz .
c. Insert an alignment tool in the VCO shield opening and spread or squeeze the turns of L8 until a Voltmeter reading of +4.0 Vdc is observed with the alignment tool withdrawn from the VCO shield.
4. Output Loop Alignment
a. Connect the Digital Voltmeter to test point E2.
b. Tune receiver to 00.00499 MHz .
c. Adjust capacitor C61 until a Voltmeter reading of +3.0 Vdc is observed with the alignment tool withdrawn from the VCO shield.
d. Using the Frequency Counter, verify that a frequency of $32.205010 \mathrm{MHz}+/-3 \mathrm{~Hz}$ is present at output pin B15.
5. Final Adjustments
a. Deenergize the receiver.
b. Remove the 2nd LO Synthesizer board from the extender card and return it to the receiver.
c. Mount the top protective cover on the receiver (use only four fasteners to secure the top cover).
d. Energize the receiver and allow it to operate for a minimum of 30 minutes.
e. Tune the receiver to 00.00499 MHz .
f. With the receiver in operation, remove the bottom protective cover.
g. Using the Digital Voltmeter, check the Loop Test Point Voltages as indicated in Table 4-39.

Table 4-39. Loop Test Point Voltages

| Parameter | Pin Number | Test Point Voltage |
| :---: | :---: | :---: |
| 32 :MHz Loop TP | A5XA2-B57 | $+3 \mathrm{Vdc}+/-0.1 \mathrm{Vdc}$ |
| Programmable Loop TP | A5XA2-A51 | $+4 \mathrm{Vdc}+/-0.1 \mathrm{Vdc}$ |
| Output Loop TP | A5XA2-A55 | $+3 \mathrm{Vdc}+/-0.1 \mathrm{Vdc}$ |

## NOTE

Test Point Voltages may drift from initial settings. If any Test Point Voltage is not within tolerance, repeat the appropriate loop alignment procedure. Set the Test Point Voltage(s) high or low as required to compensate for any drift observed in Step g. Do not proceed to Step h until the voltages in Table 4-39 are observed after the receiver has been in operation for 30 minutes with both covers in place.
h. Using the Frequency Counter, verify that a frequency of $32.205010 \mathrm{MHz}+/-3 \mathrm{~Hz}$ is present at pin A5XA2-B15.
i. Tune the receiver first to 00.00000 MHz and then to 00.00999 MHz . The appropriate Loop Test Point Voltages and the 2nd LO Output Frequency are given in Table 4-40.

Table 4-40. 2nd LO Synthesizer Tuning Parameters

|  |  | RECEIVER TUNED FREQUENCY |  |
| :--- | :--- | :--- | :--- |
| Parameter |  | 00.00000 MHz | 00.00999 MHz |
| 32 MHz Loop TP | A5XA2-B57 | $+3 \mathrm{Vdc}+/-0.2 \mathrm{Vdc}+3 \mathrm{Vdc}+/-0.2 \mathrm{Vdc}$ |  |
| Programmable Loop TP | A5XA2-A51 | $>7.0 \mathrm{Vdc}$ | $>1.5 \mathrm{Vdc}$ |
| Output Loop TP | A5XA2-A55 | $+3 \mathrm{Vdc}+/-0.2 \mathrm{Vdc}+3 \mathrm{Vdc}+/-0.2 \mathrm{Vdc}$ |  |
| 2nd LO Frequency | A5XA2-B15 | 32.21000 MHz | 32.20001 MHz |

j. Mount the top protective cover on the receiver.
k. This completes the 2nd LO Synthesizer Alignment Procedure.

### 4.3.6.2.3 2nd LO Filter Adjustment

1. Deenergize the receiver.
2. Remove plug P13 from A5XA2-B15/16.
3. Connect the RF Voltmeter and 50 ohm adapter to A5XA2-B15 using a coaxial cable with clip leads on one end. Connect cable ground lead to the A5 motherboard ground plane.
4. Set Voltmeter to $0 \mathrm{dBm}(0.3 \mathrm{mV})$ scale and energize the receiver.
5. Adjust A 5 C 13 for maximum Voltmeter reading. A5C13 is located on the bottom side of the Synthesizer Motherboard (A5) near the front panel of the receiver.
4.3.6.2.4 3rd LO Synthesizer, p/o A5A1, (p/o 791630) Alignment
6. Deenergize the receiver.
7. Mount the 1 st and 3rd LO Synthesizer (A5A1A2) on extender cards and connect the Digital Voltmeter to Pin 8 of U22.
8. Energize the receiver. Adjust capacitor C33 until a reading of 3.0 Vdc is seen on the Voltmeter.
9. Deenergize the receiver and disconnect Digital Voltmeter.
4.3.6.2.5 2 MHz Time Base, p/o A5A1, (p/o 791630) Adjustment NOTE

Before performing the following adjustment, the receiver should have been in operation for at least one hour at normal operation temperature to allow the circuit to stabilize.

1. Deenergize the receiver.
2. Mount 1st and 3rd LO Synthesizer (A5A1A2) on extender cards.
3. Connect the Digital Counter to rear panel 1 MHz Ref connector J11.
4. Set the Clock switch S2 to INT position.
5. Energize the receiver. Allow at least a 5 minute warm-up to stabilize the circuits. (This assumes power was not off more than 5 minutes to make the cable connections.)
6. While observing the Counter display, adjust 2 MHz Crystal Oscillator (U14) for a reading of 1.000000 MHz $+/-3 \mathrm{~Hz}$.
7. Deenergize the receiver and disconnect Digital Counter. Replace A5A1A2 board into the proper slots.

### 4.3.6.2.6 BFO Synthesizer, A5A3, (791576) Alignment

Two alignments are required for the BFO Synthesizer (A5A3). Capacitor C8 and resistor R1 are interdependent and must be aligned simultaneously.

1. Mount the BFO Synthesizer board on extender cards.
2. Adjust C 8 until the closest reading to 3.0 Vdc is seen at module pin 7.
3. Adjust R1 until the voltage difference between gate to source of $\mathrm{Q4}$ (Pins 3 and 2) is 0 Vdc. (The voltage from gate to ground and from source to ground will be approximately 1.2 Vdc .)
4. Adjust C 8 again until the closer reading to 3.0 Vdc is seen at module pin 7.
4.3.6.3 Receiver Alignment
4.3.6.3.1 Input Converter, A3, (791592) Alignment
5. Deenergize the receiver and loosen the two (2) captivated screws holding the A3 module to the chassis. Pull the A3 module out and remove its cover. Connect test equipment as shown in Figure 4-2. Be careful that Input Converter does not short to the adjacent power supply circuitry.


Figure 4-2. Input Converter Alignment Test Setup
2. Set receiver controls as follows:
a. Meter - Signal Strength
b. Gain Mode - Manual
c. Detection Mode- AM
d. RF Gain - Maximum Clockwise
e. Phone Level - N/A
f. IF Bandwidth - 50 kHz
g. BFO offset - N/A
3. Energize the receiver.
4. Set the Signal Generator to -97 dBm , unmodulated at 15.0050 MHz . Tune receiver to 15.00500 MHz .
5. While observing RF Voltmeter, adjust C19 of A3A2 and C1 of A3A2 for a maximum meter reading of approximately $-15 \mathrm{dBm}(40 \mathrm{mV})$.
6. Deenergize the receiver and disconnect test equipment.
7. Replace the cover on the Input Converter (A3). Install the Input Converter in chassis.

## .3.6.3.2 10.7 MHz Filter Switch, A4A1, (791594) Adjustment

1. Deenergize the receiver.
2. Connect the test equipment as shown in Figure 4-3. Set the Generator for 15.005 MHz , unmodulated, at -64 dBm .


Figure 4-3. 10.7 MHz Filter Switch Adjustment, Test Setup
3. Remove A4A1 and A4A2 boards.
4. Place A4A1 on an extender card.
5. Energize the receiver and tune to 15.00500 MHz .
6. Select the 3.2 kHz IF Bandwidth position and adjust A4A1R26 for a $-36 \mathrm{dBm}(3.5 \mathrm{mV})$ RF Voltmeter reading.

## NOTE

If -36 dBm cannot be obtained, adjust for maximum dBm reading. Record this reading.
7. Select the 6.0 kHz IF Bandwidth position and adjust A4A1R28 for the same dBm reading obtained in step 6.
8. Select the 50 kHz IF Bandwidth position and adjust A4A1R30 for the same dBm reading obtained in step 6 .
9. Deenergize the receiver and disconnect test equipment.
10. Install A4A2 and A4A1 into the proper slots.
4.3.6.3.3 $\quad 455 \mathrm{kHz}$ Amplifier/AM Detector, A4A7, (76002) Response Alignment

1. Deenergize the receiver.
2. Remove cards A4A3 and A4A10. Place A4A7 on an extender card.
3. Connect the test equipment as shown in Figure 4-4.
4. Set up the Sweep Generator as follows:

| a. | Power | - | ON |
| :--- | :--- | :--- | :--- |
| b. | CW/Sweep | - | SYM |
| c. | Trig/Line/Free | - | Line |
| d. | Fast/Slow/Manual | - | Fast |
| e. | Crystal Cal | - | OFF |
| f. | Range | - | 11 |
| g. Sym Sweep Width | - | $.1 / 1$ |  |
|  | Vernier |  |  |
| h. | 1 kHz Mod | - |  |
| i. Output Level | - | -60 dBm |  |
| j. Frequency | - | 455 kHz |  |

5. Set up the Marker Generator for a 455 kHz output, unmodulated, at -80 dBm .
6. Set the receiver controls as follows:
a. Meter

- N/A
b. Gain Mode - Manual
c. Detection Mode - N/A
d. RF Gain - Maximum Clockwise
e. Phone Level - N/A
f. IF Bandwidth - N/A
g. Receiver Frequency - N/A
h. BFO offset - N/A

7. Energize the receiver. Adjust Sweep Generator Frequency control to center the response pattern on the Oscilloscope screen.
8. Adjust A4A7L2 and A4A7L3 for an Oscilloscope waveform which has maximum amplitude and is symmetrical about the marker. See Figure 4-5 for a typical waveform.
9. Deenergize the receiver and disconnect test equipment.
10. Install A4A3 and A4A10 cards in the proper card slots.


Figure 4-4. 455 kHz Amplifier/AM Detector Response Alignment, Test Setup


Figure 4-5. 455 kHz Amplifier/AM Detector Response Alignment, Typical Response
4.3.6.3.4 $\quad 455 \mathrm{kHz}$ Amplifier/AM Detector, A4A7, (76002) Gain Adjustment

1. Connect the test equipment as shown in Figure 4-6.
2. Set the receiver controls as follows:

| a. Meter | - | Signal Strength |  |
| :--- | :--- | ---: | :--- |
| b. | Gain Mode | - | Manual |
| c. Detection Mode- | AM |  |  |
| d. | RF Gain | - | Maximum Clockwise |
| e. Phone Level | - | N/A |  |
| f. | IF Bandwidth | - | 50 kHz |
| g. | BFO offset | - | N/A |



Figure 4-6. 455 kHz Amplifier/AM Detector Gain Adjustment, Test Setup
3. Energize the receiver.
4. Set the RF Voltmeter to the 100 mV scale.
5. Set the Signal Generator to 15.0050 MHz , unmodulated at $-97 \mathrm{dBm}(3 \mathrm{~V})$. Also tune receiver to 15.00500 MHz .
6. Adjust A4A7R7 for a 40 mV reading on the RF Voltmeter.
7. Deenergize the receiver and disconnect test equipment.
4.3.6.3.5 FM Discriminator, p/o A4A9, (791599) Alignment

1. Deenergize the receiver.
2. Remove cards A4A7, A4A9, and A4A10.
3. Put A4A9 on an extender card.
4. Connect the test equipment as shown in Figure 4-7.
5. Set up the Sweep Generator as follows:

| a. | Power | - | ON |
| :---: | :---: | :---: | :---: |
| b. | CW/Sweep | - | SYM |
| c. | Trig/Line/Free | - | Line |
| d. | Fast/Slow/Manual | - | Fast |
| e. | Crystal Cal | - | OFF |
| f. | Range | - | 11 |
| g . | Sym Sweep Width | - | .1/1 |
|  | Vernier |  | OFF |
| h. | 1 kHz Mod | - | -10 |
| j. | Frequency | - | 455 |

6. Set up the Marker Generator for a 455 kHz output, unmodulated, at -25 dBm .
7. Set the receiver controls as follows:
a. Meter - N/A
b. Gain Mode - N/A
c. Detection Mode - FM
d. RF Gain - N/A
e. Phone Level - N/A
f. IF Bandwidth - N/A
g. Receiver Frequency N/A
h. BFO offset - N/A
8. Energize the receiver. Adjust Sweep Generator Frequency control to center the response pattern on the Oscilloscope screen.
9. Adjust A4A9L1 and A4A9T1 for an Oscilloscope waveform which has maximum amplitude and is symmetrical and linear about the marker. See Figure 4-8 for a typical waveform.
10. Deenergize the receiver.
11. Disconnect the test equipment and install A4A7, A4A9, and A4A10 boards into the proper slots.


Figure 4-7. FM Discriminator Alignment, Test Setup


Figure 4-8. FM Discriminator Alignment, Typical Response

### 4.3.6.3.6 LED Intensity Adjustment

The intensity of the front panel Frequency Display can be varied by potentiometer R2, which is located inside the front panel on the left side of the Frequency Display LED's. Turning R2 clockwise increases the LED intensity.

### 4.3.6.4 Frequency Extender Alignment

### 4.3.6.4.1 1st LO Synthesizer (FE-A1A1A1) (370689) Alignment

The only alignment points for the 1st LO Synthesizer are in the VCO (FEA1A1A2) which is a very sensitive circuit; care must be taken to ensure proper operation. This procedure should be performed only when a definite alignment is needed. Table 4-41 lists the components and their parameters used in this procedure.

1. Remove the Frequency Extender, FE-A1, from the receiver.
2. Remove the cover plate to gain access to the 1st LO.
3. Connect a Digital Voltmeter to terminal E5.
4. Beginning at Band 0 , align the 7 VCO Bands indicated in Table 4-41. Alignment is accomplished by monitoring the voltage at pin B1 and adjusting the indicated components. Note that L2, L3 and L4 will cause interaction between the alignment of several bands.
5. Check the 1 st LO frequency band (test point E10 in the VCO) while dialing the tuned frequency in 1 MHz steps starting with 30.00000 ViHz .

Table 4-41. VCO Alignment Parameters

| VCO BAND | 1ST LO FREQ | PIN B1 VOLTAGE | COMPONENT |
| :---: | :--- | :--- | :--- |
| 0 | $190-199$ | -8.5 to 6.0 | C6*, L1 |
| 1 | $200-209$ | -7.5 to 4.1 | L2 |
| 2 | $210-219$ | -7.2 to 2.8 | L3 |
| 3 | $220-229$ | -5.3 to 3.9 | L2, L3 |
| 4 | $230-239$ | -6.6 to 2.7 | L4 |
| 5 | $240-249$ | -6.0 to 2.2 | L4, L2 |
| 6 | $250-259$ | -6.2 to 0.4 | L3, L4 |

### 4.3.6.4.2 Preselector (FE-A1A1A3) (794274) Alignment

1. Deenergize the receiver.
2. Connect the test equipment as shown in Figure 4-9. Set the Generator for 53.000 MHz , unmodulated, at -64 dBm .


Figure 4-9. Preselector Alignment, Test Setup
3. Open the Frequency Extender FE-A1 and gain access to FEA1A1A3.
4. Energize the receiver and tune to 53.00000 MHz .
5. Select the 50 kHz IF Bandwidth position and adjust C6 and C12 for a maximum RF Voltmeter reading.
6. Tune the receiver and generator to 99.00000 MHz . Adjust C8 and C13 for a maximum RF voltmeter reading.
7. Deenergize the receiver and disconnect test equipment.
10. Replace the cover plate back on the Frequency Extender.
4.3.6.4.3 2nd LO Synthesizer (FE-A1A2A1) (794270) Alignment

1. Deenergize the receiver.
2. Open the Frequency Extender and gain access to the 2nd LO, FE-A1A2A1.
3. Connect a digital voltmeter to U3-6.
4. Energize the receiver. Adjust capacitor C19 until a reading of 3.0 Vdc is seen on the Voltmeter.
5. Deenergize the receiver and disconnect Digital Voltmeter.
6. Replace the cover plate on the Frequency Extender.

## SECTION V

## REPLACEMENT PARTS LIST

### 5.1 UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations (electrical symbol numbers) has been used to identify assemblies, subassemblies (and modules) and parts. An example of the unit numbering method follows:

Subassembly Designation A1
Identify from right to left as:

R1 Class and No. of Item
First (1) resistor (R) of first (1) subassembly (A)

As shown on the main chassis schematic, components which are an integral part of the main chassis have no subassembly designation.

### 5.2 REFERENCE DESIGNATION PREFIX

Partial reference designations have been used on the equipment and on the illustra tions in this manual. The partial reference designations consist of the class letter(s) and identifying item number. The complete reference designations may be obtained by placing the proper prefix before the partial reference designations. Reference Designation Prefixes are provided on drawings and illustrations in parentheses within the figure titles.

### 5.3 LIST OF MANUFACTURERS

| Mfr. <br> Code | Name and Address <br> 00779 |
| :--- | :--- |
|  | AMP, Incorporated <br>  <br>  <br> Harrisburg, Box 3608 |
|  | $l$ |

01121 Allen-Bradley Company 1201 South 2nd Street Milwaukee, WI 53204

Texas Instruments, Inc. Semiconductor-Components Div. 15300 North Central Expressway Dallas, TX 75231

02114 Ferroxcube Corporation
P.O. Box 359

Mt. Marion Road
Saugerties, NY 12477

Mfr. Code 02735

04713
Motorola Incorporated Semiconductor Products Div. 5005 East McDowell Road Phoenix, AZ 85008

Vernitron Corp. AIE Div. 701 Murfreesboro Rd. Nashville, TN 37210

| Mfr. Code | Name and Address |  | Mfr. Code. | Name and Address |
| :---: | :---: | :---: | :---: | :---: |
| 07263 | Fairchild Camera \& Instrn Semiconductor Division 464 Ellis Street <br> Mountain View, CA 94040 | Corp. | 17856 | Siliconix, Inc. <br> 2201 Laurelwood Road <br> Santa Clara, CA 95050 |
| 07388 | Toretel Incorported 13402 South 71 Highway Grandview, MO 64030 |  | 18324 | Signetics Corporation 811 East Arques Avenue Sunnyvale, CA 94086 |
| 09021 | Airco Ine. Airco Electronics Bradford, PA 17055 |  | 18565 | Chomerics Inc. Woburn, MA 01801 |
| 09353 | $\mathrm{C} \& \mathrm{~K}$ Components, Inc. 103 Morse Street <br> Watertown, MA 02172 |  | 18714 | RCA Corporation <br> Solid State Division <br> Fostoria Road <br> Findlay, OH 45840 |
| 12498 | Teledyne Crystalonics 147 Sherman Street Cambridge, MA 02140 |  | 19080 | Robison Electronics Inc. <br> 3580 Sacramento Dr. <br> P.O. Box Y <br> San Luis Obispo, CA 93406 |
| 13103 | Thermalloy Company 2021 W. Valley View Lane Dallas, TX 75234 |  | 19209 | General Electric Company Battery Business Department <br> P.On Box 114 <br> Gainsville, FL 32602 |
| 14632 | Watkins-Johnson Company 700 Quince Orchard Road Gaithersburg, MD 20878 |  | 19505 | Applied Eng. Products, Co. Division of Samarious, Inc. 300 Seymour Avenue Derby, CT 06418 |
| 14655 | Cornell-Dubilier Electronics <br> Div. of Federal Pacific <br> Electric Company <br> 150 Avenue L <br> Newark, NJ 07101 |  | 21604 | The Buckeye Stamping Co. 555 Marion Road Columbus, OH 43207 |
| 15818 | Teledyne Semiconductor Teledyne Inc. Company 1300 Tera Bella Ave. Mountain View, CA 94043 |  | 22526 | Du Pont EI De Nemours and Photo Products Dept. <br> Berg Electronics Div. <br> Route 83 <br> New Cumberland, PA 17070 |
|  |  |  | 25088 | Siemens America, Inc. 186 Wood Avenue |
| 16428 | Belden Corporation <br> P.O. Box 1101 <br> Richman, IN 47374 |  |  | S. Iselin, NJ 08830 |


| Mfr. Code | Mfr. Name and Address | Codes | Name and Address |
| :---: | :---: | :---: | :---: |
| 27014 | National Semi-Conductor Corpn 2950 San Ysidro Way <br> Santa Clara, CA 95051 | 72982 | Erie Technological Prod., 644 West 12th Street Erie, PA 16512 |
| 27956 | Relcom 3333 Hillview Avenue Palo Alto, CA 94304 | 73138 | Beckman Instruments, Inc. Helipot Division 2500 Harbor Boulevard Fullterton, CA 92634 |
| 28480 | Hewlett-Packard Company Corporate Headquaters 1501 Page Mill Road Palo Alto, CA 94304 | 74306 | Piezo Crystal Company 100 K Street Carlisle, PA 17013 |
| 31918 | IEE/Schadow Incorporated 8081 Wallace Road Eden Prairie, MN 55343 | 74868 | Bunker Ramo Corporation The Amphenol RF Division 33 East Franklin Street Danbury, CT 06810 |
| 33095 | Spectrum Control, Inc. 152 E. Main Street Fairview, PA 16415 | 75042 | TRW Electronic Components IRC Fixed Resistors 401 North Broad Street Philadelphia, PA 19108 |
| 52673 | KSW Electronics Corp. Burlington, MA 01803 | 75915 | Littlefuse, Incorporated 800 E. Northwest Highway Des Plaines, IL 60016 |
| 56289 | Sprague Electric Company Marshall Street <br> North Adams, MA 01247 | 80058 | Joint Electronic Type Designation System |
| 71279 | Cambridge Thermionic Corp. 445 Concord Avenue Cambridge, MA 02138 | 80103 | Lambda Electronics Corp. Div. of Veeco Instr., Inc. 51 Broad Hollow Road Melville, NY 11746 |
| 71400 | Bussman Manufacturing <br> Division of McGraw-Edison Co. 2536 W. University Street <br> St. Louis, MO 63107 | 80131 | Electronic Industries Assoc. 2001 Eye Street, N.W. Washington, DC 20006 |
| 71785 | TRW Electronic Components Cinch Connector Operations 1501 Morse Avenue Elk Grove Village, IL 60007 | 81312 | Winchester, Electronics Division of Litton Ind. Oakville, CT 06779 |
| 72136 | Electro Motive Mfg. Co., Inc. South Park \& John Streets Willimantic, CT 06226 | 81349 | Military Specifications |


| Mfr. Code | Name and Address | Mfr. <br> Code | Name and Address |
| :---: | :---: | :---: | :---: |
| 81350 | Joint Army-Navy Specifications | 93332 | Sylvania Elec. Products, Ine. Semiconductor Products Div. 100 Sylvan Road Woburn, MA 01801 |
| 82389 | Switcheraft, Incorporated 5555 North Elston Avenue Chicago, IL 60630 | 93958 | Republic Electronics Corp. <br> 176 East 7th Street <br> Paterson, NJ 07524 |
| 84411 | TRW Electric Components TRW Capacitors 112 W. First Street Ogallala, NE 69153 | 95121 | Quality Components, Inc. <br> P.O. Box 113 <br> St. Mary's, PA 15857 |
| 88245 | Litton Industries USECO Division 13536 Saticoy Street Van Nuys, CA 91409 | 96733 | San Fernando Electric Mfg. Con San Fernando, CA 91341 |
| 91293 | $\begin{aligned} & \text { Johanson Manufacturing Co. } \\ & \text { P.O. Box } 329 \\ & \text { Boonton, NJ } 07005 \end{aligned}$ | 98291 | Sealectro Corporation 225 Hoyt <br> Mamaroneck, NY 10544 |
| 91418 | Radio Materials Company 4242 West Bryn Mawr Avenue Chicago, IL 60646 | 98978 | International Electronic Research Corporation 135 West Magnolia Blvd. Burbank, CA 91502 |
| 91984 | Maida Development Co. 205 Libby <br> P.O. Box 3529 <br> Hampton, VA 23663 | 99800 | American Precision Industries Delevan Electronics Division 270 Quaker Road East Aurora, NY 14052 |
| 92825 | Whitso Incorporated 93330 Bryon Street Schiller Park, IL 60176 | 99848 | Wilco Corporation 4030 West 10th Street P.O. Box 22248 Indianapolis, IN 46222 |

## 5.4 <br> PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear or damage. When ordering replacement parts from Watkins-Johnson Company, specify the type and serial number of the equipment and the reference designation and description of each part ordered. The list of manufacturers provided in paragraph 5.3 and the manufacturer's part number for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment; however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

## NOTE

As improved semiconductors become available, it is the policy of Watkins-Johnson to incorporate them in proprietary products. For this reason some transistors, diodes, and integrated circuits installed in the equipment may not agree with those specified in the parts list and schematic diagrams of this manual. However, the semiconductors designated in the manual may be substituted in every case with satisfactory results.
5.5 ASSEMBLY REVISION LEVEL

N/A

TYPE WJ-8718-19/FE HF RECEIVER, MAIN CHASSIS

| REF <br> DESIG | DESCRIPTION | $\begin{aligned} & \hline \text { QTY } \\ & \text { PER } \\ & \text { ASSY } \end{aligned}$ | MANUFACTURER'S PART NO. | MFR. CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | Power Distribution | 1 | 76240 | 14632 |  |
| A2 | Input Filter | 1 | 791616 | 14632 |  |
| A3 | Input Converter | 1 | 791592-8 | 14632 |  |
| A4 | IF Motherboard | 1 | 791569-1 | 14632 |  |
| A5 | Synthesizer Motherboard | 1 | 791570-1 | 14632 |  |
| A6 | Interface Motherboard | 1 | 791580-1 | 14632 |  |
| FE-A1 | Frequency Extender | 1 | 794278-1 | 14632 |  |
| FE-A2 | RF Input Switch Assembly | 1 | 794276-1 | 14632 |  |
| FE-A3 | 1 MHz Filter Assembly | 1 | 794327-1 | 14632 |  |
| FE-A4 | Serial I/O Buffer | 1 | 794300-1 | 14632 |  |
| MFP-A1 | Front Panel Motherboard | 1 | 796013-5 | 14632 |  |
| MFP-A2 | Encoder Assembly | 1 | 791202-5 | 14632 |  |
| BT1 | Battery | 1 | 41B901BD16G1 | 19209 |  |
| Cl | Capacitor, Ceramic, Disc: . 1 uf, 20 \%, 50 V | 4 | 34475-1 | 14632 |  |
| C2 | Same as Cl |  |  |  |  |
| C3 | Same as Cl |  |  |  |  |
| C4 | Same as C1 |  |  |  |  |
| C5 | Capacitor, Ceramic, Disc: . 47 uf, 20 \%, 50 V | 2 | 34452-1 | 14632 |  |
| C6 | Same as C5 |  |  |  |  |
| C7 | Capacitor, Feedthru: . 01 uf, 20\%, 600 V | 6 | F1A6103K | 96733 |  |
| C8 |  |  |  |  |  |
| Thru | Same as C7 |  |  |  |  |
| C12 |  |  |  |  |  |
| C13 | Not used |  |  |  |  |
| C14 | Capacitor, Ceramic, Disc: . 01 uf, 20 \%, 50 V | 1 | 34453-1 | 14632 |  |
| CR1 | Diode | 2 | 1N1614 | 80131 | 02735 |
| CR2 | Same as CR1 |  |  |  |  |
| E1 | Terminal, Standoff | 3 | 7A1A1 | 92825 |  |
| E2 | Same as El |  |  |  |  |
| E3 | Same as E1 |  |  |  |  |
| E4 | Terminal, Standoff | 1 | 160-2381-01-05-00 | 71279 |  |
| E5 |  |  |  |  |  |
| Thru | Terminal, Feed Through | 6 | SFU16Y | 04013 |  |
| E10 |  |  |  |  |  |
| F1 | Fuse Cartridge: 1 AMP, 3 AG Slow-blow | 1 | MDL1 | 71400 |  |
| F2 | Fuse Cartridge: $1 / 2$ AMP, 3 AG, Slow-blow | 1 | MD L1/2 | 71400 |  |
| FEW5 | Cable Assembly | 1 | 17300-320-5 | 14632 |  |
| FEW6 | Cable Assembly | 1 | 17300-320-6 | 14632 |  |
| FEW7 C | Cable Assembly | 1 | 370704 | 14632 |  |
| EW8 | Cable Assembly | 1 | 370703 | 14632 |  |
| FEWY C | Cable Assembly | 1 | 17300-320-7 | 14632 |  |
| FEW10 C | Cable Assembly | 1 | 17300-320-8 | 14632 |  |



Figure 5-1. WJ-8718-19/FE HF Receiver, Front Panel, Location of Components


DENOTES HIDDEN PARTS

Figure 5-2. WJ-8718-19/FE HF Receiver, Rear Panel, Location of Components

MAIN CHASSIS

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | RECA VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| FEW11 | Cable Assembly | 1 | 17300-320-9 | 14632 |  |
| FEW12 | Cable Assembly | 1 | 17300-320-10 | 14632 |  |
| FEW13 | Cable Assembly | 1 | 17300-320-11 | 14632 |  |
| FEW5P1 | Connector/Plug, Sub-Miniature, Right Angle | 3 | UG1466U | 80058 |  |
| FEW5P2 | Connector/Plug, Sub-Miniature, Straight | 8 | UG1465U | 80058 |  |
| FEW6P1 | Same as FEW5P2 |  |  |  |  |
| FEW6P2 | Same as FEW5 P1 |  |  |  |  |
| FEW7P2 |  |  |  |  |  |
| FEW7P6 |  |  |  |  |  |
| FEW8P7 |  |  |  |  |  |
| FEW9P3 | Same as FEW5 P2 |  |  |  |  |
| FEW9P6 | Same as FEW5P1 |  |  |  |  |
| FEW10P\% | Same as FEW5P2 |  |  |  |  |
| FEW10P4 | Same as FEW5P2 |  |  |  |  |
| FEW11P | Same as FEW5P2 |  |  |  |  |
| FEW11P | Same as FEW5P2 |  |  |  |  |
| FEW12P | Connector/Plug, Sub-Miniature, Screw On | 1 | UG1468U | 80058 |  |
| FEW12P\% | Same as FEW5P2 |  |  |  |  |
| FEW13P | Connector/Plug, 3 position, single row | 1 | 87499-5 | 00779 |  |
| FL1 | Filter, Power | 1 | 34505-1 | 14632 |  |
| FL2 | Filter, Monolithic, $32.205 \mathrm{MHz}, 12 \mathrm{kHz} \mathrm{BW}$ | 1 | 92241 | 14632 |  |
| J1 | Connector, Plug: SMC Series Part of W14 | 8 | UG1468/U | 80058 | 19505 |
| J2 | Conneactor, Receptacle | 1 | 205203-1 | 00779 |  |
| J3 | Same as J1 Part of W2 |  |  |  |  |
| J4 | Same as J1 Part of W3 |  |  |  |  |
| J5 | Same as J1 Part of W4 |  |  |  |  |
| J6 | Not Used |  |  |  |  |
| J7 | Same as J1 Part of W12 |  |  |  |  |
| J8 | Same as Jl Part of Wil3 |  |  |  |  |
| J9 | Same as J1 Part of w9 |  |  |  |  |
| J10 | Same as J1 Part of W10 |  |  |  |  |
| J11 | Connector, Receptacle: BNC Series Part of W11 | 2 | 225398-7 | 00779 |  |
| J12 | Same as J11 Part of W15 |  |  |  |  |
| J13 | Connector, Phone Jack | 1 | L12B | 82389 |  |
| J14 | Connector/Receptacle | 1 | MS3122E14-19S | 96906 |  |
| J15 | Connector/Receptacle | 1 | MS3122E10-6P | 96906 |  |
| J16 | Connector/Receptacle | 1 | MS3122E10-6S | 96906 |  |
| M1 | Meter | 1 | 34455-1 | 14632 |  |
| 4 FPCl | Capacitor, Ceramic, Disc: . 47 uf, 20\%, 50 V | 2 | 34452-1 | 14632 |  |
| MFPC2 | Same as MFPC1 |  |  |  |  |
| MF P.P1 | Connector, Plug Part of MFP-W1 | 1 | 88475-2 | 00779 |  |
| MF PP2 | Connector, Plug Part of MFP-W1 | 1 | 88475-3 | 00779 |  |



Figure 5-3. WJ-8718-19/FE HF Receiver, Top View, Location of Components(Sheet 1 )


Figure 5-3. WJ-8718-19/FE HF Receiver, Top View, Location of Components(Sheet 2)

MAIN CHASSIS

| REF DESIG | DESCRIPTION |  | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MFPP3 | Connector, Plug | Part of MFP-W1 | 1 | 3332-0000 | 75037 |  |
| MFPP6 | Connector, Plug | Part of MFP-W2 | 2 | 88476-7 | 14632 |  |
| MFPP7 | Same as MFP-P7 |  |  |  |  |  |
| MFPP8 |  |  |  |  |  |  |
| Thru | Connector, Plug, Faston Receptacle |  | 9 | 42236-1 |  |  |
| MFPP13 |  |  |  |  |  |  |
| MFPP14 | Connector, Receptacle Faston Tab |  | 2 | 62073-1 | 0779 |  |
| MFPP15 | Same as MFP-P14 |  |  |  |  |  |
| MFPP16 | Connector, Plug |  | 1 | 1-87499-1 | 0779 |  |
| MFPP17 | Same as MFP-P8 |  |  |  |  |  |
| MFPP18 | Same as MFP-P8 |  |  |  |  |  |
| MFPP21 | Same as MFP-P8 |  |  |  |  |  |
| MFPP22 | Connector, Plug |  | 1 | 87499-5 | 0779 |  |
| MFPU1 | Voltage Regulator |  | 1 | LAS1405 | 80103 |  |
| MFPW1 | Cable Assembly |  | 1 | 371048-1 | 14632 |  |
| MFPW2 | Cable Assembly |  | 1 | 380092-2 | 14632 |  |
| MFPW3 | Cable Assembly |  | 1 | 380142-1 | 14632 |  |
| MP1 | Handle, Front Panel |  | 2 | 32306-1 | 14632 |  |
| MP2 | Same as MP1 |  |  |  |  |  |
| MP3 | Knob |  | 1 | PS50D1/70C2/BLK | 21604 |  |
| MP4 | Knob |  | 1 | PS70D1/B | 21604 |  |
| MP5 | Knob |  | 1 | 280064-1 | 14632 |  |
| MP6 | Display Window (small) |  | 1 | 170368-1 | 14632 |  |
| MP7 | Display Window (large) |  | 1 | 271001 | 14632 |  |
| MP8 | Handle; Rear (p/o MP8) |  | 1 | 390507-1 | 14632 |  |
|  | Handle; Rear (p/o MP8) |  | 1 | 390507-2 | 14632 |  |
| MP9 | Cover, Transistor |  | 1 | 8903 NW | 13103 |  |
| P1 | Connector Plug | Part of W1 |  |  |  |  |
| P2 | Same as P1 |  |  |  |  |  |
| P3 | Connector, Plug: SMC Series | Part of W2 | 7 | UG1466U | 80058 | 19505 |
| P4 | Same as P3 | Part of W4 |  |  |  |  |
| P5 | Same as P3 | Part of W3 |  |  |  |  |
| P6 | Not Used |  |  |  |  |  |
| P7 | Faston, Receptacle | Part of W5 | 30 | 42236-1 | 00779 |  |
| P8 | Same as P3 | Part of W5 |  |  |  |  |
| P9 | Connector, Plug: SMC Series | Part of W6 |  |  |  |  |
| P10 | Same as P9 | Part of W6 |  |  |  |  |
| P11 | Same as P9 | Part of W7 |  |  |  |  |
| P12 | Same as P9 | Part of W7 |  |  |  |  |
| P13 | Plug Assembly |  | 1 | 34704-1 | 14632 |  |
| P14 | Plug Assembly | Part of W9 |  |  |  |  |
| 15 S | Same as P14 | Part of W10 |  |  |  |  |



| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| P16 | Same as Plt Part of W11 |  |  |  |  |
| P17 | Same as Pl4 Part of W12 |  |  |  |  |
| P18 | Same as Pl4 Part of W13 |  |  |  |  |
| P19 | Same as P14 Part of W14 |  |  |  |  |
| P20 | Same as P14 Part of W15 |  |  |  |  |
| P21 | Same as P14 Part of W17 |  |  |  |  |
| P22 | Plug Assembly | 1 | 34529-2 | 14632 |  |
| P23 | Plug Assembly | 1 | 34529-3 | 14632 |  |
| P24 | Plug Assembly | 1 | 470487-1 | 14632 |  |
| P25 | Connector, Plug Faston Part of W17 | 11 | 2-350804-2 | 00779 |  |
| P26 | Same as P6 Part of W18 | . |  |  |  |
| P27 | Same as P25 Part of W18 |  |  |  |  |
| P28 | Same as P3 Part of W16 |  |  |  |  |
| P29 | Same as P3 Part of W16 |  |  |  |  |
| P30 <br> Thru <br> P38 | Same as P6 |  |  |  |  |
| P39 | Same as P25 |  |  |  |  |
| P40 | Same as P25 |  |  |  |  |
| P41 <br> Thru <br> P45 | Same as P6 |  |  |  |  |
| P46 | Not Used |  |  |  |  |
| P47 | Not Used |  |  |  |  |
| P48 | Plug Assembly | 1 | 34529-1 | 14632 |  |
| P49 | Same as P25 Part of W19 |  |  |  |  |
| P50 | Same as P6 Part of W20 |  | . |  |  |
| P51 | Same as P25 Part of W20 |  |  |  |  |
| P52 | Same as P6 |  |  |  |  |
| P53 | Same as P6 |  |  |  |  |
| P54 | Plug Assembly | 1 | 34529-4 | 14632 |  |
| P55 | Same as P6 |  |  |  |  |
| P56 | Not Used |  |  |  |  |
| R1 | Resistor, Variable, Composition: $25 \mathrm{k}, 10 \%, 1 \mathrm{~W}$ | 1 | 70A3L036L253A |  |  |
| RA1 | Radiator, Heat | 3 | UP2-T03-CB | 98978 |  |
| RA2 | Same as RA1 |  |  |  |  |
| RA3 | Same as RA1 |  |  |  |  |
| S1 | Switch, Pushbutton | 1 | 8161-S-H-23-Q-E | 09353 |  |
| S2 | Switch, Slide | 1 | $11 \mathrm{Al211}$ | 82389 |  |
| T1 | Transformer, Power | 1 | 380083 | 14632 |  |
| T2 | Transformer, Audio | 1 | 841004 | 14632 |  |
| U1 | Voltage Regulator | 1 | LM340AKC15 | 27014 |  |
| U2 | Voltage Regulator | 1 | LAS18A15 | 80103 |  |
| U3 | Voltage Regulator | 1 | LAS1405 | 80103 |  |

MAIN CHASSIS

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline Q T Y \\ P E R \\ A S S Y \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| U 4 | Rectifier, Bridge. 200 PRV, 12 A | 1 | PK20F | 83701 |  |
| W1 | Cable Assembly, Power Line Cord | 1 | 17250 | $16+28$ |  |
| W2 | Cable Assembly | 1 | 34701-1 | 14632 |  |
| W3 | Cable Assembly | 1 | 34701-2 | 14632 |  |
| W4 | Cable Assembly | 1 | 34701-3 | $1+632$ |  |
| W5 | Cable Assembly | 1 | 34701-4 | 14632 |  |
| W6 | Cable Assembly | 1 | 34701-5 | 14632 |  |
| W7 | Cable Assembly | 1 | 34701-6 | $1+632$ |  |
| W8 | Not Used |  |  |  |  |
| W9 | Cable Assembly | 1 | 34700-1 | 14632 |  |
| W10 | Cable Assembly | i | 34700-2 | 14632 |  |
| W11 | Cable Assembly | 1 | 34702-1 | 14632 |  |
| W12 | Cable Assembly | 1 | 34700-3 | 14632 |  |
| W13 | Cable Assembly | 1 | 34700-4 | 14632 |  |
| W14 | Cable Assembly | 1 | 34700-5 | 14632 |  |
| W15 | Cable Assembly | 1 | 34702-2 | 14632 |  |
| W16 | Cable Assembly | 1 | 34701-7 | 14632 |  |
| W17 | Cable Assembly | 1 | 380005-1 | 14632 |  |
| W18 | Cable Assembly | 1 | 380005-2 | 14632 |  |
| W19 | Cable Assembly | 1 | 380005-3 | 14632 |  |
| W20 | Cable Assembly | 1 | 380005-4 | 14632 |  |
| XBTI | Socket, Battery | 1 | 794298 | 14632 |  |
| XF2 | Fuseholder | 1 | 342004 | 75915 |  |
| XU1 | Socket Assembly | 1 | 34506-1 | 14632 |  |
| XU2 | Socket Assembly | 1 | 34506-2 | 14632 |  |
| XU3 | Socket Assembly | 1 | 34506-3 | 14632 |  |
| $\begin{gathered} \text { RS232* } \\ \text { J1 } \end{gathered}$ | Connector, Receptacle | 1 | MS3122E12-10P | 96906 |  |
| $\begin{gathered} \text { RS232* } \\ \mathrm{J} 2 \end{gathered}$ | Connector, Receptacle | 1 | MS3122E12-10S | 96906 |  |

5.6 .1

TYPE 76240 POWER DISTRIBUTION
REF DESIG PREFIX A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Electrolytic, Aluminum: 2200 uF, $-10+75 \%, 25 \mathrm{~V}$ | 2 | 39D228G025HP4 | 56289 |  |
| C2 | Same as Cl |  |  |  |  |
| C3 | Capacitor, Electrolytic, Aluminum: 8000 uF, $-10+75 \%, 15 \mathrm{~V}$ | 2 | 39D808G015JT4 | 56289 |  |
| C4 | Same as C3 |  |  |  |  |
| CR1 | Diode | 4 | IN4998 | 80131 | 04713 |
| CR2 <br> Thru CR4 | Same as CR1 |  |  |  |  |
| J1 | Faston Tab | 20 | 62073-1 | 00779 |  |
| J2 Thru J14 | Same as Jl |  |  |  |  |
| J15 <br> Thru J18 | Not Used |  |  |  |  |
| J19 | Same as J1 |  |  |  |  |
| J20 | Same as J1 |  |  |  |  |
| J21 | Same as J1 |  |  |  |  |
| J22 |  |  |  |  |  |
| Thru | Not Used |  |  |  |  |
| J30 |  |  |  |  |  |
| J31 | Same as J1 |  |  |  |  |
| J32 | Same as Jl |  |  |  |  |
| J33 | Not Used |  |  |  |  |
| J34 | Not Used |  |  |  |  |
| J35 | Same as J1 |  |  |  |  |



Figure 5-5. Type 76240 Power Distribution, Location of Components

### 5.6.2 TYPE 791616-1 RF FILTER

REF DESIG PREFIX A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PEER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{\|l\|} \hline \mathrm{A} 1 \\ \mathrm{~J} 1 \\ \mathrm{~L} 1 \\ \mathrm{HP} 1 \\ \mathrm{R} 1 \\ \mathrm{R} 2 \\ \mathrm{R} 3 \\ \hline \end{array}$ | 30 hHz Low Pass Filter <br> Connector, Receptacle: BNC Series <br> Coil, Toroidal <br> Cover Assembly (Not Shown) <br> Resistor, Fixed, Composition: 8.2 ohm, $5 \%, 1 / 8 \mathrm{~W}$ <br> Resistor, Fixed, Composition: 560 ohm, $5 \%, 1 / 8$ <br> Same as R2 | 1 <br> 1 <br> 1 <br> 1 <br>  <br>  <br>  | $\begin{aligned} & 280093 \\ & \text { UG1094/U } \\ & 20681-208 \\ & 280091-1 \\ & \text { CF 1/8-8.2 OH.MS/J } \\ & \text { CF1/8-560 OH.MS/J } \end{aligned}$ | $\begin{aligned} & 14632 \\ & 80058 \\ & 14632 \\ & 14632 \\ & 09021 \\ & 09021 \end{aligned}$ | 74868 |



Figure 5-6. Type 791616-1 RF Filter (A2), Location of Components
5.6.2.1 Part 38009330 MHz Low Pass Filtep REP DESIG PREFIX A2A1



Figure 5-7. Part 28009330 hHz Low Pass Filter (A2A1), Location of Components
5.6.3 TYPE 791592-7 INPUT CONVERTER REF DESIG PREFIX A3



Figure 5-8. Type 791592-1 Input Converter (A3), Location of Components



Figure 5-9. Part 370611-7 1st Mixer, 1st IF (A3A1), Location of Components
5.6.3.2 Part 370646-6 2nd Mixer, 2nd IF REF DESIG PREFIX A3A2

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Cl | Capacitor, Variable, Ceramic: $2.5-11 \mathrm{pF}, 350 \mathrm{~V}$ | 1 | 538-011B2.5-11 | 72982 |  |
| C2 | Capacitor, Ceramic, Disc: 1000 pF, GMV, 500 V | 2 | B-GP1000 PF P | 91418 |  |
| C3 | Same as C2 |  |  |  |  |
| C4 | Capacitor, Ceramic, Disc: $0.01 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 5 | 34453-1 | 14632 |  |
| C5 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { C8 } \end{aligned}$ | Same as C4 |  |  |  |  |
| C9 | Capacitor, Ceramic, Disc: $0.1 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 1 | 34475-1 | 14632 |  |
| C10 | Capacitor, Ceramic, Disc: $470 \mathrm{pF}, 20 \%, 1000 \mathrm{~V}$ | 5 | BHD470-20 PCT | 91418 |  |
| C11 <br> Thru C13 | Same as C10 |  |  |  |  |
| C14 | Capacitor, Mica, Dipped: $47 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM05ED470G03 | 81349 |  |
| C15 | Same as C10 |  |  |  |  |
| C16 | Capacitor, Ceramic, Disc: $4.7 \mathrm{pF},+/-.25 \mathrm{pF}, 100 \mathrm{~N}$ | 1 | 8101-100-C0H0-479C | 72982 |  |
| C17 | Capacitor, Ceramic, Disc: $0.47 \mathrm{~F}, 20 \%$, 50 V | 1 | 34452-1 | 14632 |  |
| C18 | Capacitor, Electrolytic, Tantalum: $4.7 \mathrm{FF}, 20 \%, 35 \mathrm{~V}$ | 1 | 196 D 475 X0035JE3 | 56289 |  |
| C19 | Capacitor, Variable, Ceramic: 9 -35 pF, 350 V | 1 | 538-011D9-35 | 72982 |  |
| CR1 | Diode | 1 | 1 N 4446 | 80131 |  |
| CR2 | Diode | 1 | 5082-3039 | 28480 |  |
| FB1 | Ferrite Bead | 3 | 56-590-65-4 A | 02114 |  |
| FB2 | Same as FB1 |  |  |  |  |
| FB3 | Same as FB1 |  |  |  |  |
| FL1 | Filter, Bandpass: 10.7 MHz | 1 | 92266 | 14632 |  |
| J1 | Connector, Receptacle: SMC Series | 2 | 34520-1 | 14632 |  |
| J2 | Same as J1 |  |  |  |  |
| L1 | Coil, Fixed: 10 uh | 4 | 1537-36 | 99800 |  |
| L2 | Same as Ll |  |  |  |  |
| L3 | Same as L1 |  |  |  |  |
| L4 | Coil, Fixed: 0.56 uh | 1 | 202-11 | 99848 |  |
| L5 | Same as L1 |  |  |  |  |
| L6 | Coil, Fixed: 0.15 uH | 1 | 1537-00 | 99800 |  |
| L7 | Coil, Fixed: 0.33 uH | 1 | 1537-04 | 99800 |  |
| L8 | Coil, Fixed: 1.8 uH | 1 | 1537-18 | 99800 |  |
| MP1 | Transipad | 2 | 7717-89D AP | 13103 |  |
| : P2 2 | Transipad | 2 | 7717-22DAP | 13103 |  |
| MP3 | Transipad | 1 | 7717-46DAP | 13103 |  |
| Q1 | Transistor | 1 | 2N2222A | 80131 |  |
| Q2 | Transistor | 1 | CP643 | 12498 |  |
| Q3 | Transistor | 3 | 2N5109 | 80131 |  |
| Q4 | Same as Q3 |  |  |  |  |



Figure 5-10. Part 370646-7 2nd Mixer, 2nd IF (A3A2), Location of Components

REF DESIG PREFIX A3A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Q5 | Transistor | 1 | 2N2857/JAN | 81350 |  |
| Q6 | Same as Q3 |  |  |  |  |
| R1 | Resistor, Fixed, Film: 2.3 k, 5\%, 1/4W | 2 | CF $1 / 4-2.2 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R2 | Resistor, Fixed, Composition: 82 ohm,5\%, 1/4 W | 1 | RCR07G820JS | 81349 |  |
| R3 | Resistor, Fixed, Film: $100 \mathrm{hm}, 5 \%, 1 / 4 \mathrm{~W}$ | 5 | CF1/4-10 OH.MS/J | 09021 |  |
| 24 | Resistor, Fixed, Film: $1.8 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-1.8K/J | 09021 |  |
| 25 | Resistor, Fixed, Composition: 220 ohm, 5\%, 1/4 | N 2 | RCR07G221JS | 81349 |  |
| R6 | Resistor, Fixed, Composition: $3.3 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G332JS | 81349 |  |
| R7 | Same as R1 |  |  |  |  |
| R8 | Resistor, Fixed, Film: $1.0 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | CF1/4-1K/J | 09021 |  |
| R9 | Resistor, Fixed, Composition: 200 ohm, 5\%, 1/4 | W1 | RCR07G201JS | 81349 |  |
| R10 | Same as R3 |  |  |  |  |
| R11 | Resistor, Fixed, Composition: 47 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | W 1 | RCR07G470JS | 81349 |  |
| R12 | Resistor, Fixed, Composition: 4.7 ohm, 5\%, $1 / 4 \mathrm{~W}$ | W 1 | RCR07G4R7JS | 81349 |  |
| R13 | Resistor, Fixed, Composition: 68 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G680JS | 81349 |  |
| R14 | Resistor, Fixed, Composition: 390 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G391JS | 81349 |  |
| R15 | Same as R13 |  |  |  |  |
| R16 | Resistor, Fixed, Film: $2.7 \mathrm{k}, 5 \%$, $1 / 4 \mathrm{~W}$ | 1 | CF $1 / 4-2.7 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R17 | Same as R8 |  |  |  |  |
| R18 | Same as R3 |  |  |  |  |
| R19 | Resistor, Fixed, Composition: 22 ohm, 5\%, 1/4 W | 1 | RCR07G220JS | 81349 |  |
| R20 | Same as R5 |  |  |  |  |
| R21 | Resistor, Fixed, Composition: 560 ohm, 5\%, 1/4 | W 1 | RCR07G561JS | 81349 |  |
| R22 | Resistor, Fixed, Film: 150 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 2 | CF1/4-150 OH:MS/J | 09021 |  |
| R23 | Resistor, Fixed, Film: 15 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-15 OH:MS/J | 09021 |  |
| R24 | Same as R8 |  |  |  |  |
| R25 | Resistor, Fixed, Composition: 470 ohm, 5\%, 1/4 | W 1 | RCR07G471JS | 81349 |  |
| R26 | Resistor, Fixed, Composition: 330 ohm, 5\%, 1/4 | W 1 | RCR07G331JS | 81349 |  |
| R27 | Same as R3 |  |  |  |  |
| R28 | Resistor, Fixed, Film: 12 ohm, 5\%, 1/4 W | 1 | CF1/4-12 OHMS/J | 09021 |  |
| R29 | Same as R22 |  |  |  |  |
| R30 | Same as R3 |  |  |  |  |
| RA1 | Heatsink | 1 | 1118 C | 13103 |  |
| T1 | Transformer Assembly | 1 | 22295-53 | 14632 |  |
| T2 | Transformer Assembly | 1 | 22295-54 | 14632 |  |
| T3 | Transformer Assembly | 1 | 22295-56 | 14632 |  |
| T4 | Transformer Assembly | 1 | 22295-55 | 14632 |  |
| U1 | Mixer, Balanced: $0.05-200 \mathrm{MHz}$ | 1 | M9 A | 27956 |  |

### 5.6.4 TYPE 794278-1 FREQUENCY EXTENDER REF DESIG PREFIX FE A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER. } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | RECM |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | VLF Preselector, 1st LO Assembly | 1 | 794315-1 | 14632 |  |
| A2 | Input Converter, 2nd LO Assembly | 1 | 794316-1 | 14632 |  |
| W1P1 | Connector, Plug. Sub-min Straight Angle | 6 | UG1465/U | 80058 |  |
| W2P1 | Same as W1Pl |  |  |  |  |
| W3P1 | Same as W1P1 |  |  |  |  |
| W + P1 | Same as W1P1 |  |  |  |  |
| W1P2 | Connector, Plug, Sub-min Right Angle | 2 | UG1466U | 80058 |  |
| W2P2 | Same as W1P1 |  |  |  |  |
| W3P2 | Same as W1P1 |  |  |  |  |
| W4P2 | Same as W1P2 |  |  |  |  |
| W1 | Cable Assembly | 1 | 17300-320-1 | 14632 |  |
| W2 | Cable Assembly | 1 | 17300-320-2 | 14632 |  |
| W3 | Cable Assembly | 1 | 17300-320-3 | 14632 |  |
| W4 | Cable Assembly | 1 | 17300-320-4 | 14632 |  |

(SEE FIGURE 5-3, SHEET 2, FOR LOCATION OF FREQUENCY EXTENDER COMPONENTS)

Figure 5-11. Type 794278-1 Frequency Extender (FE A1), Location of Components
5.6.4.1 TYPE 794315-1 VHF PRESELECTOR/IST LO ASSEMBLYREF DESIG PREFIX PE-A1AI

$\square$


Figure 5-12. Type 794315-1 VHF Preselector/1st LO Assembly (A1A1), Location of Components

REF DESIG PREFIX FE-A1A1A1

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Cl | Capacitor, Electrolytic, Tantalum: 18uF, 10\%, 20 | 1 | 196D186 X9020KE3 | 56289 |  |
| C2 | Capacitor, Electrolytic, Tantalum: $1 \mathrm{uF}, 20 \%, 35$ | 1 | 1960105 X0035 HE3 | 56289 |  |
| C3 | Capacitor, Polyes., Foil: $0.01 \mathrm{uF}, 2 \%, 100 \mathrm{~V}$ | 2 | PE51-.010-100-2 | 27735 |  |
| C4 | Same as C3 |  |  |  |  |
| C5 | Capacitor, Ceramic, Disc: $0.01 \mathrm{uF}, 20 \%, 50 \mathrm{~V}$ | 5 | 34453-1 | 14632 |  |
| C6 | Same as C5 |  |  |  |  |
| C7 | Capacitor, Ceramic, Disc: 0.1 UF, $20 \%, 50 \mathrm{~V}$ | 6 | 34475-1 | 14632 |  |
| C8 | Same as C7 |  |  |  |  |
| C9 | Same as C7 |  |  |  |  |
| C10 | Same as C5 |  |  |  |  |
| C11 | Same as C5 |  |  |  |  |
| $\begin{aligned} & \text { C12 } \\ & \text { Thru } \\ & \text { C14 } \end{aligned}$ | Same as C7 |  |  |  |  |
| C15 | Capacitor, Mics, Dipped: $300 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM05F D301G03 | 81349 |  |
| C16 | Capacitor, Mica, Dipped: $150 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | C:M05FD151G03 | 81349 |  |
| C17 | Same as C16 |  |  |  |  |
| C18 | Same as C15 |  |  |  |  |
| $\Sigma_{1}$ <br> Thru E18 | Terminal, Forked | 18 | 140-1941-02-01 | 71279 |  |
| L1 | Coil, Fixed: 10 uH, 10\% | 1 | 1537-36 | 99800 |  |
| R1 | Resistor, Fixed, Composition: $10 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 5 | RCR05G103JS | 81349 |  |
| R2 | Same as R1 |  |  |  |  |
| R3 | Resistor, Fixed, Composition: $47 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 2 | RCR07G473JS | 81349 |  |
| R4 | Resistor, Fixed, Composition: $15 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G153JS | 81349 |  |
| R5 | Same as R3 |  |  |  |  |
| R6 | Same as R4 |  |  |  |  |
| R7 | Resistor, Fixed, Composition: 22 ohms, 5\%, 1/4 W | 1 | RCR07G220JS | 81349 |  |
| R8 | Resistor, Fixed, Composition: 750 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G751JS | 81349 |  |
| R9 | Same as R8 |  |  |  |  |
| R10 | Resistor, Fixed, Composition: $3.0 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G302JS | 81349 |  |
| R11 | Resistor, Fixed, Composition: $1.0 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G102JS | 81349 |  |
| R12 | Resistor, Fixed, Composition: $2.2 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G222JS | 81349 |  |
| R13 | Resistor, Fixed, Composition: $1.5 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | RCR07G152JS | 81349 |  |
| R14 | Same as R13 |  |  |  |  |
| R15 | Same as R13 |  |  |  |  |
| R16 <br> thru <br> R18 | Same as R1 |  |  |  |  |
| 19 | Resistor, Fixed, Film: $4.22 \mathrm{k}, 1 \%, 0.10 \mathrm{w}$ | 2 | RN55C4221F | 81349 |  |

REF DESIG PREFIX FE-A1A1A1



Figure 5-13. Type 370689-1 1st LO Synthesizer (AlAlA1). Location of Components
5.6.4.1.2TYPE 370690-1 VCO PRINTED CIRCUIT ASSEMBLY REF DESIG PREFIX FE-A1A1A2

| REF DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CR1 | Diode | 3 | MPN3401 | 04713 |  |
| CR2 | Same as CRI |  |  |  |  |
| CR3 | Same as CR1 |  |  |  |  |
| CR4 | Diode | 1 | U11-3102 | 52673 |  |
| Cl | Capacitor, Ceramic, Chip: $2200 \mathrm{pF},+/-10 \%$, 50 V | 2 | C1005C222K5XAH | 26654 |  |
| C2 | Capacitor, Ceramic, Chip: 200 pF , NOP 50\%, 500 | $\vee 9$ | 32-257578-40 | 91984 |  |
| C3 | Same as C2 |  |  |  |  |
| C4 | Same as C2 |  |  |  |  |
| C5 | Not Used |  |  |  |  |
| C6 | Capacitor, Ceramic, Chip: 3 pF, .25 pF Tol, 500 | V1 | 603C0G3R0C | 91984 |  |
| C7 | Capacitor, Ceramic, Mono: $6.8 \mathrm{pF},+/-.5 \mathrm{pF}, 100$ | V 1 | 8101-100-C0H0-6890 | 72982 |  |
| C8 | Capacitor, Ceramic, Tub: $3.9 \mathrm{pF}, 10 \%, 500 \mathrm{~V}$ | 1 | QC3.9PFK | 95121 |  |
| C9 | Capacitor, Composition, Tub: $1.0 \mathrm{pF}, 10 \%, 500$ | 1 | QC1.0PFK | 95121 |  |
| C10 | Not Used |  |  |  |  |
| C11 | Not Used |  |  |  |  |
| C12 | Same as C2 |  |  |  |  |
| C13 | Same as C2 |  |  | . |  |
| C14 | Same as C2 |  |  |  |  |
| C15 | Capacitor, Ceramic, Disc: $470 \mathrm{pF}, 5 \%, 50 \mathrm{~V}$ NPO | 2 | 8121-050-C0G0-471J | 72982 |  |
| C16 | Same as C15 |  |  |  |  |
| C17 | Same as C2 |  |  |  |  |
| C18 | Same as C2 |  |  |  |  |
| C19 | Same as C2 |  |  |  |  |
| C20 | Same as C1 |  |  |  |  |
| C21 | Capacitor, Ceramic, Disc: $0.01 \mathrm{uF}, 20 \%, 50 \mathrm{~V}$ | 1 | 34453-1 | 14632 |  |
| E1 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { E11 } \end{aligned}$ | Terminal, Forked | 11 | 140-1941-02-01 | 71279 |  |
| L1 | Coil, Air | 1 | 24592-2 | 14632 |  |
| L2 | Coil, Air | 1 | 24592-3 | 14632 |  |
| L3 | Coil, Air | 1 | 24593-4 | 14632 |  |
| L3 | Coil, Air | 1 | 24593-3 | 14632 |  |
| L5 | Coil, Fixed: 0.56 uh, 15\%. | 1 | 202-11 | 99848 |  |
| Q1 | Transistor | 1 | U310 | 17856 |  |
| Q2 | Transistor | 2 | 2N2857/JAN | 81350 |  |
| Q3 | Same as Q2 |  |  |  |  |
| R1 | Resistor, Fixed, Composition: 100 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR05G101JS | 81349 |  |
| R2 | Resistor, Fixed, Composition: $33 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | RCR05G333JS | 81349 |  |
| R3 | Not Used |  | . |  |  |
| R4 | Same as R2 |  |  |  |  |

REF DESIG PREFIX PE-A1A1A2



Figure 5-14. Type 370690-1 VCO (A1A1A2),
Location of Components
5.6.4.1.3TYPE 794274-1 PRESELECTOR

REF DESIG PREFIX FE-A1A1A3


REF DESIG PREFIX PE-A1A1A3



Figure 5-15. Type 794274-1 Prelelector (A1A1A3), Location of Components
5.6.4.2 TYPE 794316-1 INPUT CONVERTER/2ND LO ASSEMBLYREF DESIG PREFIX FE-A1A2



Figure 5-16. Type 794316-1 Input Converter/2nd LO Assembly(A1A2), Location of Components

5．6．4．2．1TYPE 794270－1 2ND LOCAL OSCILLATOR
REF DESIG PREFIX FE－A1A2A1

| REF <br> DESIG | DESCRIPTION ． | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER＇S PART NO． | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| CR1 | Diode，Varicap： 11 pF at $3 \mathrm{Vdc}, 2 \mathrm{pF}$ at 25 Vdc ． $F$ equals 1 MHz | 1 | KV3901 | 52673 |  |
| C1 | Capacitor，Ceramic，Disc： $0.1 \mathrm{uF}, 20 \%, 50 \mathrm{~V}$ | 8 | 34475－1 | 14632 |  |
| C2 | Capacitor，Electrolytic，Tantalum：18uF，10\％， 20 | 1 | 196D186 X9020KE3 | 56289 |  |
| C3 | Capacitor，Electrolytic，Tantalum： $1 \mathrm{uF}, 20 \%, 35$ | 11 | $196 \mathrm{D} 105 \times 0035 \mathrm{HE} 3$ | 56289 |  |
| C4 | Capacitor，Polyes．，Foil： 0.015 uF，2\％， 100 V | 2 | PE51－．015－100－2 | 27735 |  |
| C5 | Same as C4 |  |  |  |  |
| C6 | Same as Cl |  |  |  |  |
| C7 | Capacitor，Ceramic，Disc： 0.01 uF，20\％， 50 V | 1 | 34453－1 | 14632 |  |
| C8 | Same as C1 |  |  |  |  |
| C9 | Same as Cl | － |  |  |  |
| C10 | Same as C1 |  |  |  |  |
| C11 | Capacitor，Ceramic，Disc： 1000 pF，10\％， 200 V | 4 | CK05BX102K | 81349 |  |
| C12 | Same as Cll |  |  |  |  |
| C13 | Same as C1 |  |  |  |  |
| C14 | Same as C1 |  |  |  |  |
| C15 | Capacitor，Ceramic，Tubular： $3.3 \mathrm{pF},+/-.25,500 \%$ | 1 | 301－000C0J0－339C | 72982 |  |
| C16 | Capacitor，Ceramic，Tubular： $2.2 \mathrm{pF},+/-.25,500 \gamma$ | 1 | 301－000C0J0－229C | 72982 |  |
| C17 | Same as Cll |  |  |  |  |
| C18 | Same as Cll |  |  |  |  |
| C19 | Capacitor，Variable，Ceramic： $2.5-11 \mathrm{pF}, 350 \mathrm{~V}$ | 1 | 538－011B2．5－11 | 72982 |  |
| C20 | Same as C1 |  |  |  |  |
| C21 | Capacitor，Ceramic，Disc： 3900 DF， $10 \%, 100 \mathrm{~V}$ | 2 | CK06B X392K | 81349 |  |
| C22 | Same as C21 |  |  |  |  |
| C23 | Capacitor，Mica，Dipped： $270 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 4 | C．M05FD271G03 | 81349 |  |
| C24 | Same as C23 |  |  |  |  |
| C25 | Same as C23 |  |  |  |  |
| C26 | Same as C23 |  |  |  |  |
|  |  |  |  |  |  |
| Thru E4 | Terminal，Forked | 4 | 140－1941－02－01 | 71279 |  |
| L1 | Coil，Fixed： 10 uH，10\％ | 1 | 1537－36 | 99800 |  |
| L2 | Coil，Fixed：． 032 uH | 1 | 75F328．MPC | 76493 |  |
| Q1 | Transistor | 2 | U310 | 17856 |  |
| Q2 | Same as Q1 |  |  |  |  |
| R1 | Resistor，Fixed，Composition： $1.5 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G152JS | 81349 |  |
| R2 | Resistor，Fixed，Composition： 240 ohms，5\％，1／4W | 1 | RCR07G241JS | 81349 |  |
| R3 | Resistor，Fixed，Composition： $3.9 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 4 | RCR07G392JS | 81349 |  |
| R4 | Resistor，Fixed，Composition： $22 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G223JS | 81349 |  |
| R5 | Same as R3 |  |  |  |  |

REF DESIG PREFIX FE-A1A2A1



[^1]5.6.4.2.2TYPE 270907-1 2ND LO CONVERSION

REF DESIG PREFIX FE-A1A2A2

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline Q T Y \\ P E R \\ A S S Y \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Cl | Capacitor, Ceramic, Disc: . $1 \mathrm{uF}, 20 \%, 50 \mathrm{~V}$ | 4 | 34475-1 | 14632 |  |
| C2 | Same as C1 |  |  |  |  |
| C3 | Capacitor, Ceramic, Disc: 200 pF, 5\%, 100 V | 3 | 8121-100-C0G0-201J | 72982 |  |
| C4 | Same as Cl |  |  |  |  |
| C5 | Same as C3 |  |  |  |  |
| C6 | Same as C3 |  |  |  |  |
| C7 | Same as Cl |  |  |  |  |
| E1 |  |  |  |  |  |
| Thru <br> E4 | Terminal, Forked | 4 | 140-1941-02-01 | 71279 |  |
| L1 | Coil, Fixed: 10 uH, 10\% | 2 | 1537-36 | 99800 |  |
| L2 | Same as Ll |  |  |  |  |
| R1 | Resistor, Fixed, Composition: 300 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | $N 2$ | RCR07G301JS | 81349 |  |
| R2 | Resistor, Fixed, Composition: 18 ohms, 5\%, 1/4 W | 1 | RCR07G180JS | 81349 |  |
| R3 | Same as R1 |  |  |  |  |
| U1 | Amplifier: $5-300 \mathrm{MHz}$ | 1 | A87-2 | 14482 |  |
| U2 | Amplifier: $5-500 \mathrm{MHz}$ | 1 | A72 | 14482 |  |
| U3 | Mixer, Balanced | 1 | M2B | 14482 |  |

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REF DESIG PREFIX FE-A1A2A3



Figure 5-19. Type 270901-1 1st Conversion (A1A2A3), Location of Components
5.6.4.3 TYPE 794276-1 RF INPUT SWITCH

REF DESIG PREFIX FE-A2



Figure 5-20. Part 794276-1 RF Input Switch Assembly (FE-A2), Location of Components
5.6.4.3.1Type 270935-1 RP Input Switch PW Assembly REF DESIG PREFIX PE-A2A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{array}{\|c\|} \hline \text { RECM } \\ \text { VENDOR } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \mathrm{C} 1 \\ & \mathrm{C} 2 \end{aligned}$ | Capacitor, Ceramic, Disc: . $1 \mathrm{uF}, 20 \%, 50 \mathrm{~V}$ Same as C1 | 2 | 34475-1 | 14632 |  |
| E1 | Terminal/Forked .062 Mat'l Thkness $x$. 156 High $.046 \times .094$ Deep Groove, Silver Plate | 3 | 140-1941-02-01 | 71279 |  |
| E2 | Same as E1 |  |  |  |  |
| E3 | Same as E1 |  |  |  |  |
|  | Connector, Receptacle: SMC Straight PC Mount | 5 | 34520-1 | 14632 |  |
| J2 <br> Thru J5 | Same as J1 |  |  |  |  |
| U1 | Switch/RF, SP2T 5 Vde © 100 VA PC, Mt. Freq. $1-100 \mathrm{MHz}$ | 2 | DS0042-10 | 28983 |  |
| U2 | Same as U1 |  |  |  |  |



Figure 5-21. Type 270935-1 RF Input Switch, PW Assembly (FE-A2A1), Location of Components

### 5.6.4.4 TYPE 794327-1 1 MHZ FILTER ASSEMBLY REF DESIG PREFIX FE-A3

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Mica, Dipped: $820 \mathrm{pF}, 2 \%, 300 \mathrm{~V}$ | 1 | D M15-821G | 72136 |  |
| C2 | Capacitor, Mica, Dipped: $36 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CMC4ED360G03 | 81349 |  |
| C3 | Capacitor, Mica, Dipped: 1200 pF, $2 \%, 100 \mathrm{~V}$ | 1 | D. $\mathrm{M} 15-122 \mathrm{G}$ | 72136 |  |
| C4 | Capacitor, Mica, Dipped: 91 pF, 2\%, 500 V | 1 | CM04FD910G03 | 81349 |  |
| C5 | Capacitor, Mica, Dipped: 750 pF | 1 | D.M15-751G | 72136 |  |
| E1 | Term., Feedthru, Ins. | 1 | SFU16Y | 04013 |  |
| J1 | Connector, Receptacle | 2 | 10-0104-002 | 19505 |  |
| J2 | Same as J1 |  |  |  |  |
| L1 | Coil, Fixed, Mold.: 39 uH | 1 | 1025-58 | 99800 |  |
| L2 | Coil, Fixed: 33 uh, 10\% | 1 | 1025-56 | 99800 |  |
| R1 | Resistor, Fixed, Composition: 220 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR05G221JS | 81349 |  |



## * Denotes hidden parts

Figure 5-22. Type 794327-1 1 MHz Assembly (FE-A3), Location of Components

### 5.6.5 TYPE 791569-1 IF MOTHERBOARD

REF DESIG PREFIX A4



Figure 5-23. Type 791569-1 IF hotherboard (A4), Location of Components
5.6.5.1 Type 791594-1 10.7 MHz Filter Switch REF DESIG PREFIX A4AI



Figure 5-24. Type 791594-1 10.7 MHz Filter Switch (A4A1), Location of Components

REF DESIG PREFIX A4A1

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER. } \\ \text { ASSY } \\ \hline \end{array}$ | MANL'FACTURER'S PART NO. | MFR. <br> CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R6 | Same as R2 |  |  |  |  |
| R7 | Resistor, Fixed, Composition: 680 ohms,5\%, 1/4 ¢ | 3 | CF1/4-680 OHMS/J | 09021 |  |
| R8 | Same as R7 |  |  |  |  |
| R9 | Same as R7 |  |  |  |  |
| R10 | Resistor, Fixed, Composition: 10 ohms,5\%, 1/4 W | 6 | CF1/4-10 OHYS/J | 09021 |  |
| 811 | Resistor, Fixed, Composition: 220 ohms,5\%, 1/4 W | 3 | CF1/4-220 OH.MS/J | 09021 |  |
| R12 | Resistor, Fixed, Composition: 22 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 5 | CF1/4-22 OHUS/J | 09021 |  |
| R13 | Resistor, Fixed, Composition: 33 ohms,5\%,1/4 W | 5 | CF1/4-33 OH.MS/J | 09021 |  |
| R14 | Same as R10 |  |  |  |  |
| R15 | Same as R11 |  |  |  |  |
| R16 | Same as R12 |  |  |  |  |
| R17 | Same as R13 |  |  |  |  |
| R18 | Same as R10 |  |  |  |  |
| R19 | Same as R11 |  |  |  |  |
| R20 | Same as R12 |  |  |  |  |
| R21 | Same as R13 |  |  |  |  |
| R22 | Same as R13 |  |  |  |  |
| R23 | Resistor, Fixed, Composition: 510 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 4 | CF1/4-510 OHMS/J | 09021 |  |
| R24 | Same as R13 |  |  |  |  |
| R25 | Resistor, Fixed, Composition: 100 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 7 | CF1/4-100 OHMS/J | 09021 |  |
| R26 | Resistor, Variable, Film: 200 ohms, 10\%, 1/2 W | 3 | 62 PR 200 | 73138 |  |
| R27 | Same as R25 |  |  |  |  |
| R28 | Same as R26 |  |  |  |  |
| R29 | Same as R25 |  |  |  |  |
| R30 | Same as R26 |  |  |  |  |
| R31 | Same as R12 |  |  |  |  |
| R32 | Resistor, Fixed, Composition: 22 k ohm, $5 \%, 1 / 4 \mathrm{k}$ | 3 | CF $1 / 4-22 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R33 | Resistor, Fixed, Composition: 4.7 k ohm, $5 \%, 1 / 4$ | 3 | CF1/4-4.7K/J | 09021 |  |
| R34 | Same as R32 |  |  |  |  |
| R35 | Same as R33 |  |  |  |  |
| R36 | Same as R32 |  |  |  |  |
| R37 | Same as R33 |  |  |  |  |
| R38 | Resistor, Fixed, Composition: 560 ohms, $5 \%, 1 / 4 W$ | 4 | CF 1/4-560 OHMS/J | 09021 |  |
| R39 | Same as R38 |  |  |  |  |
| R40 | Same as R38 |  |  |  |  |
| R41 | Same as R10 |  |  |  |  |
| R42 | Resistor, Fixed, Composition: 47 ohms,5\%, 1/4 W | 3 | CF 1/8-47 OHMS/J | 09021 |  |
| R43 | Same as R10 |  |  |  |  |
| ${ }^{2} 44$ | Resistor, Fixed, Composition: 12 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 3 | CF1/4-12 OHMS/J | 09021 |  |

REF DESIG PREFIX AAAI

5.6.5.2 Type $794254-1 \quad 10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter

REF DESIG PREFIX A4A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER. } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Ceramic, Disc | 1 | 8121-100-C0G0-910J | 14632 |  |
| C2 | Capacitor, Variable, Ceramic: $9-35 \mathrm{pF}, 350 \mathrm{~V}$ | 1 | 538-011D9-35 | 72982 |  |
| C3 | Capacitor, Ceramic, Disc | 17 | 34453-1 | 14632 |  |
| C4 | Same as C3 |  |  |  |  |
| C5 | Same as C3 |  |  |  |  |
| C6 | Same as C3 |  |  |  |  |
| C7 | Capacitor, Ceramic, Dise: $0.1 \mathrm{uF}, 20 \%, 50 \mathrm{~V}$ | 8 | 34475-1 | 14632 |  |
| C8 | Same as C7 |  |  |  |  |
| C9 | Same as C7 |  |  |  |  |
| C10 | Same as C7 |  |  |  |  |
| C11 | Same as C3 |  |  |  |  |
| C 12 | Same as C7 |  |  |  |  |
| C13 | Same as C7 |  |  |  |  |
| C14 | Capacitor, Electrolytic, Tantalum: 18uF, 20\%, 50V | $\vee 2$ | 1960186 X9020KE3 | 56289 |  |
| C15 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { C19 } \end{aligned}$ | Same as C3 |  |  |  |  |
| C20 | Same as C7 |  |  |  |  |
| C21 | Same as C7 |  |  |  |  |
| C22 | Same as C3 |  |  |  |  |
| C23 | Capacitor, Ceramic, Disc: $130 \mathrm{pF}, 5 \%, 100 \mathrm{~V}$ | 1 | 8121-100-C0G0-131J | 72982 |  |
| $\begin{aligned} & \text { C24 } \\ & \text { Thru } \\ & \text { C28 } \end{aligned}$ | Same as C3 |  |  |  |  |
| C29 | Capacitor, Ceramic, Disc: $68 \mathrm{pF}, 5 \%, 100 \mathrm{~V}$ | 1 | 8121-100-C0G0-680J | 72982 |  |
| C30 | Capacitor, Ceramic, Dise | 1 | 8121-100-C0G0-361J | 14632 |  |
| C31 | Same as C3 |  |  |  |  |
| C32 | Capacitor, Ceramic, Dise | 2 | 8131-100-C0G0-392J | 14632 |  |
| C33 | Same as C32 |  |  |  |  |
| C34 | Capacitor, Ceramic, Disc | 1 | 8121-100-C0G0-162J | 14632 |  |
| C35 | Same as Cl4 |  |  |  |  |
| FL1 | Filter, Bandpass | 1 | 92246 | 14632 |  |
| Ll | Coil, Fixed, Molded: 1.5 uH, 10\% | 1 | 1025-24 | 99800 |  |
| L2 | Coil, Fixed, Molded: $1.8 \mathrm{MH}, 10 \%$ | 1 | 1025-26 | 99800 |  |
| L3 | Coil, Fixed, Molded: 100 uH, 10\% | 1 | 1025-68 | 99800 |  |
| L4 | Coil, Fixed: 3.3 ut | 1 | 1025-32 | 99800 |  |
| L5 | Coil, Fixed, Molded: $12 \mathrm{uH}, 10 \%$ | 1 | 1025-46 | 99800 |  |
| L6 | Coil, Fixed, Molded: 82 uH | 1 | 1025-66 | 99800 |  |
| Q1 | Transistor | 4 | 2N3904 | 801.31 |  |
| Q2 | Same as Q1 |  |  |  |  |
| Q3 | Same as Q1 |  |  |  |  |

REF DESIG PREFIX A4A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Q4 | Same as Q1 |  |  |  |  |
| Q5 | Transistor | 1 | 2N2708 | 18714 |  |
| R1 | Resistor, Fixed, Film: $13 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | CF $1 / 4-13 \mathrm{~K} / \mathrm{J}$ | $09021$ |  |
| R2 | Resistor, Fixed, Film: $3.0 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | CF $1 / 4-3 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R3 | Same as R1 |  |  |  |  |
| R4 | Same as R2 |  |  |  |  |
| R5 | Resistor, Fixed, Film: 10 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 4 | CF $1 / 4-10$ OH.MS/J | 09021 |  |
| R6 | Resistor, Fixer, Film: 220 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 2 | CF1/4-220 OH:MS/J | 09021 |  |
| R7 | Resistor, Fixed, Film: 22 ohms, 5\%, 1/4 W | 6 | CF1/4-22 OHMS/J | 09021 |  |
| R8 | Resistor, Fixed, Film: 680 ohms, $5 \%, 1 / 4$ w | 2 | CF1/4-680 OHMS/J | 09021 |  |
| R9 | Resistor, Fixed, Film: 33 ohms, $5 \%, 1 / 4 \mathrm{~W}$ | 5 | CF1/4-33 OHMS/J. | 09021 |  |
| R10 | Same as R5 |  |  |  |  |
| R11 | Same as R6 |  |  |  |  |
| R12 | Same as R7 |  |  |  |  |
| R13 | Same as R8 |  |  |  |  |
| R14 | Same as R9 |  |  |  |  |
| R15 | Same as R7 |  |  |  |  |
| R16 | Resistor, Fixed, Film: 100 ohms, 5\%, 1/4 W | 5 | CF $1 / 4-100$ OH US/J | 09021 |  |
| R17 | Resistor, Trim, Film: 200 ohms, 10\%, $1 / 2 \mathrm{~W}$ | 2 | 62 PR200 | 73138 |  |
| R18 | Same as R16 |  |  |  |  |
| R19 | Same as R9 |  |  |  |  |
| R20 | Same as R9 |  |  |  |  |
| R21 | Resistor, Fixed, Film: 560 ohms, 5\%, 1/4 W | 4 | CF1/4 560 OHMS/J | 09021 |  |
| R22 | Same as Ri7 |  |  |  |  |
| R 23 | Resistor, Fixed, Film: $22 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | CF1/4-22K/J | 09021 |  |
| R24 | Resistor, Fixed, Film: $4.7 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | CF1/4 $4.7 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R25 | Same as R23 |  |  |  |  |
| R26 | Same as R24 |  |  |  |  |
| R27 | Same as R5 |  | . |  |  |
| R28 | Same as R21 |  |  |  |  |
| R29 | Resistor, Fixed, Film: 12 ohms, 5\%, 1/4 W | 2 | CF1/4-12 OHMS/J | 09021 |  |
| R30 | Same as R5 |  |  |  |  |
| R31 | Resistor, Fixed, Film: 560 ohms, $5 \%, 1 / 4$ W | 1 | CF1/4 560 OHMS/J | 09021 |  |
| R32 | Same as R29 |  | - |  |  |
| R33 | Same as R7 |  |  |  |  |
| R34 | Same as R16 |  |  |  |  |
| R35 | Same as R16 |  |  |  |  |
| R36 | Resistor, Fixed, Film: $33 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 C | CF $1 / 4-33 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R37 | Resistor, Fixed, Film: $6.2 \mathrm{k}, 5 \%, 1 / 4 \mathrm{H}$ | 1 | CF $1 / 4-6.2 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R38 | Resistor, fixed, Film: $10 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 C | CF1/4-10K/J | 09021 |  |

REF DESIG PREFIX A4A2



Figure 5-25. Type 794254-1 $10.7 \mathrm{MHz} / 455 \mathrm{kHz}$ Converter (A4A2), Location of Components

### 5.6.5.3 Type 791595-1 455 kHz Filter Switch

REF DESIG PREFIX A4A3

ref desig prefix a4a3



Figure 5-26. Type 791595-1 455 kHz Filter Switch (A4A3).
Location of Components

REF DESIG PREFIX A4A6

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C 1 | Capacitor, Electrolytic, Tantalum: $47 \mathrm{uF}, 10 \%, 20$ Not Used | $\checkmark 2$ | CS13BE476K | 81349 | 56289 |
| C3 | Capacitor, Ceramic, Disc: $0.47 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 2 | 34452-1 | 14632 |  |
| C4 | Capacitor, Electrolytic, Tantalum: $33 \mathrm{uF}, 10 \%, 10 \mathrm{~V}$ | 1 | CS13BC336K | 81349 | 56289 |
| C5 | Same as C3 |  |  |  |  |
| C6 | Capacitor, Ceramic, Disc: $0.1 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 1 | 34475-1 | 14632 |  |
| C7 | Same as C1 |  |  |  |  |
| C8 | Same as C6 |  |  |  |  |
| CR1 | Not Used |  |  |  |  |
| CH2 | Not Used |  |  |  |  |
| CR3 | Not Used |  |  |  |  |
| CR4 | Not Used |  |  |  |  |
| CR5 | Diode | 5 | 1N4449 | 80131 | 93332 |
| CR6 <br> Thru CR9 | Same as CR5 |  |  |  |  |
| CR10 | Diode | 1 | 5082-2800 | 28480 |  |
| Q1 | Transistor | 6 | 2N2222A | 80131 | 04713 |
| Q2 | Transistor | 1 | 2N 2907/JAN | 81350 |  |
| Q3「hru Q7 | Same as Q1 |  |  |  |  |
| R1 | Resistor, Fixed, Film: $100 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 5 | CF1/4-100K/J | 09021 |  |
| R2 | Resistor, Fixed, Film: $47 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | CF $1 / 4-47 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R3 | Resistor, Fixed, Composition: $470 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G474JS | 81349 |  |
| K4 | Resistor, Fixed, Film: 100 ohms 5\%, 1/4 W | 5 | CF1/4-100 OHMS/J | 09021 |  |
| R5 | Same as R1 |  |  |  |  |
| R6 | Resistor, Fixed, Film: $330 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-330K/J | 09021 |  |
| K7 | Resistor, Fixed, Composition: $6.8 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 4 | RCR07G682JS | 81349 |  |
| R8 | Same as R4 |  |  |  |  |
| R9 | Resistor, Fixed, Film: $15 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 4 | CFI/4-15K/J | 09021 |  |
| R10 | Resistor, Fixed, Film: $150 \mathrm{k}, 5 \%, 1 / 4 \mathrm{iv}$ | 2 | CF1/4-150 K/J | 09021 |  |
| R11 | Resistor, Fixed, Film: $10 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 9 | CF1/4-10K/J | 09021 |  |
| R12 | Resistor, Fixed, Composition: $82 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G823JS | 81349 |  |
| R13 | Resistor, Fixed, Film: $1.0 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 5 | CF1/4-1.0K/J | 09021 |  |
| R14 | Resistor, Fixed, Film: $1.2 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF $1 / 4-1.2 \mathrm{~K} / \mathrm{J}$ | 09021 | $\cdots$ |
| R15 | Same as R7 |  |  |  |  |
| K16 | Same as R7 |  |  |  |  |
| R17 | Resistor, Fixed, Film: $22 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 C | CFI/4-22K/J | 09021 |  |
| R18 | Kesistor, Fixed, Film: $270 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1. | CF1/4-270K/J | 09021 |  |
| $R 19$ | Resistor, Fixed, Composition: $680 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 R | RCR07G684JS | 81349 |  |



Figure 5-26. Type 796175-1 AGC Amplifier (A4A6), Location of Components

REF DESIG PREFIX A4A6

|  | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R20 | Same as R11 |  |  |  |  |
| R21 | Same as R9 |  |  |  |  |
| R22 | Same as R9 |  |  |  |  |
| R23 | Same as R3 |  |  |  |  |
| R24 | Same as R9 |  |  |  |  |
| R25 | Resistor, Fixed, Film: $1.5 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF $1 / 4-1.5 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R26 | Resistor, Fixed, Film: $2.2 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-2.2K/J | 09021 |  |
| R27 | Same as R11 |  |  |  |  |
| R28 | Same as R4 |  |  |  |  |
| R29 | Same as R4 |  |  |  |  |
| R30 | Same as R11 |  |  |  |  |
| R31 | Resistor, Fixed, Film: $2.7 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-2.7K/J | 09021 |  |
| R32 | Resistor, Fixed, Film: 390 ohms, 5\%, 1/4 W | 2 | CF1/4-390 OHMS/J | 09021 |  |
| R33 | Resistor, Fixed, Film: $4.7 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | CF $1 / 4-4.7 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R34 | Not Used |  |  |  |  |
| R35 | Same as R33 |  |  |  |  |
| R36 | Resistor, Fixed, Composition: $68 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | RCR07G683JS | 81349 |  |
| R37 | Same as R1 |  |  |  |  |
| R38 | Same as R36 |  |  |  |  |
| R39 | Same as R36 |  |  |  |  |
| R40 | Same as R1 |  |  |  |  |
| R41 | Same as R7 |  |  |  |  |
| R42 | Same as R4 |  |  |  |  |
| R43 | Same as R2 |  |  |  |  |
| RS4 | Not Used |  |  |  |  |
| R45 | Same as R11 |  |  |  |  |
| R46* | Resistor, Fixed, Film: $39 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | CR1/4-39K/J | 09021 |  |
| R47 | Resistor, Fixed, Composition: 820 ohm, 5\%, 1/4 | W 2 | RCR07G821JS | 81349 |  |
| R48 | Resistor, Fixed, Composition: 68 ohms, 5\%, 1/4 | W 1 | RCR07G680JS | 81349 |  |
| R49 | Same as R46 |  |  |  |  |
| R50* | Resistor, Fixed, Film: $3.9 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | CR1/4-3.9K/J | 09021 |  |
| R51* | Same as R32 |  |  |  |  |
| R52 | Same as R13 |  |  |  |  |
| R53 | Same as R1 |  |  |  |  |
| R54 | Same as R10 |  |  |  |  |
| R55 | Resistor, Fixed, Film: $3.3 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-3.3K/J | 09021 |  |
| R56 | Resistor, Fixed, Film: $100 \mathrm{k}, 1 \%, 1 / 10 \mathrm{~W}$ | 1 | RN55C1003F | 81349 |  |
| R57 | Resistor, Fixed, Film: $1.5 \mathrm{k}, 1 \%, 1 / 10 \mathrm{~W}$ | 1 | RN55C1501F | 81349 |  |
| * | Nominal value, final value factory selected. |  |  |  |  |



| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Ceramic, Disc: $0.47 \mathrm{uF}, 20 \%, 50 \mathrm{~V}$ | 21 | 34452-1 | 14632 |  |
| C2 | Same as Cl |  |  |  |  |
| C3 | Capacitor, Ceramic, Disc: 0.01 UF, 20\%, 50 V | 2 | 34453-1 | 14632 |  |
| C4 | Capacitor, Ceramic, Disc: 0.1 uf, 20\%, 50 V | 2 | 34475-1 | 14632 |  |
| C5 | Same as C1 |  |  |  |  |
| C6 | Same as Cl |  |  |  |  |
| C7 | Same as C3 |  |  |  |  |
| C8 | Same as C4 |  |  |  |  |
| C9 | Same as Cl |  |  |  |  |
| C10 | Same as Cl |  |  |  |  |
| C11* | Capacitor, Mica, Dipped: $100 \mathrm{pf}, 2 \%, 500 \mathrm{~V}$ | $1{ }^{\text {- }}$ | CM05FD101G03 | 81349 |  |
| C12 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { C20 } \end{aligned}$ | Same as Cl |  |  |  |  |
| C21 | Not Used |  |  |  |  |
| C 22 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { C25 } \end{aligned}$ | Same as Cl |  |  |  |  |
| C26 | Capacitor, Mica, Dipped: 75 pf, $2 \%, 500 \mathrm{~V}$ | 1 | C:M05ED750G03 | 81349 |  |
| C27 | Same as Cl |  |  |  |  |
| C28 | Not Used |  |  |  |  |
| C29 | Capacitor, Electrolytic, Tantalum: 15 uF, 10\%, 20 V | 1 | CS13BE156K | 81349 | 56289 |
| C30 | Same as Cl |  |  |  |  |
| C31 | Capacitor, Ceramic, Disk: . 012 uf, 10\%, 100 V | 1 | CK06BX123K | 81349 |  |
| C32 | Not used |  |  |  |  |
| C33 | Not used |  |  |  |  |
| C34* | Capacitor, Mica, Dipped: $150 \mathrm{pf}, 2 \%, 500 \mathrm{~V}$ | 1 | CM05FD151G03 |  |  |
| C35 | Capacitor, Ceramic, Disk: 2200 pf, 5\%, 50 V, NPO | 1 | 8131-050-COGO-222J | 72982 |  |
| C36 | Same as C35 |  |  |  |  |
| CR1 | Diode | 3 | 1N4449 | 80131 | 93332 |
| CR2 | Same as CRI |  |  |  |  |
| CR3 | Diode, hot carrier | 2 | 5082-2800 | 28480 |  |
| CR4 | Same as CR3 |  |  |  |  |
| CR5 | Same as CR1 |  |  |  |  |
| L1 | Coil, Fixed: 6.8 mH | 5 | 553-3635-47 | 71279 |  |
| L2 | Same as L1 |  |  |  |  |
| L3 | Coil, variable | 2 | 558-7107-34 | 71279 |  |
| L4 | Same as L1 |  |  |  |  |
| L5 | Same as L1 |  |  |  |  |
| L6 | Same as L1 |  |  |  |  |
| L7 | Coil, Fixed: 3.3 mH | 15 | 553-3635-43 | 71279 |  |
| L8 | Coil, Variable Pot. Core Assembly | 13 | 30705-39 | 14632 |  |

REF DESIG PREFIX A4A7


Location of Components
Figure 5-27. Type 726002-2 455 kHz Amplifier/AM Detector (A4A7),

5.6.5.8 Type 791599-4 FM/CW/SSB Detector

REF DESIG PREFIX A4A9

| REF <br> DESIG | DESCRIPTION | $\begin{aligned} & \text { QTY } \\ & \text { PER } \\ & \text { ASSY } \end{aligned}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Cl | Capacitor, Ceramic, Disc: $0.47 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 8 | 34452-1 | 14632 |  |
| C2 |  |  |  |  |  |
| Thru C5 | Same as Cl |  |  |  |  |
| C6 | Capacitor, Mica, Dipped: $470 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | D W15-471G | 72136 |  |
| C7 | Capacitor, Mica, Dipped: $270 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 2 | CM05FD271G03 | 81349 | 72136 |
| C8 | Capacitor, Mica, Dipped: $390 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | C.M05F D391 G03 | 81349 | 72136 |
| C9 | Capacitor, Ceramic, Disc: $150 \mathrm{pF}, 5 \%, 50 \mathrm{~V}$ | 1 | IU150RJ | 93958 |  |
| C10 | Capacitor, Mica, Dipped: $330 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | C.M05FD331G03 | 81349 |  |
| C11 | Capacitor, Plastic, Tub: . 015 uF, 5\%, 100 V | 1 | 663Uw153-5-1W | 84411 |  |
| C12 | Same as C1 |  |  |  |  |
| C13 | Capacitor, Electrolytic, Tantalum: 18 uF, 10\%,20 | $V_{1}$ | 196 D186 X9020KE356289 |  |  |
| C14 | Same as Cl |  |  |  |  |
| C15 | Same as Cl |  |  |  |  |
| C16 | Capacitor, Ceramic, Disc: 1 F, $20 \%, 50 \mathrm{~V}$ | 1 | 8131-050-651-105M | 72982 |  |
| C 17 | Capacitor, Mica, Dipped: $2700 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM06FU272G03 | 81349 | 72136 |
| C18 | Capacitor, Electrolytic, Tantalum: 15 uF, 10\%,20 | $\checkmark 1$ | CS13BE156K | 81349 | 56289 |
| C19 | Capacitor, Electrolytic, Tantalum: 4.7 uF, $20 \%, 35$ | $\bigcirc 1$ | 196D475 X0035JE3 | 56289 |  |
| FB1 | Ferrite Bead | 2 | 56-590-65-4 A | 02114 |  |
| Fb2 | Same as FB1 |  |  |  |  |
| L1 | Coil, Variable | 1 | 30312-258 | 14632 |  |
| L2 | Not used |  |  |  |  |
| L3 | Coil, Fixed: 15 mH | 1 | 553-3635-51 | 71279 |  |
| Q1 | Transistor | 2 | 2N2907/JAN | 81350 |  |
| Q2 | Transistor | 2 | 2N2222A | 80131 | 04713 |
| Q3 | Same as Q1 |  |  |  |  |
| Q4 | Same as Q2 |  |  |  |  |
| R1 | Resistor, Fixed, Composition: $10 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 4 | RCR07G103JS | 81349 |  |
| R2 | Resistor, Fixed, Composition: $1.0 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | RCR07G102JS | 81349 |  |
| R3 | Resistor, Fixed, Composition: 220 ohm, 5\%, 1/4 | W 1 | RCR07G221JS | 81349 |  |
| R4 | Kesistor, Fixed, Composition: 47 ohms, 5\%, $1 / 4$ | W 3 | RCR07G470JS | 81349 |  |
| R5 | Resistor, Fixed, Composition: $68 \mathrm{k}, 5 \%, 1 / 4 \mathrm{H}$ | 3 | RCR07G683JS | 81349 |  |
| R6 | Resistor, Fixed, Composition: $47 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | RCR07G473JS | 81349 |  |
| R7 | Resistor, Fixed, Composition: $56 \mathrm{k}, 5 \%, 1 / 4 \mathrm{H}$ | 1 | RCR07G563JS | 81349 |  |
| R8 | Resistor, Fixed, Composition: $4.7 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G563JS | 81349 |  |
| R9 | Resistor, Fixed, Composition: $2.2 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~N}$ | 1 | RCR07G222JS | 81349 |  |
| R10 | Resistor, Fixed, Composition: $560 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G564JS | 81349 |  |
| R11 | Resistor, Fixed, Composition: $470 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G474JS | 81349 |  |
| R12 | Resistor, Fixed, Composition: $15 \mathrm{k}, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | RCR07G153JS | 8.1349 |  |
| R13 | Same as R12 |  |  |  |  |



Figure 5-28. Type 791599-4 FM, CW and SSB Detector (A4A9), Location of Components

REF DESIG PREFIX A4A9


### 5.6.5.9 Type 7459 Audio Amplifier

| REF DESIG | DESCRIPTION | QTY. PER ASSY. | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM. <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Ceramic, Disc: $0.47 \mu \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 6 | 34452-1 | 14632 |  |
| C2 | Capacitor, Ceramic, Disc: 0.1 HF, 20\%, 50 V | 2 | $33475-1$ |  |  |
| C3 | Same as C1 |  |  | 14632 |  |
| C4 | Capacitor, Electrolytic, Tantalum: $4.7 \mu \mathrm{~F}, 10 \%, 35 \mathrm{~V}$ | 2 | CS13BE475K | 81349 | 56289 |
| C5 | Not Used |  |  |  |  |
| C6 | Same as Cl |  |  |  |  |
| C7 | Same as C1 |  |  |  |  |
| C8 | Same as C2 |  |  |  |  |
| C9 | Same as C1 |  |  |  |  |
| C10 | Same as C4 |  |  |  |  |
| C11 | Not Used |  |  |  |  |
| C12 | Capacitor, Electrolytic, Tantalum: $15 \mu \mathrm{~F}, 10 \%, 20 \mathrm{~V}$ | 2 | CS13BE156K | 13 | 56 |
| C13 | Same as C12 |  |  |  |  |
| C14 | Same as C1 |  |  |  |  |
| C15 | Not Used |  |  |  |  |
| C16 | Not Used |  |  |  |  |
| C17 | Capacitor, Ceramic, Disc: $5000 \mathrm{pF}, \mathbf{2 0 \%}, 500 \mathrm{~V}$ | 1 | SM5000PFM | 91418 |  |
| C18 | Capacitor, Electrolytic, Tantalum: $47 \mu \mathrm{~F}, 10 \%, 35 \mathrm{~V}$ | 3 | CS13BE476K | $81349$ | 56289 |
| C19 | Same as C18 |  |  |  |  |
| C20 | Same as C18 |  |  |  |  |
| C21 | Capacitor, Mica, Dipped: $24 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | CM05ED240J03 |  |  |
| CR1 | Diode | 1 | 1N4449 |  | 72136 |
| CR2 | Diode |  | 1N4449 | 80131 | 93332 |
| CR3 | Same as CR2 | 2 | 1N198A | 80131 | 93332 |
| CR4 | Diode |  |  |  |  |
| Q1 | Transistor | 1 | 1N4003 | 80131 | 04713 |
| Q1 | Transistor | 1 | U1899E | 15818 |  |
| Q2 | Transistor | 1 | TIP 29 | 01295 |  |
| R1 | Resistor, Fixed, Composition: $22 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | RCR07G223JS | 81349 | 01121 |
| R2 | Resistor, Fixed, Composition: $330 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G334JS | 81349 | 01121 |
| R3 | Resistor, Fixed, Composition: $47 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G473JS |  |  |
| R4 | Same as R3 |  | RCR07G473JS | 81349 | 01121 |
| R5 | Resistor, Fixed, Composition: $2.2 \mathrm{M} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G225JS | 81349 |  |
| R6 | Resistor, Fixed, Film: $2.0 \mathrm{k} \Omega, 1 \%, 1 / 10 \mathrm{~W}$ | 2 | RN55C2001F | 81349 |  |
| R7 | Resistor, Fixed, Composition: $100 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 3 | RCR07G104JS |  | 01121 |
| R8 | Same as R7 |  | RCR07G104JS | 81349 | 01121 |
| R9 | Resistor, Fixed, Film: $100 \mathrm{k} \Omega, 1 \%, 1 / 10 \mathrm{~W}$ | 4 | RN55C1003F | 81349 |  |
| R10 | Same as R9 |  | RN5SC1003F | 81349 | 75042 |
| R11 | Same as R1 |  |  |  |  |
| R12 | Resistor, Fixed, Composition: $12 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G123JS |  |  |
| 13 | Resistor, Fixed, Composition: $27 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G273JS |  |  |
| 214 | Resistor, Fixed, Composition: $6.8 \mathrm{k} \Omega, 5 \%, 1 / 4 \mathrm{~W}$ |  |  | 81349 | 01121 |
|  |  | 2 | RCR07G682JS | 81349 | 01121 |

REF DESIG PREFIX A4A10



Figure 5－29．Type 7459 Audio Amplifier（A4A10）， Location of Components
5.6.6 TYPE 791570-1 SYNTHESIZER MOTHERBOARD REF DESIG PREFIX A5



Figure 5-30. Type 791570-1 Synthesizer Motherboard (A5), Location of Components

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline Q T Y \\ P E R \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | 1st LO VCO Assemoly | 1 | 791629 | 14632 |  |
| A2 | 1st and 3rd LO Synthesizer | 1 | 791600 | 14632 |  |
| Cl | Capacitor, Mica, Didped: $1600 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 2 | C M06FD162G03 | 81349 | 72136 |
| C2 | Capacitor, Ceramic, Disc: 0.47 uF, $20 \%, 100 \mathrm{~V}$ | 2 | 8131.M100-651-474n | 72982 |  |
| C3 | Same as Cl |  |  |  |  |
| $\mathrm{C4}$ | Capacitor, Ceramic, Disc: 0.05 UF, 20\%, 100 V | 2 | C023B101R503.M | 56289 |  |
| C5 | Capacitor, Electrolytic, Tantalum: $47 \mathrm{uF}, 20 \%, 20$ | $\mathrm{V}_{2}$ | 1960475 X0020-PE4 | 56289 |  |
| C6 | Same as C2 |  |  |  |  |
| C7 | Same as C5 |  |  |  |  |
| C8 | Same as C4 |  |  |  |  |
| C9 | Capacitor, Electrolytic, Tantalum: 2.2 uF,20\%,35 | $N 1$ | 196 D 225 X 0035 JE 3 | 56289 |  |
| FB1 | Ferrite Bead | 17 | 56-590-65-4 A | 02114 |  |
| FB2 <br> Thru <br> FB17 | Same as FB1 |  |  |  |  |
| L1 | Coil, Fixed: 10 mH | 2 | 553-3635-49 | 71279 |  |
| L2 | Coil, Fixed: 0.82 uH | 1 | 1537-10 | 99800 |  |
| L3 | Same as Ll |  |  |  |  |
| L4 | Coil, Fixed: 4.7 mH | 1 | 553-3635-45 | 99800 |  |
| MP1 | Terminal | 20 | S0S1 | 04013 |  |
| UP2 | Insulator | 1 | 60-11-5791-1674 | 18565 |  |
| R1 | Resistor, Fixed, Composition: 100 ohms, 5\%, 1/4 | W 1 | CF1/4-100 OHVS/J | 09021 |  |
| R2 | Resistor, Fixed, Film: 10 k ohms, $1 \%, 1 / 10 \mathrm{~W}$ | 1 | RN55C1002F | 81349 | 75042 |
| R3 | Resistor, Fixed, Film: 1.0 k ohms, $1 \%, 1 / 10 \mathrm{w}$ | 1 | RN55C1001F | 81349 | 75042 |
| R4 | Resistor, Fixed, Composition: 1.0k ohms,5\%, 1/4 | W 1 | CF1/4-1.0K/J | 09021 |  |
|  | Resistor, Fixed, Film: 1.82 k ohms, $1 \%, 1 / 10$ w | 1 | RN55C1821F | 81349 | 75042 |
| VR1 | Voltage Regulator | 1 | MC7912CP | 04713 |  |



Figure 5-31. Type 791630-1 1st and 3rd LO Synthesizer/Timebase (A5A1), Location of Components (Sheet 1 of 2 )


Figure 5-31. Type 791630-1 1st and 3rd LO Synthesizer/Timebase (A5A1), Location of Components (Sheet 2 of 2)
5.6.6.1.1Type 791629 1st LO VCO Assembly REF DESIG PREFIX A5A1A1



Figure 5-32. Type 791629 1st LO VCO Assembly (A5A1A1), Location of Components
5.6.6.1.2Part 34750 1st LO Voltage Controlled Oscillator REF DESIG PREFIX A5A1A1A1

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C 1 | Capacitor, Ceramic, Chip: $200 \mathrm{pF}, 50 \%, 500 \mathrm{~V}$ | 10 | 32-257578-40 | 91984 |  |
| C2 |  |  |  |  |  |
| Chru $\mathrm{C4}$ | Same as C1 |  |  |  |  |
| C5 | Capacitor, Ceramic, Chip: $3 \mathrm{pF}, 500 \mathrm{~V}$ | 1 | 603C0G3R0C | 91984 |  |
| C6* | Capacitor, Ceramic, Tubular:5.1 pF, $+/-0.5 \mathrm{pF}, 500 \mathrm{~V}$ | V 2 | 301-000C0H0-519D | 72982 |  |
| C7 | Capacitor, Composition, Tubular: $2.7 \mathrm{pF}, 10 \%, 500 \mathrm{~V}$ | V 1 | QC2.7PFK | 95121 |  |
| C8 | Same as Cl |  |  |  |  |
| C9 | Capacitor, Compoosition, Tubular: $1.0 \mathrm{pF}, 10 \%, 500 \mathrm{~V}$ | V1 | QC1.0PFK | 95121 |  |
| C10 | Same as Cl |  |  |  |  |
| C11 | Capacitor, Ceramic, Disc: $0.1 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 1 | 34475-1 | 14632 |  |
| C12 | Same as Cl |  |  |  |  |
| C13 | Same as C1 |  |  |  |  |
| C14 | Capacitor, Ceramic, Disc: 470 pF, 20\%, 1000 V | 7 | BHD470-20 PCT | 91418 |  |
| C15 | Capacitor, Mica, Dipped: $100 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM04FD101G03 | 81349 | 72136 |
| C16 | Same as C1. |  |  |  |  |
| C17 | Same as C1 |  |  |  |  |
| C18 | Capacitor, Electrolytic, Tantalum: 2.2 uF, $10 \%, 2 \mathrm{VV}$ | 1 | CS13BE225K | 81349 | 56289 |
| $\begin{aligned} & \text { C19 } \\ & \text { Thru } \end{aligned}$ | Same as C14 |  |  |  |  |
| C21 | Same as C1 |  |  |  |  |
| C22 | Not Used |  |  |  |  |
| C23 | Same as C14 |  |  |  |  |
| C24 | Not Used |  |  |  |  |
| C25 | Same as C14 |  |  |  |  |
| C26 | Capacitor, Ceramic, Disc: $5000 \mathrm{pF}, 20 \%, 100 \mathrm{~V}$ | 2 | C023B101E502M | 56289 |  |
| C27 | Same as C26 |  |  |  |  |
| C28 | Same as C6 |  |  |  |  |
| C29 | Same as C14 |  |  |  |  |
| CH1 | Diode, Pin Switching | 3 | MPN3401 | 04713 |  |
| CR2 | Same as CR1 |  |  |  |  |
| CR3 | Same as CR1 |  |  |  |  |
| CR4 | Diode, Tuning VHF and UHF | 1 | U11-3102 | 52673 |  |
| FB1 | Ferrite Bead | 1 | 56-590-65-4 A | 02114 |  |
| L1 | Coil, Air | 1 | 24592-1 | 14632 |  |
| L2 | Coil, Air | 2 | 24593-1 | 14632 |  |
| L3 | Same as L2 |  |  |  |  |
| L4 | Coil, Air | 1 | 24593-2 | 14632 |  |
| Ls | Coil, Fixed: 0.56 uH | 1 | 202-11 | 99848 |  |
| - | Nominal value, final value factory selected. |  |  |  |  |

REF DESIG PREFIX A5A1A1A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASS' } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| viP1 | Transipad | 4 | 7717-46DAP | 13103 |  |
| MP2 | Transipad | 1 | 7717-22DAP | 13103 |  |
| Q1 | Transistor | 1 | U310 | 17856 |  |
| Q2 | Transistor | r | 2N2857/JAN | 81350 |  |
| Q3 | Same as Q2 |  |  |  |  |
| Q4 | Transistor | 1 | 2N4918 | 80131 | 04713 |
| Q5 | Transistor | 1 | 2N3251 | 80131 | 04713 |
| Q6 | Not used |  |  |  |  |
| Q7 | Transistor | 1 | 2N5109 | 80131 | 02735 |
| R1 | Resistor, Fixed, Composition: $33 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 2 | CF1/8-33K/J | 09021 |  |
| R2 | Resistor, Fixed, Composition: $12 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 1 | CF1/8-12K/J | 09021 |  |
| R3 | Resistor, Fixed, Composition: $22 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 1 | CF $1 / 8-22 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R4 | Resistor, Fixed, Composition: 470 ohm, $5 \%, 1 / 8$ | W 4 | CF1/8-470 OH:MS/J | 09021 |  |
| R5 | Resistor, Fixed, Composition: $100 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 1 | CF $1 / 8-100 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R6 | Resistor, Fixed, Composition: $8.2 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 2 | CF $1 / 8-8.2 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R7 | Resistor, Fixed, Composition: $5.6 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 2 | CF $1 / 8-5.6 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R8 | Resistor, Fixed, Composition: 300 ohms,5\%, 1/8 | W 2 | CF1/8-300 OHMS/J | 09021 |  |
| R9 | Resistor, Fixed, Composition: 220 ohms,5\%, 1/8 | W 1 | CF $1 / 8 \mathbf{- 2 2 0}$ OH:MS/J | 09021 |  |
| R10 | Resistor, Fixed, Composition: 68 ohms, 5\%, 1/8 | W 2 | CF1/8-68 OH.MS/J | 09021 |  |
| R11 | Resistor, Fixed, Composition: 180 ohms,5\%, 1/8 | W 1 | CF1/8-180 OHMS/J | 09021 |  |
| R12 | Same as R10 |  |  |  |  |
| R13 | Same as R6 |  |  |  |  |
| R14 | Same as R7 |  |  |  |  |
| R15 | Resistor, Fixed, Composition: 47 ohms, 5\%, 1/8 | W 4 | CF1/8-47 OHMS/J | 09021 |  |
| R16 | Same as R8 |  |  |  |  |
| R17 | Resistor, Fixed, Composition: 150 ohms,5\%, 1/8 | W 1 | CF1/8-150 OHMS/J | 09021 |  |
| R18 | Resistor, Fixed, Composition: $1.0 \mathrm{k}, 5 \%, 1 / 8 \mathrm{~W}$ | 2 | CF1/8-1.0K/J | 09021 |  |
| R19 | Resistor, Fixed, Composition: 390 ohms,5\%, 1/8 | W 1 | CF1/8-390 OHMS/J | 09021 |  |
| R20 | Resistor, Fixed, Composition: 10 ohms, 5\%, 1/4 | W 1 | CF $1 / 4-10$ OHMS/J | 09021 |  |
| R21 | Same as R4 |  |  |  |  |
| R22 | Same as R4 |  |  |  |  |
| R23 | Resistor, Fixed, Composition: 10 ohms, 5\%, 1/8 | W 1 | CF1/8-10 OH.MS/J | 09021 |  |
| R24 | Resistor, Fixed, Composition: 33 ohms, 5\%, 1/8 | W 1 | CF1/8-33 OH.MS/J | 09021 |  |
| R25 | Resistor, Fixed, Composition: 270 ohms, 5\%, 1/8 | W 1 | CF1/8-270 OH:MS/J | 09021 |  |
| R26 | Same as R15 |  |  |  |  |
| R27 | Same as R1 |  |  |  |  |
| R28 | Same as R15 |  |  |  |  |
| $\begin{aligned} & \text { R29 } \\ & \text { R30 } \end{aligned}$ | Resistor, Fixed, Composition: 22 ohms, $5 \%, 1 / 8$ Same as R15 | W 1 | CF1/8-22 OH.MS/J | 09021 |  |



Figure 5-33. Part 34750 1st LO Voltage Controlled Oscillator (A5A1A1A1), Location of Components
5.6.6.1.3Type 791600-1 1st and 3rd LO Synthesizer

REF DESIG PREFIX A5A1A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASS' } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. |  | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Cl | Capacitor, Mica, Dipped: 47 2F, 2\%, 500 V | 2 | C.V04ED470G03 | 81349 | 72136 |
| C2 | Same as Cl |  |  |  |  |
| C3 | Capacitor, Ceramic, Disc: $470 \mathrm{pF}, 2 \%, 1000 \mathrm{~V}$ | 2 | BHD470-20 PCT | 91418 |  |
| C4 |  |  | . |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { C6 } \end{aligned}$ | Not Used |  |  |  |  |
| C7 | Capacitor, Ceramic, Disc: $0.01 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 13 | 34453-1 | 14632 |  |
| C8 |  |  |  |  |  |
| Thru C15 | Same as C7 |  |  |  |  |
| C16 | Capacitor, Electrolytic, Tantalum: 22 UF,20\%, 15 | V 5 | 196 D 226 X 0015 KE 3 | 56289 |  |
| C17 | Same as C3 |  |  |  |  |
| C18 | Capacitor, Fixed, Plastic: $4700 \mathrm{pF}, 10 \%, 100 \mathrm{~V}$ | 1 | WMF1D47 | 14655 |  |
| C19 | Not Used |  |  |  |  |
| C20 | Capacitor, Ceramic, Disc: 0.1 F, 20\%, 100 V | 2 | 8131M100-651-104M | 72982 |  |
| C21 | Same as C7 |  |  |  |  |
| C22 | Capacitor, Ceramic, Disc: $1000 \mathrm{pF}, \mathrm{GMV}, 500 \mathrm{~V}$ | 1 | B-GP1000 PFP | 91418 |  |
| C23 | Capacitor, Mica, Dipped: $820 \mathrm{pF}, 5 \%, 300 \mathrm{~V}$ | 1 | D.M15-821J | 72136 |  |
| C24 | Not Used |  |  |  |  |
| C25 | Same as Cl6 |  |  |  |  |
| C26 | Capacitor, Electrolytic, Tantalum: 22 uF, 20\%, 35 | V 2 | 196D226 X0035PE4 | 56289 |  |
| C27 | Not Used |  |  |  |  |
| C28 | Capacitor, Ceramic, Tubular: $47 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | 308-000C0G0-470J | 72982 |  |
| C29 | Capacitor, Electrolytic, Tantalum: 100 uF,20\%,10 | $\vee 1$ | $196 \mathrm{D} 107 \times 0010$ PE4 | 56289 |  |
| C30 | Capacitor, Electrolytic, Tantalum: 2.2 uF, $20 \% 35$ | $V_{1}$ | $196 \mathrm{D} 225 \times 0035 \mathrm{JE} 3$ | 56289 |  |
| C31 | Same as Cl6 |  |  |  |  |
| C32 | Same as C20 |  |  |  |  |
| C33 | Capacitor, Variable, Ceramic: $2-8 \mathrm{pF}, 350 \mathrm{~V}$ | 1 | 538-006A2-8 | 72982 |  |
| C34 | Capacitor, Mica, Dipped: $220 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 2 | CM05FD221G03 | 81349 | 72136 |
| C35 | Same as C34 |  |  |  |  |
| C36 | Same as C7 |  |  |  |  |
| C37 | Same as C7 |  |  |  |  |
| C38 | Same as C16 |  |  |  |  |
| C39 | Same as C26 |  |  |  |  |
| C40 | Not used |  |  |  |  |
| C41 | Same as C7 |  |  |  |  |
| C42 | Same as C16 |  |  |  |  |
| C43* | Capacitor, Mica, Dipped: $15 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | CMO4CD150J03 | 81349 | 72136 |
|  | Nominal value, final value factory selected. |  |  |  |  |



Figure 5-34. Type 791600-1 1st and 3rd LO Synthesizer (A5A1A2), Location of Components


REF DESIG PREFIX A5A1A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { R9 } \\ & \text { Thru } \\ & \text { R12 } \end{aligned}$ | Same as R1 |  |  |  |  |
| R13 | Resistor, Fixed, Composition: 100 ohms,5\%, 1/8 | 10 | CF1/8-100 OHMS/J | 09021 |  |
| R14 <br> Thru <br> R22 | Same as R13 |  |  |  |  |
| R23 | Resistor, Fixed, Composition: 2.2 k ohm, $5 \%, 1 / 4$ | W 6 | CF1/4-2.2K/J | 09021 |  |
| R24 | Resistor, Fixed, Composition: 10 k ohm, $5 \%, 1 / 4$ | 17 | CF $1 / 4-10 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R25 | Same os R4 |  |  |  |  |
| R26 | Resistor, Fixed, Composition: 20 k ohm,5\%, 1/4 | d 3 | CF $1 / 4-20 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R27 | Same as R23 |  |  |  |  |
| R28 | Same as R24 |  |  |  |  |
| R29 | Same as R26 |  |  |  |  |
| R30 | Same as R23 |  |  |  |  |
| R31 | Same as R24 |  |  |  |  |
| R32 | Same as R26 |  |  |  |  |
| R33 | Same as R4 |  |  |  |  |
| R34 | Resistor, Fixed, Composition: 5.6 k ohm, $5 \%, 1 / 4$ | W 2 | CF $1 / 4-5.6 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R35 | Same as R34 |  |  |  |  |
| R36 | Resistor, Fixed, Composition: 27 k ohm, $5 \%, 1 / 8$ |  | CF $1 / 8-27 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R37 | Same as R36 |  |  |  |  |
| R38 | Resistor, Fixed, Composition: 1.2 k ohm, $5 \%$, 1/4 | 1 | CF $1 / 4-1.2 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R39 | Same as R23 |  |  |  |  |
| R40 | Resistor, Fixed, Composition: 270 ohms,5\%, 1/4 | 5 | CF1/4-270 OHMS/J | 09021 |  |
| R41 | Same as R23 |  |  |  |  |
| R42 | Same as R23 |  |  |  |  |
| R43 | Resistor, Fixed, Composition: 1.0 k ohm, 5 \%, 1/4 | W 14 | CF $1 / 4-1.0 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R44 | Same as R2 |  |  |  |  |
| R45 | Same as R36 |  |  |  |  |
| R46 | Same as R40 |  |  |  |  |
| R47 | Same as R40 |  |  |  |  |
| R48 | Same as R43 |  |  |  |  |
| R49 | Resistor, Fixed, Composition: 330 ohms, 5\%, 1/4 | W 1 | CF1/4-330 OH:MS/J | 09021 |  |
| R50 | Same as R24 |  |  |  |  |
| R51 | Same as R43 |  |  |  |  |
| R52 | Same as R43 |  |  |  |  |
| R53 | Same as R24 |  |  |  |  |
| R54 | Resistor, Fixed, Composition: 22 ohms, 5\%, 1/4 | 3 | CF1/4-22 OHMS/J | 09021 |  |
| R55 | Resistor, Fixed, Composition: 27 ohms, 5\%, 1/4 | Y 1 | CF1/4-27 OH:MS/J | 09021 |  |
| R56 | Same as R40 |  |  |  |  |

REF DESIG PREFIX A5A1A2

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R57 | Same as R54 |  |  |  |  |
| R58 | Resistor, Fixed, Composition: 150 ohms, $5 \%, 1 / 4$ | 2 | CF1/4-150 OHMS/J | 09021 |  |
| R59 | Same as R58 |  |  |  |  |
| R60 | Not Used |  |  |  |  |
| R61 | Same as R24 |  |  |  |  |
| R62 | Not Used |  |  |  |  |
| R63 | Resistor, Fixed, Composition: 220 ohms, $5 \%, 1 / 4$ V | 1 | CF1/4-220 OH:MS/J | 09021 |  |
| R64 | Resistor, Fixed, Composition: 3.3 ohms, $5 \%, 1 / 4 \mathrm{~h}$ | 1 | CF1/4-3.3 OHMS/J | 09021 |  |
| R65 |  |  |  |  |  |
| Thru R68 | Same as R43 |  |  |  |  |
| R69 | Resistor, Fixed, Composition: 1.0 k ohm, $5 \%, 1 / 8 \mathrm{~h}$ | 4 | CF $1 / 8-1.0 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R70 Thru |  |  |  |  |  |
| $\begin{aligned} & \text { Thr } \\ & \text { R72 } \end{aligned}$ | Same as R69 |  |  |  |  |
| R73 | Same as R24 |  |  |  |  |
| R74 | Same as R2 |  |  |  |  |
| R75 | Same as R43 |  |  |  |  |
| R76 | Same as R43 |  |  |  |  |
| R77 | Same as R54 |  |  |  |  |
| R78 | Resistor, Fixed, Composition; 47 k ohm, $5 \%, 1 / 8$ | 2 | CF1/8-47K/J | 09021 |  |
| R79 | Same as R78 |  |  |  |  |
| R80 | Same as R43 |  |  |  |  |
| R81 | Same as R43 |  |  |  |  |
| R82 | Resistor, Fixed, Composition: 47 ohms, $5 \%, 1 / 4$ | 1 | CF 1/4-47 OHMS/J | 09021 |  |
| R83 | Same as R1 |  |  |  |  |
| R84 | Same as R43 |  |  |  |  |
| R85 | Same as R43 |  |  |  |  |
| R86 | Same as R40 |  |  |  |  |
| RA1 | Heatsink | 1 | 2225 B | 13103 |  |
| T1 | Transformer Assembly | 1 | 22295-69 | 14632 |  |
| U1 | Integrated Circuit | 1 | MC12013L | 04713 |  |
| U2 | Integrated Circuit | 1 | SN74S196J | 01295 |  |
| U3 | Integrated Circuit | 1 | MC12014L | 04713 |  |
| U4 | Integrated Circuit | 1 | 841013 | 14632 |  |
| U5 | Integrated Circuit | 2 | MC4044P | 04713 |  |
| U6 | Integrated Circuit | 1 | 867400 | 14632 |  |
| U7 | Integrated Circuit | 1 | CA6741T | 02735 |  |
| U8 | Integrated Circuit | 3 | SN74LS190N | 01295 |  |
| U9 | Integrated Circuit | 6 | SN74LS196N | 01295 |  |
| '10 | Same as U8 |  |  |  |  |


|  | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASS' } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| U11 | Same as U8 |  |  |  |  |
| $\mathrm{Ul}_{12}$ | Integrated Circuit | 1 | SN7S74N | 01295 |  |
| U13 | Integrated Circuit | 1 | SN74184N | 01295 |  |
| U14 | Integrated Circuit | 1 | 841043 | 14632 |  |
| U15 | Same as U9 |  |  |  |  |
| U16 | Integrated Circuit | 1 S | SN75140N | 01295 |  |
| $\begin{aligned} & \text { U17 } \\ & \text { Thru } \\ & \text { U20 } \end{aligned}$ | Same as U9 |  |  |  |  |
| U21 | Integrated Circuit | 1 S | SN74LS74N | 01295 |  |
| U22 | Same as U5 |  |  |  |  |
| U23 | Integrated Circuit | 1 S | SN74125N | 01295 |  |
| U24 | Integrated Circuit | 1 S | SN74LS02N | 01295 |  |
| VR1 | Voltage Regulator | 17 | 78M05 HC | 07263 |  |
| Y1 | Crystal, Quartz: 11.155 MHz | 1 C | CR64U/11.155iMHz | 80058 |  |

5.6.6.2Type 791601 2nd LO Synthesizer

REF DESIG PREFIX A5A2

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASS' } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Ceramic, Disc: $0.47 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 3 | 34452-1 | 14632 |  |
| C2 | Same as C1 |  |  |  |  |
| C3 | Capacitor, Electrolytic. Tantalum: $47 \mathrm{uF}, 20 \%, 20$ | $\vee 3$ | 1960476 X0020PE4 | 56289 |  |
| C4 | Capacitor, Electrolytic, Tantalum: 22 uF, 20\% 10 | $\vee 7$ | 196D226 X0010JE3 | 56289 |  |
| C5 | Capacitor, Electrolytic, Tantalum: $1 \mathrm{uF}, 20 \%, 35$ | V 2 | 196 D 105 X 0035 HE 3 | 56289 |  |
| C6 | Capacitor, Ceramic, Disc: $2200 \mathrm{pF}, 10 \%, 200 \mathrm{~V}$ | 1 | CK06BX222K | 81349 | 72136 |
| C7 | Same as C4 |  |  |  |  |
| C8 | Same as C3 |  |  |  |  |
| C9 | Capacitor, Mica, Dipped: $12 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | C:M05CD120J03 | 81349 | 72136 |
| C10 | Capacitor, Ceramic, Disc: 0.1 F, 20\%, 50 V | 2 | 34475-1 | 14632 |  |
| C11 | Capacitor, Ceramic, Disc: $0.01 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 17 | 34453-1 | 14632 |  |
| C12 | Same as C11 |  |  |  |  |
| C13 | Same as C10 |  |  |  |  |
| C14 | Capacitor, Electrolytic, Tantalum: $22 \mathrm{uF}, 20 \%, 35$ | V 2 | $196 \mathrm{D} 226 \mathrm{X0035PE4}$ | 56289 |  |
| C15 | Same as C4 |  |  |  |  |
| C16 | Capacitor, Ceramic, Disc: $470 \mathrm{pF}, 20 \%, 1000 \mathrm{~V}$ | 3 | BHD470-20 PCT | 91418 |  |
| C17 | Capacitor, Electrolytic, Tantalum: 150 uF, $20 \%, 6$ | V 1 | 196 D157 X0006PE4 | 56289 |  |
| C18 | Same as C5 |  |  |  |  |
| C19 |  |  |  |  |  |
| Thru <br> C21 | Same as Cll |  |  |  |  |
| C22 | Capacitor, Ceramic, Tubular: $10 \mathrm{pF},+/-0.5 \mathrm{pF} 50$ | V 1 | $301-000 \mathrm{COH0}-100 \mathrm{D}$ | 72982 |  |
| C23 | Capacitor, Mica, Dipped: $220 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM05FD221G03 | 81349 | 72136 |
| C24 | Same as Cll |  |  |  |  |
| C25 | Same as C3 |  |  |  |  |
| C26 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { C28 } \end{aligned}$ | Same as C4 |  |  |  |  |
| C29 | Capacitor, Plastic, Tubular: $0.022 \mathrm{~F}, 5 \%, 100 \mathrm{~V}$ | 1 | 663UW223-5-1 W | 84411 |  |
| C30 | Capacitor, Fixed, Plastic: $4700 \mathrm{pF}, 10 \%, 100 \mathrm{~V}$ | 1 | W:MF1D47 | 14655 |  |
| C31 | Not Used |  |  |  |  |
| C32 | Same as C4 |  |  |  |  |
| C33 | Same as C16 |  |  |  |  |
| C34 | Same as C16 |  |  |  |  |
| C35 | Same as Cll |  |  |  |  |
| C36 | Capacitor, Ceramic, Disc: $1000 \mathrm{pF}, \mathrm{GMV}, 500 \mathrm{~V}$ | 7 | B-GP1000 PF P | 91418 |  |
| C37 | Same as C14 |  |  |  |  |
| C38 | Same as C36 |  |  |  |  |
| C39 | Same as C36 |  |  |  |  |
| C40 | Same as C11 |  |  |  |  |
| C41 | Same as C36 |  |  |  |  |



Figure 5-35. Type 791601 2nd LO Synthesizer (A5A2), Location of Components

REF DESIG PREFIX A5A2

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C42 <br> Thru <br> C49 | Same as Cll |  |  |  |  |
| C50 | Capacitor, Ceramic, Tubular: $27 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | 308-000C0G0-270J | 72982 |  |
| C51 | Capacitor, Variable, Air: .4-2.5pF, 500 V | 2 | 7283 | 91293 |  |
| C52 | Capacitor, Ceramic, Tubular: $6.8 \mathrm{pF},+/-.25 \mathrm{pF}, 50 \mathrm{dV}$ | $\vee 2$ | $301-000 \mathrm{C} 0 \mathrm{H} 0-689 \mathrm{C} 72982$ |  |  |
| C53 | Capacitor, Ceramic, Tubular: $47 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 5 | 308-000 C0G0-470J | 72982 |  |
| C54 | Same as C53 |  |  |  |  |
| C55 | Same as C36 |  |  |  |  |
| C56 | Capacitor, Ceramic, Tubular: $8.2 \mathrm{pF},+/-.5 \mathrm{pF}, 50 \mathrm{dV}$ | V 1 | 301-000-C0H0-829D | 72982 |  |
| C57* | Capacitor, Ceramic, Tubular: $5.6 \mathrm{pF},+/-.5 \mathrm{pF}, 50 \mathrm{OV}$ | $\mathrm{V}_{1}$ | 301-000T2J0-569D | 72982 |  |
| C58 | Same as Cll |  |  |  |  |
| C59 | Capacitor, Ceramic, Tubular: $33 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | 308-000C0G0-330J | 72982 |  |
| C60 | Same as C53 |  |  |  |  |
| C61 | Same as C51 |  |  |  |  |
| C62 | Same as C52 |  |  |  |  |
| C63 | Same as C53 |  |  |  |  |
| C64 | Same as C53 |  |  |  |  |
| C65 | Same as C36 |  |  |  |  |
| C66* | Capacitor, Ceramic, Tubular: $2.7 \mathrm{pF},+/-.25 \mathrm{pF}, 50 \mathrm{VV}$ | $V_{1}$ | 301-000C0J0-279C | 72982 |  |
| C67 | Capacitor, Ceramic, Tubular: $5.6 \mathrm{pF},+/-.5 \mathrm{pF}, 50 \mathrm{VV}$ | $V_{1}$ | 301-000U2J0-569D | 72982 |  |
| C68 | Capacitor, Mica, Dipped: $150 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM05FD151G03 | 81349 | 72136 |
| C69 | Capacitor, Ceramic, Tubular: $4.7 \mathrm{pF},+/-0.1 \mathrm{pF}, 500 \mathrm{~V}$ | $\vee 1$ | 301-000 C0H0-479B | 72982 |  |
| C70 | Capacitor, Ceramic, Tubular: $2.2 \mathrm{pF},+/-.25 \mathrm{pF}, 50 \mathrm{VV}$ | V 1 | 301-000C0J0-229C | 72982 |  |
| C71 | Capacitor, Ceramic, Tubular: $15 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | 301-000 C0G0-150J | 72982 |  |
| C72 | Capacitor; Mica, Dipped: $1000 \mathrm{pF}, 5 \%, 100 \mathrm{~V}$ | 1 | D.415-102J | 72136 |  |
| C73 | Same as C36 |  |  |  |  |
| C74 | Same as Cl |  |  |  |  |
| C75 | Capacitor, Mica, Dipped: $100 \mathrm{pF}, 2 \%, 500 \mathrm{~V}$ | 1 | CM04FD101G03 | 81349 | 72136 |
| CR1 | Diode, LED | 2 | HLMP-1301 | 28480 |  |
| CR2 | Diode | 1 | 1N4446 | 80131 | 93332 |
| CR3 | Diode, Varicap | 3 | BB109-YELLOW | 25088 |  |
| CR4 | Same as CR3 |  |  |  |  |
| CR5 | Same as CR3 |  |  |  |  |
| CR6 | Same as CR1 |  |  |  |  |
| L1 | Coil, Fixed, Molded: 0.47 uH | 1 | 1537-06 | 99800 |  |
| L2 | Coil, Fixed, Molded: 1.5 uH | 1 | 1537-16 | 99800 |  |
| L3 | Not Used |  |  |  |  |
|  | Nominal value, final value factory selected. |  |  |  |  |

REF DESIG PREFIX A5A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| L4 | Coil, Fixed: 22 mH | 1 | 553-3635-53 | 71279 |  |
| L5 | Coil, Fixed, Molded: 680 uH | 1 | 2500-20 | 99800 |  |
| L6 | Coil, Fixed: 0.82 uH | 2 | 1537-10 | 99800 |  |
| L7 | Same as L6 |  |  |  |  |
| L8 | Inductor | 1 | 21210-183 | 14632 |  |
| L9 | Coil, Fixed: 2.2 uH | 1 | 1025-28 | 99800 |  |
| L10 | Coil, Fixed: 10 ut | 1 | 553-3635-13 | 71279 |  |
| L11 | Coil, Fixed: 100 uH | 1 | 1537-76 | 99800 |  |
| MP1 | Transipad | 3 | 7717-44DAP | 13103 |  |
| MP2 | Transipad | 3 | 7717-46 D AP | 13103 |  |
| MP3 | Cover Assembly | 1 | 24469-1 | 14632 |  |
| MP4 | Cover Assembly | 1 | 24469-2 | 14632 |  |
| MP5 | Cover Assembly | 1 | 24469-3 | 14632 |  |
| MP6 | 2nd LO Shield Assembly | 1 | 34844-1 | 14632 |  |
| Q1 | Transistor | 3 | 2N2857/JAN | 81350 |  |
| Q2 | Transistor | 1 | 2N2222A | 80131 | 04713 |
| Q3 | Transistor | 1 | 841001-1 | 14632 |  |
| Q4 | Not Used |  |  |  |  |
| Q5 | Same as Q1 |  |  |  |  |
| Q6 | Same as Q1 |  |  |  |  |
| Q7 | Transistor | 1 | U310 | 17856 |  |
| R1 | Resistor, Fixed, Composition: 22 ohms,5\%, 1/4 | $N 4$ | CF1/4-22 OHMS/J | 09021 |  |
| R2 | Same as R1 |  |  |  |  |
| R3 | Same as R1 |  |  |  |  |
| R4 | Resistor, Fixed, Composition: 1.8 k ohm,5\%, 1/4 | W 1 | CF1/4-1.8K/J | 09021 |  |
| R5 | Resistor, Fixed, Composition: 10 ohms, 5\%, $1 / 4$ | $N 7$ | CF1/4-10 OHMS/J | 09021 |  |
| R6 | Resistor, Fixed, Composition: 1.0 k ohm, $5 \%, 1 / 4$ | W 13 | CF $1 / 1-1.0 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R7 | Resistor, Fixed, Composition: 1.2 k ohm, $5 \%, 1 / 4$ | W 1 | CF $1 / 4-1.2 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R8 | Same as R5 |  |  |  |  |
| R9 | Same as R6 |  |  |  |  |
| R10 | Resistor, Fixed, Composition: 5.6 ohms,5\%, 1/4 中 | 1 | CF1/4-5.6 OHMS/J | 09021 |  |
| R11 | Resistor, Fixed, Composition: 5.1 k ohm,5\%, 1/4 | W 1 | CF1/4-5.1K/J | 09021 |  |
| R12 | Same as R6 |  |  |  |  |
| R13 | Same as RS |  |  |  |  |
| R14 | Same as R6 |  |  |  |  |
| R15 | Resistor, Fixed, Composition: 47 ohms,5\%, 1/4 W | 8 | CF1/4-47 OHMS/J | 09021 |  |
| R16 <br> Thru <br> R18 | Same as R15 |  |  |  |  |
| R19 | Resistor, Fixed, Composition: 820 ohms, $5 \%, 1 / 4$ |  | CF $1 / 4-820$ OHMS/J | 09021 |  |
| R20 | Resistor, Fixed, Composition: 2.2 k ohm, 5\%, 1/4 | W 2 | CF1/4-2.2K/J | 09021 |  |

REF DESIG PREFIX A5A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION |  | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R21 | Same as R20 |  |  |  |  |
| R22 | Resistor, Fixed, Composition: 100 ohms,5\%, 1/4 W | 1 | CF 1/4-100 OHMS/J | 09021 |  |
| R23 | Resistor, Fixed, Composition: 18 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF $1 / 4-18 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R24 | Same as R6 |  |  |  |  |
| R25 | Same as R6 |  |  |  |  |
| R26 | Same as R5 |  |  |  |  |
| R27 | Resistor, Fixed, Composition: 2.7 k ohm, 5\%, 1/4 N | - 2 | CF1/4-2.7K/J | 09021 |  |
| R28 | Same as R5 |  |  |  |  |
| R29 | Same as R6 |  |  |  |  |
| R30 | Resistor, Fixed, Composition: 270 ohms,5\%, 1/4 W | 1 | CF1/4-270 OHMS/J | 09021 |  |
| R31 | Resistor, Fixed, Composition: 1.0 M ohm, $5 \%, 1 / 4 \mathrm{~W}$ | W 1. | CF 1/4-1.0. $/ \mathrm{J}$ | 09021 |  |
| R32 | Resistor, Fixed, Composition: 820 k ohm, $5 \%, 1 / 4 \mathrm{~N}$ | N 1 | CF $1 / 4-820 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R33 | Resistor, Fixed, Composition: 100 k ohm, $5 \%, 1 / 4 \mathrm{~N}$ | N 1 | CF $1 / 4-100 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R34 | Resistor, Fixed, Composition: 360 ohms,5\%, 1/4 W |  | CF1/4-360 OH:MS/J | 09021 |  |
| R35 | Same as R27 |  |  |  |  |
| R36 | Same as R5 |  |  |  |  |
| R37 | Resistor, Fixed, Composition: 4.7 ohms, 5\%, 1/4 W | N 1 | CF1/4-4.7 OH. ${ }^{\text {OS/J }}$ | 09021 |  |
| R38 | Same as R5 |  |  |  |  |
| R39 | Resistor, Fixed, Composition: 56 ohms, 5\%, 1/4 W |  | CF1/4-56 OHMS/J | 09021 |  |
| R40 | Resistor, Fixed, Composition: 470 ohms, $5 \%, 1 / 4 \mathrm{~W}$ |  | CF1/4-470 OHMS/J | 09021 |  |
| R41 | Same as R6 |  |  |  |  |
| R42 | Resistor. Fixed, Composition: 10 k ohm, $5 \%, 1 / 4 \mathrm{~h}$ |  | CF1/4-10K/J | 09021 |  |
| R43 | Not Used |  |  |  |  |
| R44 | Resistor, Fixed, Composition: 47 k ohm, $5 \%, 1 / 4$ \% |  | CF $1 / 4-47 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R45 | Not Used |  |  |  |  |
| R46 | Resistor, Fixed, Composition: 1.5 k ohm, $5 \%, 1 / 4 \mathrm{~N}$ | $\text { N } 1$ | CF $1 / 4-1.5 \mathrm{~K} / \mathrm{J}$ | $09021$ |  |
| R47 | Resistor, Fixed, Composition: 750 ohms,5\%, 1/4 | 1 | CF1/4-750 OHMS/J | $09021$ |  |
| R48 | Same as R15 |  |  |  |  |
| R49 | Same as R15 |  |  |  |  |
| R50 | Same as R40 |  |  |  |  |
| $\dot{\mathrm{R}} 51$ | Same as R40 |  |  |  |  |
| R52 | Same as R6 |  |  |  |  |
| R23 | Same as R6 |  |  |  |  |
| R54 | Same as R40 |  |  |  |  |
| R55 | Same as R40 |  |  |  |  |
| R56 | Not Used |  |  |  |  |
| R57 | Not Used |  |  |  |  |
| R58 | Not Used |  |  |  |  |
| R59 | Same as R15 |  |  |  |  |
| R60 | Same as R6 |  |  |  |  |

REF DESIG PREFIX A5A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R61 | Same as R6 |  |  |  |  |
| R62 | Same as R42 |  |  |  |  |
| R63 | Same as R42 |  |  |  |  |
| R64 | Resistor, Fixed, Composition: 10 k ohm, 5\%, 1/8 | W 3 | CF1/8-10K/J | 09021 |  |
| R65 | Resistor, Fixed, Film: 18.2 k ohm, 1\%, $1 / 10 \mathrm{w}$ | 4 | RN55C1822F | 81349 | 75042 |
| R66 | Same as R65 |  |  |  |  |
| R67 | Resistor, Fixed, Composition: 22 ohms, 5\%, 1/8 W | 2 | CF1/8-22 OHMS/J | 09021 |  |
| R68 | Resistor, Fixed, Film: 3.92 k ohm, 1\%, 1/10 W | 2 | RN55C3922F | 81349 | 75042 |
| R69 | Same as R64 |  |  |  |  |
| R70 | Same as R65 |  |  |  |  |
| R71 | Same as R65 |  |  |  |  |
| R72 | Same as R67 |  |  |  |  |
| R73 | Same as R68 |  |  |  | , |
| R74 | Resistor, Fixed, Composition: 220 ohms,5\%, 1/4 $\psi$ | 1 | CF1/4-220 OHMS/J | 09021 |  |
| R75 | Same as R1 |  |  |  |  |
| R76 | Same as R64 |  |  |  |  |
| R77 | Not Used |  |  |  |  |
| R78 | Same as R15 |  |  |  |  |
| R79 | Same as R42 |  |  |  |  |
| R80 | Same as R6 |  |  |  |  |
| U1 | Integrated Circuit | 3 | MC4044P | 04713 |  |
| U2 | Integrated Circuit | 1 | SN74177N | 01295 |  |
| U3 | Integrated Circuit | 1 | SN74S74N | 01295 |  |
| U4 | Integrated Circuit | 1 | 796 HC | 07263 |  |
| U5 | Integrated Circuit | 1 | N5733K | 18324 |  |
| U6 | Same as U1 |  |  |  |  |
| U7 | Integrated Circuit | 1 | SN74LS190N | 01295 |  |
| U8 | Integrated Circuit | 3 | SN74LS191N | 01295 |  |
| U9 | Same as U8 |  |  |  |  |
| U10 | Same as U8 |  |  |  |  |
| U11 | Integrated Circuit | 2 | SN74LSOON | 01295 |  |
| U12 | Same as Ull |  |  |  |  |
| U13 | Not Used |  |  |  |  |
| U14 | Integrated Circuit | 1 | SN74LS168N | 01295 |  |
| U15 | Integrated Circuit | 2 | MC12013P | 04713 |  |
| U16 | Same as U15 |  |  |  |  |
| U17 | Integrated Circuit | 2 | SN74LS196N | 01295 |  |
| 018 | Not Used |  |  |  |  |
| U19 | Same as U17 |  |  |  |  |
| $\mathrm{U}_{20}$ | Same as Ull |  |  |  |  |
| VR1 | Diode, Zener: 8.2 V | 1 | 1N756A | 80131 | 04713 |


| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Cl | Capacitor, Electrolytic, Tantalum: $3.3 \mathrm{uF}, 20 \%, 35 \mathrm{~V}$ | 1 | 1960335 X0035JE3 | 56289 |  |
| C2 | Capacitor, Ceramic, Disc: $0.1 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 1 | 34475-1 | 14632 |  |
| C3 | Capacitor, Electrolytic, Tantalum: $47 \mathrm{uF}, 20 \%, 20 \mathrm{~V}$ | $\checkmark 3$ | 196 D476 X0020 PE4 | 56289 |  |
| C4 | Capacitor, Ceramic, Disc: $0.47 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 1 | 34452-1 | 14632 |  |
| C5 | Capacitor, Ceramic, Disc: $0.01 \mathrm{~F}, 20 \%, 50 \mathrm{~V}$ | 9 | 34453-1 | 14632 |  |
| C6 | Capacitor, Ceramic, Tubular: $33 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | 308-000C0G0-330J | 72982 |  |
| C7 | Capacitor, Ceramic, Tubular: $47 \mathrm{pF}, 5 \%, 500 \mathrm{~V}$ | 1 | 308-000C0G0-470J | 72982 |  |
| C8 | Capacitor, Variable, Ceramic: $2-8 \mathrm{pF}, 350 \mathrm{~V}$ | 1 | 538-006 A2-8 | 72982 |  |
| C9 | Same as C5 |  |  |  |  |
| C10 | Capacitor, Mica, Dipped: $10 \mathrm{pF}, ~ \$ 0.5 \mathrm{pF}, 500 \mathrm{~V}$ | 2 | CM04CD100D03 | 81349 | 72136 |
| C11 | Capacitor, Ceramic, Disc: $1000 \mathrm{pF}, \mathrm{GM}$, 500 V | 2 | B-GP1000PFP | 91418 |  |
| C12 | Same as C11 |  |  |  |  |
| C 13 | Same as C5 |  |  |  |  |
| C14 | Same as C10 |  |  |  |  |
| C15 | Not Used |  |  |  |  |
| C16 | Same as C3 |  |  |  |  |
| C17 <br> Thru <br> C21 | Same as C5 |  |  |  |  |
| C22 | Same as C3 |  |  |  |  |
| C23 | Same as C5 |  |  |  |  |
| CR1 | Diode, Varicap: | 1 | BB109-YELLOW | 25088 |  |
| L1 | Coil, Fixed: 27 uH | 1 | 1537-48 | 99800 |  |
| L2 | Coil, Fixed, Molded: 330 uH | 1 | 2500-04 | 99800 |  |
| L3 | Coil, Fixed: 0.82 uH | 1 | 1537-10 | 99800 |  |
| MP1 | Transipad | 4 | 7717-89DAP | 13103 |  |
| MP2 | Shield, BFO | 1 | 34982-1 | 14632 |  |
| Q1 | Transistor | 12 | 2N2857/JAN | 81350 |  |
| Q2 | Transistor | 18 | 841001-2 | 14632 |  |
| Q3 | Transistor 1 | 12 | 2N706 | 80131 | 04713 |
| Q4 | Transistor 1 | 13 | 3N128 | 80131 | 02735 |
| R1 | Resistor, Variable, Film: 500 ohms, 10\%, $1 / 2 \mathrm{~W} \quad 1$ | 16 | 62 PAR500 | 73138 |  |
| R2 | Resistor, Fixed, Composition: 1.0 k ohm, $5 \%, 1 / 4$ W 1 | 15 | CF $1 / 4-1.0 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R3 | Resistor, Fixed, Composition: 10 k ohm, $5 \%, 1 / 4$ W 3 | 3 C | CF1/4-10K/J | 09021 |  |
| R4 | Same as R2 |  |  |  |  |
| R5 | Resistor, Fixed, Composition: 10 ohms, 5\%, 1/4 W 3 | 3 C | CF1/4-10 OH:MS/J | 09021 |  |
| R6 | Same as R2 |  |  |  |  |
| R7 | Same as R3 |  |  |  |  |
| R8 | Resistor, Variable, Film: 4.22 k ohm, 1\%, 1/10 w 1 | 1 R | RN55C4221F | 81349 | 75042 |
| R9 | Resistor, Variable, Film: 17.8 k ohm, $1 \%, 1 / 10 \mathrm{~W}$ | 2 R | RN55C1782F | 81349 | 75042 |



Figure 5-36. Type 791576-1 BFO Synthesizer (A5A3), Location of Components

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | $\begin{gathered} \text { MFR. } \\ \text { CODE } \end{gathered}$ | RECM VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R10 | Same as R9 |  |  |  |  |
| R11 | Same as R5 |  |  |  |  |
| R12 | Resistor, Fixed, Composition: 560 ohms, $5 \%, 1 / 4$ h | 1 | CF1/4-560 OHVS/J | 09021 |  |
| R13 | Resistor, Fixed, Composition: 100 k ohm, $5 \%, 1 / 4$ | W 1 | CF1/4-100K/J | 09021 |  |
| R14 | Resistor, Fixed, Composition: 1.0 M ohm, $5 \%, 1 / 4$ | W 1 | CF1/4-1.0. $\mathrm{W} / \mathrm{J}$ | 09021 |  |
| R15 | Resistor, Fixed, Composition: 820 k ohm, $5 \%, 1 / 4$ | W 1 | CF1/4-820K/J | 09021 |  |
| R16 | Same as R5 |  |  |  |  |
| R17 | Same as R3 |  |  |  |  |
| R18 | Same as R2 |  |  |  |  |
| R19 | Same as R2 |  |  |  |  |
| R20 | Resistor, Fixed, Composition: 220 ohms,5\%, 1/4 | 1 | CF1/4-220 OH.MS/J | 09021 |  |
| R21 | Resistor, Fixed, Composition: 62 ohms,5\%, 1/4 W | 1 | CF1/4-62 OH:MS/J | 09021 |  |
| R22 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { R31 } \end{aligned}$ | Same as R2 |  |  |  |  |
| U1 | Integrated Circuit | 4 | SN74LS190N | 01295 |  |
|  |  |  |  |  |  |
| Thru U4 | Same as Ul |  |  |  |  |
| U5 | Integrated Circuit | 2 | SN7425N | 01295 |  |
| U6 | Integrated Circuit | 1 | SN74LS11N | 01295 |  |
| U7 | Same as U5 |  |  |  |  |
| U8 | Integrated Circuit | 1 | 867474 | 14632 |  |
| U9 | Integrated Circuit | 1 | MC4044P | 04713 |  |
| U10 | Integrated Circuit | 1 | SN74LS90N | 01295 |  |




Figure 5-37. Type 791580 I/O Notherboard (A6), Location of Components
5.6.7.1 TYPE 794275 SYNTHESIZER INTERFACE/MEMORY REF DESIG PREFIX A6AI

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BT1 | Battery: 2.4 V | 1 | 41 B901BD16G1 | 19209 |  |
| Cl | Capacitor, Ceramic, Disc: $0.1 \mathrm{uF}, 20 \%, 100 \mathrm{~V}$ | 7 | 8131M100-651-104.M | 72982 |  |
| $\mathrm{C} 2$ |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { C5 } \end{aligned}$ | Same as C1 |  |  |  |  |
| C6 | Capacitor, Electrolytic, Tantalum: 22 uF, $20 \%, 15 \mathrm{l}$ | $\vee 2$ | 196D226 X0015KE3 | 56289 |  |
| C7 | Same as C6 |  |  |  |  |
| C8 | Capacitor, Ceramic, Disc: $680 \mathrm{pF}, 5 \%, 100 \mathrm{~V}$ | 1 | 8121-100-C0G0-681J | 72982 |  |
| C9 | Capacitor, Ceramic, Disc: 0.47 UF, 20\%, 50 V | 1 | 34452-1 | 14632 |  |
| C10 | Capacitor, Polycarbonate, Tubular: 1uF, $10 \%$, 30 N | 1 | ECR105AK | 50558 |  |
| C11 | Same as Cl |  |  |  |  |
| $\mathrm{Cl2}$ | Same as C1 |  |  |  |  |
| CR1 | Diode | 2 | 1N449 | 80131 |  |
| CR2 | Same as CR1 |  |  |  |  |
| Q1 | Transistor | 1 | 2N3251 | 80131 |  |
| R1 | Not Used |  |  |  |  |
| R2 | Resistor, Fixed, Film: 820 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF $1 / 4-820$ OHMS/J |  |  |
| R3 | Resistor, Fixed, Film: 82 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-82K/J |  |  |
| R4 | Resistor, Fixed, Film: 150 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-150 OH:MS/J |  |  |
| R5 | Resistor, Fixed, Film: 390 ohm, 5\%, 1/4 W | 1 | CF1/4-390 OHMS/J |  |  |
| R6 | Same as R3 |  |  |  |  |
| R7 | Resistor, Fixed, Film: 10 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-10k/J |  |  |
| R8 | Same as R5 |  |  |  |  |
| R9 | Resistor, Fixed, Film: 1.0 k ohm, $5 \%, 1 / 4 \mathrm{~N}$ | 1 | CF1/4-1.0K/J |  |  |
| R10 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { R13 } \end{aligned}$ | Same as R9 |  |  |  |  |
| R14 | Resistor, Fixed, Film: 3.3 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-3.3K/J |  |  |
| R15 <br> Thru <br> R19 | Same as R7 |  |  |  |  |
| U1 | Integrated Circuit (EPROM) | 1 | B2732 | 34649 |  |
| U2 | Not Used |  |  |  |  |
| U3 | Integrated Circuit | 1 | 841093 | 14632 |  |
| U4 | Integrated Circuit | 1 | MD74SC245AC | 36665 |  |
| U5 | Integrated Circuit | 2 | UD74SC374AC | 36665 |  |
| U6 | Same as U5 |  |  |  |  |
| U7 | Integrated Circuit | 1 in | MD74SC138AC | 36665 |  |
| U8 | Same as U7 |  |  |  |  |
| U9 | Integrated Circuit | 1 . | M.174PC00 | 27014 |  |
| U10 | Integrated Circuit | 1 S | SN741S09N | 01295 |  |
| U11 | Integrated Circuit | 1 S | SN74LS14N | 01295 |  |

REF DESIG PREFIX A6A1

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. |  | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| U12 | Integrated Circuit | 5 | :h.M74374N | 27014 |  |
| U13 |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { U16 } \end{aligned}$ | Same as U12 |  |  |  |  |
| U17 | Not Used |  |  |  |  |
| U18 | Integrated Circuit | 1 | P808\%A | 34649 |  |
| VR1 | Diode, Zener: 8.2 V | 3 | ICN-246-S5-T | 34649 |  |



[^2]

Figure 5-38. Type 794275 Synthesizer/Interface/ Memory (A6A1) Location of Components
5.6.7.2 TYPE 796032-2 IF INTERFACE

REF DESIG PREFIX A6A2

| REF <br> DESIG | DESCRIPTION | $\begin{aligned} & \text { QTY } \\ & \text { PER } \\ & \text { ASSY } \end{aligned}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | RECM VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Electrolytic, 47 uf, 20\%, 20V | 3 | 196D47 X0020PE4 | 56289 |  |
| C2 | Same as Cl |  |  |  |  |
| C3 | Same as Cl |  |  |  |  |
| C4 | Capacitor, Ceramic, Disc: . 1 uf, $20 \%, 100 \mathrm{~V}$ | 9 | 8131M100-651-104: | 72982 |  |
| C5 |  |  |  |  |  |
| Thru C10 | Same as C4 |  |  |  |  |
| C11 | Capacitor, mica, dipped: $20 \mathrm{pf}, 5 \%, 500 \mathrm{~V}$ | 3 | 196D105X0035 HE3 | 56289 |  |
| C12 | Same as C1l |  |  |  |  |
| C13 | Capacitor, Electrolytic, Tantalum: $1 \mathrm{uF}, 20 \%, 35$ | 3 | 196D105 X0035 HE 3 | 81349 | 56289 |
| C14 | Same as C4 |  |  |  |  |
| C15 | Capacitor, mica, dipped: $330 \mathrm{pf}, 2 \%, 100 \mathrm{~V}$ | $1{ }^{\text {* }}$ | CM04FA331G03 | 81349 |  |
| C 16 | Capacitor, mica, dipped: $15 \mathrm{pf}, 5 \%, 500 \mathrm{~V}$ | 1 | CM04CD150J03 | 81349 |  |
| C 17 | Not used |  |  |  |  |
| C18 | Same as C13 |  |  |  |  |
| C19 | Same as C13 |  |  |  |  |
| C20 | Same as C4 |  |  |  |  |
| C21 | Capacitor, electrolytic, tantalum: $4.7 \mathrm{uf}, 20 \%, 35 \mathrm{~V}$ | 2 | 196D475 X0035JE3 | 56289 |  |
| C22 | Capacitor, ceramic, disc: . $47 \mathrm{uf}, 20 \%, 100 \mathrm{~V}$ | 4 | 8131M100-651-474: | 72982 |  |
| C23 | Same as C22 |  |  |  |  |
| C24 | Same as C22 |  |  |  |  |
| C25 | Same as C22 |  |  |  |  |
| C26 | Same as C21 |  |  |  |  |
| C27 | Capacitor, ceramic, disc: .01uf, 20\%, 200V | 1 | 8131A200Z5U103M | 72982 |  |
| C28 | Capacitor, ceramic, disc: . $01 \mathrm{uf}, 5 \%, 100 \mathrm{~V}$, NPO | 1 | 8131-100-COGO-103J | 72982 |  |
| CR1 | Diode | 3 | 1N4449 | 80131 |  |
| CR2 | Same as CR1 |  |  |  |  |
| CR3 | Same as CR1 |  |  |  |  |
| CR4 | Diode | 1 | 1N4446 | 80131 |  |
| CR5 | Diode | 2 | 1 N 462 A | 80131 |  |
| CR6 | Same as CR5 |  |  |  |  |
| CR7 | Diode | 2 | MPD 400 | 09213 |  |
| J1 | Connector, Receptacle | 1 | 1-87567-6 | 00779 |  |
| Q1 | Transistor | 1 | 2N3251 | 80131 |  |
| Q2 | Transistor | 1 2 | 2N2222A | 80131 |  |
| R1 | Resistor, Fixed, Comp: 10 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 5 R | RCR07G103JS | 81349 |  |
| R2 | Resistor, Fixed, Composition: 22 ohm,5\%, 1/4 W | 1 | RCR07G220JS | 81349 |  |
| R3 | Resistor, Fixed, Composition: 1.2 k ohm, $5 \%, 1 / 4 \%$ | 2 | RCR07G122JS | 81349 |  |
| R4 | Resistor, Fixed, Composition: 3.9 k ohm, $5 \%, 1 / 4 \mathrm{k}$ | 2 | RCR07G392JS | 81349 |  |
| R5 | Resistor, Fixed, Composition: 6.8 k ohm, $5 \%, 1 / 4 \mathrm{~h}$ | 2 | RCR07G682JS | 81349 |  |
| 6 | Same as R3 |  |  |  |  |
| R7 | Resistor, Fixed, Composition: 750 ohm, 5\%, $1 / 4 \mathrm{~W}$ | 1 | RCR07G751JS | 81349 |  |
| R8 | Resistor, Fixed, Composition: 202 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 R | RCR07G202JS | 81349 |  |

REF DESIG PREFIX A6A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{aligned} & \text { QTY } \\ & \text { PER } \\ & \text { ASSY } \end{aligned}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| R9 | Resistor, Fixed, Composition: 6.2 k ohm, $5 \%, 1 / 4 \mathrm{~h}^{\text {\% }}$ | 1 | RCR07G622JS | 81349 |  |
| R10 | Resistor, Trim, Film: 1 k ohm, 10\%, $1 / 2 \mathrm{~W}$ | 1 | 62PAR1K | 73138 |  |
| R11 | Not Used |  |  |  |  |
| R12 | Resistor, Fixed, Composition: 1.5 k ohm, $5 \%, 1 / 4 \mathrm{k}$ | 1 | RCR07G152JS | 81349 |  |
| R13 | Same as R12 |  |  |  |  |
| R14 | Resistor, Trim, Film: 2 k ohm, 10\%, 1/2 W | 1 | 62PAR2K | 81349 |  |
| R15 | Resistor, Fixed, Composition: 2.7 k ohm, $5 \%, 1 / 4 \mathrm{k}$ | 3 | RCR07G272JS | 81349 |  |
| R16 | Resistor, Fixed, Composition: 51 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G513JS | 81349 |  |
| R17 | Resistor, Fixed, Composition: 82 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G820JS | 81349 |  |
| R18 | Same as R1 |  |  |  |  |
| R19 | Not used |  |  |  |  |
| R20 | Same as R1 |  |  |  |  |
| R21 | Same as R15 |  |  |  |  |
| R22 | Same as R15 |  |  |  |  |
| R23 | Same as R1 |  |  |  |  |
| R24 | Same as R1 |  |  |  |  |
| R25 | Resistor, Fixed, Composition: 820 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G821JS | 81349 |  |
| R26 | Resistor.Trim, Film: 1 k ohm, $10 \%, 1 / 2 \mathrm{~W}$ | 1 | 62 PR1K | 73138 |  |
| R27 | Resistor, Fixed, Composition: $1.0 \mathrm{M}, 5 \%, 1 / 8 \mathrm{~W}$ | 4 | RCR05G105JS | 81349 |  |
| $\begin{aligned} & \text { R28 } \\ & \text { Thru } \\ & \text { R30 } \end{aligned}$ | Same as R27 |  |  |  |  |
| R31 | Resistor, Fixed, Composition: 120 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | RCR07G121JS | 81349 |  |
| R32 | Resistor, Fixed, Composition: 10 k ohm, $5 \%, 1 / 8 \mathrm{w}$ | 1 | RCR05G103JS | 81349 |  |
| R33 | Same as R32 |  |  |  |  |
| R34 | Same as R33 |  |  |  |  |
| U1 | Integrated Circuit | 1 | P8085 A | 34649 |  |
| U2 | Integrated Circuit | 1 | SN74LS125N | 01295 |  |
| U3 | Integrated Circuit | 1 | CD4013BE | 02735 |  |
| U4 | Integrated Circuit | 1 | SN74LS14N | 01295 |  |
| U5 | Integrated Circuit | 1 | MM74C14N | 27014 |  |
| U6 | Resistor/Netowrk | 1 | 764-1-R10K | 73138 |  |
| U7 | Integrated Circuit | 1 | SN74LS138N | 01295 |  |
| U8 | Integrated Circuit | 1 | CD4053BE | 02735 |  |
| U9 | Integrated Circuit | 1 | SN74LS241N | 01295 |  |
| U10 | Integrated Circuit | 3 | SN74LS273N | 01295 |  |
| U11 | Integrated Circuit | 1 | MM74C374N | 27014 |  |
| U12 | Same as U10 |  |  |  |  |
| U13 | Same as U10 |  |  |  |  |
| U14 | Integrated Circuit | 1 | SN74LS240N | 01295 |  |
| U15 | Integrated Circuit | 1 | MC14050BCP | 04713 |  |
| U16 | Not used |  |  |  |  |
| 1112 |  |  |  | 07263 |  |

REF DESIG PREFIX A6.4?

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. <br> CODE | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| U'18 | Same as U1: |  |  |  |  |
| U19 | Inregrated Circuit | 1 | YC1408L. 8 | 04713 |  |
| U'20 | Integrared Circuit | 1 | ADCO800 PCN | 27014 |  |
| C21 | Integrated Circuit | 1 | SNT4LSn8N | 01295 |  |
| U2? | Integrater Cirruit | 1 | NE555N | 18324 |  |
| lR1 | Diode, 7ener: 3.3 V | 1 | 1N746A | 80131 |  |
| $V \mathrm{R}$ ? | Diore. Zener: 12 V | 1 | 1N759A | 80131 |  |
| VR3 | Diode, Zener: 5.1 V | 2 | 1N751A | 80131 |  |
| VR4 | Same as VR3 |  |  |  |  |



Figure 5-39. Type 796032-2 IF Interface (A6A2)
Location of Components
5.6.7.3 TYPE 796037 ASYNCHRONOUS I/O BOARD

REF DESIG PREFIX A6A3

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | RECM VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 | Capacitor, Electrolytic, Tantalum: 22 uF,20\%,15\% | 3 | 196D226 X0015KE3 | 56289 |  |
| C2 | Same as Cl |  |  |  |  |
| C3 | Same as Cl |  |  |  |  |
| C4 | Capacitor, Ceramic, Disc: 0.1 uF, 20\%, 100 V | 5 | 8131:M100-651-104: | 72982 |  |
| C5 | Same as C4 |  |  |  |  |
| C6 | Same as C4 |  |  |  |  |
| C7 | Same as C4 |  |  |  |  |
| C8 | Same as C4 |  |  |  |  |
| J1 | Connector, Receptacle | 2 | 87567-6 | 00779 |  |
| J2 | Same as Jl |  |  |  |  |
| J3 | Connector, Receptacle | 18 | 006-4800 | 98291 |  |
|  |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { J20 } \end{aligned}$ | Same as J3 |  |  |  |  |
| P1 | Connector, Plug | 6 | 021-4802-0 | 98291 |  |
|  |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { P6 } \end{aligned}$ | Same as P1 |  |  |  |  |
| R1 | Resistor, Fixed, Composition: 100 ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 2 | RCR07G101JS | 81349 |  |
| R2 | Same as R1 |  |  |  |  |
| R3 | Resistor, Fixed, Composition: 3.3 k ohm, $5 \%, 1 / 8 \mathrm{~W}$ | 2 | RCR05G332JS | 81349 |  |
| R4 | Same as R3 |  |  |  |  |
| R5 | Resistor, Fixed, Composition: 10 k ohm, $5 \%, 1 / 8 \mathrm{~W}$ | 4 | RCR05G103JS | 81349 |  |
| R6 | Same as R5 |  |  |  |  |
| R7 | Same as R5 |  |  |  |  |
| R8 | Same as R5 |  |  |  |  |
| S1 | Switch, Slide | 1 | 206-4 | 71450 |  |
| S2 | Switch, Slide | 1 | 206-8 | 71450 |  |
| U1 | Integrated Circuit | 1 | P8251A | 34649 |  |
| U2 | Integrated Circuit | 1 | SN74LS273N | 01295 |  |
| U3 | Integrated Circuit | 1 | D.M81 LS96N | 27014 |  |
| U4 | Integrated Circuit | 1 | SN74LS138N | 01295 |  |
| U5 | Integrated Circuit | 1 | COM5046P | 53848 |  |
| U6 | Integrated Circuit | 1 S | SN74LS04N | 01295 |  |
| U7 | Integrated Circuit | 29 | 9616 PC | 07263 |  |
| U8 | Same as U7 |  |  |  |  |
| U9 | Integrated Circuit | 29 | 9617 PC | 07263 |  |
| U10 | Same as U9 |  |  |  |  |
| U11 | Resistor, Network | 17 | 764-1-R10K | 73138 |  |
| VR1 | Diode, Zener: 12 V | 21 | 1N759A | 80131 |  |
| VR2 | Same as VRI |  |  |  |  |

REF DESIG PREFIX A6A3



Figure 5-40. Type 796037 Asynchronous $1 / O$ Board (A6A3), Location of Components

### 5.6.7.4 TYPE 794300-1 SERIAL I/0 BUFFER REF DESIG PREFIX A6A4



5.6.7.5 TYPE 794255-1 SYNCHRONOUS SERIAL INPUT/OUTPUTREF DESIG PREFIX A6A5

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \\ \hline \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | RECM <br> VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Cl | Capacitor, Electrolytic, Tantalum: $22 \mathrm{uF}, 20 \%, 15 \mathrm{~V}$ | 1 | 196D226 X0015KE3 | 56289 |  |
| C2 | Capacitor, Ceramic, Disc: . $1 \mathrm{uF}, 20$ \%, 50 V | 3 | 34475-1 | 14632 |  |
| C3 | Same as C2 |  |  |  |  |
| C4 | Same as C2 |  |  |  |  |
| J1 | Connector, Receptacle | 1 | 87567-4 | 00778 |  |
| K1 | Resistor, Fixed, Film: 1.0 k ohm, $5 \%, 1 / 8 \mathrm{~W}$ | 3 | CF1/8-1.0K/J | 09021 |  |
| ส2 | Same as R1 |  |  |  |  |
| R3 | Same as R1 |  |  |  |  |
| U1 | Integrated Circuit | 2 | P8255A | 34649 |  |
| U2 | Same as U1 |  |  |  |  |
| U3 | Integrated Circuit | 4 | SN74LS299N | 01295 |  |
| U1 | Same as U3 |  |  |  |  |
| U5 | Same as U3 |  |  |  |  |
| Uô | Same as U3 |  |  |  |  |
| U7 | Integrated Circuit | 1 | SN74LS138N | 01295 |  |
| U8 | Integrated Circuit | 1 | SN74LS04N | 01295 |  |
| U9 | Integrated Circuit | 1 | SN74LS273N | 01295 |  |
| U10 | Integrated Circuit | 1 | SN74LS148N | 01295 |  |
| U11 | Integrated Circuit | 1 | SN74LS32N | 01295 |  |
| U12 | Integrated Circuit | 1 | SN74LS08N | 01295 |  |



Figure 5-42. Type794255-1 Synchronous Serial I/O (A6A5) Location of Components

### 5.6.8 TYPE 796013-5 FRONT PANEL MB REF DESIG PREFIX MFP AI




Figure 5-43. Type 796013-5 Front Panel MB (MFP A1), Location of Components
5.6.8.1 TYPE 796056-1 FRONT PANEL ENCODE

REF DESIG PREFIX MFP AlAI

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | MFR. CODE | $\begin{aligned} & \text { RECM } \\ & \text { VENDOR } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Cl | Capacitor, Ceramic, Disc: 0.1 UF, 20\%, 100 V | 11 | 8131.M100-651-104M | 72982 |  |
| C2 |  |  |  |  |  |
| Thru C10 | Same as Cl |  |  |  |  |
| Cl 1 | Capacitor, Ceramic, Disc: 0.01 UF, 20\%, 200 V | 1 | 8131 A20025U103M | 72982 |  |
| C 12 | Capacitor, Electrolytic, Tantalum: $47 \mathrm{uF}, 20 \%, 20 \%$ | 2 | 196D476 X0020PE4 | 56289 |  |
| C 13 | Same as C12 |  |  |  |  |
| C14 | Capacitor, Electrolytic, Tantalum: 100 uF, $20 \%, 2 \mathrm{VV}$ | $\vee 3$ | 196 D107 X0020TE4 | 56289 |  |
| C15 | Same as Cl4 |  |  |  |  |
| C16 | Same as Cl4 |  |  |  |  |
| C17 | Same as Cl |  |  |  |  |
| C18 | Capacitor, Ceramic, Disc: 0.47 uF, 20\%, 100 V | 1 | 8131M100-651-474M - | 772982 |  |
| C19 | Capacitor, Electrolytic, Tantalum: 22 uF, 20\%, 10 | 1 | $196 \mathrm{D} 226 \mathrm{X0010JE3}$ | 56289 |  |
| CR1 | Diode | 3 | 1N4449 | 80131 |  |
| CR2 | Same as CR1 |  |  |  |  |
| CR3 | Same as CR1 |  |  |  |  |
| J1 | Connector, Receptacle | 1 | 1-87567-6 | 00779 |  |
| J2 | Connector, Receptacle Faston Tab | 1 | 62073-1 | 00779 |  |
| R1 | Resistor, Fixed, Film: 6.8 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF1/4-6.8K/J | 09021 |  |
| R2 | Resistor, Fixed, Film: 3.9 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF $1 / 4-3.9 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R3 | Resistor, Fixed, Film: 3.3 k ohm, $5 \%, 1 / 4 \mathrm{~W}$ | 1 | CF $1 / 4-3.3 \mathrm{~K} / \mathrm{J}$ | 09021 |  |
| R4 | Resistor, Fixed, Film: 10 k ohm, 5\%, 1/4 W | 14 | CF1/4-10K/J | 09021 |  |
| R5 | Same as R4 |  |  |  |  |
| R6 | Same as R4 |  |  |  |  |
| R7 | Resistor, Fixed Film: 43 ohms, 5\%, 1/4 W | 1 | CF1/4-43 OH.MS/J | 09021 |  |
| R8* | Resistor, Fixed, Film: 1.8 k ohm, 5\%, 1/4 W | 1 | CF1/4-1.8K/J | 09021 |  |
| R9 | Same as R4 |  |  |  |  |
| R10 | Not Used |  |  |  |  |
| $\mathrm{Rl1}^{\text {R11 }}$ |  |  |  |  |  |
| $\begin{aligned} & \text { Thru } \\ & \text { R18 } \end{aligned}$ | Same as R4 |  |  |  |  |
| R19 | Resistor, Fixed, Film: 2.0 k ohm, 5\%, $1 / 4 \mathrm{~W}$ | 1 | CF1/4-2.0K/J | 09021 |  |
| R20 | Same as R4 |  |  |  |  |
| R21 | Same as R4 |  |  |  |  |
| U1 | Integrated Circuit | 2 | P8279 | 34649 |  |
| U2 | Same as U1 |  |  |  |  |
| U3 | Integrated Circuit | 2 | DS8857N | 27014 |  |
| $U_{4}$ | Integrated Circuit | 2 | CD4067BE | 02735 |  |
| U5 | Integrated Circuit | 4 | DS8863N | 27014 |  |
| U6 | Same as U5 |  |  |  |  |
| J7 | Same as U3 <br> * Nominal value, final value factory selected. |  |  |  |  |



Figure 5-44. Type 796056-1 Front Panel Encoder Board (MFP A1A1), Location of Components

REF DESIG PREFIX MFP AlAI

5.6.8.2 TYPE 796057-5 FRONT PANEL SWITCH BOARD REF DESIG PREFIX MPP A1A2

| REF <br> DESIG | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | $\begin{gathered} \text { RECM } \\ \text { VENDOR } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| C1 DS5 DS6 | ```Capacitor, Electrolytic, Tantalum: 1uF,20%,35V Not Used Not Used``` | 1 | $196 \mathrm{D105} \mathrm{X0035} \mathrm{HE3}$ | 56289 |  |
| DS1* | Display LED | 6 | 5082-7623 | 28480 |  |
| DS14 | Not Used |  |  |  |  |
| DS17 | Not Used |  |  |  |  |
| DS18 | Not Used |  |  |  |  |
| DS19 | Part of S33 |  |  |  |  |
| DS2* | Same as DS1 |  |  |  |  |
| DS20 | Part of S17 |  |  |  |  |
| DS21 | Part of S18 |  |  |  |  |
| DS22 | Part of S19 |  |  |  |  |
| DS23 | Part of S20 |  |  |  |  |
| DS24 | Part of S21 |  |  |  |  |
| DS25 | Part of S22 |  |  |  |  |
| DS26 | Part of S23 |  |  |  |  |
| DS27 | Part of S24 |  |  |  |  |
| DS28 | Part of S25 |  |  |  |  |
| DS29 | Part of S26 |  |  |  |  |
| DS3* | Same as DS 1 |  |  |  |  |
| DS30 | Part of S27 |  |  |  |  |
| DS31 | Not Used |  |  |  |  |
| DS32 | Part of S29 |  |  |  |  |
| DS33 | Part of S30 |  |  | , |  |
| DS34 | Part of S31 |  |  |  |  |
| DS35 | Not Used |  |  |  |  |
| DS36 | Part of S34 |  |  |  |  |
| DS37 | Part of S35 |  |  |  |  |
| DS38 | Part of S36 |  |  |  |  |
| DS39 | Part of S37 |  |  |  |  |
| DS4* | Same as DS1 |  |  |  |  |
| DS40 | Part of S38 |  |  |  |  |
| DS41 | Not Used |  |  |  |  |
| DS42 | Not Used |  |  |  |  |
| DS43 | Not Used |  |  |  |  |
| DS44 | Part of S41 |  |  |  |  |
| DS45 | Part of S44 |  |  |  |  |
| DS46 | Part of S42 |  |  |  |  |
| DS47 | Part of S45 |  |  |  |  |
| DS48 | Part of S46 |  |  |  |  |



Figure 5-45. Type 796057-5 Front Panel Switch Board (MFPA1A2) Location of Components

REF DESIG PREFIX MFP A1A2



### 5.6.9 TYPE 791202-5 ENCODER ASSEMBLY REF DESIG PREFIX A2

| $\begin{aligned} & \text { REF } \\ & \text { DESIG } \end{aligned}$ | DESCRIPTION | $\begin{array}{\|l\|} \hline \text { QTY } \\ \text { PER } \\ \text { ASSY } \end{array}$ | MANUFACTURER'S PART NO. | $\begin{aligned} & \text { MFR. } \\ & \text { CODE } \end{aligned}$ | RECM VENDOR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| P1 | Housing | 1 | 87456-2 | 00779 |  |
| U1 | Encoder Assembly | 1 | 34836-1 | 14632 |  |



RETAINING RING

Figure 5-46. Type 791202-5 Encoder Assembly (MFP-A2)
Location of Components



Figure 6-2. Type 794278-1 Frequency Extender (FE-A1) Schematic Diagram 370820
notes.
UNLESS OTHERWISE SPECIFIED:
airesistance is in ohms, $\pm 3 \%$, t/aw.
blcapacitance is in of.


Figure 6-3. Type 794315-1 VhF Preselector/lst J.O (FE-A1^1) Schematic Diagram 470632



Figure 6-5. T'ype 370690-1 V(CO (FE-A1A1A2) Schematic Diagram 470470



Figure 6-7. Type 794316-1 Input Converter/2nd I.O (FE-AIA2 schemntic Diagrem 370706


HOTES:

1. UNLESS OTHERWISE SPECIFIED:
Ol RESISTANCE IS IN OHMS. $\because 5 \%, 1 / 4 \mathrm{w}$.
bleapacitance is in $\mu$ f.
2. nominal value, final value to be factory selected.







Figure 6-14. Type 791569 IF Motherboard (A4)


Figure 6-14. Type 791569 IF Motherboard (A4)
Schematic diagram 570)Iyl




BE USEO AS ALTERMARE IN TMS APPLICATION.
5. NOUIMAL VALUE, FIMAL VULUE FACTOMY SELECTED.



Figure 6-18. Type 796175-1 AGC Amplifice (A4AG)












to front panel motherboard (mpp-al)


















[^0]:    * NOTE: In the 232M Option, the master must be connected to the first Slave using a reverse (modem bypass) cable.

[^1]:    : gure 5-17. Type 794270-1 2nd Local Oscillator (A1A2A1), Location of Components

[^2]:    5-112

