INSTALLATION, OPERATION, AND INTERMEDIATE LEVEL MAINTENANCE MANUAL FOR THE WJ-8710A DIGITAL HF RECEIVER

P/N 181253-001, Revision L

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REVISION RECORD

Revision	Description	Date
A	Initial issue.	1/94
B	Add Synchronous AM Detection Mode and Variable AGC Feature.	5/94
C	Updated for 797214 Digital Control PC Assembly (A2).	5/95
D	Updated for WJ-8710A/REF Reference Generator Option.	8/95
E	Updated manual to reflect 871Y Control Version 04.01.05. Added information about the use of the CI-V Level Converter when using the CSMA Interface.	12/95
F	Corrected errata. Bit 6 of the Event Summary Status Register is not used. It cannot be used to flag front panel actions that cause a parameter change. Improved AGC attack time specification from 15 ms to 5 ms.	4/96
G	Added WJ part number to the title page. Incorporated a List of Effective Pages. Added page numbers to section cover pages and their back pages. Removed "intentionally left blank" pages and replaced with "Notes" pages that are formatted with headers and page numbers.	9/97
H	Incorporated ECO 039683.	6/99
J	Incorporated ECO 039883.	4/00
K	Incorporated ECO 040754.	12/00
L	Incorporated ECO 042584.	11/02

TECHNICAL NOTE

HANDLING OF LITHIUM BATTERIES

WARNING

This unit contains a lithium battery as back up power for memory retention. Extreme care should be used in storage, handling, and disposal of lithium batteries. Improper handling may present explosion hazard.

- Always wear eye protection when handling batteries.
- Do not puncture, compact, incinerate, short circuit, or expose to temperatures above 160°F (71°C).
- Do not expose batteries to charging currents.
- Do not store loose batteries in bins. Always store in original containers.
- Dispose of batteries properly. Discharged cells should be handled with care, as they retain significant energy. They should be electrically isolated and packaged for disposal. Dispose in accordance with local regulations for hazardous material disposal. DO NOT INCINERATE OR COMPACT.

WJ-8710A DIGITAL HF RECEIVER BATTERY REPLACEMENT FOR UNITS CONTAINING THE TYPE 797012 DIGITAL ASSEMBLY (A2)

The lithium battery contained in the WJ-8710A Receiver is mounted in a battery holder on the Type 797012 Digital Assembly (A2). If replacement is required, carefully insert a blunt, nonmetallic, tool between the bottom face of the battery and the holder at one of the five slots provided. Pry the battery up at a slight angle and remove with fingers. Take care to avoid shorting the positive (+) and negative (-) contacts during the removal process. Install the replacement battery with the positive contact face up. Insert battery under the battery clip at a slight angle and slide in place.

WJ-8710A DIGITAL HF RECEIVER BATTERY REPLACEMENT FOR UNITS CONTAINING THE TYPE 797214 DIGITAL ASSEMBLY (A2)

Refer to the instructions contained in **paragraph 7.7.9**.

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GENERAL DESCRIPTION

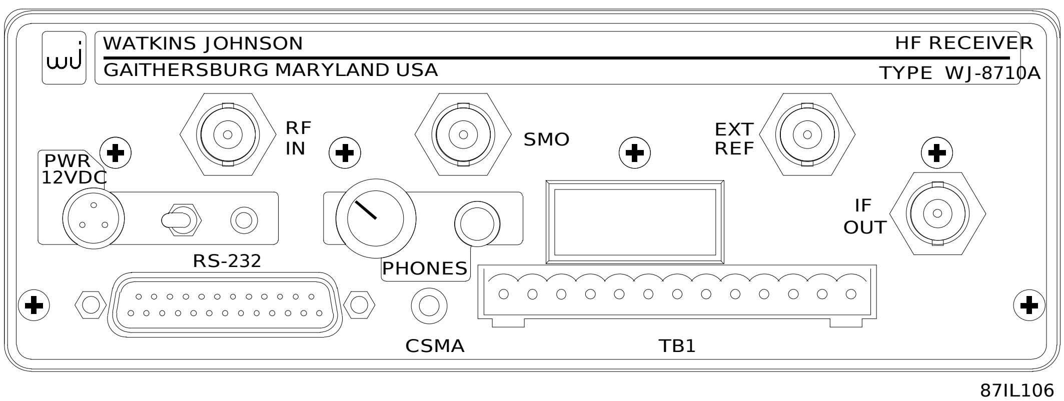

Figure 1-1. WJ-8710A Digital HF Receiver

SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The WJ-8710A Digital HF Receiver is a remote controlled, synthesized receiver capable of continuous 1 Hz tuning resolution over the frequency range of 5 kHz to 30.0 MHz. Available detection modes are AM, FM, CW, ISB, USB, LSB, and Synchronous AM (SAM). Selectable IF bandwidths, including 66 digital IF bandwidth filters and a tunable (non-linear phase) IF notch filter, are standard. Manual or automatic gain control (AGC) modes are selectable. In CW detection mode, beat frequency oscillator (BFO) and passband tuning capabilities are available. The BFO is adjustable over a ±8000 Hz range in 10 Hz steps. Passband tuning, which is an operator aid that facilitates simultaneous adjustments of tuned frequency and BFO, is adjustable over a ±2000 Hz range.

The receiver's squelch threshold can be set to any value from 0 to -135 dBm or can be turned off. For use with HF transmitters, audio signals can be muted via the presence of an external control signal input at the receiver's rear panel.

In addition to fixed frequency tuning, the WJ-8710A provides a flexible scanning capability. Three scan types are available: channel scan, frequency-to-frequency scan (F1 to F2), and frequency-to-frequency scan with lockouts. In channel scan mode, the receiver steps through a sequence of up to 100 user-programmable memory channels. Receiver parameters stored in each channel include frequency, IF bandwidth, detection mode, BFO, gain control mode, manual gain value, and squelch threshold. Prior to initiating the channel scan, the operator may select a specific range of channels to scan through. Individual channels within the range can be identified for the receiver to skip over during the scan. In both frequency-to-frequency scan modes, the receiver monitors frequencies between programmed start and stop frequencies according to a selected step size between 1 Hz and 25 kHz. For all scan modes, the receiver automatically stops when a signal is acquired that breaks the squelch threshold level. The duration of time the receiver holds on a signal before resuming scan (dwell time) is operator-selectable between 0.5 and 20 seconds. An infinite dwell time can also be selected. A built-in-test (BITE) function is available which can be used to verify equipment performance.

The WJ-8710A is operated remotely via one of two selectable serial interfaces. With the exception of audio output level and remote control mode selection, all receiver parameters are controllable and accessible via an RS-232C remote interface. A Carrier Sense/Multiple Access with Collision Detection (CSMA) interface with limited instruction set may be enabled, in lieu of RS-232C, to allow the WJ-8710A to be controlled using an alternate command protocol. A different set of remote control commands is utilized with each of the two interfaces. Selection of the active interface is made via an internal switch setting. Additionally, a built-in-test (BITE) function can be initiated from the RS-232C interface as well as status reporting.

The WJ-8710A's internal power supply accepts +11 to +16 Vdc line power as its power source. The unit's internal power supply automatically adjusts to the input voltage, providing it is within the acceptable limits. Total power consumption is less than 20 watts.

Refer to **Table 1-1** for a complete listing of WJ-8710A Digital HF Receiver specifications.

Table 1-1. WJ-8710A Digital HF Receiver Specifications

Frequency Range	5 kHz to 30 MHz (Tunable to 0 Hz, degraded performance below 500 kHz)
Tuning Resolution	1 Hz
Internal Reference Stability	Better than 0.7 PPM (0 to 50°C), Standard.
External Reference Frequency	Accepts 1, 2, 5 or 10 MHz (±1 PPM or better, 200 mV rms into high impedance load). Automatically switches to external reference upon application of signal
Synthesizer Lock Time	Less than 10 msec typical
Antenna Input	
Impedance	50 ohms, nominal
VSWR	2:1 maximum at receiver's tuned frequency
Maximum Input Signal	+30 dBm
Connector	BNC female
Third Order Intercept Point	+30 dBm typical, +25 dBm minimum (for signals separated by 50 kHz minimum)
Second Order Intercept Point	+60 dBm typical
Noise Figure	14 dB maximum (11 dB maximum with preamplifier engaged)
Detection modes	AM, FM, CW, USB, LSB, ISB, and SAM. (Consult factory for additional demodulation modes)

Sensitivity (500 kHz - 30 MHz)

Modulation	IF BW	S+N/N Min	Without Preamp Min dBm/µV
AM (50% mod. at 400 Hz)	6.0 kHz	10 dB	-103/(1.58)
FM (4.8 kHz dev. 400 Hz mod)	16.0 kHz	17 dB (SINAD)	-99/(2.50)
USB/LSB/ISB	3.2 kHz	10 dB	-112/(0.56)
CW	0.3 kHz	16 dB	-116/(0.35)

CW Sensitivity, 5 kHz - 500 kHz, without Preamp
(0.3 kHz IF Bandwidth)

50 kHz - 500 kHz	-113 dBm (0.5 µV) typical for 16 dB S+N/N
20 kHz - 50 kHz	-105 dBm (1.27µV) typical for 16 dB S+N/N
5 kHz - 20 kHz	-78 dBm (28 µV) typical for 16 dB S+N/N

Table 1-1. WJ-8710A Digital HF Receiver Specifications (Continued)

IF Bandwidths: ....

3 dB Bandwidths	Typical Shape Factor (3/60 dB)	3 dB Bandwidths	Typical Shape Factor (3/60 dB)
.056 kHz	1.45:1	1.000 kHz	1.40:1
.063 kHz	1.40:1	1.100 kHz	1.40:1
.069 kHz	1.40:1	1.200 kHz	1.35:1
.075 kHz	1.35:1	1.300 kHz	1.35:1
.081 kHz	1.35:1	1.400 kHz	1.35:1
.088 kHz	1.35:1	1.500 kHz	1.35:1
.094 kHz	1.35:1	1.600 kHz	1.30:1
.100 kHz	1.30:1	1.800 kHz	1.45:1
.113 kHz	1.45:1	2.000 kHz	1.40:1
.125 kHz	1.40:1	2.200 kHz	1.40:1
.138 kHz	1.40:1	2.400 kHz	1.35:1
.150 kHz	1.35:1	2.600 kHz	1.35:1
.163 kHz	1.35:1	2.800 kHz	1.35:1
.175 kHz	1.35:1	3.000 kHz	1.35:1
.188 kHz	1.35:1	3.200 kHz	1.30:1
.200 kHz	1.30:1	3.600 kHz	1.45:1
.255 kHz	1.45:1	4.000 kHz	1.40:1
.250 kHz	1.40:1	4.400 kHz	1.40:1
.275 kHz	1.40:1	4.800 kHz	1.35:1
.300 kHz	1.35:1	5.200 kHz	1.35:1
.325 kHz	1.35:1	5.600 kHz	1.35:1
.350 kHz	1.35:1	6.000 kHz	1.35:1
.375 kHz	1.35:1	6.400 kHz	1.30:1
.400 kHz	1.30:1	7.200 kHz	1.45:1
.450 kHz	1.45:1	8.000 kHz	1.40:1
.500 kHz	1.40:1	8.800 kHz	1.40:1
.550 kHz	1.40:1	9.600 kHz	1.35:1
.600 kHz	1.35:1	10.400 kHz	1.35:1
.650 kHz	1.35:1	11.200 kHz	1.35:1
.700 kHz	1.35:1	12.000 kHz	1.35:1
.750 kHz	1.35:1	12.800 kHz	1.30:1
.800 kHz	1.30:1	14.400 kHz	1.25:1
.900 kHz	1.45:1	16.000 kHz	1.20:1

(Consult factory for alternate or additional IF bandwidths)

Table 1-1. WJ-8710A Digital HF Receiver Specifications (Continued)

IF Output	
Center Frequency	455 kHz, nominal
Output Level	-20 dBm, nominal
Output Impedance	50 ohms, nominal
Connector Type	BNC female
Signal Monitor Output	
Center Frequency	455 kHz, nominal; inverted
Bandwidth	30 kHz (-6 dB) minimum
Output Level	30 dB above RF Input, nominal
Output Impedance	50 ohms, nominal
Connector Type	BNC female
Gain Control Modes	Manual, AGC Fast, and Slow
AGC Range	100 dB minimum
AGC Threshold	Remotely enabled by operator with AGT command and controlled with RFG command
AGC Attack Time	5 msec typical
AGC Decay Time	Fast: 10-100 msec variable in 10 ms steps Medium: 100-1000 ms variable in 100 ms steps Slow: 1-5 sec variable in 0.5 sec steps
Selectable Front End Gain/Attenuation	
Preamplifier Gain	10 dB (±2 dB)
Attenuation	15 dB (±2 dB)
Beat Frequency Oscillator (BFO)	
Tuning Range	±8000 Hz
Tuning Resolution	10 Hz
Image Rejection	90 dB minimum
IF Rejection	85 dB minimum, greater than 90 dB typical
Internal Spurious Responses	<-114 dBm referenced to RF input
Local Oscillator Phase Noise	-110 dBc @ 1 kHz offset, typical
Reciprocal Mixing	With a desired signal of 25 µV in the 3.2 kHz IF bandwidth, the desired signal-to-noise ratio is greater than 20 dB, when an undesired signal 70 dB higher in amplitude and 35 kHz removed in frequency is present.
Cross Modulation	With a desired signal of 10 µV an undesired signal 86 dB higher, 30% AM modulated produces less than 10% cross modulation for frequency separation of greater than 50 kHz in the 1 kHz bandwidth.
Blocking	An unwanted signal of 1 mV, which is separated from a desired signal of 1 µV by 20 kHz causes no fall in the IF output.

Table 1-1. WJ-8710A Digital HF Receiver Specifications (Continued)

Line Audio Outputs	
Number of Outputs	Two center-tapped, balanced outputs. For ISB mode, USB and LSB on separate outputs. For all other modes, audio signal is common to both outputs.
Output Level	0 dBm nominal into 600-ohm load
Connector Type	Screw Terminals
Speaker Output	
Number of Outputs	One output. For ISB mode, USB and LSB can be selected individually or combined.
Bandwidth	100 Hz to 13 kHz
Output Level	Adjustable up to 2 Vrms into 8-ohm load
Total Harmonic Distortion	Less than 3%
Connector Type	Screw terminals
Headphone Output	
Number of Outputs	Two unbalanced outputs. For ISB mode, one output contains USB (left channel), the other contains LSB (right channel). In all other modes, the audio signal is common to both outputs
Output Level	Adjustable up to 10 mW into 600-ohm load
Connector Type	Miniature 1/4" stereo jack
Remote Control	RS-232 or CSMA; selectable by internal switch
RS-232	Full duplex, 3-wire serial interface; rear panel 25-pin female D-shell connector
CSMA	Carrier Sense/Multiple Access with Collision Detection; half duplex; rear panel miniature phone jack
Baud Rates (Both Interfaces)	75, 150, 300, 600, 1200, 2400, 4800 and 9600; selectable by internal switches.
Operating Temperature	0°C to +50°C
Storage Temperature	-40°C to +70°C
Humidity	10 Cyclic days (240 Hrs.) Procedure III for Continuous Exposure to 95% RH.
Altitude	50,000 ft. non-operating 24,000 ft. operating
MTBF	In excess of 10,000 hrs. Estimated in accordance with MIL-HDBK 217E for Ground Fixed, +40°C environment.
Power Requirements	+12 Vdc (+11 to +16 Vdc)
Power Consumption	Less than 20 watts, typical
Dimensions	2.5" x 7.5" x 11.5" (6.35 x 19.05 x 29.21 cm) (excluding connectors and controls)
Weight	Less than 7 pounds (3.17 kG)

1.2 MECHANICAL CHARACTERISTICS

The WJ-8710A is a desk top unit which measures approximately 2.5 inches in height, 7.5 inches in width and 11.5 inches in depth. All controls and all input and output connectors are located on the front panel. Connector types are BNC, multipin, miniphones, 1/8-inch miniature stereo headphones jack and a 13-terminal audio terminal block.

The WJ-8710A enclosure and main chassis are constructed of vinyl clad steel and aluminum respectively. Removal of the enclosure provides access to all internal circuitry including the following three major assemblies: the Type 797214-1 Digital Assembly, the Type 797006-5 RF Tuner Assembly, and the Type 766027-1 DC/DC Power Supply Assembly.

1.3 OVERALL FUNCTIONAL DESCRIPTION

Functionally, the WJ-8710A can be divided into four subsystems: the RF Subsystem, the Digital Signal Processing (DSP) Subsystem, the IF/Audio Output Subsystem, and the Control Subsystem (see **Figure 1-2**).

The 5 kHz to 30.0 MHz RF antenna input signal is first applied to the RF subsystem. Here the RF signal is mixed with three local oscillator (LO) signals to produce an intermediate frequency (3rd IF) centered at 25 kHz. The 1st LO tunes from 40.455 to 70.455 MHz in 1 kHz steps to produce a 1st IF of 40.455 MHz. The 1st IF is mixed with the 2nd LO, which is fixed at 40 MHz, to produce a 2nd IF of 455 kHz. The 2nd LO is also routed to the DSP Subsystem for use as a system clock for the DSP processors.

The 2nd IF signal is then split. One path of the signal is routed to the rear panel SMO connector as the signal monitor output. The other path of the 2nd IF is routed to a mixer where it is mixed with the 3rd LO. The 3rd LO signal is fixed at 430 kHz to produce a 3rd IF of 25 kHz. The 3rd LO is also routed to the IF/Audio Output Subsystem to be used for final IF conversion.

The timing and synchronization of the LO's are driven by a 10 MHz reference signal. This reference can be generated by an internal 10 MHz clock or can be driven by an external reference input of 1, 2, 5, or 10 MHz.

The DSP Subsystem performs the majority of the signal processing functions within the receiver. This subsystem is comprised of a 16-bit analog-to-digital (A/D) converter, a 24-bit fixed-point Digital Signal Processor (DSP), and associated static random-access memory (SRAM).

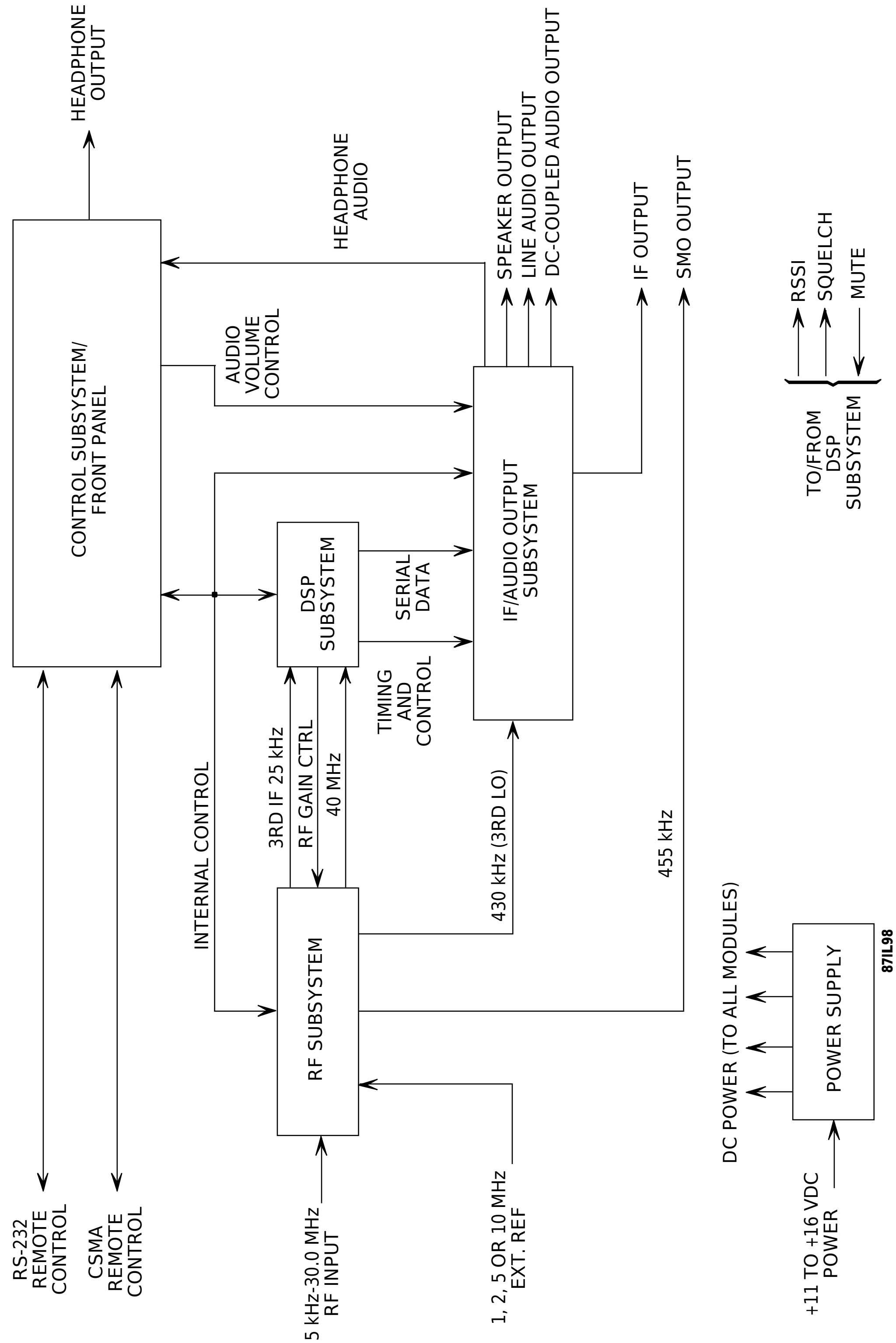

Figure 1-2. WJ-8710A Overall Functional Block Diagram

The 3rd IF signal, provided by the RF Subsystem, is sampled by the A/D converter to 16 bits of resolution at an output sampling rate of 100 kHz. This digitized output signal of the A/D is then applied to the DSP which performs the following functions to the sampled waveform:

- Fine tuning (in 1 Hz steps) in accordance with the operator selected tuned frequency,
- IF filtering in accordance with the operator-selected IF bandwidth,
- Gain control (AGC Fast, AGC Medium, AGC Slow or Manual),
- Determination of the received signal strength,
- Signal demodulation in accordance with the operator-selected detection mode, and BFO tuning resolution.
- Noise blanking, and
- Generation of a multiplexed digital serial data stream containing two demodulated audio channels and a post filtered IF signal for analog reconstruction by the IF/Audio Output Subsystem.

The IF/Audio Output Subsystem takes the multiplexed IF and audio serial data received from the DSP Subsystem and reconstructs it into two separate audio signals and one filtered IF signal. The two analog audio signals are processed in this subsystem to provide the following outputs:

- Two-channel (stereo) headphone outputs to the front panel PHONES jack,
- An 8-ohm speaker output that consists of one or both audio channels, and
- Two balanced line outputs with a fixed nominal output level of 0 dBm into 600 ohms.

Following analog reconstruction, the filtered IF signal is converted up to 455 kHz by a sample of the 430 kHz 3rd LO supplied by the RF Subsystem. The up-converted IF signal is passed through a bandpass roofing filter to remove unwanted mixer products, is buffered, and is then routed to the rear panel as the IF Output.

The Control Subsystem consists of a control microprocessor and its associated memory, an RS-232 interface, a Carrier Sense/Multiple Access (CSMA) interface. The control microprocessor monitors remote commands (via the remote interfaces), processes the instructions, and sends internal control data to the other subsystem in the receiver to update hardware. The control microprocessor also monitors the action of the hardware and appropriately updates and transmits remote responses (when queried) over the remote interface.

The Power Supply section of the receiver generates the dc supply voltages required by the subsystems of the receiver. The power supply is powered by the +11 to +16 Vdc input connected at the rear panel PWR 12 Vdc connector.

1.4 EQUIPMENT SUPPLIED

Equipment supplied with the WJ-8710A consists of an Installation and Operation Manual, and an accessory kit consisting of:

- Connector, Plug (mates with PWR 12 VDC connector)
- Fuse (replaces fuse on Power Supply Assembly, A1)
- Terminal Block (mates with audio terminal block)
- Rubber feet (four feet with mounting hardware)
- Installation Tool (used when installing or removing the WJ-8710 bottom housing for access to the Digital Assembly or the Power Supply Assembly).

1.5 EQUIPMENT REQUIRED BUT NOT SUPPLIED

To obtain full utilization of the receiver, equipment from the following list should be selected:

- HF Antenna, 50 ohm
- Headphones, 600 ohms
- Headphone adapter 1/4 inch to 1/8 inch (Radio Shack P/N 274-366)
- Phone plug (Switchcraft P/N 35HDNN)
- Line audio monitoring equipment
- Signal Monitoring equipment
- Remote Controller, CSMA or RS-232C compatible

1.6 RECEIVER OPTIONS

1.6.1 WJ-8710A/REF REFERENCE GENERATOR OPTION

This factory-installed option improves the WJ-8710A internal reference generator stability from better than 0.7 ppm to better than 0.1 ppm over an operating range of 0°C to 50°C. Refer to **Appendix A** for further information on the WJ-8710A/REF option.

1.6.2 WJ-8710/DSO1 DIGITAL SIGNAL OUTPUT OPTION

This option provides a digital signal output for external digital signal processing. A 15-pin D-subminiature connector is provided on the rear panel of the receiver for digital signal output. Refer to **Appendix D** for further information on the WJ-8710/DSO1 option.

1.6.3 WJ-871Y/PCSM PERSONAL COMPUTER SIGNAL MONITOR OPTION

This option enables the user to perform receiver control and monitoring functions via an IBM PC-compatible computer. A real time IF panoramic display is also available for use as a receiver tuning aid. The Microsoft Windows™-compatible software provided with this option provides the user with an easy-to-use, desk-top type control program environment.

1.6.4 WJ-871Y/485 485 INTERFACE OPTION

This option provides multidrop interface capability to the receiver via a rear panel connector. Refer to **Appendix H** for more information concerning the WJ-871Y/485 485 Interface option.

1.6.5 WJ-871Y/MULT

This option provides RS-232 multidrop capability to the receiver.

1.6.6 WJ-871Y/SEU SPEECH ENHANCEMENT UNIT

The WJ-871Y/SEU Speech Enhancement Unit option uses adaptive filtering techniques to provide enhancement of audio signals that are received from signals in the HF frequency band. The option utilizes these filter techniques to accomplish wideband noise reduction and automatic notch filtering of the audio signals. See **Appendix I**.

1.7 WJ-8710A SOFTWARE VERSION RELEASE HISTORY

To ensure efficient receiver operations, the WJ-8710A uses two microprocessors, each running its own software code. The digital microprocessor (A2U1) runs the internal control code, and the digital signal processor (A2U37) runs the digital signal processing (DSP) code.

1.7.1 WJ-8710A INTERNAL CONTROL SOFTWARE RELEASE HISTORY

The WJ-8710A internal control software is contained in EPROM A2U12. The original internal control software is version 03.01.00.

Software version 4.01.05 corrected deficiencies in the CSMA interface. Released on November 13, 1995, this version is to be used with RS-232 and CSMA only.

1.7.2 WJ-8710A DSP SOFTWARE RELEASE HISTORY

The WJ-8710A DSP software is stored in EPROM A2U56. The original DSP software is version 04.00.00.

SECTION II

INSTALLATION

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SECTION II

INSTALLATION

2.1 UNPACKING AND INSPECTION

Signia-IDT, Inc. ships the WJ-8710A and its accessories cushioned between molded-in-place expanded plastic pads in a double-walled carton. After unpacking the equipment, retain the shipping container and packing material until the equipment has been thoroughly inspected and it is ensured that reshipment is not necessary. Perform the following initial inspection:

1. Carefully inspect the outside of the shipping container for discoloring, stains, charring, or other signs of exposure to excessive heat, moisture, or liquid chemicals. Check for any signs of excessive shock or careless handling.

2. Remove all equipment and accessories from the shipping container. If any items are missing, contact the factory or your Signia-IDT, Inc. representative.

3. Remove and retain the white 5x6 inch PRODUCT DISCREPANCY REPORT card. This card should be used if reshipment of the equipment is required. It also contains important warranty adjustment information.

4. Carefully inspect the equipment for dents, scratches, damaged or loose pushbuttons or knobs, or any other signs of physical abuse or careless handling during shipment.

If damage is found, forward an immediate request to the delivering carrier to perform an inspection and prepare a concealed-damage report. Do not destroy any packing material until it has been examined by an agent of the carrier. Concurrently, report the nature and extent of damage to Signia-IDT, Inc., giving equipment serial numbers, so that necessary action can be taken. Under U.S. shipping regulations, claims for damage must be collected by the consignee; do not return the equipment to Signia-IDT, Inc. until a claim for damages has been established.

2.2 INSTALLATION

2.2.1 MOUNTING

The WJ-8710A Digital HF Receiver is a desk top unit which requires no special mounting instructions. If desired, the four rubber feet (mounted on the base of the unit) may be removed so that the unit can be secured to a flat mounting surface. **Foldout FO-1** shows the location of the four mounting holes. These holes are threaded to accept 6-32 screws.

CAUTION

Damage will occur to the WJ-8710A if the mounting screws penetrate further than 1/8-inch into the mounting holes on the bottom panel of the receiver. When mounting, make certain that the mounting screws used are of a length that do not penetrate further than 1/8-inch into the bottom panel.

2.2.2 POWER REQUIREMENTS AND FUSE REPLACEMENT

The WJ-8710A requires an input voltage of +11 to +16 VDC for operation. The receiver's internal power supply circuitry automatically adjusts to the power input applied (providing it is within the specified range). Therefore, no manual power source voltage selection is required. The connector supplied with the receiver (part of the accessory kit) connects to the three-pin PWR 12 VDC connector (J1) located on the front panel. The WJ-8710A requires less than 20 watts (typical) for operation.

A 3 amp fuse (A1F1) is provided and located on the Power Supply PC Assembly (A1). This fuse is accessible when the main chassis is removed from the enclosure. To replace the fuse, perform the following procedures:

1. Turn off the receiver and disconnect the power plug form the front panel PWR 12VDC connector.

2. Remove two black pan-head screws from the lower left and right corners of the front panel (**Figure 2-1**).

3. Remove four flat-head screws and two pan-head screws from the rear panel (**Figure 2-1**).

4. Remove the rear panel and then slide the main chassis (complete with front panel) out of the enclosure.

5. Locate the RFI gasket (the long copper strip) on each side of the receiver's deck assembly (between the deck assembly and the bottom housing).

6. Insert the special installation tool (included with the accessory kit) between the RFI gasket fingers, and the bottom housing along the entire length of the deck assembly (in the left side of the deck as viewed from the rear of the receiver). Insure that the tool is down against the flange on the deck and then slide the housing away from the front panel until it is free of the deck assembly.

7 Unplug the fuse from the DC/DC Power Supply Assembly (A1) (**Figure 2-2**).

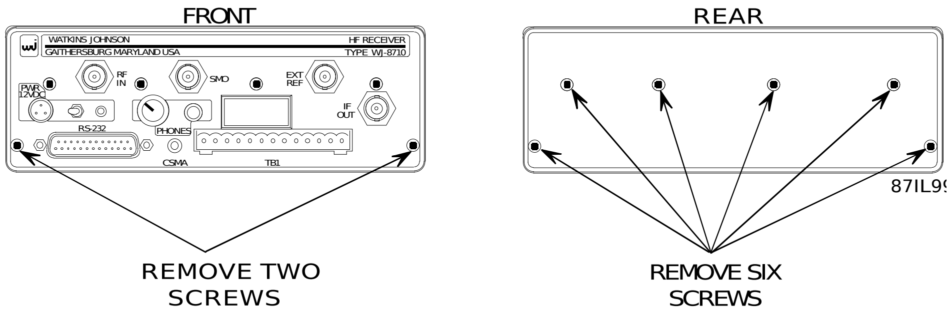


Figure 2-1. Detaching the Enclosure from the Main Chassis

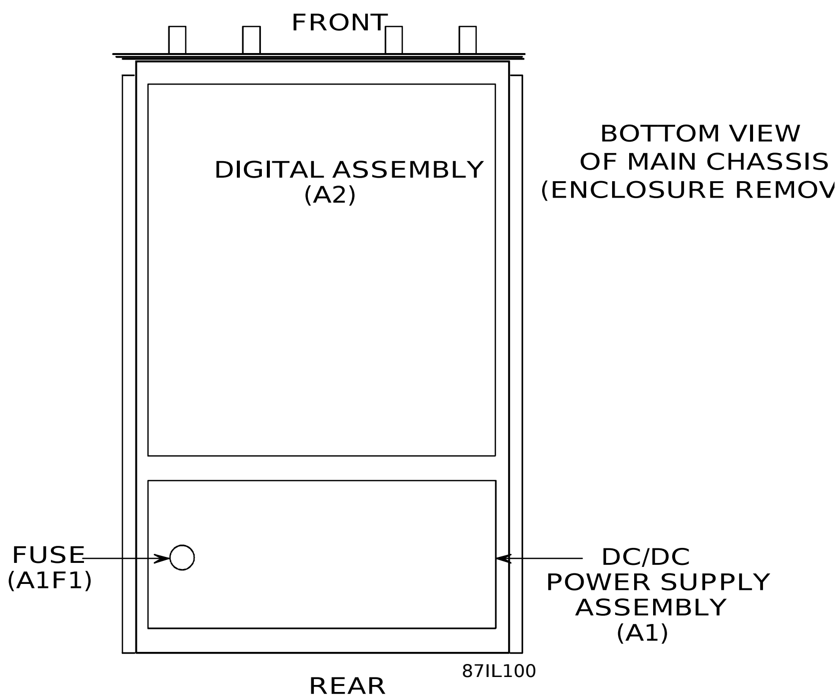


Figure 2-2. Location of Line Power Fuse A1F1

8. Insert a new 3-amp plug-in fuse into the fuse socket. (Use Tracor Littlefuse part no. 273003 or equivalent).

9. Install the bottom housing by laying the tool along the right side of the deck (as viewed from the rear of the unit). Position the tool so that the RFI gasket fingers are covered by the tool along the entire length of the deck. Align the bottom housing grooves with the deck flanges and slide the housing forward until it contacts the front panel. Lift the tool out of position so that the RFI fingers now contact the housing.

10. Slide the main chassis back into the enclosure, reinstall the rear panel and secure both panels in place with the screws that were removed in steps 2 and 3, respectively.

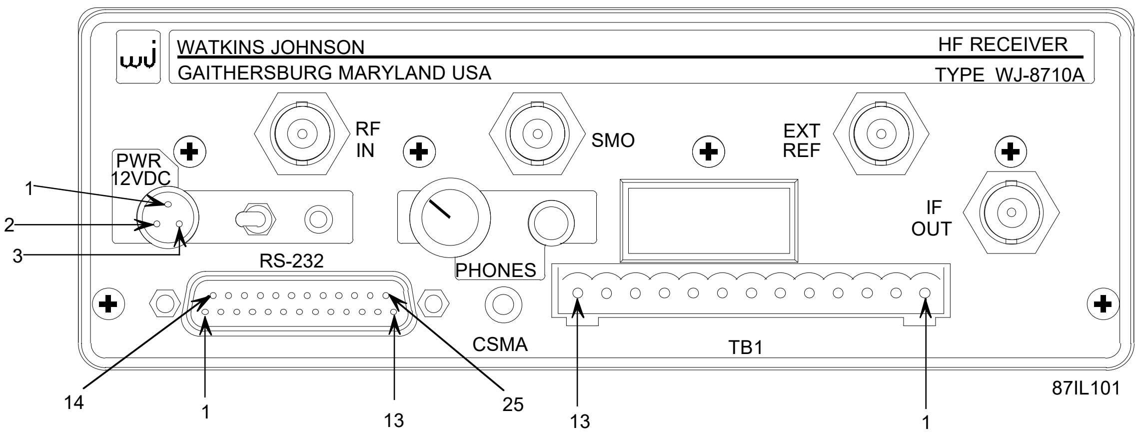
11. Reconnect the power plug to the front panel PWR 12 VDC connector.

2.2.3 CONNECTOR SIGNALS

All external connectors of the WJ-8710A are located on the front panel. **Table 2-1** lists these connectors and provides a brief description and the reference designation for each. **Figure 2-3** shows the location of the front panel connectors. The following paragraphs provide details of the signals resident at the connectors.

Table 2-1. List of Connectors

Connector	Reference Designation	Function
RF IN	A3J1	BNC female. RF input from an antenna.
SMO	A3J2	BNC female. Signal monitor output.
EXT REF	A3J3	BNC female. 1, 2, 5, or 10 MHz reference input.
IF OUT	A2J1	BNC female. Post-filtered IF output.
CSMA	A2J2	Mini-phone. Carrier Sense/Multiple Access (CSMA) remote interface port.
RS-232	A2J3	D-Type, 25-pin. RS-232C remote serial interface port.
TB1	TB1	Thirteen-terminal audio terminal block. Provides connection for two line audio outputs, DC-coupled audio output, speaker output, remote signal strength indication output, squelch output, and mute input.
PWR 12VDC	J1	Three-pin male receptacle, mates with the plug provided in the accessory kit. +11 to +16 Vdc power input.
PHONES	J2	Miniature stereo headphones jack. Headphones audio. To prevent damage to PHONES jack J2 use Switchcraft connector P/N 35HDNN for external wiring and Radio Shack adapter P/N 274-366 for headphones.



PWR 12VDC

PIN #	FUNCTION
1	+12 VDC INPUT*
2	GROUND
3	GROUND

*PIN 1 IS LOCATED NEXT TO CONNECTOR KEY

RS-232

PIN #	FUNCTION
1	NOT USED
2	TXD
3	RXD
4-6	NOT USED
7	GROUND
8-25	NOT USED

TB1

PIN #	FUNCTION
1	LINE A (+)
2	LINE A (CT)
3	LINE A (-)
4	LINE B (+)
5	LINE B (CT)
6	LINE B (-)
7	SPEAKER COM
8	SPEAKER (+)
9	DC AUDIO
10	RSSI
11	SQUELCH
12	MUTE
13	GROUND

Figure 2-3. WJ-8710A Front Panel Connectors

2.2.3.1 **RF IN, Antenna Input (A3J1)** - This BNC female connector accepts the 5 kHz-30.0 MHz RF input from the antenna. Input impedance is nominally 50 ohms.

2.2.3.2 **SMO, Signal Monitor Output (A3J2)** - The signal monitor output is a BNC female connector, which provides a sample of the 2nd intermediate frequency, centered at 455 kHz with a minimum (-6 dB) bandwidth of 30 kHz and an inverted spectrum. The nominal output impedance is 50 ohms with typically 25 dB of gain from the antenna input. This output may be used by a signal monitor or other ancillary equipment.

2.2.3.3 **EXT REF, External Reference Input (A3J3)** - This female BNC connector allows an external 1 MHz, 2 MHz, 5 MHz, or 10 MHz reference input, having a minimum level of 200 mV rms into a high impedance load, to be used as the time base for the receiver. The WJ-8710A automatically switches to external reference operation upon sensing the external reference input signal (providing it is within the specified limits).

2.2.3.4 **IF OUT, Post-Filtered IF Output (A2J1)** - This BNC female connector provides the post-filtered IF output. The output is centered at 455 kHz with a bandwidth equal to the operator-selected IF bandwidth. The nominal output level is -20 dBm into a 50 ohm load.

2.2.3.5 **CSMA, Carrier Sense/Multiple Access Port (A2J2)** - This mini-phone connector is used as the interface port for Carrier Sense/Multiple Access (CSMA) remote operations. The connector's center conductor carries the remote data while the sleeve is ground. See **Section V** of this manual for details on the CSMA remote interface and operations.

2.2.3.6 **RS-232, RS-232C Serial Interface Port (A3J3)** - This D-type, 25-pin connector is used as the interface port for RS-232C remote operations. The RS-232C interface operates as a full duplex interface at a selectable baud rate of 75 to 9600 bps. Pin 2 of this connector is the transmit data line (TXD), pin 3 is the receive data line (RXD) and pin 7 is ground. See **Section IV** of this manual for details on the RS-232C remote interface and operations.

2.2.3.7 **TB1, Audio Terminal Block (TB1)** - This terminal block contains 13 terminals for connection of various inputs and outputs of the receiver such as line audio outputs, speaker outputs, DC-coupled audio output, remote signal strength indicator output, squelch output, and mute input. These input and outputs at the terminals of A2TB1 are further described in the following paragraphs.

2.2.3.7.1 **Line Audio Outputs (TB1 Terminals 1 thru 6)** - Terminals 1 thru 6 of TB1 provide two, center-tapped balanced line audio outputs. One of the line audio outputs (LINE A) is provided on the combination of terminals 1, 2, and 3. Terminal 1 is the positive output (LINE A (+)), terminal 3 is the negative output (LINE A (-)) and terminal 2 is the ungrounded center tap output (LINE A (CT)).

The other line audio output (LINE B) is provided on the combination of terminals 4, 5, and 6. Terminal 4 is the positive output (LINE B (+)), terminal 6 is the negative output (LINE B (-)), and terminal 5 is the ungrounded center tap output (LINE B (CT)).

When the independent sideband (ISB) detection mode is selected, the LINE A output provides upper sideband (USB) audio while the LINE B output provides lower sideband (LSB) audio. In all other detection modes, the LINE A and LINE B outputs provide identical signal content.

The output signal level for input signals above the AGC threshold is 0 dBm nominal (±3 dB). Output impedance for both line audio outputs is 600 ohms.

2.2.3.7.2 **Speaker Output (TB1 Terminals 7 and 8)** - Terminals 7 and 8 of TB1 provide an audio output, sufficient to drive an external 8 ohm speaker. Terminal 7 is common (SPEAKER COM), and terminal eight is positive (SPEAKER (+)). The bandwidth of the output audio is 0.1 to 13.0 kHz at ±2 dB. Output level is 2 Vrms minimum with less than 3% total harmonic distortion.

Lower sideband (LSB) or upper sideband (USB) audio can be selected individually or combined, while in the ISB detection mode, and made available at the speaker output.

2.2.3.7.3 **DC-Coupled Audio Output (TB1 Terminal 9)** - Terminal 9 of TB1 provides a DC-coupled version of the audio provided at the speaker output (see **paragraph 2.2.3.7.2**).

2.2.3.7.4 **Remote Signal Strength Indicator Output (TB1 Terminal 10)** - Terminal 10 of TB1 provides an analog output representing the strength of the current detected signal which can be used to drive an external signal strength indicator. The output is a dc voltage which is a linear representation of the strength of the received signal. The output is 0 Vdc for a signal strength of -120 dBm and +5 Vdc for a signal strength of +10 dBm into a high impedance load.

2.2.3.7.5 **Squelch Output (TB1 Terminal 11)** - Terminal 11 of TB1 provides a low impedance to ground (capable of sinking 150 mA) when the receiver's signal squelch circuitry is activated (i.e., the detected signal is above the set squelch level). This output is provided for system integration of the WJ-8710. This output appears as a +5 Vdc source through a 100 kΩ impedance when signal squelch is not active.

2.2.3.7.6 **Mute Input (TB1 Terminal 12)** - Terminal 12 of TB1 is provided to accept a logic level mute input from an external source. When the input at this terminal is grounded (or driven to a CMOS logic low) all audio outputs of the receiver are disabled.

2.2.3.8 **<u>PWR 12VDC, Power Input (J1)</u>** - This three-pin male connector accepts a +12 Vdc power input for the receiver. Pin 1 of the connector is the +12 Vdc input, pin 2 and pin 3 are ground. The receiver requires less than 20 watts for operation.

CAUTION

To prevent damage to PHONES jack J2 use Switchcraft connector P/N 35HDNN for external wiring and Radio Shack adapter P/N 274-366 for headphones.

2.2.3.9 **PHONES, Front Panel Headphones Jack (J2)** - The PHONES connector is a miniature stereo headphones jack. Each channel of this output provides a minimum of 10 mW at less than 5% total harmonic distortion into a 600 ohm load, when the input signal is above the AGC threshold. Located beside the PHONES jack on the front panel is a volume control knob. A clockwise rotation of this knob results in an increase in headphones output signal level. When the independent sideband (ISB) detection mode is selected, the right channel provides lower sideband (LSB) audio while the left channel provides upper sideband (USB) audio. In all other detection modes, both channels provide identical signal content.

2.2.4 CONFIGURING THE RECEIVER FOR REMOTE OPERATIONS

The WJ-8710A contains two DIP switches that are used to configure the receiver for remote operation. These switches are mounted on the Digital PC Assembly (A2) and are accessed by removing the receiver's main chassis from the enclosure. Refer to the procedures provided in **paragraph 2.2.2** for details on removing the main chassis from the enclosure. Refer to **Figure 2-4** for the location of the switches and details on the switch assignments. The switches are designated A2S1 and A2S2. Each switch contains eight rocker-type switches. The rocker switches are on when they are in the down position and are off when in the up position.

NOTE

Receiver power must be cycled in order for switch settings to take effect. Use the front panel PWR 12VDC switch to recycle power after a switch setting change for A2S1 or A2S2.

The rocker switches in A2S1 are used to enable either the RS-232C or the CSMA interface for remote operations, and to set the baud rate for the selected interface. Setting switch 4 of A2S1 to off (up) enables the RS-232C interface. Conversely, setting switch 4 to on enables the CSMA interface.

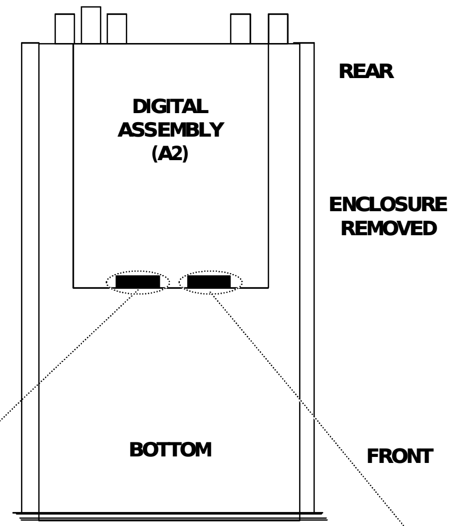
The positions of switches 1, 2, and 3 of A2S1 are used to set the baud rate for remote operations. Selectable baud rates are 75, 150, 300, 600, 1200, 2400, 4800, and 9600 bps. See **Figure 2-4** for the proper positions of switches 1, 2, and 3 of A2S1 to select the desired baud rate.

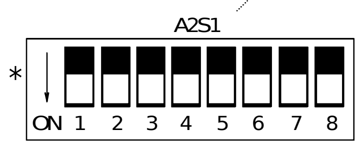
Switches 1 thru 6 of A2S2 are used to set the receiver's address on the CSMA bus during CSMA remote operations. Valid addresses are from 01 to 63 (address 00 is reserved). See **Figure 2-4** for the proper positions of switches 1 thru 6 of A2S2 to select the desired CSMA bus address. When it is desirable to have the WJ-8710A emulate the ICOM R71A HF Receiver, the CSMA address should be set to 26.

Switch 8 of A2S2 is used to set the tuned frequency command and response formats on the CSMA interface to four bytes or five bytes. Setting this switch to the on (down) position selects the five-byte format and setting it to the off (up) position selects the four-byte format. It is recommended that the WJ-8710A be set for four bytes.

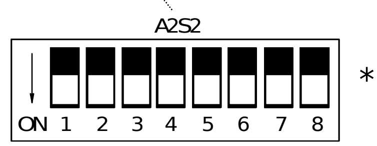
When determining the switch settings to achieve a specific binary value, a switch in the off (up) position corresponds to a binary 0 while a switch in the on (down) position corresponds to a binary 1.

Figure 2-5 gives an example of switches A2S1 and A2S2 set to positions to provide particular configurations. In the example, switch A2S1 is set to select CSMA remote operation with a baud rate of 2400 bps. Switch A2S2 is set to provide a CSMA address of 26 and a four-byte tuned frequency format.





Off (Up) = 0
On (Down) = 1



A2S1

** ROCKER SWITCH:	FUNCTION:
4	Remote Interface Selection
0	RS-232 Interface
1	CSMA Interface

3 2 1	BAUD RATE (bps)
0 0 0	9600
0 0 1	4800
0 1 0	2400
0 1 1	1200
1 0 0	600
1 0 1	300
1 1 0	150
1 1 1	75

A2S2

** ROCKER SWITCH	FUNCTION:
1 thru 6	CSMA Address Selection

6 5 4 3 2 1	Address	6 5 4 3 2 1	Address	6 5 4 3 2 1	Address
0 0 0 0 0 1	1	0 1 0 1 1 0	22	1 0 1 0 1 1	43
0 0 0 0 1 0	2	0 1 0 1 1 1	23	1 0 1 1 0 0	44
0 0 0 0 1 1	3	0 1 1 0 0 0	24	1 0 1 1 0 1	45
0 0 0 1 0 0	4	0 1 1 0 0 1	25	1 0 1 1 1 0	46
0 0 0 1 0 1	5	0 1 1 0 1 0	26	1 0 1 1 1 1	47
0 0 0 1 1 0	6	0 1 1 0 1 1	27	1 1 0 0 0 0	48
0 0 0 1 1 1	7	0 1 1 1 0 0	28	1 1 0 0 0 1	49
0 0 1 0 0 0	8	0 1 1 1 0 1	29	1 1 0 0 1 0	50
0 0 1 0 0 1	9	0 1 1 1 1 0	30	1 1 0 0 1 1	51
0 0 1 0 1 0	10	0 1 1 1 1 1	31	1 1 0 1 0 0	52
0 0 1 0 1 1	11	1 0 0 0 0 0	32	1 1 0 1 0 1	53
0 0 1 1 0 0	12	1 0 0 0 0 1	33	1 1 0 1 1 0	54
0 0 1 1 0 1	13	1 0 0 0 1 0	34	1 1 0 1 1 1	55
0 0 1 1 1 0	14	1 0 0 0 1 1	35	1 1 1 0 0 0	56
0 0 1 1 1 1	15	1 0 0 1 0 0	36	1 1 1 0 0 1	57
0 1 0 0 0 0	16	1 0 0 1 0 1	37	1 1 1 0 1 0	58
0 1 0 0 0 1	17	1 0 0 1 1 0	38	1 1 1 0 1 1	59
0 1 0 0 1 0	18	1 0 0 1 1 1	39	1 1 1 1 0 0	60
0 1 0 0 1 1	19	1 0 1 0 0 0	40	1 1 1 1 0 1	61
0 1 0 1 0 0	20	1 0 1 0 0 1	41	1 1 1 1 1 0	62
0 1 0 1 0 1	21	1 0 1 0 1 0	42	1 1 1 1 1 1	63

* All positions on both switches are shown in the On (down) position.

** Rocker switches not listed are not used.

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Figure 2-4. Locating and Setting Configuration DIP Switches A2S1 and A2S2

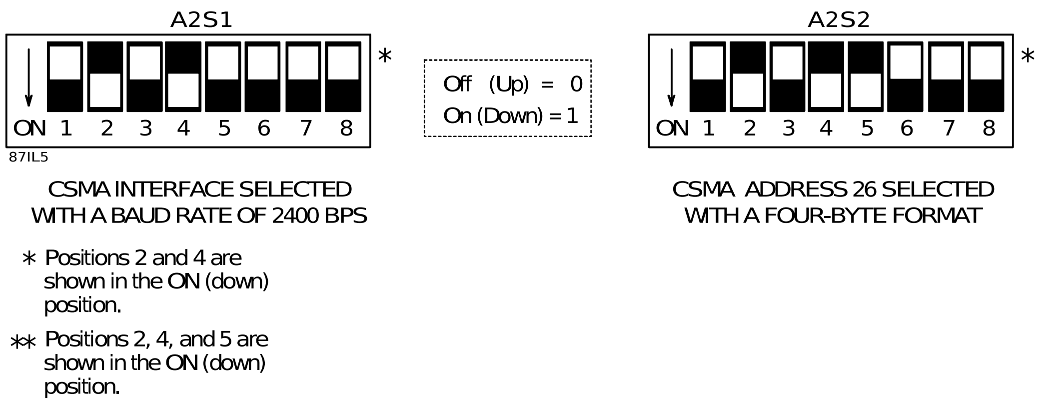

Figure 2-5. Examples of Set DIP Switches A2S1 and A2S2

2.3 EQUIPMENT MALFUNCTIONS

This unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. If an apparent malfunction is encountered after installation, verify that the correct input signals are present at the proper connectors. Prior to taking any corrective maintenance action or breaking any seals, contact your Signia-IDT, Inc. representative, or Signia-IDT, Inc. Customer Service Department to prevent the possibility of voiding the terms of the warranty. Contact Signia-IDT, Inc. via mail, telephone, wire, or cable at:

Signia-IDT, Inc.
Customer Service Department
700 Quince Orchard Road
Gaithersburg, Maryland 20878-1794

Toll Call: (301) 948-7550, Extension 7201
TELEX: 89-8402
TELEFAX: (301) 921-9479

If reshipment is necessary, follow the instructions in the following paragraph (Preparation for Reshipment or Storage). Do not return the equipment until a Return for Maintenance Authorization (RMA) number has been obtained from Signia-IDT, Inc. Customer Service Department. See Item 10 in the General Terms and Conditions of Sale paper (Form #WJ-151-X) for more information on equipment returns.

2.4 PREPARATION FOR RESHIPMENT OR STORAGE

If the equipment must be prepared for reshipment, the packaging method should follow the pattern established in the original shipment. Use the best packaging materials available to protect the equipment during reshipment or storage. When possible, use the original packing containers and cushioning material. If the original packing materials are not available, use the following procedure:

1. Wrap the equipment in sturdy paper or plastic.

2. Place the wrapped equipment in strong shipping containers and place a layer of shock-absorbing material (3/4-inch minimum thickness) around all sides of the equipment to provide a firm cushion and to prevent movement inside the container.

3. If shipping the equipment for service, fill out all information on the 5x6-inch PRODUCT DISCREPANCY REPORT card (Form # WJC-QA55-0) that was provided with the original shipment. Also ensure that the Return for Maintenance Authorization (RMA) number is recorded on the card. (See **paragraph 2.3** for details on obtaining this number.) If this card is not available, attach a tag to the equipment containing the following information:

    a. Return for Maintenance Authorization (RMA) number.

    b. The Type/Model number of the equipment.

    c. Serial number.

    d. Date received.

    e. Date placed in service.

    f. Date of failure.

    g. Warranty adjustment requested, yes or no.

    h. A brief description of the discrepant conditions

    i. Customer name and return address.

    j. Original Purchase Order/Contract number.

4. Thoroughly seal the shipping container and mark FRAGILE.

    When storing the equipment for extended periods, follow the above packing instructions to prevent damage to the equipment. The safe limits for storage environment are as follows:

    Temperature: -40 to +70°C
    Humidity: less than 95%

5. Ship to:

   Signia-IDT, Inc.
   700 Quince Orchard Road
   Gaithersburg, MD 20878-1794
   U.S.A.

SECTION III

LOCAL OPERATION

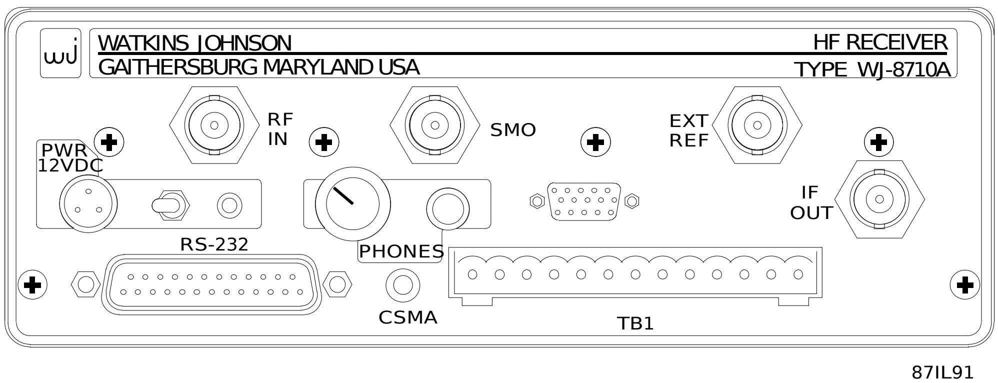

Figure 3-1. Front Panel Controls and Indicators

SECTION III

LOCAL OPERATION

3.1 INTRODUCTION

This section provides information related to the local operation of the WJ-8710A Digital HF Receiver using its front panel.

3.2 DESCRIPTION OF CONTROLS

The front panel of the receiver contains all of the controls that are used for local and remote operation. The receiver is basically a slave unit controlled by the remote controller as described in **Sections IV** and **V**. **Figure 3-1** shows the control locations on the front panel.

Front panel controls consist of the PWR 12 VDC switch, and the PHONES volume control.

3.2.1 THE PHONES OUTPUT VOLUME CONTROL KNOB

The PHONES output volume control knob is located to the left of the PHONES jack near the center of the front panel. This knob is used to increase or decrease the volume level of the audio output on both channels of the PHONES jack. A clockwise rotation increases the volume of a nominal audio signal up to approximately 10 milliwatts and a counterclockwise rotation decreases the volume to approximately 0 milliwatt.

CAUTION

To prevent damage to PHONES jack J2 use Switchcraft connector P/N 35HDNN for external wiring and Radio Shack adapter P/N 274-366 for headphones.

3.2.2 THE POWER SWITCH

The PWR 12 VDC switch is a miniature toggle switch located on the left-hand side of the front panel. This switch is used to turn the receiver on and off. When the switch is set to the right (off) position, the receiver is turned off. When set to the left (on) position, the red LED (next to the switch) illuminates and the receiver starts its power-up and initialization routine (refer to **paragraph 3.3**).

3.3 TURNING ON THE RECEIVER

The receiver is turned on when the PWR 12 VDC switch is set to the left (on) position. From the off state, turning the receiver on causes it to go into its power-up and initialization routine.

After approximately one second, initialization is complete, and the receiver automatically returns to the last set of operating parameters.

The WJ-8710A is equipped with battery backed-up memory. When the receiver is turned off, all current receiver parameters (including channel set-ups) are saved in memory. When the receiver is powered up, the receiver parameters that were set, prior to the receiver being turned off, are reset.

NOTES

SECTION IV

RS-232 REMOTE OPERATION

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SECTION IV

RS-232 REMOTE OPERATION

4.1 INTRODUCTION

The WJ-8710A Digital HF Receiver has the built-in capability of being controlled remotely by a computer or other controller device that is equipped with an RS-232 serial interface and capable of transmitting and receiving ASCII-standard encoded characters. Physically, the controller device needs only a transmit line (TXD), a receive line (RXD), and a ground line to communicate with the receiver.

The WJ-8710A can be set for RS-232 remote control. Switch 4 of DIP switch A2S1 can be set to the off (up) position to activate the RS-232 remote control. A baud rate hardware default can also be selected. Refer to **paragraph 2.2.4** for details on configuring DIP switch A2S1.

Various receiver parameters can be controlled and/or monitored over the RS-232 interface. These parameters are:

- tuned frequency,
- BFO frequency,
- detection mode,
- squelch level,
- speaker type,
- IF bandwidth,
- gain mode,
- built-in-test (BITE) execution,
- error status (both current and latched),
- selection of remote control, or remote control with local lockout,
- selection of F1-to-F2 scan start and stop frequencies,
- selection of channel scan start and stop channels,
- passband tuning offset frequency,
- tunable notch filter adjustment
- external reference,
- signal strength,
- squelch status,
- mute status,
- receiver identity,
- manual gain,
- signal dwell time,
- blanking time,
- selection of channel scanning, F1-to-F2 scanning, or F1-to-F2 scanning with local lockouts,
- selection of F1-to-F2 scan increment,
- selection of frequency lockouts,
- store current receiver parameters to selected memory channel,
- store current internal control software version

This section of the manual contains all the information necessary to enable an operator to control and monitor the above receiver parameters from an RS-232 controller. Details on how to properly format and transmit remote messages and how to read responses from the receiver are provided.

Before attempting to operate the receiver remotely, it is recommended that the operator become familiar with the operation and capabilities of the receiver by viewing the information provided in **Section III** of this manual. It is also recommended that the operator become familiar with the operation of the controller by viewing its literature, prior to remote control operation of the WJ-8710A.

NOTE

All remote RS-232 messages must be terminated with a line feed. **Refer to paragraph 4.3.1**.

4.2 INTERFACING WITH THE WJ-8710A

The RS-232 interface of the WJ-8710A is physically implemented on the RS-232 connector (A2J3), located on the rear panel. This interface has a full duplex operation, meaning that it can transmit and receive data simultaneously. The interface is set up as a "three-wire" RS-232 configuration, implemented on the transmit data line (TXD), the receive data line (RXD), and ground. These three wires are provided at the front panel RS-232 connector on pins 2, 3, and 7, respectively.

This interface supports software handshaking only, including XON/XOFF (receiver protocol) and ACK/NAK (transmitter protocol). Hardware handshake signals such as RTS (request to send), CTS (clear to send), DTR (data terminal ready), or DSR (data set ready) are not supported.

RS-232 serial interfaces use a method of transmitting data one bit at a time over the TXD and RXD lines. For example, an eight-bit character takes eight sequential transmissions to complete the character. In RS-232 serial transmissions, data is sent in frames (or packets). Each bit within the frame is determined by a voltage level. The voltage levels used by this interface are -8 Vdc (nominal) for a logic "1" and +8 Vdc (nominal) for a logic "0". In the inactive or quiet state, the transmit line is held at a logic 1.

The baud rate (rate of data flow in bits per second) for the WJ-8710A is selectable (75, 150, 300, 600, 1200, 2400, 4800, or 9600 bps). Switches 1, 2, and 3 of DIP switch A2S1 can be set to appropriate positions to select the hardware default baud rate. Refer to **paragraph 2.2.5** in **Section II** of this manual for details on configuring DIP switch A2S1.

The WJ-8710A is set up with a fixed data word frame format consisting of ten bits, and comprised of the following:

- one start bit,
- an eight-bit character, and
- no parity bit.
- one stop bit.

An example illustration of the fixed data word format is shown in **Figure 4-1**.

START BIT	BIT0	BIT1	BIT2	BIT3	BIT4	BIT5	BIT6	BIT7	STOP BIT

Figure 4-1. Fixed Data Word Format

It is important in serial data transmissions that the receiving device knows when data is being transferred and when data being transferred is about to stop. This information is conveyed by the above start and stop bits. The start bit synchronizes the receiving device so it reads the data properly. The stop bit notifies the receiving device that the data frame has ended. The WJ-8710A's fixed data word frame format does not contain a parity bit.

4.3 COMMAND MESSAGE FORMATTING

Command messages for the WJ-8710A are exclusively ASCII-encoded data, consisting of command headers and arguments. Command headers consist of three character mnemonics. All queries consist of a command header, followed by a question mark (?). All command arguments are in the "forgiving" numerical representation form. (Refer to **paragraph 4.3.3.**)

Command messages are divided into two categories: receiver device messages and communication messages. (Refer to **paragraphs 4.4** and **4.5** respectively.)

Multiple commands may be sent to the receiver at once by transmitting them as a string. All commands in the string must be separated by a semicolon (;) (i.e., DET 1;BWS 4).

4.3.1 TERMINATORS FOR COMMANDS AND QUERIES

Terminators are used to signal the end of a command or string. When a properly formatted message is ready to be sent, a LF (line feed) character should be entered. The LF character instructs the receiver to process the preceding message(s).

The WJ-8710A also transmits a terminator when responding to queries. After the query response is transmitted the receiver issues a CR,LF (carriage return, line feed characters), indicating end of response.

4.3.2 FORMATS OF QUERY RESPONSES

The WJ-8710A transmits responses to queries in a fixed-field format. Query responses begin with the three-letter mnemonic of the query in upper-case characters, followed by a numeric argument. In all query responses, the mnemonic and argument are separated by a space. Numeric arguments are represented by the least number of digits possible, while still representing the entire range of the value. If a negative value is allowed for the argument, a positive or negative sign is always given. Responses due to multiple queries are linked together in a query string, with each query and its argument separated with a semicolon from other queries in the string. The WJ-8710A terminates all responses to single queries or query strings with the CR (carriage return) and LF (line feed) characters.

4.3.3 REPRESENTATION OF NUMERIC ARGUMENTS

Arguments for commands and queries in this manual are represented by an nrX (where X is either f, 1, or 2). The nrf representation is used for command numeric arguments. The nr1 and nr2 are used for the representation of query response arguments.

Numeric arguments that are used with commands are accepted in a forgiving numeric representation (nrf). This implies that the WJ-8710A is a forgiving listener. Specific details on numeric representation are given below.

- nrf - The nrf (forgiving numeric representation) data element for commands is composed of the sequential fields listed below. All fields (1-5) are optional with one restriction: at least one digit must be present with the active data element of the argument.

Field	Data
1	Plus (+) or minus (-) sign.
2	Any number of digits, up to eight.
3	A decimal point (.).
4	Any number of digits, up to eight.
5	An upper-case "E" or lower-case "e" followed by an optional sign and at least one digit but no more than two digits.

  If the WJ-8710A receives an nrf of a precision greater than it can handle, it rounds the number rather than truncating it. When rounding, the unit ignores the sign of the number and rounds up on values greater than or equal to one half. It rounds down on values less than one half.

- nr1 - The nr1 is a numeric query response data format for integers, composed of an optional sign field, followed by any number of digits. The decimal point is implicitly defined to always follow the last digit and is therefore, not present in the response data element.

- nr2 - The nr2 numeric response data format is composed of an optional sign field, followed by any number of digits, a decimal point, and any number of digits. At least one digit is always present on both sides of the decimal point.

4.4 RECEIVER DEVICE MESSAGES

Receiver Device Messages are commands that affect the operational parameters of the receiver. These commands are listed in **Table 4-1**. The following paragraphs provide information on the setting and/or selection of a number of the operational parameters listed in **Table 4-1**.

Table 4-1. Receiver Device Messages

Command	Response	Description
ADV		Advance to next scan frequency. Operates when WJ-8710A is in dwell mode during scan.
AGC nrf		Select gain control mode. Range: 0 - 3 Where: 0 - Manual 1 - Slow AGC 2 - Fast AGC 3 - Medium AGC
AGC?	AGC nr1	Request active gain control mode. Reset: AGC 2 Default: AGC 2 Example: AGC 0
AGD nrf nrf		Set decay time for gain control modes.
Field	Parameter	
1	Gain control mode	Where: 1 - Slow AGC 2 - Fast AGC 3 - Medium AGC
2	Time (milliseconds)	If Slow AGC -1000 to 5000 (rounds up to next lower 400 millisecond step) Fast AGC -10 to 100 (round to next lower 10 millisecond step) Medium AGC -100 to 1000 (round to next lower 100 millisecond step)
AGD? nrf	AGD nr1, nr1	Recall the decay time associated with the specified AGC mode. Range: 1 - 3 Reset: AGD 1, 2000 AGD 2, 20 AGD 3, 200 Example: AGD 1, 2500 AGD 2, 20 AGD 3, 250

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
AGT nrf		Select AGC threshold mode. (Refer to **paragraph 4.4.3.1**.) Range: 0 - 1 Where: 0 - Off 1 - On
AGT?	AGT nr1	Request active gain control mode. Reset: AGT 0 Default: AGT 0 Example: AGT 1
BFO nrf		Set frequency in Hz (10 Hz steps). Range: -8000 to +8000 Where: +0000 = BFO Off
BFO?	BFO nr1	Request current BFO frequency. Reset: BFO +0000 Default: BFO +1000 Example: BFO -7990
BLK nrf		Select blanking setting. Range: 0 to 10
BLK?	BLK nr1	Request active blanking setting. Example: BLK 5 Default: BLK 0
BWC nrf		Select an IF bandwidth size in Hz. Range: 0 to 16000 Note: If the value entered is not a standard IF bandwidth (see **Table 1-1**), the standard IF bandwidth that is greater in value and closest to the requested IF bandwidth will be selected.
BWC?	BWC nr1	Request the current IF bandwidth in Hz. Reset: 06000 Default: 06000 Example: 03200

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
BWN nrf		Select one of the 66 available IF bandwidth filters. Where nrf represents the filter number. The narrowest bandwidth (.056 kHz) being number 1 and the widest bandwidth (16.0 kHz) being number 66. Range: 001 to 066 Where: 001 = .056 kHz 034 = 1.00 kHz 002 = .063 kHz 035 = 1.10 kHz 003 = .069 kHz 036 = 1.20 kHz 004 = .075 kHz 037 = 1.30 kHz 005 = .081 kHz 038 = 1.40 kHz 006 = .088 kHz 039 = 1.50 kHz 007 = .094 kHz 040 = 1.60 kHz 008 = .100 kHz 041 = 1.80 kHz 009 = .113 kHz 042 = 2.00 kHz 010 = .125 kHz 043 = 2.20 kHz 011 = .138 kHz 044 = 2.40 kHz 012 = .150 kHz 045 = 2.60 kHz 013 = .163 kHz 046 = 2.80 kHz 014 = .175 kHz 047 = 3.00 kHz 015 = .188 kHz 048 = 3.20 kHz 016 = .200 kHz 049 = 3.60 kHz 017 = .225 kHz 050 = 4.00 kHz 018 = .250 kHz 051 = 4.40 kHz 019 = .275 kHz 052 = 4.80 kHz 020 = .300 kHz 053 = 5.20 kHz 021 = .325 kHz 054 = 5.60 kHz 022 = .350 kHz 055 = 6.00 kHz 023 = .375 kHz 056 = 6.40 kHz 024 = .400 kHz 057 = 7.20 kHz 025 = .450 kHz 058 = 8.00 kHz 026 = .500 kHz 059 = 8.80 kHz 027 = .550 kHz 060 = 9.60 kHz 028 = .600 kHz 061 = 10.4 kHz 029 = .650 kHz 062 = 11.2 kHz 030 = .700 kHz 063 = 12.0 kHz 031 = .750 kHz 064 = 12.8 kHz 032 = .800 kHz 065 = 14.4 kHz 033 = .900 kHz 066 = 16.0 kHz
BWN?	BWN nrl	Request active IF bandwidth number. Reset: BWN 055 Default: BWN 055 Example: BWN 028

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
BWS nrf	BWS nr1	Select an IF bandwidth. Range: 1-5 Where: 1 - 0.30 kHz 2 - 1.00 kHz 3 - 3.20 kHz 4 - 6.00 kHz 5 - 16.0 kHz
BWS?	BWS nr1	Request the active IF bandwidth slot. Reset: BWS 4 Default: BWS 4 Example: BWS 1
CHA nrf		Select start channel for channel scan. Range: 00 to 98
CHA?	CHA nr1	Request currently selected channel for channel scan. Example: CHA 25 Default: CHA 0
CHB nrf		Select stop channel for channel scan. Range: 01 to 99
CHB?	CHB nr1	Request currently selected stop channel for channel scan. Example: CHB 26 Default: CHB 99
CHI nrf		Include channel when in channel scan. Range: 0 to 99
CHS nrf		Skip channel when in channel scan. Range: 0 to 99
CLM		Clear all memories.
CTL nrf		Set the device control mode. Range: 0 - 2 Where: 0 - Local 1 - Remote 2 - Remote w/Local Lockout
CTL?	CTL nr1	Request the device control mode. Default: CTL 0 Example: CTL 1

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
DET nrf		Set the detection mode. Range: 1 - 6 Where: 1 - AM 2 - FM 3 - CW 4 - USB 5 - LSB 6 - ISB 7 - SAM
DET?	DET nr1	Request the active detection mode. Reset: DET 1 Default: DET 1 Example: DET 4
ENA		Continue suspended scan command.
EXE nrf		Recall and execute specified memory channel. Range: 0 to 99
FRA nrf		Select start frequency for Frequency-to-Frequency (F1-to-F2) scan in MHz. Range: 0.000000 to 29.999999
FRA?	FRA nr2	Request current Frequency-to-Frequency (F1-to-F2) scan start frequency in MHz. Example: FRA 23.123456 Default: FRA 00.000000
FRB nrf		Select stop frequency for Frequency-to-Frequency (F1-to-F2) scan in MHz. Range: 0.000001 to 30.000000
FRB?	FRB nr2	Request current Frequency-to-Frequency (F1-to-F2) scan stop frequency in MHz. Example: FRB 27.123456 Default: FRB 30.000000

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
FRQ nrf		Set the tuned frequency in MHz (1-Hz steps). Range: 00.000000 to 30.000000
FRQ?	FRQ nr1	Request the tuned frequency. Reset: FRQ 20.000000 Default: FRQ 20.000000 Example: FRQ 12.345678
INC nrf		Select Frequency-to-Frequency (F1-to-F2) scan increment in kHz. Range: 0.001 to 25.000
INC?	INC nr2	Request current Frequency-to-Frequency (F1-to-F2) scan increment in kHz. Example: INC 20.000 Default: INC 25.000
LCK nrf nrf		Enter a lockout to be used in the (F1-to-F2) scan w/Lock mode. The lockout is specified as a center frequency only. The lockout width is ± half of the current IF bandwidth selection. Once stored, the lockout width remains the same, regardless of future IF bandwidth changes. The channel number assigned with this command remains constant as channels are added or deleted. This lockout data overwrites any data previously stored in the selected lockout channel. Field / Parameter / Range 1 / Channel number / 0 to 99 2 / Lockout center frequency / 0.000000 to 30.000000
MUT?	MUT nr1	Request the current mute status. Range: 0,1 Where: 0 = Audio not muted 1 = Audio muted

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
NFM nrf		Set the tunable notch filter mode. Range: 0,1 Where: 0 = OFF 1 = Relative (ON)
		Request the current tunable notch filter mode. Range: 0 to 4 Where: 0 = OFF 1 = Relative (ON) 2 = Not Used 4 = Disabled Note: A disabled response occurs when the notch filter relative setting is outside the specified limits of the selected bandwidth. Refer to **paragraph 4.4.11**.
NRF nrf		Set the tunable notch filter setting. Refer to **para 4.4.11** for a list of the maximum relative settings for each bandwidth. Range: -9999 to +9999 Hz
NRF?	NFR nr1	Request the current tunable notch filter setting. Reset: 0000 Default: 0000 Example: -6200

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
OPR nrf		Select operation mode. Range: 0, 1 Where: 0 = Manual 1 = scan (type of scan is dependent on current scan type (SCF) selection.)
OPR?	OPR nr1	Request current operation mode. Example: OPR 1 Default: OPR 0 Reset: OPR 0 Default: OPR 0
PBT nrf		Selected passband tuning offset frequency. Only effective in CW detection mode. Range: -2000 to +2000 Hz (10 Hz steps)
PBT?	PBT nr1	Request current passband tuning offset frequency in Hz. Example: PBT 1250 Reset: PBT 0 Default: PBT 0
RCL? nrf	RCL nr1,nr1, nr2,nr1,nr1,nr1, nr1,nr1	Recall selected memory channel parameters. Range: 0 to 99

Field	Parameter	Range
1	Memory channel number	0 to 99
2	Skip/include channel	0 = skip, 1 = include
3	Tuned frequency (FQR)	0.000000 to 30.000000 MHz
4	AGC mode (AGC)	0 to 3
5	Detection mode (DET)	1 to 7
6	Bandwidth number (BWN)	001 to 058 (see BWN command)
7	Squelch threshold (SQL)	0 to 135 -dBm, 136 = no squelch
8	RF input (RFP)	1 to 3
9	BFO Frequency (BFO)	-8000 to +8000 Hz
10	Remote Manual Gain Level (RFG)	000 - 127

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
REF?	REF nr1	Request the status of the external reference. Range: 0 - 4 Where: 0 - Internal 1 - 10 MHz External 2 - 5 MHz External 3 - 2 MHz External 4 - 1 MHz External Example: REF 3
RFG nrf RFG?	 RFG nr1	Set the remote manual gain level. Range: 000 -127 Request the remote manual gain level. Reset: RFG 000 Default: RFG 000 Example: RFG 123
RFP nrf RFP?	 RFP nr1	Select the RF input path. Range: 1 - 3 Where: 1 - Normal 2 - Attenuated 3 - Preamplified Request the selected RF input path. Reset: RFP 1 Default: RFP 1 Example: RFP 2
RLK? nrf	RLK nr1,nr2	Recall the selected lockout channel center frequency. When the lockout memory channel is vacant a frequency of 31.000000 MHz is returned. Range: 0 to 99 Example: 12, 27.123456
SCF nrf SCF?	 SCF nr1	Select desired scan type. Range: 1 to 3 Where: 1 = Channel scan 2 = F1-to-F2 3 = F1-to-F2 w/Lock Request the currently selected scan type. Example: SCF 1 Default: SCF 2

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
SCS?	SCS nr1	Request the current receiver scan status. Range: 0 to 3 Where: 0 = No scan 1 = Scan 2 = Scan dwell 3 = Scan paused
SDW nrf		Select the scan dwell time. Range: 0.5 to 20 seconds, 0 = infinite
SDW?	SDW nr1	Request currently selected scan dwell time. Example: SDW 2 Default: SDW 0.5
SGV?	SGV nr1,nr1	Request the signal strength value (in dBm) and squelch status value. Range: +20 to -135,0-1 Where: nr1,0 - squelch on nr1,1 - squelch off Reset: No Change Example: SGV -123,0
SLM?	SLM nr1	Request number of unused lockout channels available. Range: 0 to 100 Example: SLM 75 Reset: SLM 100
SPK nrf		Select speaker type. Range: 1 to 3 Where: 1 = USB 2 = Both 3 = LSB
SPK?	SPK nr1	Request currently selected speaker type. Example: SPK 2 Default: SPK 2

Table 4-1. Receiver Device Messages (Continued)

Command	Response	Description
SQL nrf		Set squelch level in negative dBm. Range: 0 to 135, 136 = squelch off
SQL?	SQL nr1	Request the squelch level setting in -dBm (136 = squelch off). Example: SQL 90 Reset: SQL 136
STO nrf	OPR nr1	Store front panel parameters to selected memory channel. Range: 0 to 99
STS?		Request current receiver parameters. Example: FRQ12.34567, AGC2, RFG123, BFO-1234, BLK10, BWS5, DET1, SLQ123, SPK1, RFP2, PBT1250

Field	Parameter	Range
1	Tuned Frequency (FRQ)	00.000000 to 30.000000 MHz
2	AGC Mode (AGC)	0 to 3
3	Remote Manual Gain Level (RFG)	000 - 127
4	BFO Frequency in kHz (BFO)	-8000 to +8000 Hz
5	Blanking Setting (BLK)	0 to 10
6	Bandwidth Slot (BWS)	1 to 5
7	Detection Mode (DET)	1 to 6
8	Squelch Threshold (SQL)	0 TO 135 -dBm 136 = no squelch
9	Speaker Type (SPK)	1 to 3
10	RF Input Path (RFP)	1 to 3
11	Passband Tuning Offset (PBT)	-2000 to +2000 Hz

Command	Response	Description
SUS		Suspend scan command. Suspends scan in the same manner as the front panel "pause" key pauses scan. Scan may be continued using the ENA command.
ULK nrf		Unlock selected lockout memory channel. Range: 0 to 99

4.4.1 SETTING THE TUNED FREQUENCY

The frequency command (FRQ) allows the tuned frequency of the WJ-8710A to be set over the 0 to 30 MHz range in 1-Hz increments. Receiver performance is degraded below 500 kHz.

4.4.2 DETECTION MODE SELECTION

The detection mode command (DET) determines how the signal is to be demodulated. The receiver supports AM, FM, CW, USB, LSB, ISB, and synchronous AM (SAM) detection modes. When the AM, SAM, FM, or CW detection modes are selected, any of the 66 available IF bandwidths may also be selected (**paragraph 4.4.4**). When selecting the USB or LSB detection mode, IF bandwidths from 900 Hz to 3.2 kHz are available for selection. When ISB is selected, IF bandwidths from 1.8 kHz to 3.2 kHz may be selected. Operation with these detection modes is further described below.

In all detection modes except for Independent Sideband (ISB), the demodulated audio, provided at each of the outputs contains the same signal information. After demodulation, the audio is routed to the LINE A, LINE B, SPEAKER, and DC AUDIO terminals of the rear panel terminal bus (TB1). The audio is also directed to the Left and Right channels of t he PHONES jack. In the ISB detection mode, both the upper and lower sidebands are simultaneously demodulated, and the audio signals are routed in a manner that permits both sidebands to be simultaneously monitored. The lower sideband audio is routed to the Left channel of the PHONES jack and to the LINE B terminals of TB1. The upper sideband audio is routed to the Right channel of the PHONES jack and to the LINE A terminals of TB1. The audio present at the DC AUDIO and SPEAKER terminals of TB1 are selectable, using the SPK command. Upper sideband audio (SPK 1), lower sideband audio (SPK 2), or both (SPK 3) may be selected, as desired.

Synchronous AM provides a detection mode that causes the receiver to lock on the carrier frequency in both frequency and phase. This mode improves the signal-to-noise ratio of the audio output. In addition, this mode provides greater immunity to signal loss due to fading.

The operation of the receiver in the Synchronous AM Mode can be enhanced by employing the Variable AGC feature (see **paragraph 4.4.3**). During instances of severe fading on AM signals, the synchronous AM demodulator attempts to synchronize itself to the distorted fading signal. Loss of signal lock may occur in some cases. By using the Variable AGC Threshold feature, the operator can reduce the gain applied to the faded signal such that it will be too weak to force the synchronous AM demodulator out of lock.

4.4.3 GAIN CONTROL MODE SELECTION

The receiver supports Automatic Gain Control (AGC) or manual attenuation operation for output level control. The operator may select Manual (AGC 0), Slow AGC (AGC 1), or Fast AGC (AGC 2) or Medium AGC (AGC 3) via the AGC command.

Three modes of AGC are available: fast, medium, or slow. The fast AGC mode provides a 15 millisecond attack time and a decay time constant variable (in 10 millisecond increments) from 10 milliseconds to 100 milliseconds. The medium AGC mode provides a 15 milliseconds attack time and a decay time constant variable (in 100 millisecond increments) from 100 milliseconds to 1000 milliseconds. The slow

AGC mode provides a 15 millisecond attack time and a decay time constant variable (in 500 millisecond increments) from 1 second to 5 seconds. Attack time and decay time are defined as the length of time that it takes for the audio outputs to return to a nominal level after a moderate instantaneous increase or decrease in the input signal level has occurred, respectively.

When in the Manual Gain Control mode (AGC 0), the RFG command sets the receiver gain. The manual gain range of 0 to 100 dB is divided into 127 increments.

4.4.3.1 <u>Variable AGC Function</u>

The Variable AGC Function provides an adjustable Automatic Gain Control threshold which allows the operator to force the receiver to stay in Manual Gain Control mode until a signal exceeding a preset AGC threshold level is detected. Once this strong signal is detected, the receiver forces itself into AGC to help prevent overload and distortion.

The Variable AGC feature is most useful in single sideband (SSB) or severely fading signals. With the feature disabled, and the SSB signal inactive, the RF noise floor is amplified to full scale of the audio channel. When feature is enabled, all signals below the specified threshold are unaffected by AGC and are not brought up to full scale.

The remote mnemonic that controls the AGC Threshold is AGT. The value of 1 turns the AGC Threshold on while a value of 0 turns the AGC Threshold off. The mnemonic RFG controls the AGC threshold remotely. Default value for AGC Threshold is “off”. See **Table 4-1** for a listing of Receiver Device Messages and associated parameters.

The operation of this feature can be verified by tuning to a SSB signal and slowly reducing the AGC threshold. While the strong SSB signal should sound the same, the noise between the SSB activity drops out since the receiver does not apply AGC.

4.4.4 IF BANDWIDTH SELECTION

The operator may select one of 66 available IF bandwidth filters when in the AM, FM, or CW detection modes. Selection of the desired IF bandwidth is accomplished by using the BWN command and entering the desired bandwidth number from 1 to 66 (see **Table 4-1**, BWN nrf). The receivers current IF bandwidth may be determined by using the BWN? query. A response from 1 to 66 (.056 to 16.00 kHz respectively) will be returned to the operator.

When the receiver is in the USB or LSB detection modes, only those IF bandwidths from 900 Hz to 3200 Hz are available for selection. When the receiver is in the ISB detection mode, only those bandwidths from 1800 Hz to 3200 Hz may be selected.

An alternate method of selecting an IF bandwidth is to use the BWC command (see **Table 4-1**). Using this command, the desired IF bandwidth size is entered in Hz. If the value entered is not a standard IF bandwidth (see **Table 1-1)**, the standard IF bandwidth that is greater in value and closest to the requested IF bandwidth will be selected. The BWC? query returns the IF bandwidth size in Hz.

The operator may also select one of five factory selected IF bandwidths by using the BWS command. Selectable IF bandwidths are 0.3, 1.0, 3.2, 6.0, and 16.0 kHz as selected by entering an nrf value of 1 to 5 respectively.

4.4.5 BFO FREQUENCY AND PASSBAND TUNING IN CW DETECTION MODE

For CW detection mode operations, the Beat Frequency Oscillator (BFO) and passband tuning capabilities are available. The BFO is adjustable over a ±8000 Hz range in 10-Hz steps. The BFO frequency can be applied to the received CW signal to alter its audio pitch as a detection aid. Passband tuning, which is an operator aid that facilitates simultaneous adjustments of tuned frequency and BFO, is adjustable over a ±2000 Hz range in 10-Hz steps. The BFO and passband frequencies are respectively selected by the BFO and PBT commands. The passband tuning function has the effect of shifting the IF bandwidth without changing the frequency of the audio output signals so that unwanted CW signals can be placed outside of the IF bandwidth while keeping the desired CW signals inside the bandwidth. This is especially useful in FSK demodulation applications for monitoring mark and space frequencies while other CW signals close in frequency are present.

4.4.6 FLEXIBLE SCANNING MODES

The WJ-8710A Digital HF Receiver provides a selection of three types of frequency scanning, The F1-to-F2 and F1-to-F2 with Lockouts provide a signal search capability within a contiguous segment of the specified portion of the RF spectrum. These two scan types are identical in operation, except that the F1-to-F2 with Lockouts permits undesired signal activity to be locked out, causing them to be ignored during the scan process. The third scan type is the Channel Scan. This scan type causes the receiver to step through a sequence of discrete frequencies programmed in memory. Prior to using any of the three scan types, the receiver memory must be programmed with the appropriate receiver parameters, and the desired scan type must be selected.

Once the receiver is properly programmed, the scan is initiated by first selecting the scan type (SCF 1, SCF 2, SCF 3) and then activating the scan operation (OPR 1). When activated, the scan begins, and continues until a signal exceeding the receiver squelch level is encountered. It dwells on the intercepted signal for the specified dwell time (SDW x.x), and then continues. The receiver may be commanded to continue scanning before the dwell time expires by sending a command to advance (ADV).

At any time the selected scan may be terminated (OPR 0), or temporarily suspended (SUS) to regain manual receiver control. If the scan is suspended (SUS), it is temporarily stopped and manual control is permitted. This permits changing of receiver parameters to optimize the signal, changing the receiver memory contents, storing parameters into channel memory, changing the dwell time, and storing lockout frequencies. If the scan is suspended with SUS command, it may be restarted with the ENA command. This causes the scan to restart at the point where it was suspended, without having to restart from the beginning. If the scan is terminated (OPR 0), it may only be restarted with the OPR 1 command, forcing it to restart at the beginning of the sequence.

4.4.6.1 **Channel Scan**

In channel scan, the receiver steps through a sequence of up to 100 user programmable memory channels. Receiver parameters stored in each channel include frequency, IF bandwidth, detection mode, gain control, and squelch control. The store (STO) command is used to store current receiver parameters to a selected memory channel. Prior to initiating the channel scan, the operator may select a specific range of channels to scan through. The CHA command is used to select the start channel. CHB is the stop channel selection command. The CHI and CHS commands are respectively used to include or skip a selected channel in the channel scan mode.

4.4.6.2 **Frequency-To-Frequency Scan (F1-to-F2)**

In the frequency-to-frequency scan (F1-to-F2) mode, the receiver monitors frequencies between programmed start and stop frequencies according to a selected step size between 1 Hz and 25 kHz. The INC command is used to select the increment step size. FRA and FRB commands are used to select start and stop frequencies in the frequency-to-frequency (F1-to-F2) scan mode.

4.4.6.3 **Frequency-To-Frequency Scan With Lockouts**

In addition to the LCK and ULK commands the commands used for this scan mode are the same as those described in **paragraph 4.4.6.2**. To enter a lockout frequency in the (F1-to-F2) scan with lock mode use the LCK command. The lockout is specified as a center frequency only. Refer to **Table 4-1** for the operating parameters of the LCK command. The ULK command is used to unlock a previously selected lockout memory channel.

4.4.7 THE SQUELCH LEVEL SELECTION

For both the fixed frequency tuning and flexible scanning modes of operation the squelch level is set by utilizing the SQL command. In addition to the off setting, the squelch range is from 0 to 135 expressed in negative dBm. Squelch off is 136.

The squelch can be adjusted to a level, depending on the strength of the signals being received. If a signal is received that is not quite strong enough for proper demodulation (i.e., its audio is unclear), the squelch level can be adjusted to block it from being applied to the audio outputs. The squelch should be set to a level where it does not block clear signals but does block noisy unwanted signals. Several adjustments may have to be made to find the optimum level. Only signals that have a power level above the set squelch level will be provided at the audio outputs.

Terminal 12 (MUTE) of TB1 on the rear panel is provided for the input of external squelch control in system setups. When an external mute is asserted (mute line pulled low), the receiver's squelch is activated. The receiver mute status may be requested in accordance with the MUT? query. Refer to **Table 4-1** for the MUT command parameters.

4.4.8 DWELL TIME SELECTION

The duration of time the receiver holds on a signal before resuming scan (dwell time) is operator-selectable between 0.5 and 20 seconds. An infinite dwell time can also be selected. The SDW command is used to set the dwell time. An infinite setting is obtained by the 0 (zero) setting.

4.4.9 RF INPUT PATH SELECTION

Depending on the receiver's tactical location, signals may be, in general, too powerful or not powerful enough for ideal reception. In these situations the input signals can be attenuated or amplified by selecting the appropriate RF input path for the input signals. The RFP command is used to make the selection, which can be normal, attenuated, or preamplified.

When preamplified is selected, all input signals are amplified by 10 dB. When attenuated is selected, all input signals are attenuated by 15 dB. When normal is selected, the input signals are unaffected at this point.

4.4.10 EXECUTE BUILT-IN TEST (BITE) FUNCTION

The Built-in Test (BITE) function is executed by the TST command. This command is a communication message, and is listed in **Table 4-2**. The command is used to verify equipment performance in accordance with the parameters shown in **Table 4-2**.

4.4.11 USING THE TUNABLE NOTCH FILTER

The Tunable Notch filter function is available, while in the AM, FM, USB, LSB, and ISB detection modes, to aid in the reduction of unwanted signals outside the passband. The Tunable Notch Filter can be enabled by using the NFM command. (see **Table 4-1**). The relative position of the Tunable Notch Filter can be adjusted, using the NFR command, to +/- 9999 Hz from the tuned carrier frequency. However, each available IF bandwidth filter has its own limits. **Table 4-2** list the available IF bandwidths and there respective tunable notch filter range.

Table 4-2. Tunable Notch Filter IF Bandwidth and Relative Setting from the Tuned Carrier

IF Bandwidth (kHz)	Maximum Relative Setting from the Tuned Carrier Frequency
.056, .063, .069, .075, .081, .088, .094, .100	+/-197 Hz
.113, .125, .138, .150, .163, .175, .188, .200	+/-195 Hz
.225, .250, .275, .300, .325, .350, .375, .400	+/-390 Hz
.450, .500, .550, .600, .650, .700, .750, .800	+/-781 Hz
.900, 1.000, 1.100, 1.200, 1.300, 1.400, 1.500, 1.600	+/-1562 Hz
1.800, 2.000, 2.200, 2.400, 2.600, 2.800, 3.000, 3.200	+/-3125 Hz
3.600, 4.000, 4.400, 4.800, 5.200, 5.600, 6.000, 6.400	+/-6250 Hz
7.200, 8.000, 8.800, 9.600, 10.400, 11.200, 12.000, 12.800, 14.400, 16.000	+/-12500 Hz

NOTE

The WJ-8710A software will allow tunable notch filter settings of +/-9999 Hz in all IF bandwidths. However, settings outside the specified maximum limit for each bandwidth will automatically disable the tunable notch filter.

The current notch filter setting is returned by using the NFR? query.

4.5 COMMUNICATION MESSAGES

Communication messages are always valid. These are commands which establish communications between the WJ-8710A and the controller. All WJ-8710A communication messages are listed in **Table 4-3**. Common communication messages are prefixed with an asterisk.

Table 4-3. Communication Messages

Command	Response	Description
CDE?	CDE nr1	Request the current Device-Dependent Error Register value. Example: CDE 00255 Range: 00000 - 65535 See **Table 4-7** for bit-mapped detail.
*CLS		Clears all communication status registers.
*ESE nrf		Set the Event Summary Enable Register. See discussion of the Event Summary Registers for bit-mapped details. Range: 0 - 255
*ESE?	*ESE nr1	Request the Event Summary Enable Register value. Reset: No change Default: *ESE 000 Example: *ESE 128
*ESR?	*ESR nr1	Request the Event Summary Status Register value. See **Table 4-4** for bit-mapped details. Example: *ESR 016 Range: 0 - 255 Bit 0 - OPC Operation Complete Bit 1 - Not Used Bit 2 - QYE Query Error Bit 3 - DDE Device-Dependent Error Bit 4 - EXE Execution Error Bit 5 - CME Command Error Bit 6 - Not Used Bit 7 - PON Power On
*IDN?	*IDN (see example)	Request receiver identity. The fields provide information in the following order: model number, space reserved for future expansion, and software version number. Example: *IDN WJ8710A,0,1.40
LDE?	LDE nr1	Request the latched Device-Dependent Error Register value. Example: LDE 00255 Range: 00000 - 65535 See **Table 4-7** for bit-mapped detail.

Table 4-3. Communication Messages (Continued)

Command	Response	Description
*LRN?	*LRN nr2,nr1, nr1,nr1,nr1,nr1, nr1,nr1,	Request current WJ-8710A operating parameters. The data returned for this query is field dependent.

Field	Parameter	Range
1	Tuned Frequency (FRQ)	00.000000 to 30.000000 MHz
2	AGC Mode (AGC)	0 to 3
3	Detection Mode (DET)	1 to 7
4	Bandwidth slot (BWS)	1 to 5
5	Squelch threshold (SQL)	0 to 135 -dBm, 136 = no squelch
6	RF input (RFP)	1 to 3
7	BFO frequency (BFO)	-8000 to +8000 Hz (in 10 Hz steps)
8	Blanking (BLK)	0 to 10
9	Speaker (SPK)	1 to 3

Command	Response	Description
*OPC		Operation complete switch. When this command is sent with a data string, the OPC bit in the Event Summary Status Register will be set upon completion of the operation(s) in the input buffer. An SRQ may be generated with corresponding bit enabled.
*OPC?	*OPC 1	An *OPC 1 string will be loaded into the output buffer (returned at the completion of the operation in the input buffer).
*OPT?	*OPT nr1,nr1	Request the options currently installed in the receiver. The returned response is a bit-mapped value of two 8 bit bytes. Range: 0 - 255, 0 - 255 Example: *OPT 016 1st nr1 bit-mapped response: Bit 0 - Preselector Option Bit 1 - Extended Bandwidths Bit 2 - Tuned Carrier Bit 3 - Variable Line Audio Bit 4 - Tunable Notch Filter Bit 5 - AGC/Detection Mode Matching Bit 6 - Zero Digit tuning Bit 7 - Synchronous AM 2nd nr1 bit-mapped response: Bit 0 - AGC Enhancements Bit 1 to Bit 7 Reserved for future expansion

Table 4-3. Communication Messages (Continued)

Command	Response	Description
*RSE nrf		This command allows writing to a register that enables interrupts to be passed from the RSR register to the *STB register via its RSB bit. BIT FUNCTION 0 Enable PRS, signal exceeded COR event to set the RSB bit. 1-3 Not Used 4 Enable ESN, end of single scan event to set the RSB bit. 5-7 Not used.
*RSE?	*RSE nr1	Request the contents of the Receiver Status Enable Register. Reset: no change Default: *RSE 000 Example: *RSE 016
*RSR?	*RSR nr1	Read the Receiver Status Register. The information included in this register is latched. It is cleared by the *CLS command or a read of the register. The information in the register discloses the reason for the RSB bit to be set in the Status Byte Register. BIT FUNCTION 0 PRS, signal exceeded COR threshold. This is an edge triggered event on the action of a signal going from below COR threshold to above COR threshold. 1-3 Not used. 4 ESN, end of single scan. This bit indicates the end of scan has been encountered. This bit is only set while in a scan mode. (F1→F2, F1→F2 w/Lock, Channel) 5-7 Not used
*RST		For all device parameters to their reset condition.

Table 4-3. Communication Messages (Continued)

Command	Response	Description
*SRE nrf		Set the Service Request Enable Register. See discussion of the Status Byte Registers for bit-mapped details. Range: 0 - 255
*SRE?	*SRE nr1	Request the Service Request Enable Register value. Reset: No Change Default: *SRE 000 Example: *SRE 032
*STB?	*STB nr1	Request the Status Byte Register value. See **Table 4-3** for bit-mapped details. Range: 0 - 255 Example: *STB 064 Bit 0 - RSB Bit 1 - Not Used Bit 2 - Not Used Bit 3 - Not Used Bit 4 - Not Used Bit 5 - ESB Event Summary Bit Bit 6 - RQS Request Service Bit 7 - Not Used
*TST?	*TST nr1	Execute built-in-test (BITE) and report outcome. The response is a bit-mapped value of 16 bits, representing the success or failure of each test. Any failed test will set the associated bit as listed below. Range: 0 - 65535 Example: *TST 00000 Bit Failure 0 Control to DSP transmit pipeline not empty. 1 Control to DSP download unsuccessful. 2 DSP EPROM download unsuccessful. 3 Control command no acknowledged. 4 No DSP response to control request. 5 DSP memory check did not complete. 6 DSP EPROM failure. 7 DSP SRAM failure. 8 RF test failed. 9 Control A/D failure. 10 Non-SSB audio failure. 11 USB audio failure. 12 USB audio in LSB path failure. 13 LSB audio failure. 14 LSB audio in USB path failure. 15 DSP A/D failure.

4.6 RECEIVER STATUS SUMMARY

Figure 4-2 illustrates the architecture of the receiver's status registers. It is composed of six eight-bit registers and one 16-bit register, whose logic gating allows the programmer great flexibility in remote operations. The eight bit registers can be split into three pairs. Each pair consists of a status register and an enable register.

One pair is composed of the Event Summary Status Register (whose functions are summarized in **paragraph 4.6.2**) and the Event Summary Status Enable Register. Each bit in the Event Summary Status Register is logically ANDed to a bit in the Event Summary Status Enable Register. The ANDed combination of these two registers are logically ORed to set the Event Summary Status Bit (ESB) of the Status Byte Register. The Device-Dependent Error Bit (DDE) of the Event Summary Status Register is the ORed combination of the 16-bit Device-Dependent Error Register (see **paragraph 4.6.4**).

The second pair is composed of the Status Byte Register and the Service Request Enable Register. The receiver uses only three bits of the Status Byte Register as described in **Table 4-4**. The ANDed combination of bits 0 and 5 of the Status Byte Register and the Service Request Enable Register are logically ORed to determine the setting of bit six (RQS) of the Status Byte Register. If the RQS bit is set high, a service request is asserted.

Table 4-4. Status Byte Register, Bit Evaluation

Bit Number	Mnemonic	Description
0	RSB	**Receiver Status Bit -** This bit, when set, indicates that an event has caused a bit or bits in the Receiver Status Register to be set (see **paragraph 4.6.3**). This bit is cleared by *CLS or by reading the contents of the Receiver Status Register using the RSR? query.
1-4	Not Used	
5	ESB	**Event Summary Bit -** This bit, when set, indicates that the Event Summary Status Register has set SRQ. By reading the Event Summary Status Register via the *ESR? mnemonic, the host controller may identify what status event has caused the SRQ. This bit is cleared by sending, *CLS or reading the contents of the Event Status Register.
6	RQS	**Request Service Bit -** This bit, when set, indicates that the unit has asserted SRQ.
7	Not Used	

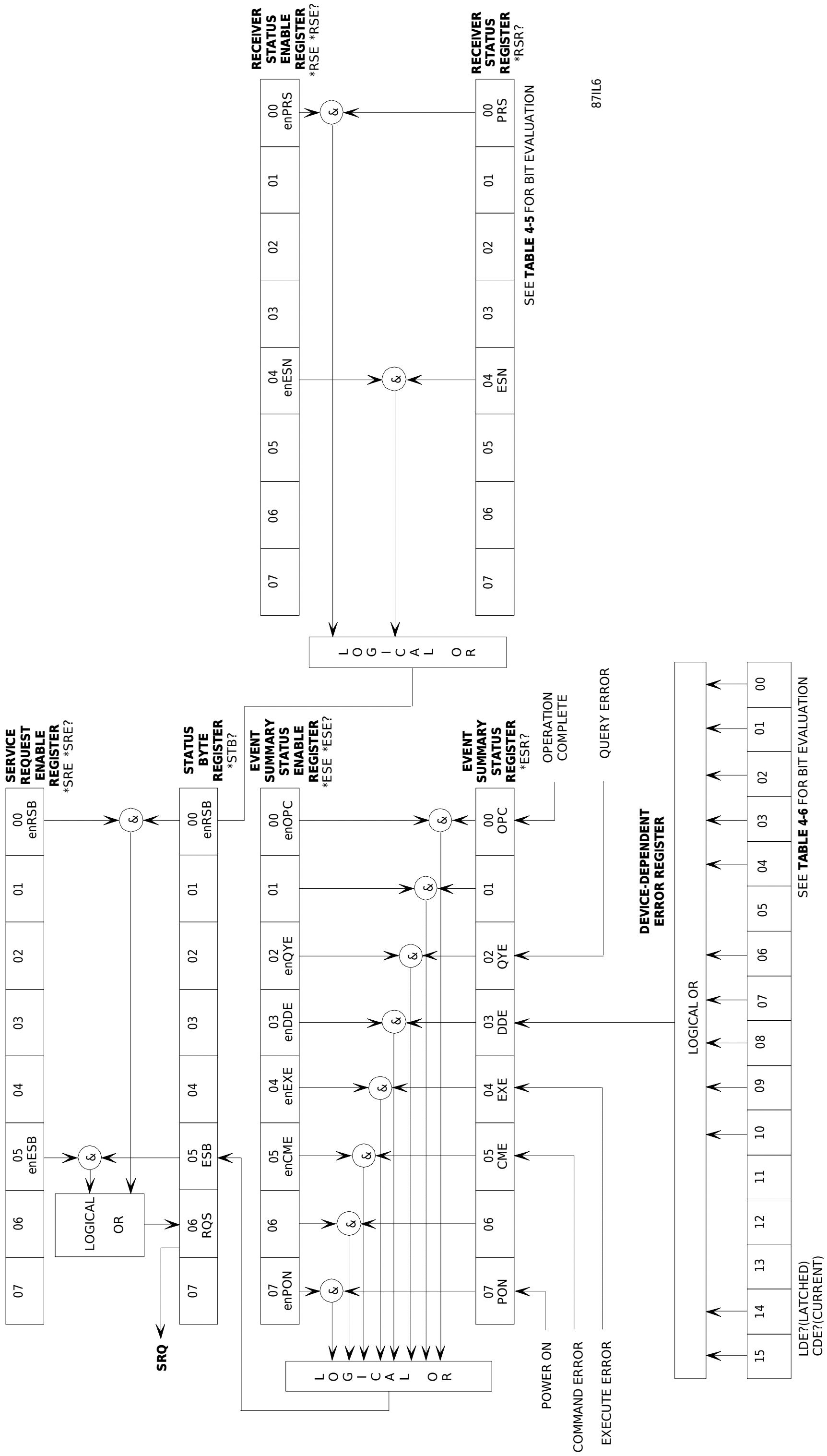

Figure 4-2. Receiver Status Data Structure

NOTES

4.6.1 STATUS BYTES

The following information discusses the operation of the SRQ interrupt and the "*STB?" query. The operation of these is very similar. The SRQ interrupt allows the controller to establish which event has caused the receiver to set the SRQ. The "*STB?" query response includes similar information as detailed below.

SRQ - This is a one byte control character (ESC) indicating a service request. When SRQ is generated, it is immediately followed by the output of the Status Byte Register if enabled. This clears the SRQ and the Status Byte Register. The evaluation of each bit in this status byte is in **Table 4-4**.

***STB? Query -** The Status Byte Register can also be read using the *STB? query. Sending *STB? does not clear the SRQ status line or the Status Byte Register.

The Service Request Enable Register allows status bits to generate service requests. Setting a status bit will set service request if and only if the corresponding enable bit is set. Service Request Enable Register bit six is ignored and reported as zero. This bit would correspond to the RQS bit of the Status Byte Register which triggers service request.

4.6.2 EVENT SUMMARY STATUS REGISTER

The following discussion covers the Event Summary Status Register and the *ESR? query. See **Table 4-5** for the Event Summary Status Register bit numbers, mnemonics and descriptions.

The Event Summary Status Register is read destructively by the *ESR? query, which clears the register. The *CLS command also clears the register. The power on sequence automatically sets the Power On bit and initially resets the remaining bits.

The Event Summary Status Enable Register allows the event flags of the Event Summary Status Register to be reflected in the Event Summary Bit (ESB) of the Status Byte. The setting of an event status flag sets ESB high <u>only</u> if the corresponding bit in the Event Summary Status Enable Register is set high. The Event Summary Status Enable Register is written to with the *ESE command. The data following the mnemonic is the decimal equivalent of a binary number representing the register bits. The *ESE? query loads the output buffer with a decimal number, which can be converted to binary to determine the setting of the Event Summary Status Enable Register.

Table 4-5. Event Summary Status Register, Bit Evaluation

Bit Number	Mnemonic	Description
0	OPC	**Operation Complete -** This bit is set on completion of operation that has been designated by the *OPC command.
2	QYE	**Query Error -** Set on an attempt to read data from the output buffer with no data stored or pending, or the output buffer is dumped for any cause except device clear, such as an overflow.
3	DDE	**Device-Dependent Error -** Set when a hardware error occurs within the receiver.
4	EXE	**Execution Error -** Set when an out of range data element follows a known message header or when a valid message count not be executed due to some device condition.
5	CME	**Command Error -** Set when an unrecognized message header has bee received.
7	PON	**Power On -** Set during the power-up sequence. Also set when a Device or Select Device Clear is received.

4.6.3 RECEIVER STATUS REGISTER

The Receiver Status Register allows for interrupts to be generated when particular operational events occur. The information in this register discloses the reason for the RSB bit to be set in the Status Byte Register. The *RSR? query reads the latched contents of this register and clears it. It is also cleared by *CLS. See **Table 4-6** for the bit evaluation of the Receiver Status Register.

Table 4-6. Receiver Status Register, Bit Evaluation

Bit	Decimal Value	Function
0	1	PRS, signal exceeded COR threshold. This is an edge triggered event on the action of a signal going from below COR threshold to above COR threshold.
1	2	Not used
2	4	Not used
3	8	Not used
4	16	ESN, end of scan. This bit indicates the end of scan has been encountered. This bit is only set while in a scan mode (F1→F2, F1→F2 w/Lock, or Channel).
5	32	Not used
6	64	Not used
7	128	Not used

4.6.4 DEVICE-DEPENDENT ERROR REGISTER

The contents of the Device-Dependent Error Register can be read to determine what event has caused the DDE bit in the Event Status Register to be set. The CDE? and LDE? queries are used as further discussed below.

The LDE? query request the latched error status. The response is a bit-mapped 16-bit word indicating the error conditions that have occurred since the last read of the register. Reading the contents of the register also clears it. See **Table 4-7** for a bit evaluation of the Device-Dependent Error Register.

The CDE? query request the current device error. The response to this query is also a bit-mapped 16-bit word. Reading this register has no effect on it.

Table 4-7. Device-Dependent Error Register, Bit Evaluation

Bit	Decimal Value	Mnemonic	Description
0	1	DSP ERR 1	Control to DSP transmit pipeline not empty.
1	2	DSP ERR 2	Control to DSP download unsuccessful.
2	4	DSP ERR 3	DSP EPROM download unsuccessful.
3	8	DSP ERR 4	Control command not acknowledged by DSP.
4	16	DSP ERR 5	No DSP response to Control request.
5	32	Not Used	
6	64	PS ERR 1	-12 Volt Supply Low.
7	128	PS ERR 2	+12 Volt Supply Low.
8	256	BATT ERR	Battery Voltage Low.
9	512	LO ERR	Local Oscillator Unlocked.
10	1024	REF ERR	Unknown External Reference.
11	2048	RAM FAIL	Control Processor RAM Failure.
12	4096	CHKSUM	EPROM Checksum Error.
13	8192	PRESEL OVRLD	Preselector Overload (when the WJ-8711/PRE option is installed).
14	16384	Not used	
15	32768	Not used	

4.7 MESSAGE PROCESSING

When the WJ-8710A receives a remote message, it stores it in an input buffer circuit until it receives a valid message terminator (LF). When the terminator is received, the message is parsed and executed.

The format of the received message is checked for validity as the message is parsed and executed. If the message fails to meet the restrictions of the command message format, it is ignored.

4.8 RS-232 COMMUNICATIONS PROTOCOL

The communications protocol for the WJ-8710A implements both ENQ/ACK (ENQuire/ACKnowledge) and XON/XOFF (ctl Q/ctl S) software handshakes. The ENQ/ACK format, typically referred to as "transmitter protocol", allows the operator to send an "ENQ" character to the WJ-8710A when an acknowledge is required. The receiver then responds with the ACK/NAK (ACKnowledge/Not AcKnowledge) character indicating the validity of the data received in the input buffer and the fact the unit has completed all current data through to the last received terminator. The XON/XOFF format supports both transmit and receive communications. This format, typically referred to as "receiver protocol", allows transmission based on the availability of buffer space (refer to **paragraph 4.8.3**).

Table 4-8 lists the supported communications control commands for RS-232 remote operation. The following paragraphs provide more details on the ENQ/ACK and XON/XOFF protocol, and buffer control.

Table 4-8. Supported RS-232C Communications Control Commands

HEX	ASCII	Receive	Transmit	Function
11	DC	x	x	XON, allow data transmission
13	DC3	x	x	XOFF, disallow data transmission
05	ENQ	x		Enquire, request acknowledge
06	ACK		x	Acknowledged, data received
15	NAK		x	Not acknowledged, data communications error
0A	LF	x	x	Line feed, start processing input buffer
0D	CR	x	x	Carriage return, no action

4.8.1 XON/XOFF PROTOCOL

The XON/XOFF communications protocol is always active in the WJ-8710A. In the event the buffer has room for less than 16 additional characters the unit will output an XOFF character. When the unit empties its input buffer, it issues an XON character. The user must stop sending data within 15 characters after receiving the XOFF character. On each character that is received while the buffer is full, the unit issues an XOFF character. The user may start sending data to the unit after receiving the XON character.

The WJ-8710A responds to the XON and XOFF commands while outputting data to the user. If the unit receives an XOFF while sending, it stops transmitting within two characters. The unit will not transmit any further data until an XON is received. The WJ-8710A assumes the XON condition at power-up.

4.8.2 ENQ/ACK PROTOCOL

When the ENQ character is sent to the WJ-8710A, it responds to a valid message with an ACK, or to an invalid message with a NAK. An invalid message is indicated on a data communications error such as framing, noise, or overrun. The transmission of a NAK indicates that one or more of the bytes received after the last ENQ has a communications error. The ACK/NAK response is only sent after the unit has completed processing any previous messages in the input buffer and has output any response necessary. See **Table 4-6**.

WJ-8710A internally maintains a communications error flag. The flag is cleared on power-up or the transmission of a NAK. The flag is set when a byte is received with a data communications error. Upon receiving an ENQ character, the unit responds with an ACK/NAK based on the condition of the communications flag, after any pending input and output operations are complete.

4.8.3 BUFFER HANDLING

4.8.3.1 Input Buffer

The input buffer is handled in circular fashion allowing simultaneous inputting and processing of data. The input buffer accepts up to 1024 bytes before overflowing. As data in the buffer is being processed, additional inputs can be accepted by the unit. Upon receiving a terminator character, the WJ-8710A processes any previous messages in the buffer. When the buffer has less than 16 unused bytes, XOFF is generated. XON is generated when the buffer has less than 16 bytes remaining to be processed.

The input buffer processing starts on the receipt of a terminator (LF). If the communications error flag is set, the buffer contents from the end of the last processed message thru the message terminator is discarded. In the event the buffer is overrun, its contents are discarded. Messages such as XON, XOFF, and ENQ have immediate actions. These commands are processed on receipt and are not buffered. All other incoming data is buffered and processed in the order in which it was received.

4.8.3.2 Output Buffer

The output buffer is handled in circular fashion allowing simultaneous additions and outputting. The transmission of XON/XOFF has priority over data in the output buffer that is awaiting transmission. The ACK/NAK transmission are buffered operations so they stay in time synchronization with query operations. The output buffer holds up to 1024 bytes of data.

SECTION V

CSMA REMOTE CONTROL

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SECTION V

CSMA REMOTE CONTROL

5.1 INTRODUCTION

This section provides information for controlling the WJ-8710A Digital HF Receiver via a CSMA/CD interface. The Carrier Sense Multiple Access with Collision Detection interface (hereafter referred to as a CSMA interface) is a media access method that allows up to 63 devices to be addressed on a common bus interface. To transmit, a controller waits for a quiet period on the medium (that is, no other device is transmitting) and then sends a message in byte-serial form. The controller waits for responses to queries or for Acknowledge (ACK) or Not Acknowledge (NAK) messages before proceeding with the next command or query. Message collisions can occur on a CSMA interface and are more likely when the system hardware limitations are pushed beyond recommendations. The CSMA interface detects these collisions and tries to overcome resulting communications loss. See **paragraph 5.9** for a full description of the behavior of the interface during collision detection.

5.2 CONTROLLING MULTIPLE RECEIVERS VIA THE CSMA INTERFACE

System hardware configuration will dictate the limitations regarding the number of units physically capable of being controlled. For best results, Signia-IDT, Inc. recommends the following:

Limit the number of bus controllers to one;

Send one command line at a time;

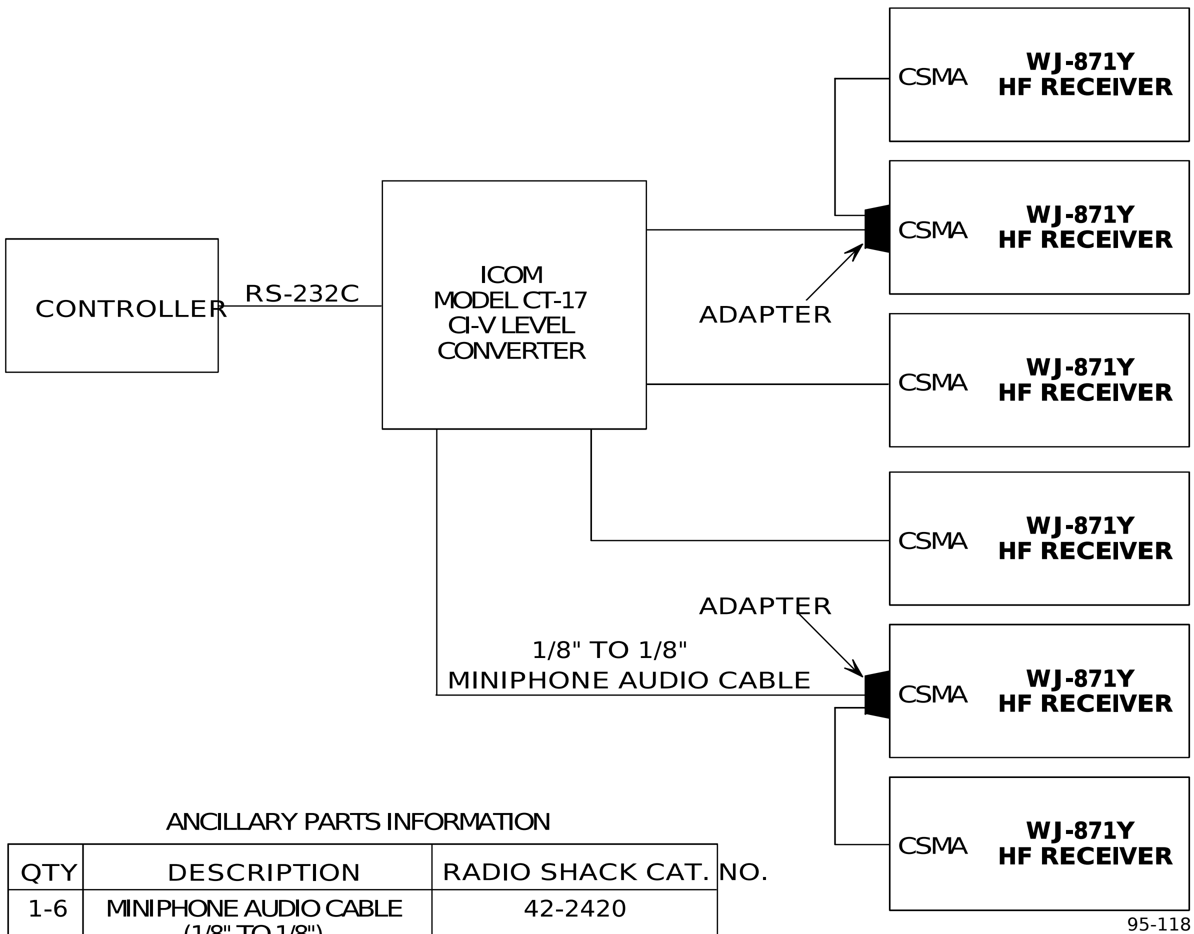
Wait for a response to a query or an Acknowledgment (ACK) or non-Acknowledgment (NAK) of a command before proceeding with the next step;

Do not string commands and queries together on a single command line;

Avoid commands that do not task the receiver to return an ACK/NAK or other response;

Limit the number of devices on the bus;

Signia-IDT, Inc. recommends the use of a ICOM CT-17 CI-V Level Converter to control multiple receivers via their CSMA interfaces when the controller is a PC equipped with an RS-232 serial interface. Refer to **Figure 5-1**. Signia-IDT, Inc. has successfully driven up to six receivers by adding audio adapter jacks to extend the four outputs provided by the ICOM CT-17.



ANCILLARY PARTS INFORMATION

QTY	DESCRIPTION	RADIO SHACK CAT. NO.
1-6	MINIPHONE AUDIO CABLE (1/8" TO 1/8")	42-2420
0-2	DUAL MINIPHONE ADAPTER	274-310

Figure 5-1. Recommended Controller Setup

5.3 SETTING UP THE RECEIVER FOR REMOTE CSMA INTERFACE

Switch 4 of DIP switch A2S1 is set to the on (down) position to activate the CSMA remote control. Baud rate is also selected using switches 1, 2 and 3 of A2S1. The CSMA address is selected with switch A2S2. The tuned frequency format can be set to four bytes or five bytes with A2S2. It is recommended that the WJ-8710A be set to four bytes. Refer to **paragraph 2.2.4** for details on configuring DIP switches A2S1 and A2S2.

The following receiver parameters are controllable via the CSMA interface:

- tuned frequency,
- BFO frequency,
- detection mode,
- IF bandwidth,
- gain mode,
- manual gain, and
- RF input path.

This section of the manual contains information necessary to enable an operator to control and monitor the above receiver parameters from an external controller on the CSMA interface. Details on how to properly format and transmit remote messages and how to read responses from the receiver are provided.

5.4 ELECTRICAL REQUIREMENTS OF THE INTERFACE

The CSMA interface is implemented on a mini-phones jack (A2J2) located on the rear panel, labeled CSMA. The sleeve of this connector is connected to chassis to ground. The center conductor carries the bidirectional serial data. For proper communications on the interface, a logic HIGH input should be +2 volts minimum. A logic LOW input should be +0.7 volts maximum. These logic levels are compatible with standard TTL and 5 volt CMOS logic drivers. With appropriate level shifting circuitry, any computer equipped with an RS-232C interface port can be used to control the WJ-8710A via its CSMA interface. To reduce the adverse effects of reflections on the line, resistive terminations are recommended on each end of the interface cable. The DC bias introduced by the terminations must exceed +2.5 volts. A single resistor at each end of the cable, connected between a clean +3 to +5 volt supply and the data line, is usually adequate. Be sure that all devices connected to the CSMA interface have sufficient drive capability to transmit data onto the line. The WJ-8710A CSMA port can sink up to 100 mA at a logic low output voltage of +0.7 volts.

5.5 SERIAL DATA TRANSMISSIONS

Data in serial transmissions is read from the transition of the change in state (i.e., high to low, or low to high). Data transmitters and data receivers connected on the interface exchange serial information using the NonReturn to Zero (NRZ) format. This means, in baseband transmissions, if a logic "1" is continuously sent, the signal does not return to logic "0" until a logic "0" is sent. The composition of one byte of data is shown in **Figure 5-2** with an example of the NRZ format.

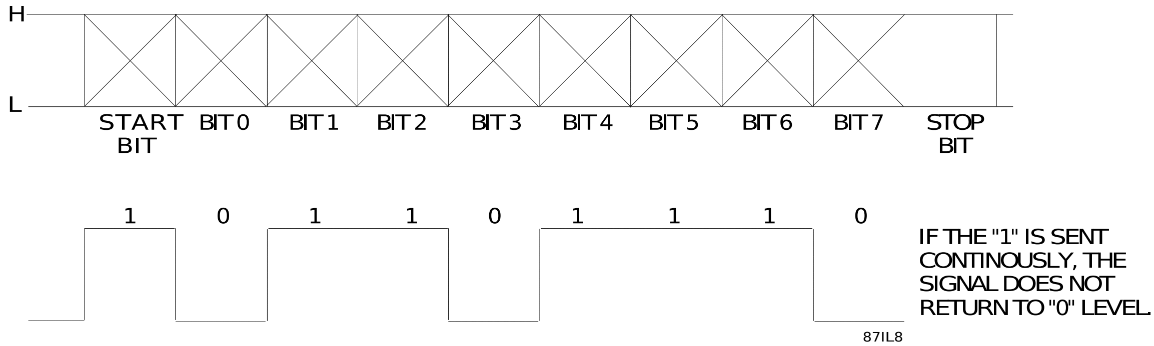


Figure 5-2. Composition of One byte of Serial Data

5.6 COMMAND MESSAGE FORMATTING

The typical message format of a command packet used with this interface is provided in **Figure 5-3**. Each block in the packet contains one byte of data. As shown in the figure the packet consists of two preamble bytes, a receiving station address byte, a transmitting station address byte, a control code byte, a varying number of data bytes, and an end of message byte. All information contained in bytes is expressed in hexadecimal except for the data bytes which may vary in number and are expressed in packed binary coded decimal (BCD).

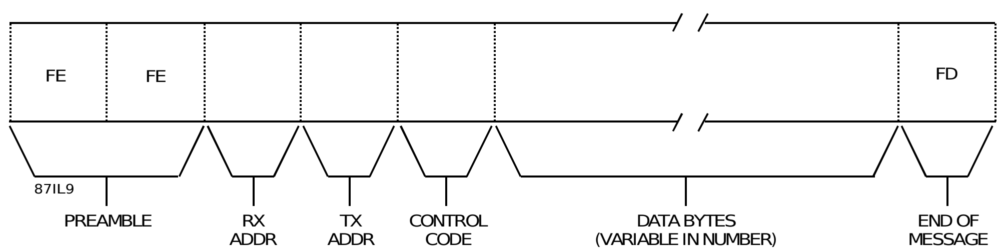


Figure 5-3. Format of Typical Command Message Packet

The preamble [FE|FE] identifies the start of a message. The receiver address (RX ADDR) identifies the address of the unit that is to receive the data. The WJ-8710A's address setting should be entered at this location. The transmitting station address identifies the address of the controller sending the data. The control code represents the WJ-8710A function that is to be controlled. This code should always be sent in hexadecimal format. The variable length data field contains data that accompanies the control code to set certain values of the function. This data field can contain any number of bytes required to send the data. Data in these bytes should always be sent in binary coded decimal format. The end of message byte [FD] identifies the end of the message being transmitted.

5.7 CONTROL CODES

Table 5-1 lists the control codes used for controlling the receiver functions. The control codes listed are shown in hexadecimal format. A description is provided for each control code. Data accompanying control codes is shown in decimal format unless otherwise noted.

Certain control codes require that an acknowledgment be sent to the host controller indicating that their format was valid and accepted. For all control codes that require an acknowledgment, hexadecimal FB (ACK) is returned to the controller when the control code is recognized and the accompanying data is within the specified range. Hexadecimal FA (NAK) is returned to the controller if either the control code sent is unsupported or if the accompanying data sent with a supported control code is out of range. Note that unless otherwise indicated the control code requires an acknowledge. **Figure 5-4** shows the format of ACK and NAK responses.

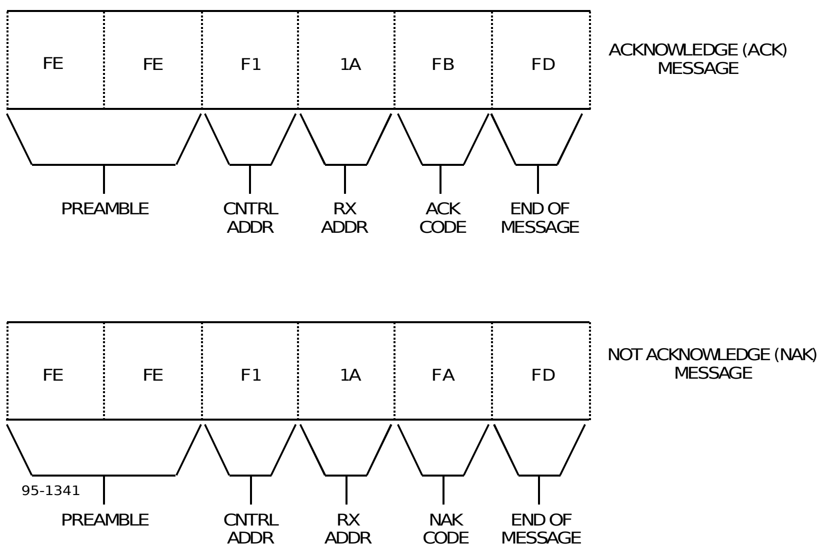


Figure 5-4. Format of ACK and NAK Messages

Table 5-1. CSMA Control Code

Control Code (Hexadecimal)	Description (Decimal)
00	Set the tuned frequency in Hz without acknowledge. Range: 00000000 - 30000000
01	Set the detection mode (first data byte) and IF bandwidth (second data byte) without acknowledge. Where: 00 - LSB 01 - USB 02 - AM 03 - CW 05 - FM 06 - ISB 07 - SAM And: 01 - 0.30 kHz 02 - 1.00 kHz 03 - 3.20 kHz 04 - 6.00 kHz 05 - 16.0 kHz
02	Request the tuned frequency range.
03	Request the tuned frequency.
04	Request the selected detection mode and IF bandwidth.
05	Set the tuned frequency in Hz with acknowledge. Range: 00000000 - 30000000
06	Set the detection mode (first data byte) and IF bandwidth (second data byte) with acknowledge. Where: 00 - LSB 01 - USB 02 - AM 03 - CW 05 - FM 06 - ISB 07 - SAM And: 01 - 0.30 kHz 02 - 1.00 kHz 03 - 3.20 kHz 04 - 6.00 kHz 05 - 16.0 kHz Note: The ISB, LSB, or USB detection modes will force the unit into the 3.20 kHz IF BW.

Table 5-1. CSMA Control Code (Continued)

Control Code (Hexadecimal)	Description (Decimal)
30	Request active gain control mode.
31	Select gain control mode with acknowledge. Where: 00 - Manual 01 - Slow AGC 02 - Fast AGC 03 - Medium AGC
32	Request the remote manual gain level.
33	Set the remote manual gain level with acknowledge. Range: 0000 - 0127
34	Request current BFO frequency.
35	Set BFO frequency in Hz (in 10 Hz steps) with acknowledge. The third data byte contains the sign in hexadecimal (0E for negative and 0A for positive). Range: -8000 to +7999 Where: +0000 = BFO Off
36	Request the device control mode.
37	Set the device control mode with acknowledge. Range: 00 - 02 Where: 00 - Local (Not Used) 01 - Remote 02 - Remote w/Local Lockout (Not Used)
38	Request the selected RF input path.
39	Select the RF input path with acknowledge. Range: 01 - 03 Where: 01 - Normal 02 - Attenuated 03 - Preamplified

5.8 DETAILS ON COMMAND AND RESPONSE FORMATS

The following paragraphs provide examples of command and response formats for each control code listed in **Table 5-1**. In the examples, the receiver's address is assumed to be hexadecimal 1A (decimal 26) and the controller's address is assumed to be hexadecimal F1 (decimal 241). It is also assumed that the tuned frequency format is set to four bytes with A2S2 (**paragraph 2.2.4**).

5.8.1 TUNED FREQUENCY COMMAND WITHOUT ACKNOWLEDGE [00]

Figure 5-5 shows an example of the typical format for setting the receiver's tuned frequency using control code [00]. This control code provides the same result as the [05] code described in **paragraph 5.8.2** except it does not require an acknowledgment. For this reason it is not the preferred method to tune a WJ-8710A.

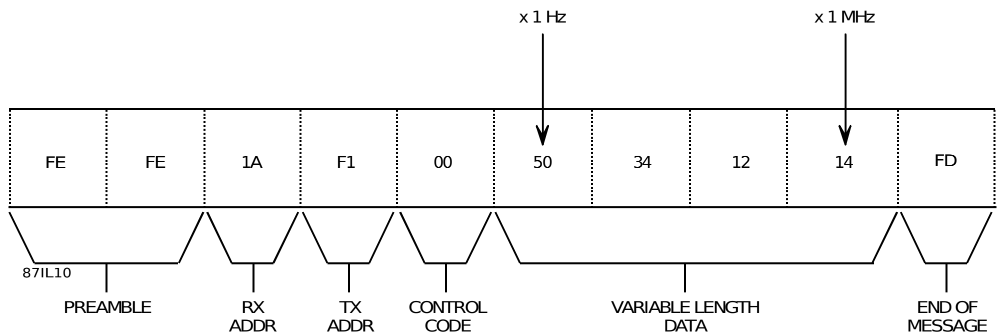


Figure 5-5. Tuned Frequency Command Format without Acknowledge

The frequency can be set to any value from 0 to 30.0 MHz at a resolution of 1 Hz. The frequency entered in the example is 14.123450 MHz. The first byte of the frequency data contains Hz data. The last (fourth) byte contains MHz data. If less than four bytes accompany the frequency control code, only those lower resolution value are changed and the higher resolution values (bytes not sent) remain the same.

5.8.2 TUNED FREQUENCY COMMAND WITH ACKNOWLEDGE [05]

Figure 5-6 shows an example of the typical format for setting the receiver's tuned frequency using control code [05]. This control code provides the same result as the [00] code described in **paragraph 5.8.1** except it requires an acknowledgment to the controller. For this reason it is the preferred method to tune a WJ-8710A.

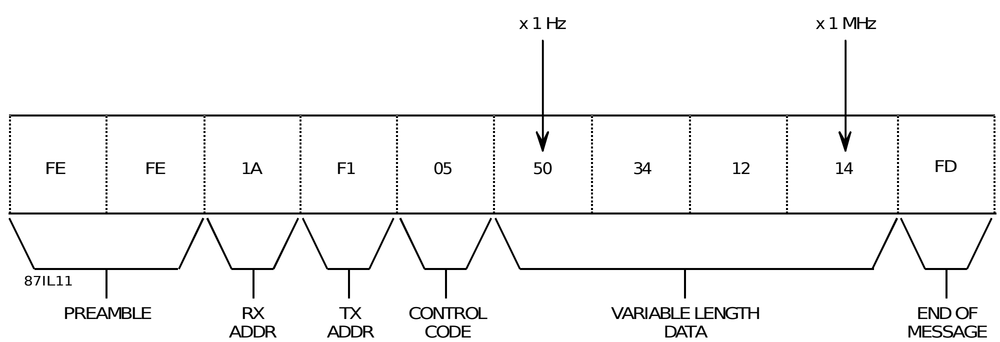


Figure 5-6. Tuned Frequency Command Format with Acknowledge

The frequency can be set to any value from 0 to 30.0 MHz at a resolution of 1 Hz. The frequency entered in the example is 14.123450 MHz. The first byte of the frequency data contains Hz data. The last (fourth) byte contains MHz data. If less than four bytes accompany the frequency control code, only those lower resolution value are changed and the higher resolution values (bytes not sent) remain the same.

5.8.3 RESPONSE TO TUNED FREQUENCY REQUESTS [03]

Figure 5-7 shows an example of the typical response format when requesting the tuned frequency with control code [03].

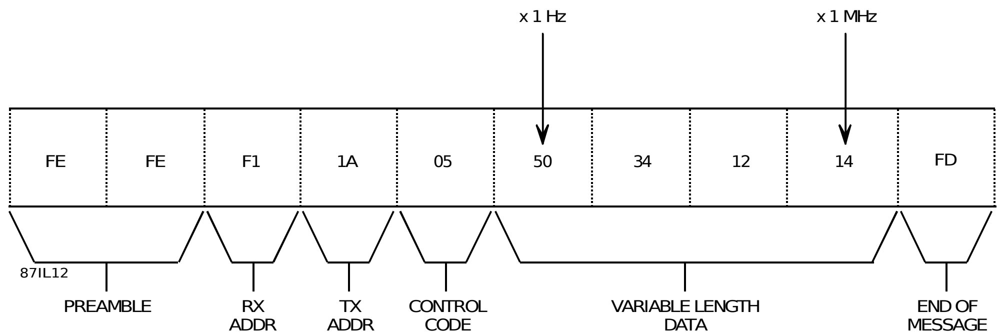


Figure 5-7. Tuned Frequency Request Response Format

The response in the example is 14.123450 MHz. The first byte of the frequency data contains Hz data. The last (fourth) byte contains MHz data. The response always contains all four bytes of the frequency data.

5.8.4 RESPONSE TO TUNED FREQUENCY RANGE REQUESTS [02]

Figure 5-8 shows an example of the typical response format when requesting the tuned frequency range of the receiver with control code [02].

In the response the upper frequency limit and the lower frequency limit are separated with 2D hex. The first byte of the frequency data in each limit of the response contains Hz data. The last (fourth) byte contains MHz data. The upper frequency limit response always contains data representing 30.000000 MHz [00|00|00|30]. The lower frequency limit response always contains data representing 0 Hz [00|00|00|00].

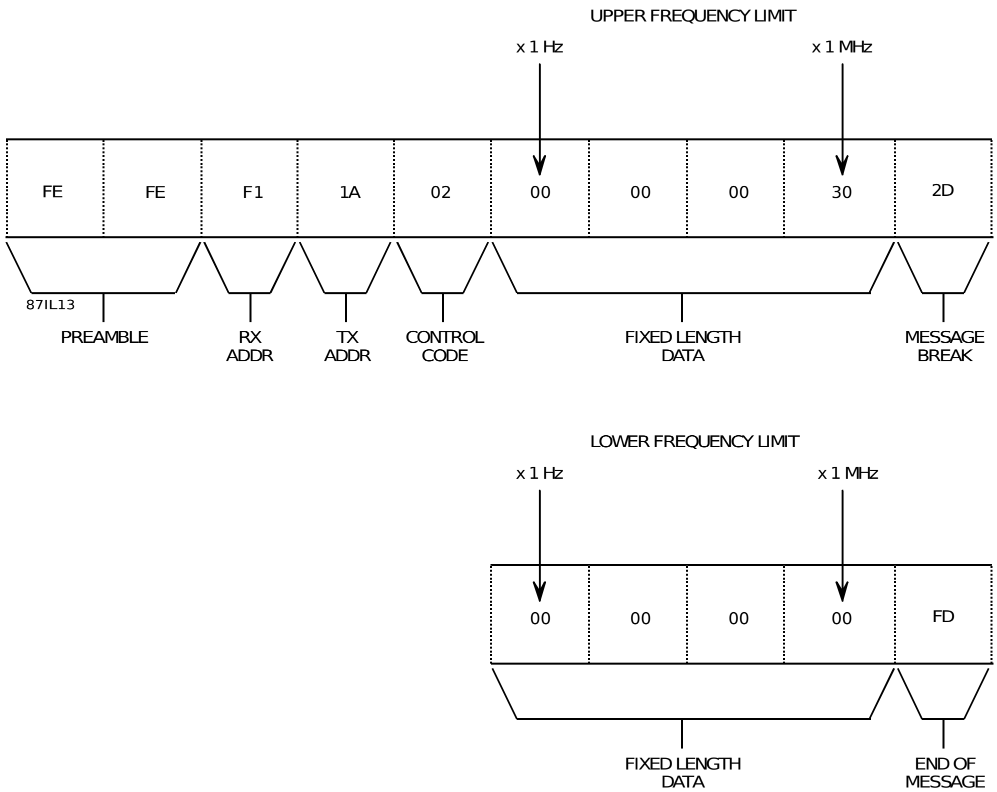


Figure 5-8. Tuned Frequency Range Request Response Format

5.8.5 DETECTION MODE/IF BANDWIDTH COMMAND WITHOUT ACKNOWLEDGE [01]

Figure 5-9 shows an example of the typical format for selecting the receiver's detection mode and IF bandwidth using control code [01]. This control code provides the same result as the [06] command described in **paragraph 5.8.6** except it does not require an acknowledgment. For this reason it is not the preferred method to change IF bandwidth or detection mode.

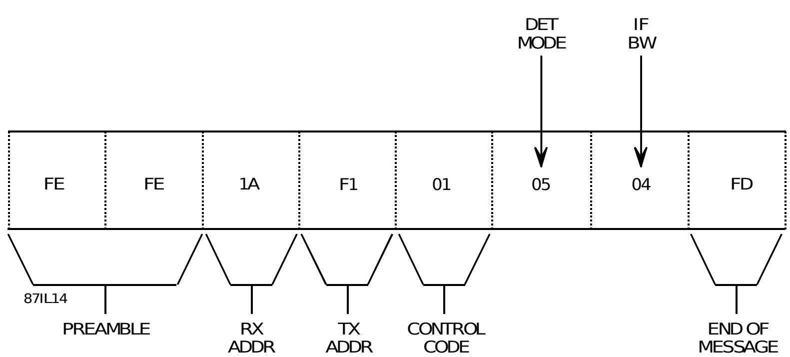


Figure 5-9. Detection Mode/IF Bandwidth Command Format Without Acknowledge

The first byte after the control code contains the detection mode code. The second byte contains the IF bandwidth code. See control code [01] in **Table 5-1** for the detection mode and IF bandwidth choices and their codes. In the example, the FM detection mode is selected with an IF bandwidth of 6.00 kHz. The IF bandwidth byte is ignored when the detection mode byte contains codes for LSB, USB, or ISB detection modes ([00], [01], or [06]). When these detection modes are selected, the IF bandwidth is automatically set to 3.2 kHz [03].

5.8.6 DETECTION MODE/IF BANDWIDTH COMMAND WITH ACKNOWLEDGE [06]

Figure 5-10 shows an example of the typical format for selecting the receiver's detection mode and IF bandwidth using control code [06]. This control code provides the same result as the [01] command described in **paragraph 5.8.5** except it requires an acknowledgment to the controller. For this reason it is the preferred method to change the IF bandwidth or detection mode.

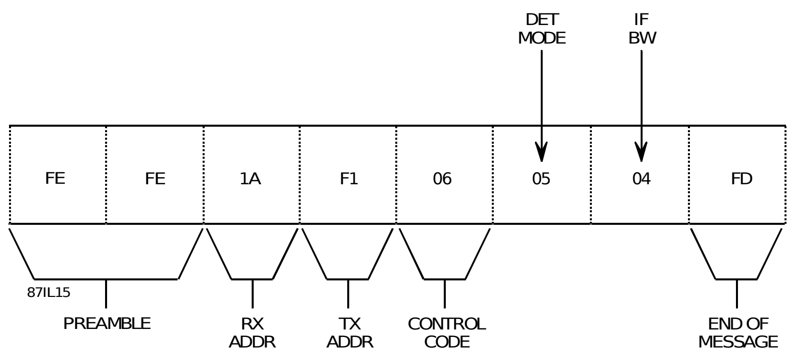


Figure 5-10. Detection Mode/IF Bandwidth Command Format With Acknowledge

The first byte after the control code contains the detection mode code. The second byte contains the IF bandwidth code. See control code [06] in **Table 5-1** for the detection mode and IF bandwidth choices and their codes. In the example, the FM detection mode is selected with an IF bandwidth of 6.00 kHz. The IF bandwidth byte is ignored when the detection mode byte contains codes for LSB, USB, or ISB detection modes ([00], [01], or [06]). When these detection modes are selected, the IF bandwidth is automatically set to 3.2 kHz [03].

5.8.7 RESPONSE TO DETECTION MODE/IF BANDWIDTH REQUESTS [04]

Figure 5-11 shows an example of the typical response format when requesting the receiver's detection mode and IF bandwidth with control code [04].

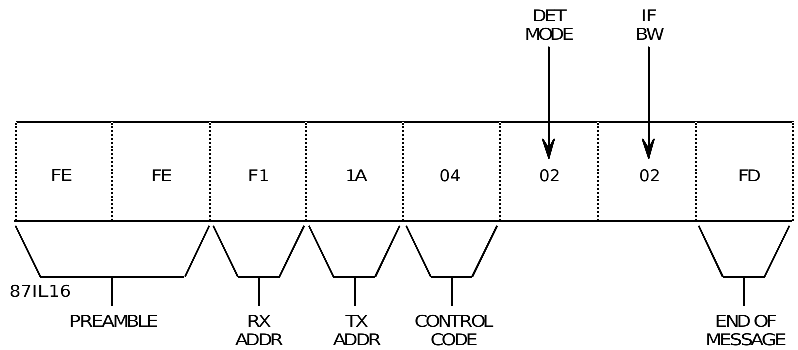


Figure 5-11. Detection Mode/IF Bandwidth Request Response Format

The first byte in the response contains the detection mode code and the second byte contains the IF bandwidth code. The response in the example is the AM detection mode with an IF bandwidth of 1.00 kHz. See control code [01] or [06] in **Table 5-1** for the possible responses for both bytes.

5.8.8 GAIN CONTROL MODE COMMAND WITH ACKNOWLEDGE [31]

Figure 5-12 shows an example of the typical format for selecting the receiver's gain control mode using control code [31]. This control code requires an acknowledgment to the controller.

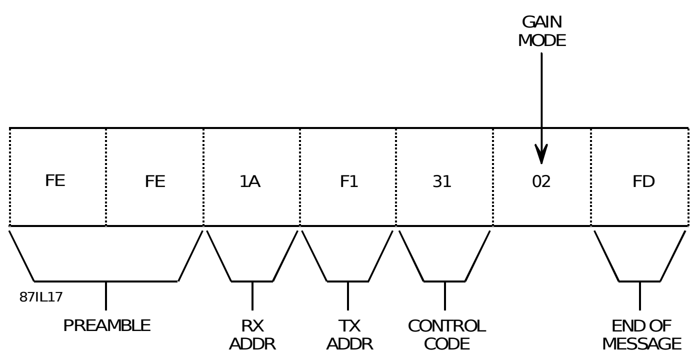


Figure 5-12. Gain Control Mode Command Format

One byte is sent with the control code. In the example, the fast AGC control mode is selected [02]. The selection can also be either slow AGC [01] or manual gain control [00].

5.8.9 RESPONSE TO GAIN CONTROL MODE REQUESTS [30]

Figure 5-13 shows an example of the typical response format when requesting the receiver's active gain control mode with control code [30].

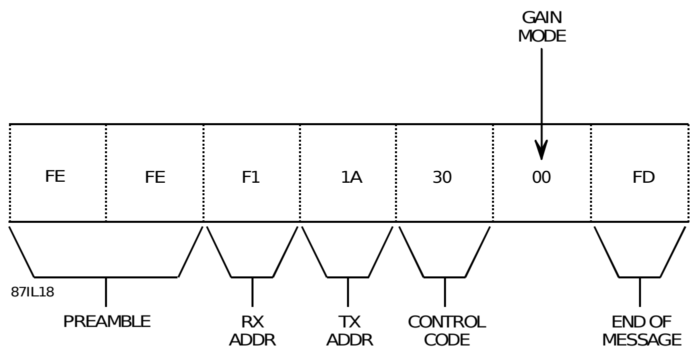


Figure 5-13. Gain Control Mode Request Format

The byte in the response after the control code contains the gain control code. The response in this byte is [00] for manual gain, [01] for slow AGC, or [02] for fast AGC. In the example, manual gain control is the response.

5.8.10 MANUAL GAIN LEVEL COMMAND WITH ACKNOWLEDGE [33]

Figure 5-14 shows an example of the typical format for selecting the receiver's manual gain level using control code [33]. This control code requires an acknowledgment to the controller.

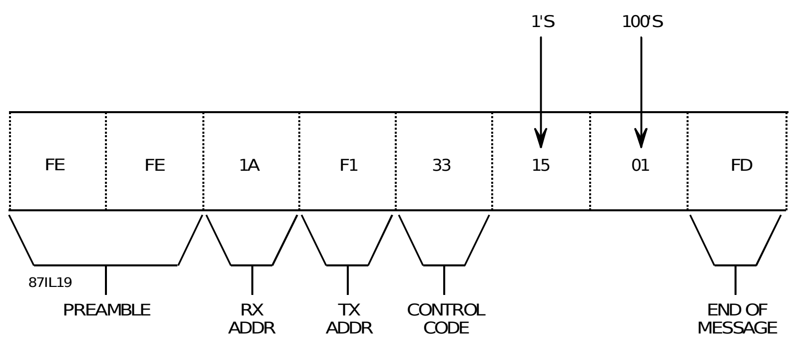


Figure 5-14. Manual Gain Level Command Format

Two bytes are sent with the control code, with the combination of both representing the value. The range is 0000 to 0127 (for 0 to 127 dB). In the example, a manual gain level of 115 dB is selected [15|01].

5.8.11 RESPONSE TO MANUAL GAIN LEVEL REQUESTS [32]

Figure 5-15 shows an example of the typical response format when requesting the receiver's manual gain level with control code [32].

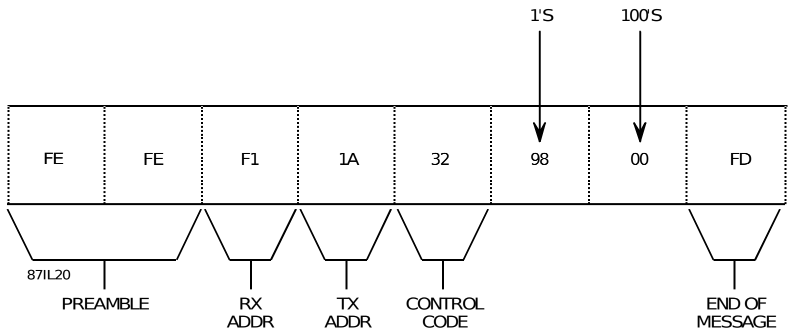


Figure 5-15. Manual Gain Level Request Format

Two bytes in the response following the control code contain the current manual gain level. The combination of the two bytes represent the value in binary coded decimal. The value can be from 0000 to 0127 (or 0 to 127 dB). In the example, the manual gain level response is 98 [98|00].

5.8.12 BFO FREQUENCY COMMAND WITH ACKNOWLEDGE [35]

Figure 5-16 shows an example of the typical format for sending the receiver's BFO frequency using control code [35]. This control code requires an acknowledgment to the controller.

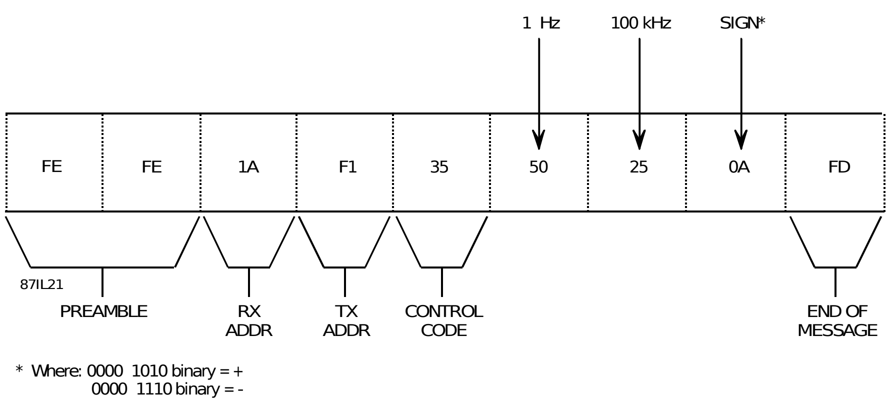


Figure 5-16. BFO Frequency Command Format

The frequency can be set to any value from +7999 to -8000 kHz at a resolution of 10 Hz. Sending +0000 sets the BFO to off. The frequency entered in the example is +2.550 kHz. The first byte of the frequency data contains Hz data. The second byte contains 100-Hz data. The third byte contains the sign, positive (+) or negative (-). For negative BFO frequencies, a hexadecimal value of [0E] should be sent in the third byte. For positive BFO frequencies, a hexadecimal value of [0A] should be sent in the third byte.

5.8.13 RESPONSE TO BFO FREQUENCY REQUESTS [34]

Figure 5-17 shows an example of the typical response format when requesting the BFO frequency with control code [34].

The response in the example is -855 Hz. The first byte of the frequency data contains Hz data. The second byte contains 100-Hz data. The third byte contains the sign, positive (+) or negative (-). A value of [0E] is returned in the third byte of the response when the frequency is a negative value. A value of [0A] is returned when the BFO frequency is positive.

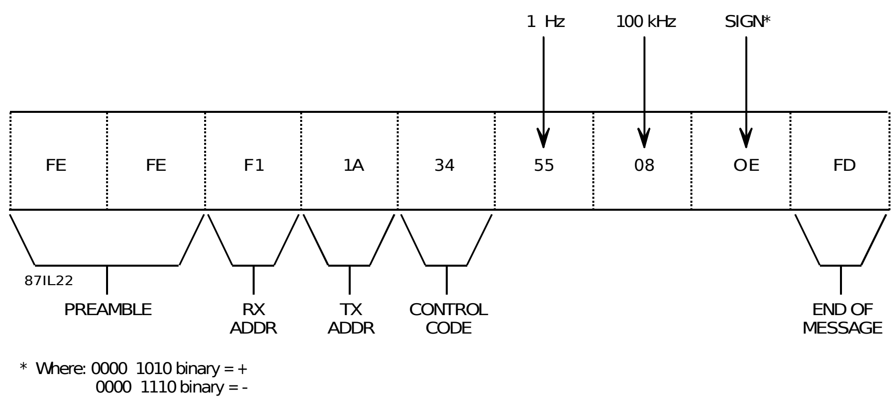


Figure 5-17. BFO Frequency Request Response Format

5.8.14 RF INPUT PATH COMMAND WITH ACKNOWLEDGE [39]

Figure 5-18 shows an example of the typical format for selecting the receiver's RF input path using control code [39]. This control code requires an acknowledgment to the controller.

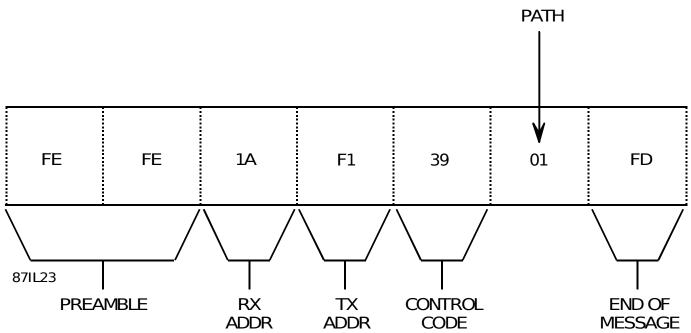


Figure 5-18. RF Input Path Command Format

One byte is sent with the control code. In the example, the normal RF input path is selected [01]. The selection can also be either attenuated [02] or preamplified [03]. The preamplifier is only allowed at tuned frequencies of 0.5 MHz and above.

5.8.15 RESPONSE TO RF INPUT PATH REQUESTS [38]

Figure 5-19 shows an example of the typical response format when requesting the receiver's current RF input path selection with control code [38].

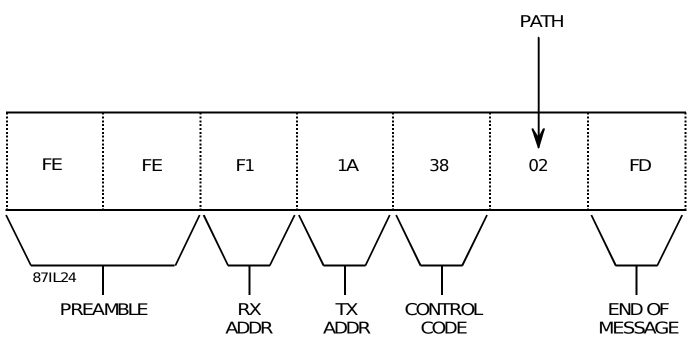


Figure 5-19. RF Input Path Request Response Format

The byte in the response after the control code contains the RF input path code. The response in this byte is [01] for normal, [02] for attenuated, or [03] for preamplified. In the example, the attenuated RF input path is selected.

5.8.16 DEVICE CONTROL MODE COMMAND WITH ACKNOWLEDGE [37]

Figure 5-20 shows an example of the typical format for selecting the receiver's control mode using control code [37]. This control code requires an acknowledgment to the controller.

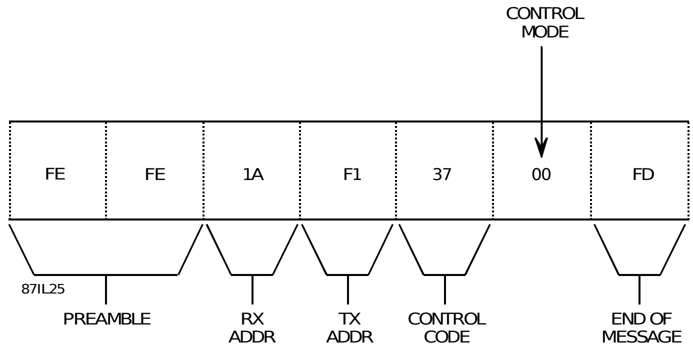


Figure 5-20. Device Control Mode Command Format

One byte is sent with the control code. In the example, the Local control mode is selected [00]. The selection can also be either Remote mode [01] or Remote with Local Lockout [02]. These commands are included for compatibility with other receivers in the WJ-871Y family. For the WJ-8710A Receiver, only the Remote mode [01] applies.

5.8.17 RESPONSE TO DEVICE CONTROL MODE REQUESTS [36]

Figure 5-21 shows an example of the typical response format when requesting the receiver's current control mode with control code [36].

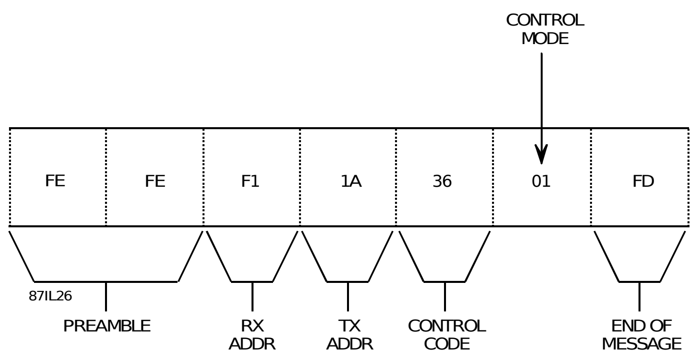


Figure 5-21. Device Control Mode Request Response Format

The byte in the response after the control code contains the device control mode code. The response in this byte is [00] for Local, [01] for Remote, or [02] for Remote with Local Lockout. In the example, the Remote control mode is selected.

5.9 **COLLISION DETECTION**

Many different data transmitting devices can be connected on the CSMA interface along with the WJ-8710A. Therefore, there is always the possibility that two or more units may want to talk at the same time, causing “data collisions” on the interface.

The WJ-8710A is designed so that it monitors all the messages that it transmits and then compares the monitored data to the transmitted data. If the transmitted data does not match the monitored data, it is assumed that a collision has occurred. The WJ-8710A immediately sends the jammer codes shown in **Figure 5-22**. The WJ-8710A waits for a period of time, checks for an idle interface, and then sends the original response. If another collision occurs, the process is repeated with an increased wait until the message goes through or until the fifth repetition. After five tries (each with an increased wait), the WJ-8710A discards the message. Only when the controller transmits a new message does the process start again. If any device detects the jammer codes, the data that it receives is disregarded.

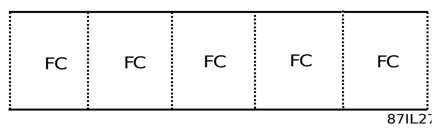


Figure 5-22. Jammer Code

SECTION VI

CIRCUIT DESCRIPTION

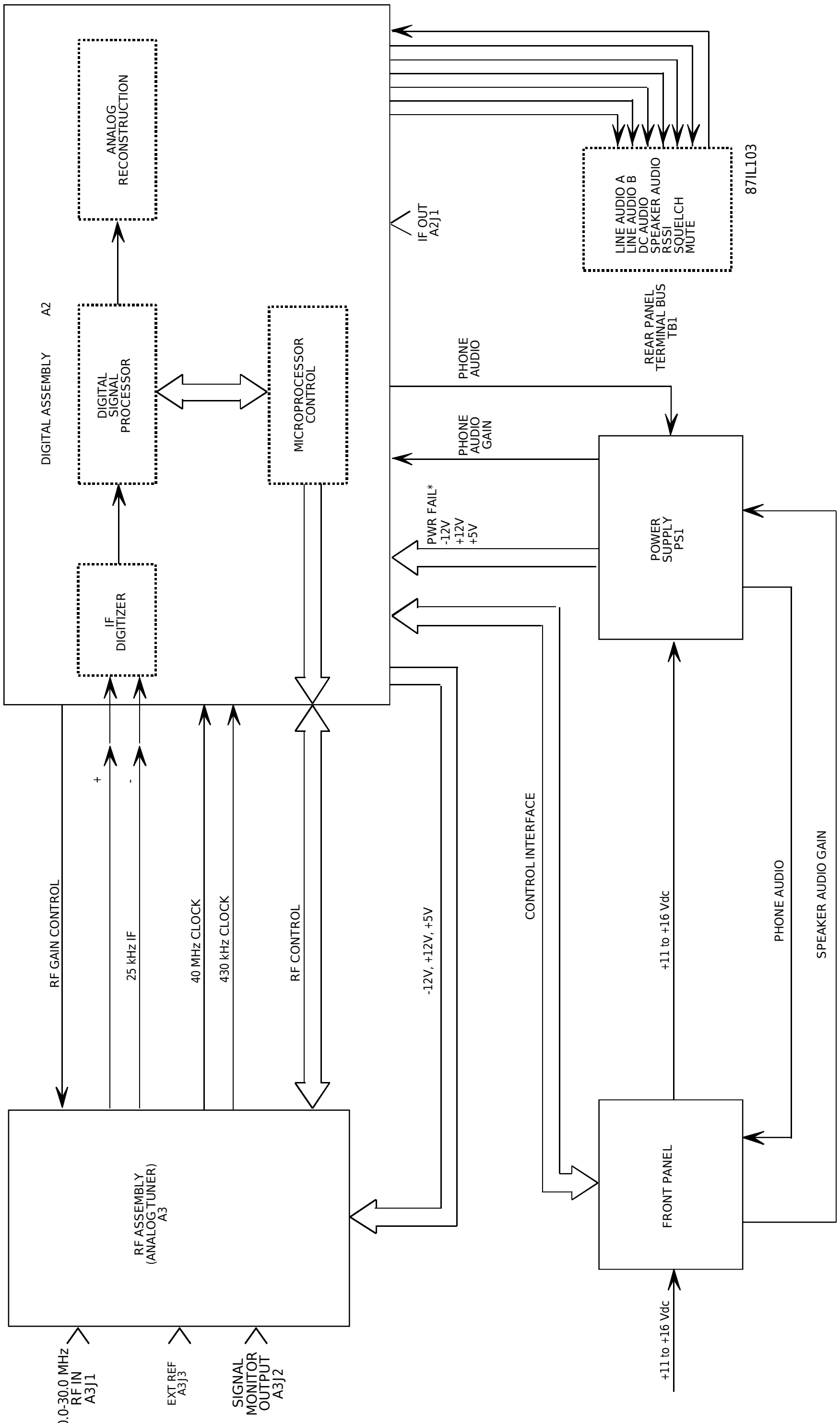


Figure 6-1. WJ-8710A Digital HF Receiver Block Diagram

SECTION VI

CIRCUIT DESCRIPTION

6.1 WJ-8710A DIGITAL HF RECEIVER FUNCTIONAL DESCRIPTION

The WJ-8710A Digital HF Receiver is a Digital Signal Processing (DSP) based receiver, consisting of an analog tuner, an IF digitizer, digital signal processing circuitry, and analog reconstruction. These operating components, and the receiver control circuitry, are contained on two printed circuit assemblies, consisting of the Type 797006 RF Assembly (A3) and the Type 797214 Digital Assembly (A2). These two assemblies, along with the Power Supply (A1), comprise the complete DSP based HF Receiver, as illustrated in **Figure 6-1**. Refer to the functional block diagram in **Figure 6-1** for the following functional description.

The Type 797214 RF Assembly (A3) functions as the analog tuner for the receiver. It performs coarse signal tuning and provides two wideband IF output signals. Three conversion stages contained in this assembly provide tuning throughout the 5 kHz to 30.0000 MHz spectrum, with a coarse tuning resolution of 1 kHz. The RF input from the antenna enters the assembly at the front panel RF INPUT connector (A3J1) and, after passing through the three conversion stages, the tuned signal is translated into two IF outputs. The first output is a 455 kHz IF output, having a nominal 30 kHz bandwidth. It is routed directly to the front panel Signal Monitor Output connector (SMO, A3J2). This is a 50-ohm wideband output suitable for connection of an external signal monitor. The second output is a 25 kHz IF output, also having a nominal 30 kHz bandwidth, that is routed to the Type 7970012 Digital Assembly (A2) for digitizing and further processing. In addition to the 25 kHz IF signal, the RF Assembly provides two clock signals to the Digital Assembly. The 40 MHz and 430 kHz signals, derived from the receiver's local oscillators, are used for signal processing synchronization and analog reconstruction.

Timing and synchronization of the local oscillators in the RF Assembly are maintained by a precision 10 MHz reference oscillator contained on the assembly. The RF Assembly reference may also be locked to an external frequency standard by connecting the external 1, 2, 5, or 10 MHz signal at the front panel EXTERNAL REFERENCE connector (A3J3). The connection of the external reference in automatically sensed and locks the reference oscillator to the external source.

The Type 797214 Digital Assembly (A2) functions as the IF Digitizer, Digital Signal Processor, and Analog Reconstruction circuit for the receiver. It also contains the microcontroller circuitry that maintains control over all receiver operations. The Digital Assembly accepts the 25 kHz IF signal from the RF Assembly, digitizes the signal, and uses Digital Signal Processing (DSP) techniques to perform the majority of the signal processing operations required to produce the final outputs. The DSP circuitry on this assembly converts the digitized IF signal from a continuous time domain signal into discrete time samples that can be stored in random access memory and processed digitally to perform a wide range of operations, normally associated with analog circuitry, such as:

- Receiver Fine Tuning to a 1 Hz resolution,
- IF Bandpass Filtering,
- Determination of Input Signal Strength,
- Receiver Gain Control,
- Signal Detection and Demodulation,
- Noise Blanking.

Upon completion of the signal processing, a serial data stream representing the receiver's bandpass filtered IF signal, and the demodulated audio extracted from the tuned signal are routed to the Analog Reconstruction circuitry. The Analog Reconstruction circuitry converts the digital data back to its analog form, separates the audio and IF signals, provides post filtering, and after completion of the analog reconstruction) provides the final audio and post filtered IF outputs. The reconstructed IF signal is converted up to 455 kHz and is provided the front panel IF OUTPUT connector (A2J1) for external use. This 50-ohm output provides the 455 kHz IF at a level of approximately -20 dBm (AGC active), with its bandwidth determined by the operator selected IF bandwidth.

The reconstructed audio is separated into left and right channels and is then directed to the various receiver audio outputs. The phone audio is routed to the front panel PHONES jack (A1J1) via the Power Distribution Assembly (A1). The audio signal is also provided to the front panel terminal bus (TB1). The LINE A and LINE B audio outputs are 600-ohm balanced audio outputs, and the SPEAKER output is an unbalanced 8-ohm output. The final audio output is the DC AUDIO, a DC coupled, unbalanced, 1-kilohm output.

The Type 797214 Digital Assembly also contains a microcontroller that provides an interface between an external controlling device and the receiver circuitry. A serial control interface is provided at the front panel to permit receiver control by an RS-232 or CSMA compatible computer via A2J3 or A2J2, respectively. A third control interface, routed to the receiver front panel (CONTROL INTERFACE, W3J1), permits the connection of a Type TF-30387 8712A Front Panel Controller Test Fixture (not supplied). With the test fixture installed, complete receiver control is provided using the controls and indicators of the test fixture.

Operating power is supplied to all of the assemblies of the WJ-8710A Receiver by the Type 766027 Power Supply assembly (A1). It accepts a DC input in the range of +11 to +16 VDC, and provides regulated outputs of +12V, -12V, +5V, and the DC supplies are passed on to the RF Assembly (A3). It also provides an interface between the front panel and the Digital Assembly for the headphone jack and the phone audio gain control.

6.2 CIRCUIT DESCRIPTIONS

6.2.1 TYPE 797006 RF ASSEMBLY, (A3)

This assembly is manufactured in five versions. The Type 797006-1 is the standard assembly. It is equipped with the standard reference generator, having a stability of better than 0.7 ppm. The Type 797006-2 version is installed in receivers containing the WJ-871Y/REF option. This version is equipped with an upgraded reference generator, having a stability of better than 0.2 ppm. The Type 797006-5 version used in the WJ-8710A is similar to the -1 version, but with covers and wraparound added for the compact mounting arrangement.

The Type 797006 RF Assembly (A3) functions as the RF tuner for the WJ-8710A Digital HF Receiver. It receives a 500 kHz to 30.0000 MHz input spectrum from the RF signal source and provides RF tuning to extract the signal of interest from the input spectrum. The signal of interest is converted to 455 kHz and 25 kHz IF signals that are provided as outputs for further processing. Refer to the Type 797006 RF Assembly Block Diagram in **Figure 6-2** as a reference for the following module description. For a more detailed illustration of the RF Assembly circuitry, refer to the Type 797006 RF Assembly schematic diagram, **Figure 9-2**.

The RF Assembly consists of an RF Input circuit, three Mixing stages for signal conversion, a highly stable reference generator, and three local oscillators. These module sections interconnect as illustrated in **Figure 6-2** to produce the required outputs.

The reference generator uses a phase-locked-loop synthesizer to control a temperature-compensated, voltage-controlled crystal oscillator, producing a highly stable 10 MHz reference signal that is used as the time base for the receiver. Additionally, the reference generator may be locked to an external reference by connecting an external 1, 2, 5, or 10 MHz reference signal, at a level of 200 mV RMS, at the front panel EXTERNAL REFERENCE connector (A3J3). When an external input at one of the specified frequencies is present at this input, its presence is automatically sensed, and the reference generator locks to the external signal. The 10 MHz reference is then provided as the time base for the 1st, 2nd, and 3rd local oscillators.

The 1st LO circuit is a translation oscillator, comprised of the 1st LO VCO, a coarse tuning phase-locked-loop synthesizer, and a fine tuning phase-locked-loop synthesizer. The combined circuitry produces the variable 1st LO output, used to provide signal tuning. The output ranges from 40.455 MHz to 70.455 MHz for tuned frequencies ranging from 0.0000 to 30.0000 MHz, respectively. This output is provided to the first mixer (U28) to produce a 40.455 MHz 1st IF.

The 2nd LO circuit produces a fixed 40 MHz output. It is produced by multiplying the 10 MHz reference signal by a factor of four. The 40 MHz output is then provided to the 2nd mixing stage (U30) to produce 455 kHz 2nd IF. The 40 MHz 2nd LO is also provided to the Digital Assembly for use as the time-base for the control microprocessor and analog-to-digital conversion circuitry. This signal is output via pin 23 of connector A3E1 (LO2).

The 3rd LO circuit uses a phase-locked-loop synthesizer, locked to the 10 MHz reference, to produce the fixed 430 kHz 3rd LO signal. This 430 kHz signal is provided to the 3rd mixing stage (U31) to produce the 25 kHz 3rd IF. The 430 kHz 3rd LO signal is also directed via pin 17 of A3E1 to the Digital Assembly. It is used in the Digital Assembly for analog reconstruction of the IF signal for output to the front panel IF OUTPUT (A2J1).

The RF/IF signal path accepts the 0.5000 to 30.0000 MHz input spectrum, provides input filtering, and using multiple conversion stages, produces the 455 kHz and 25 kHz IF outputs. The signal enters the assembly via the 50-ohm RF INPUT (A3J1). The signal passes through an lowpass input roofing filter, having a nominal 32 MHz cutoff frequency. This permits the 0.5000 to 30.0000 MHz HF spectrum to pass while attenuating signals above the receiver tuning range. The input filtering provides improved IF and image frequency rejection. Beyond the 32 MHz cutoff frequency, the filter response drops sharply, providing approximately 80 dB of ultimate attenuation. The the filtered RF input is then directed through a selectable front end gain/attenuation control circuit, providing three operator selectable front end settings. It permits the operator to route the signal directly to the 1st conversion stage, or, depending on signal conditions, introduce front end gain or attenuation. In the NORMAL mode, the signal is passed directly through this circuit with no effect on signal amplitude. Under weak signal conditions, the +10 dB gain path provides 10 dB of signal amplification. The third signal path is for extremely strong signal conditions. The -15 dB selection passes the signal through a 15 dB resistive pad to reduce the signal entering the receiver front end. This attenuation pad is capable of dissipating up to 1 watt to provide protection at the receiver input.

The 1st stage of conversion consists of a high intercept mixer that mixes the RF spectrum with the 1st LO signal, ranging from 40.455 MHz (0.0000 MHz Tuned Frequency) to 70.455 MHz (30.0000 MHz Tuned Frequency). The mixer output is amplified and bandpass filtered to select the amplified 40.455 MHz difference frequency. The 1st IF filter provides a 30 kHz bandpass, centered at 40.455 kHz.

After IF filtering and amplification, the 40.455 kHz IF signal is directed to the second conversion stage, via a voltage-controlled attenuator. This circuit provides control over the amplitude of the signal to the proper output level, preventing overload of the analog to digital converter stage in the Digital Assembly. The RF GAIN input at pin 15 of connector E1 is provided by the control processor in the Digital Assembly (A2). It is the result of the DSP microprocessor sampling the value of the signal level after digitization. This voltage ranges from 0 to +7 V, providing approximately 60 dB of gain control. This voltage is strictly dependent on the signal level and is independent of the receiver's AGC or manual gain setting.

The 2nd conversion stage mixes the signal with the fixed 40 MHz 2nd LO signal, producing the 455 kHz 2nd IF. After filtering to remove the undesired mixing products, the IF signal is split into two paths. The first path directs the 455 kHz IF out to the front panel SIGNAL MONITOR OUTPUT (A3J2). This provides a 50-ohm output at a level of approximately 30 dB greater than the RF INPUT at connector A3J1. The Signal Monitor Output bandwidth is approximately 30 kHz wide.

The second signal path for the 2nd IF signal is through the third stage of conversion. The signal is mixed with the 430 kHz 3rd LO signal, producing the 25 kHz 3rd IF signal. After filtering, the 25 kHz IF is output, via pins 19 and 20 of connector E1, to the Digital Assembly for digitization and further processing. It is a differential output, having a level approximately 53 dB greater than the RF input. The bandwidth is approximately 25 kHz.

All control over the operation of the Type 797006 RF Assembly is performed by the Digital Assembly via pins 7 through 15 of connector A3E1. Connector E1 pin 15 provides a 0 to +7 V level, controlling the gain of the RF signal path. It is the result of sampling of the IF signal level after digitization. The remaining pins are used for monitoring the RF Assembly operation and sending control data for tuning and setting RF front end Gain/Attenuation selection.

The PRE/OPT (pin 12), RF ERR (pin 13), and REF SENSE (pin 14) are all outputs from the RF assembly to the Digital Assembly. They provide the control microprocessor with the operating status. The PRE/OPT line (pin 12) is for a Preselector option not used on the WJ-8710A.

The REF SENSE line (pin 14) provides an indication when an external reference is connected at the front panel EXTERNAL REFERENCE connector (A3J3). When an external reference is connected, it causes this line to assume a logic "0" condition. The control microprocessor then tunes the reference phase-locked-loop synthesizer to each of the allowable reference input frequencies, until the reference synthesizer locks on an external input. If no external reference is present, the REF SENSE line remains at logic "1" and the internal reference provides the receiver time-base.

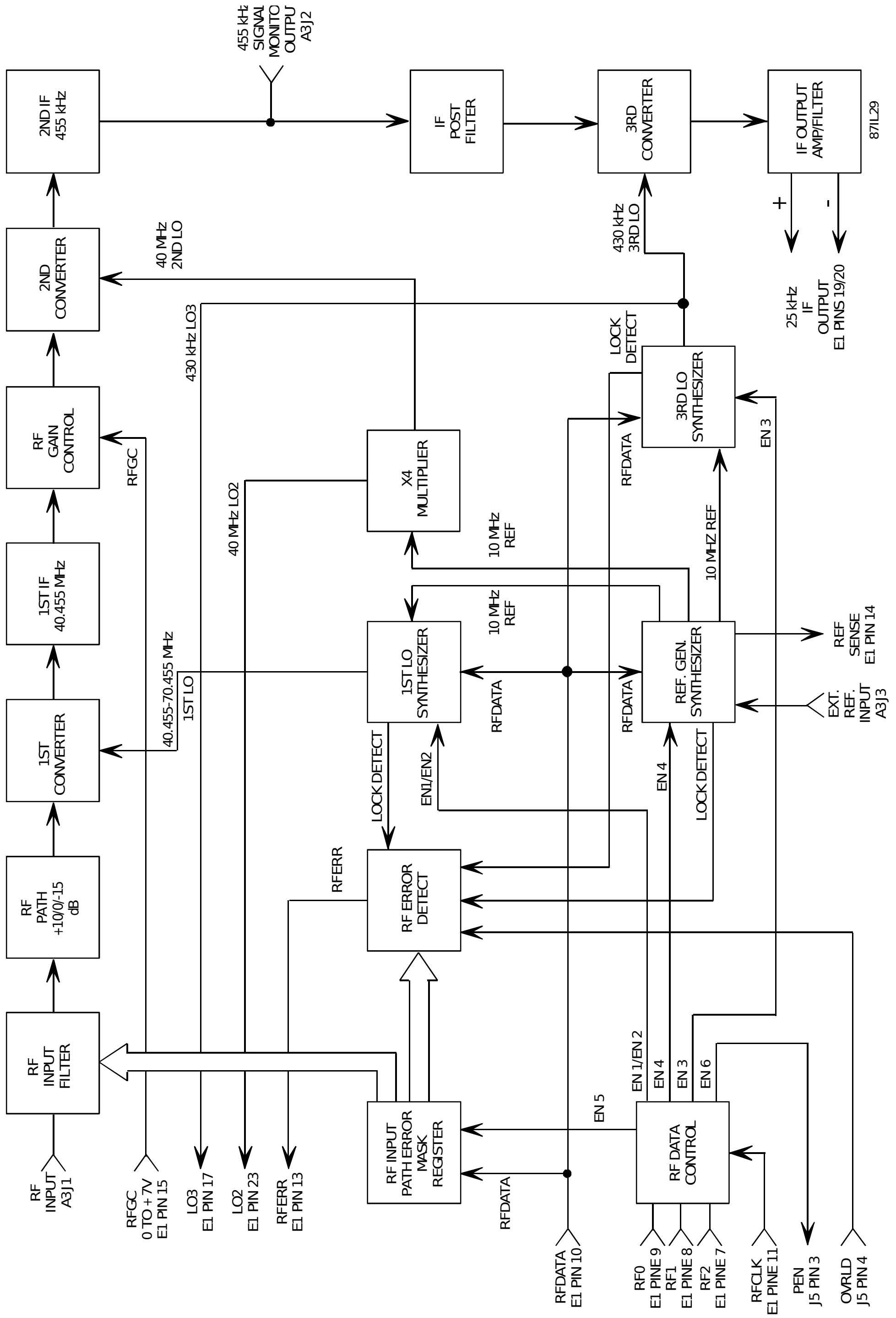


Figure 6-2. Type 797006 RF Assembly Block Diagram

The RF ERR line (pin 13) provides the control microprocessor with an indication of the operating status of the phase-locked-loop synthesizers in the RF assembly. The synthesizer lock lines of the Reference, 1st LO and 3rd LO synthesizers are ORed together, along with the preselector overload line. Any synthesizer unlock or signal overload condition causes this line to assume a logic "0" condition. Once flagged by the RF ERR line, the microprocessor individually masks each of the RF ERR controlling inputs to determine the error source and reports the appropriate error condition.

Control of the RF assembly is provided via the RF0, RF1, RF2, RF DATA, and RF CLK lines (pins 7 through 11). The RF DATA line (pin 10) carries serial data from the control microprocessor to the various controlled circuits in the RF Assembly. The data is sent as a series 8-bit data words synchronized with the data clock present on the RF CLK line (pin 11). The RF DATA line is shared by six controlled circuits each of which acts on the data only when instructed by the microprocessor via the RF0, RF1, and RF 2 control lines. These lines determine the destination of the data. Table 6-1 lists the states of the data control lines and the associated data.

Table 6-1. RF Data Control

RF2	RF1	RF0	STROBE	DATA TYPE
0	0	0	EN1	1st LO Fine Loop Tuning Data.
0	0	1	EN2	1st LO Coarse Loop Tuning Data.
0	0	1	EN3	3rd LO Tuning Data.
0	1	0	EN4	Reference Oscillator Tuning Data.
0	1	1	EN5	BITE/NORM/PREAMP/ATTEN Data.
1	0	1	EN6	Not Used

6.2.2 TYPE 797214 DIGITAL ASSEMBLY, (A2)

The Type 797214 Digital Assembly (A2) consists of three major operating sections: the Control and Interface section; the Digital Signal Processing section; and the Reconstructed Analog Section. These sections perform the IF digitization, Digital Signal Processing, Analog Reconstruction, and Receiver Control functions associated with the operation of the WJ-8710A Digital HF Receiver. The assembly also provides an interface with an external computer, or other external controlling devices, and performs the control and monitoring functions that direct the receiver operation. Refer to the Type 797214 Digital Assembly Block Diagram in **Figure 6-3** as a reference for the following assembly description. For a more detailed illustration of the Digital Assembly circuitry, refer to the Type 797214 Digital Assembly Schematic Diagram, **Figure 9-1**.

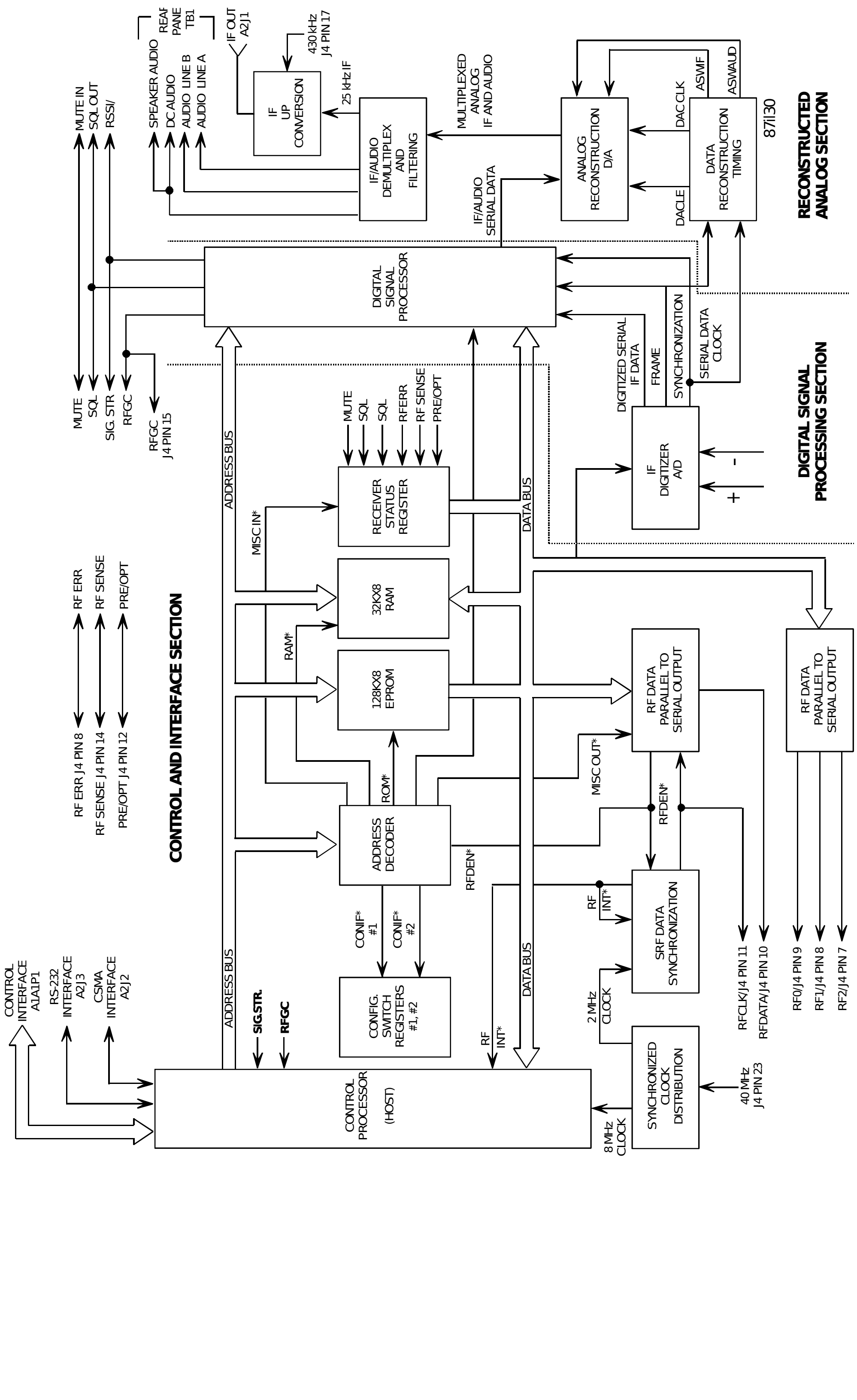


Figure 6-3. Type 797214 Digital Assembly Functional Block Diagram

Under the direction of the Control and Interface section, the Digital Signal Processing section takes the analog IF signal supplied by the RF Assembly, digitizes it, and processes the digitized signal data to extract the signal intelligence. Other than the signal tuning performed by the RF Assembly, the Digital Signal Processing section performs all of the receiver functions that ultimately produce the final outputs. The 25 kHz IF input enters the Digital Assembly at pins 19 and 20 of J4. This differential input has a 25 kHz bandwidth, and ranges in level from approximately .1 to .7 V peak-to-peak at each of the input pins. The signal is directed into the IF Digitizer where the analog signal is converted into digital data that can be read by the Digital Signal Processor. A 12.8 MHz clock, provided by synchronized clock distribution circuitry in the Control and Interface section, provides the timing for the analog-to-digital conversion. It causes the signal to be sampled at a 100 kHz rate, producing a series of data frames, each representing one sample of the analog input. Each frame is made up of 32 data bits, 16 of which contain the digitized IF sample. The samples are provided to the DSP circuitry where the continuous time domain signal samples are converted into discrete time samples for continuous processing. Using this data, the Digital Signal Processor, digitally performs fine tuning to a 1 Hz resolution, IF bandwidth filtering, signal strength calculations, signal demodulation, noise blanking, and receiver gain control.

The outputs from the Digital Signal Processing section consists of serial data containing a digital representation of the receiver's IF (limited to the selected IF bandwidth), and detected audio, multiplexed into a single data stream. This data is routed to the Reconstructed Analog section where the signals are separated, converted back to analog signals, and output to the front panel of the receiver. It also provides analog and digital outputs to the Control and Interface section, and to the front panel terminal bus (TB1) for monitoring. The Squelch output line at the front panel provides a logic level that indicates to external equipment if a tuned signal exceeds the programmed Squelch level. It is set to logic "0", whenever a tuned signal exceeds the programmed level. The signal strength output is provided at the front panel terminal bus as the RSSI output line. It is an analog voltage ranging from 0 to +5V, representing the strength of the received signal. These outputs are also provided to the Control and Interface section for monitoring. Additionally the Digital Signal Processing section provides an RF gain control output to the Type 797006 RF assembly (A3). This output is a result of the DSP sampling the signal level at the input to the IF Digitizer. It controls the gain of the RF section to prevent the signal from overdriving the input of the IF Digitizer. The voltage ranges from approximately +7.0 V with no signal present to 0 V with strong signals present.

The Reconstructed Analog section receives the Digitized IF and audio data from the Digital Signal Processing section and converts the signals back to analog form for output. In addition to the serial data, the Digital Signal Processing section provides frame synchronization and serial data clock signals for timing of the data transfer. These timing signals permit the Reconstructed Analog section to demultiplex the signals into separate IF and audio signals. The reconstructed IF signal, converted back to a 25 kHz analog IF, is mixed with a 430 kHz local oscillator signal from the RF Assembly (A3), provided via pin 17 of J4. This mixing process up-converts the IF signal to 455 kHz. The signal is then provided to front panel connector A2J1. This 50-ohm output provides a 455 kHz IF output, limited in bandwidth to the selected IF bandwidth. The level is approximately -20 dBm when loaded into 50 ohms.

The reconstructed audio is filtered and routed to the front panel terminal bus as the Line A and Line B audio outputs. These are 600-ohm balanced outputs for use with external audio monitoring devices. A DC Audio output is also provided at the front panel terminal bus. It is an unbalanced, DC coupled audio output. The final audio output is provided to the front panel PHONES jack, via the Power Supply Assembly (A1).

The Control Interface Section directs the operation of the Type 797006 RF Assembly (A3) and it directs the operation of the functions performed by the Digital Signal Processing Section, contained on this assembly.

The heart of the Control Interface Section is the 68HC11 microcontroller. It continuously monitors the receiver functions and provides control data to direct its operation. On receiver power up, the control processor enters into a power up routine that checks the two banks of configuration switches to properly configure the external control interfaces for communication with external controlling devices, and it performs a built-in-test (BITE) operation to verify proper operation of key receiver parameters. Once the configuration and testing have been completed, the microcontroller then directs control data to the RF Assembly and the Digital Signal Processing section to set the receiver parameters for operation. The communication with the Digital Signal Processing section is via the microcontroller's address and data buses. It consists of data that determines the parameters that the Digital Signal Processor uses in processing of the tuned signal.

The transfer of control data to the RF section is performed through a ribbon cable connected at J4. This data (RF DATA) is transferred serially as a sequence of 8-bit data words, via J4 pin 10, and provides the data to five control registers in the RF Assembly that: phase locks the receiver time base; tunes the RF Assembly to the desired frequency; and selects the NORMAL, PREAMPLIFIED, or ATTENUATED RF Input Path. Three control lines (RF0, RF1, and RF2) are set as each each data word is transferred, determining the destination of the data after it reaches the RF Assembly. These control lines form a three-bit address via pins 9, 8, and 7 of J4, respectively, which are decoded by the RF Assembly to properly direct the data transfer (refer to Table 6-1). The RF DATA, and the RF0, RF1, and RF2 Control lines are synchronized with the RF clock (RFCLK), J4 pin 11. This is a sequence of 8-bit clock bursts that provide timing for the data transfer.

Three status lines, provided via connector J4, are monitored by the Control Section to determine the operating status of the RF assembly. They are routed to a receiver status input register, and are checked periodically to verify proper operation and to determine if any control action is to be taken. The RFERR status line provides a logic level to notify the Control section if an error condition occurs. With an external reference connected to the receiver rear panel, and, with all of the phase-locked-loop synthesizers in the RF Assembly locked and operating normally, the RFERR line provides a constant logic "1". If any of the synthesizers fail, the unlocked synthesizer causes a logic "0". If no external reference is connected to the receiver rear panel, the internal reference is active, and logic "0" pulses occur at intervals of approximately 8 msec.

The Control and Interface section timing is synchronized with the receiver's time base by a 40 MHz signal, provided by the RF Assembly via J4 pin 23. This signal enters the synchronized clock distribution circuitry of the Control and Interface section, where it is used to generate an 8 MHz clock for the microcontroller, a 2 MHz clock to provide timing for transferring control data to the RF Assembly, and the 12.8 MHz clock for timing of the analog-to-digital conversion in the IF digitizer.

Three methods of control of the receiver operation are supported by the Control and Interface section. The RS-232 interface provides a communications link from the microcontroller to a 25-pin RS-232 connector at the receiver front panel (A2J3). This is a three-wire configuration that permits talk and listen capabilities, using RS-232 levels. The CSMA interface provides limited receiver control capabilities. The second form of receiver control is via the Control interface output (A2J7). This interface is routed to the Front Panel Assembly circuit card via a 24 conductor ribbon cable attached to A1A1E7.

6.2.3 TYPE 766027-1 POWER SUPPLY ASSEMBLY, (A1)

The Type 766027-1 Power Supply, illustrated in the WJ-8710A Main Chassis Schematic Diagram, **Figure 9-4**, provides the proper supply voltages necessary for operation of the WJ-8710A.

The assembly receives a DC input in the range of 11 to 16 Vdc. The source voltage is first passed through a low-pass filter. The output of the filter feeds two DC-DC Converter devices.

The five volt DC-DC Converter produces the +5 Vdc supply. This is low-pass filtered and fed to the power connector A1P1.

The other DC-DC Converter device produces the +12 and -12 Vdc supplies. These are low-pass filtered and fed to the power connector, A1P1.

SECTION VII

MAINTENANCE

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SECTION VII

MAINTENANCE

7.1 GENERAL

The WJ-8710A Digital HF Receiver has been designed to operate for extended periods of time with a minimum of routine maintenance. Cleaning, inspection and performance tests should be performed at regular intervals, consistent with the facility's normal scheduling and after repairs have been made.

7.2 PREVENTIVE MAINTENANCE PROCEDURES

Preventive maintenance procedures for the receiver consist of both cleaning and scheduled preventive maintenance procedures.

7.2.1 CLEANING AND LUBRICATION

The receiver should be kept free of dust, moisture, grease and other foreign matter to ensure trouble-free operation. Use low pressure air, if available, to remove accumulated dust from the interior of the receiver. A clean, dry cloth or soft bristled brush may also be used for this purpose. No lubrication is required.

7.2.2 SCHEDULED PREVENTIVE MAINTENANCE PROCEDURES

Component A2U5 is a plug-in chip that furnishes battery power (V Batt) for the Digital Control PC Assembly (A2). U5 should be changed every eight years, or more frequently if local preventive maintenance procedures dictate. Refer to **paragraph 7.7.9** for RAM/Battery (A2U5) removal and replacement procedures.

7.3 INSPECTION FOR DAMAGE AND WEAR

Many existing or potential troubles can be detected by making a thorough visual inspection of the unit. For this reason, as a first step in troubleshooting, a complete visual inspection should be made whenever the unit is inoperative. Inspect mechanical parts such as pin connectors and interconnecting cables for looseness, wear and other signs of deterioration. The subassemblies should be checked to assure that they are properly secured to the chassis and making good electrical contact. Electronic components that show signs of deterioration, such as overheating, should be inspected and a thorough investigation of the associated circuitry should be made to verify proper operation. Often, damage due to heat is a result of other, less apparent problems in the circuit.

7.4 TEST EQUIPMENT REQUIRED

Procedures for testing the WJ-8710A Receiver have been developed for performance using a minimum of common test equipment. The test equipment listed in **Table 7-1**, or equivalents, are required to perform the troubleshooting procedures and performance tests described in this section.

7.5 TROUBLESHOOTING AND FAULT ISOLATION

The test procedures that are provided in this section verify proper receiver operation and assist in fault isolation to a malfunctioning subassembly. They have been developed to set known laboratory conditions that eliminate external conditions as a possible cause of the malfunction. Use performance tests in **paragraph 7.6**, and the circuit descriptions in **Section VI** to assist in fault isolation. The loss of stored parameters between receiver power-ups may be the result of the failure of the RAM/Battery chip (A2U5). Refer to **paragraph 7.7.9** for RAM/Battery (A2U5) removal and replacement procedures.

7.6 WJ-8710A DIGITAL HF RECEIVER PERFORMANCE TESTS

The performance tests that follow are designed to verify proper operation of the WJ-8710A Receiver, and each of its operational modules. In performance of the tests, the receiver may be controlled by an external controlling computer, connected to the Rear Panel RS-232 connector, or the TF-30387 Test Fixture, connected to the front panel Control Interface connector. Each procedure provides sufficient set up information to accommodate either control device.

Table 7-1. Required Test Equipment

Equipment	Recommended Type	Requirement
Regulated Power Supply	HP-6266B	Power Supply and Measurement
Signal Generator (Qty 2)	Marconi 2031	Frequency Range -10 kHz to 2.7 GHz
Frequency Counter	Fluke 1953A	Frequency Range to 100 MHz
RF Millivoltmeter	Boonton 92B	dB Scale Referenced to 50 Ohm Load
RF Probe	Boonton 91-12F	
“T” Adapter	Boonton 91-14A	
50 Ohm Termination	Boonton 91-15A	
AC Voltmeter	HP-400EL	dB Scale Referenced to 600 Ohm Load
Distortion Analyzer	HP-334A	Harmonic Distortion Measurement
Digital Voltmeter	Fluke 8001A	AC/DC Voltage Measurement
Oscilloscope	Tektronix 2236	100 MHz Frequency Response
Control Test Fixture	TF-30387 (Signia-IDT, Inc.)	WJ-8711 Front Panel Control (Optional)
Assembly Test Cable	TF-30388 WI (Signia-IDT, Inc.)	Assembly Interface Testing
Control Computer	IBM PC Compatible	RS-232 Compatible
Headphone Adapter	Radio Shack P/N 274-366	1/4 inch to 1/8 inch adapter
Headphones	Telex PH-6 or equivalent	600 Ohm Stereo, 1/4 inch Tip-Ring Plug

7.6.1 POWER CONSUMPTION

1. Connect the WJ-8710A Receiver and test equipment as illustrated in **Figure 7-1**.

2. Adjust the Power Supply to the voltage at which the receiver is to be operated (nominal +12 Vdc).

3. Set the Signal Generator to produce a 1.0000 MHz output at a level of -90 dBm. Set the generator modulation for 400 Hz AM, 50% modulation.

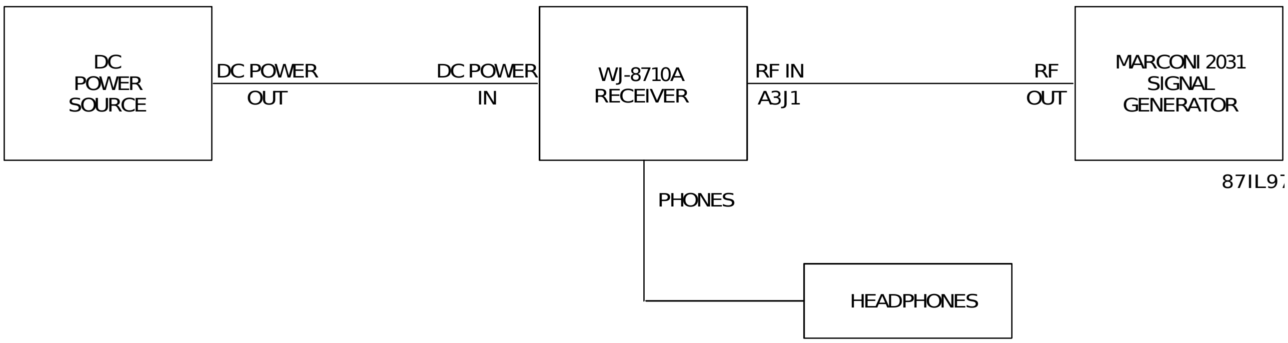

Figure 7-1. Power Consumption Performance Test Equipment Connection

4. Apply power to the receiver and set the receiver parameters as follows:

Tuned Frequency:	1.000000 MHz	FRQ 1 <Return>
Detection Mode:	AM	DET 1 <Return>
IF Bandwidth:	6.0 kHz	BWS 4 <Return>
Gain Control:	AGC Fast	AGC 2 <Return>
Squelch:	Off	SQL 136 <Return>

5. Adjust the PHONES LEVEL control for a clear 400 Hz audio tone in the headphones.

6. Verify that the power consumption level does not exceed 20 Watts by multiplying the displayed current (A) by 12 Vdc (e.g., 12 V X 1.54A = 18W).

7. Slowly increase and decrease the voltage of the Power Source from 11 to 16 Vdc while observing the power consumption level. Verify that the power consumption throughout the range at 20 Watts or less and a clear audio tone remains present in the headphones.

NOTE

The Power Supply can be used to power the receiver in all of the following tests.

7.6.2 REFERENCE FREQUENCY TIMEBASE ACCURACY

1. Connect the WJ-8710A Receiver and test equipment as illustrated in **Figure 7-2**. Apply power to the receiver and test equipment and allow a warm-up period of at least 30 minutes before proceeding with the timebase testing.

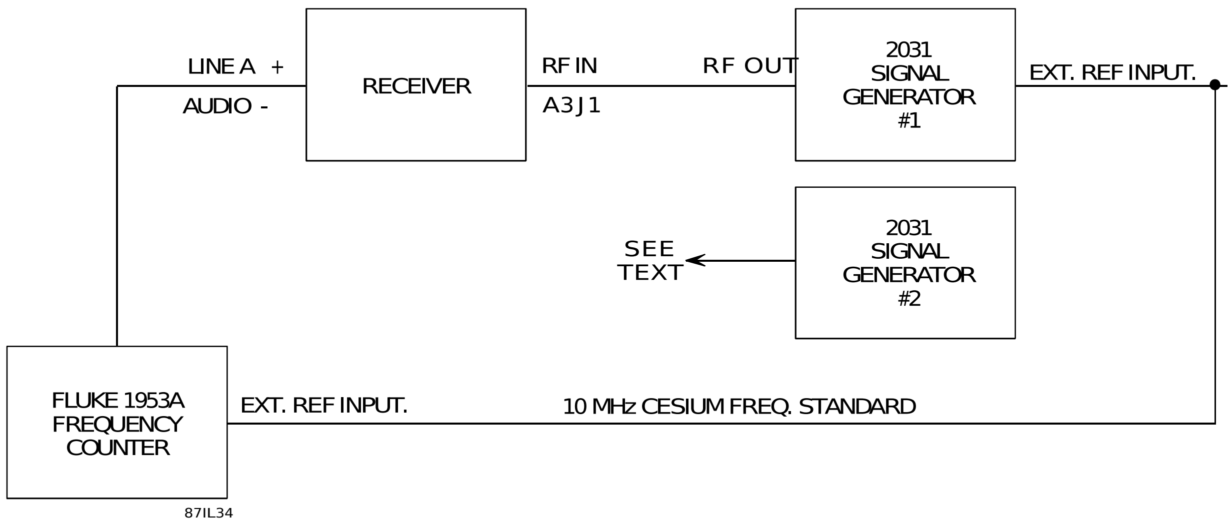

Figure 7-2. Reference Frequency Timebase Accuracy Performance Test Equipment Connection

2. Set Signal Generator #1 to produce a 30.0000 MHz CW signal at an output level of -80 dBm.

3. Set the WJ-8710A Receiver as follows:

Tuned Frequency:	30.000000 MHz	FRQ 30 <Return>
Detection Mode:	CW	DET 3 <Return>
BFO Offset:	+1.00 kHz	BFO 1000 <Return>
IF Bandwidth:	6.0 kHz	BWS 4 <Return>
Gain Control:	AGC Slow	AGC 1 <Return>
Squelch:	Off	SQL 136 <Return>

4. Set the Frequency Counter for 0.1 Hz resolution.

5. Note the frequency displayed on the Frequency Counter to determine the accuracy of the receiver timebase. The displayed frequency should fall in the range between: 994.1 and 1005.9 Hz (1.0 kHz ± 5.9 Hz) for a .2 ppm reference, 980.0 and 1020.0 Hz (1.0 kHz ± 20.0 Hz) for a .7 ppm reference.

6. Set Signal Generator #2 to produce a 10.0000 MHz CW signal at an output level of 0 dBm. Connect the Signal Generator output to the EXT. REF. connector at the receiver front panel (A3J3).

7. Note the frequency displayed on the frequency counter. This frequency should be approximately 1000 Hz, depending on the accuracy of the frequency setting in step 2.

8. While observing the frequency counter display, slowly increase and decrease the frequency of generator #2. Verify that the frequency displayed on the frequency counter changes with changes in the generator frequency, indicating that the receiver timebase is locked to the eternal reference.

NOTE

The magnitude of change on the frequency counter does not match the generator changes due to frequency scaling within the receiver.

7.6.3 FINE TUNING ACCURACY

1. Connect the WJ-8710A Receiver and test equipment as illustrated in **Figure 7-3**.

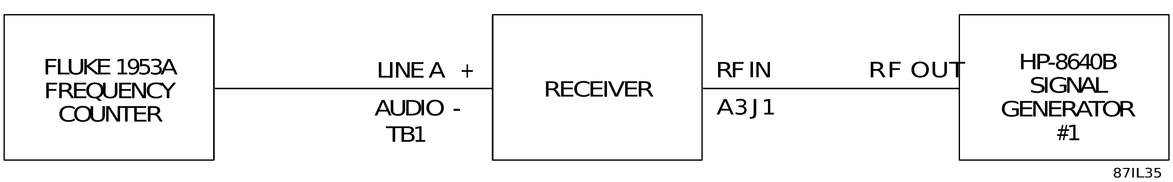

Figure 7-3. Fine Tuning Accuracy Performance Test Equipment Connection

2. Set the signal generator to produce a 10.000000 MHz CW signal at an output level of -40 dBm.

3. Set the WJ-8710A Receiver as follows:

Tuned Frequency:	10.000000 MHz	FRQ 10 <Return>
Detection Mode:	CW	DET 3 <Return>
BFO Offset:	+1.00 kHz	BFO 1000 <Return>
IF Bandwidth:	16.0 kHz	BWS 5 <Return>
Gain Control:	AGC Slow	AGC 1 <Return>
Squelch:	Off	SQL 136 <Return>

4. Set the frequency counter for 1.0 Hz resolution.

5. Note the frequency displayed on the frequency counter as a reference for the tuning accuracy tests. The displayed frequency is the difference between the receiver and the signal generator frequencies, plus the 1000 Hz BFO offset.

6. While observing the frequency counter display, slowly increase the receiver tuned frequency in 1 Hz, 10 Hz, 100 Hz, and 1 kHz steps. Verify that the magnitude of change on the frequency counter display tracks with the receiver tuned frequency changes, maintaining a frequency that is 1 kHz greater than the difference between the signal generator and receiver frequencies.

NOTE

Maintain tuned frequencies between 10.000000 and 10.008000 MHz to avoid exceeding the 16.0 kHz IF bandwidth limitations.

7.6.4 SIGNAL STRENGTH ACCURACY

1. Connect the Marconi 2031 Signal Generator to the RF Input of the WJ-8710A Receiver (A3J1).

2. Set the signal generator to produce a 15.0000 MHz CW signal at an output level of -100 dBm.

3. Connect the digital voltmeter between the RSSI pin and ground on the rear panel terminal bus (TB1). Set the digital voltmeter function to DC Voltage, 10 V range.

4. Set the WJ-8710A Receiver as follows:

Tuned Frequency:	15.000000 MHz	FRQ 15 <Return>
Detection Mode:	CW	DET 3 <Return>
BFO Offset:	+0.00 kHz	BFO 0 <Return>
IF Bandwidth:	6.0 kHz	BWS 4 <Return>
Gain Control:	AGC Slow	AGC 1 <Return>
Squelch:	Off	SQL 136 <Return>

5. Slowly increase the signal generator output level to 0 dBm, in 10 dB increments. At each increment, note the DC voltage displayed on the digital voltmeter and verify the receiver signal level using the "SGV?" query. If the TF-30387 Control Test Fixture is used, observe the signal level on the signal strength meter.

6. Verify that the receiver signal strength indication remains within ±10 dB of the signal generator output level. The DC voltage present at the RSSI output should range from approximately +1.0 V (-100 dBm) to +4.6 V (0 dBm). For each 10 dB increase of input level, the RSSI level should increase by approximately +.35 V.

7.6.5 WJ-8710A SENSITIVITY PERFORMANCE TEST

1. Connect the WJ-8710A Receiver and test equipment as illustrated in **Figure 7-4.**

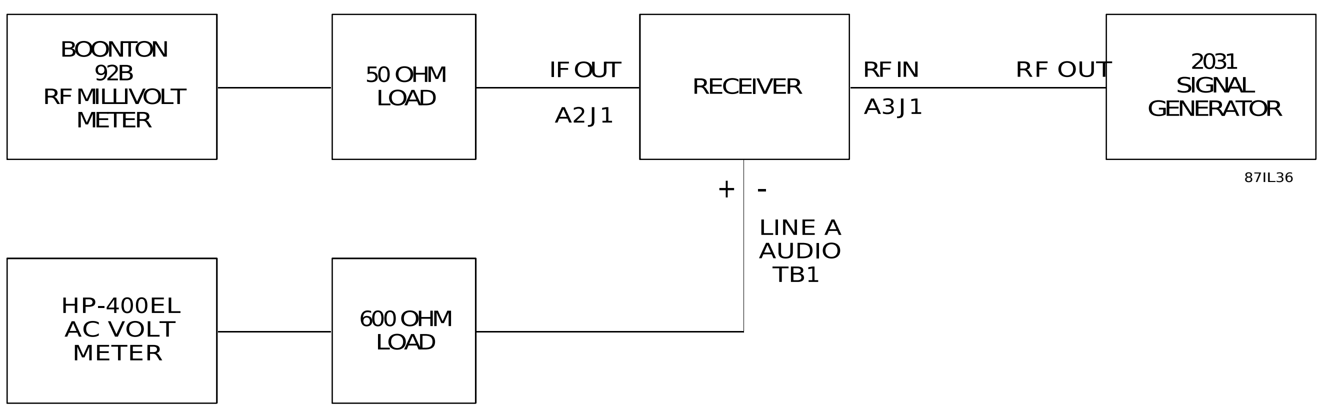

Figure 7-4. Receiver Sensitivity Performance Test Equipment Connection

2. Set the WJ-8710A Receiver as follows:

Tuned Frequency:	0.500000 MHz	FRQ .5 <Return>
Detection Mode:	CW	DET 3 <Return>
BFO Offset:	+1000 Hz	BFO 1000 <Return>
IF Bandwidth:	See **Table 7-2**	
Gain Control:	Manual	AGC 0 <Return>
Gain Setting:	Mid-Range 060	RFG 60 <Return>
RF Input Path	Preamplified	RFP 3 <Return>
Squelch:	Off	SQL 136 <Return>

3. Set the receiver tuned frequency to 0.500000 MHz [FRQ .5 <Return>] and set the signal generator to produce a .5000 MHz CW output at a level of -116 dBm.

4. Set the receiver IF bandwidth and the corresponding signal generator output level to each of the settings listed in **Table 7-2.** For each of the listed settings, perform the test described in steps 5 through 8.

Table 7-2. Sensitivity Performance Test Parameters

IF BW (kHz	COMMAND	SIG. GEN OUTPUT LEVEL (dBm)	AM MODULATION	FM MOD. FRQ / DEV.
0.30	BWS 1 <Return>	-116	100 Hz / 50%	100 Hz / 90 Hz
1.00	BWS 2 <Return>	-111	400 Hz / 50%	400 Hz / 300 Hz
3.20	BWS 3 <Return>	-106	400 Hz / 50%	400 Hz / 960 Hz
6.00	BWS 4 <Return>	-103	400 Hz / 50%	400 Hz / 1800 Hz
16.0	BWS 5 <Return>	-99	400 Hz / 50%	400 Hz / 4800 Hz

5. Set the receiver RF Gain as required to produce a -20 dBm indication on the RF millivoltmeter.

6. Note the Line A audio level indicated on the AC voltmeter as the reference level for the following CW sensitivity performance test. The typical AC voltmeter indication is 0 dbm ±3 dB.

7. While observing the AC voltmeter indication, turn off the signal generator RF Output.

8. Note the AC voltmeter level with the RF signal removed. Calculate the signal-to-noise ratio by subtracting this level from the reference level noted in step 6. The difference between these two levels should be a minimum of 16 dB.

9. Tune the receiver and signal generator to 5.0000 MHz, 15.0000 MHz, and 29.9000 MHz. At each frequency, repeat the test described in steps 4 through 8.

10. Set the receiver for a .50000 MHz tuned frequency [FRQ .5 <Return>], AGC Fast [AGC 2 <Return>], and select the AM Detection Mode [DET 1 <Return>]. Set the signal generator to produce a .5000 MHz AM modulated signal.

11. Set the receiver IF bandwidth, the corresponding signal generator RF output level, and the AM modulation as listed in **Table 7-2**. For each of the listed settings, perform the test described in steps 12 through 15.

12. Note the Line A audio level indicated on the AC voltmeter as the reference level for the following AM sensitivity performance test. The typical AC voltmeter indication is +6 dBm ±3 dB.

13. While observing the AC voltmeter indication, turn the signal generator AM modulation off.

14. Note the AC voltmeter level with the AM modulation removed. Calculate the signal-to-noise ratio by subtracting this level from the reference level noted in step 12. The difference between these two levels should be a minimum of 10 dB.

15. Tune the receiver and signal generator to 5.0000 MHz, 15.0000 MHz, and 29.9000 MHz. At each frequency, repeat the test described in steps 11 through 14.

16. Set the receiver for a .50000 MHz tuned frequency [FRQ .5 <Return>], AGC Fast [AGC 2 <Return>], and select the FM Detection Mode [DET 2 <Return>]. Set the signal generator to produce a .5000 MHz FM modulated signal.

17. Set the receiver IF bandwidth, the corresponding signal generator RF output level, and the FM modulation as listed in **Table 7-2**. For each of the listed settings, perform the test described in steps 18 through 21.

18. Note the Line A audio level indicated on the AC voltmeter as the reference level for the following FM sensitivity performance test. The typical AC voltmeter indication is +0 dBm ±3 dB.

19. While observing the AC voltmeter indication, turn the signal generator FM modulation off.

20. Note the AC voltmeter level with the FM modulation removed. Calculate the signal-to-noise ratio by subtracting this level from the reference level noted in step 18. The difference between these two levels should be a minimum of 17 dB.

21. Tune the receiver and signal generator to 5.0000 MHz, 15.0000 MHz, and 29.9000 MHz. At each frequency, repeat the test described in steps 17 through 20.

22. Set the receiver for a .50000 MHz tuned frequency [FRQ .5 <Return>], Manual Gain [AGC 0 <Return>], select the ISB Detection Mode [DET 6 <Return>] and select the 3.2 kHz IF bandwidth [BWS 3 <Return>]. Set the signal generator to produce a .5010 MHz CW output signal, at a level of -113 dBm.

23. Set the receiver RF Gain as required to produce a -20 dBm indication on the RF millivoltmeter.

24. Note the Line A audio level indicated on the AC voltmeter as the reference level for the following SSB sensitivity performance test. The typical AC voltmeter indication is +0 dBm ±3 dB.

25. While observing the AC voltmeter indication, turn off the signal generator RF Output.

26. Note the AC voltmeter level with the RF signal removed. Calculate the signal-to-noise ratio by subtracting this level from the reference level noted in step 24. The difference between these two levels should be a minimum of 16 dB.

27. Temporarily remove the AC voltmeter and 600-ohm load from the Line A output of TB1 and connect them across the + and - terminals of the Line B output. Tune the signal generator to 1.0000 kHz below the receiver tuned frequency and repeat steps 23 through 26 to verify the lower sideband of the ISB outputs.

28. Reconnect the AC voltmeter and 600-ohm load across the Line A output terminals.

29. Tune the receiver and signal generator to 5.0000 MHz, 15.0000 MHz, and 29.9000 MHz. In each case, set the signal generator frequency for 1.0000 kHz above the receiver tuned frequency. At each frequency, repeat the test described in steps 23 through 27.

7.6.6 AUDIO DISTORTION PERFORMANCE TEST

1. Connect the WJ-8710A Receiver and test equipment as illustrated in **Figure 7-5**.

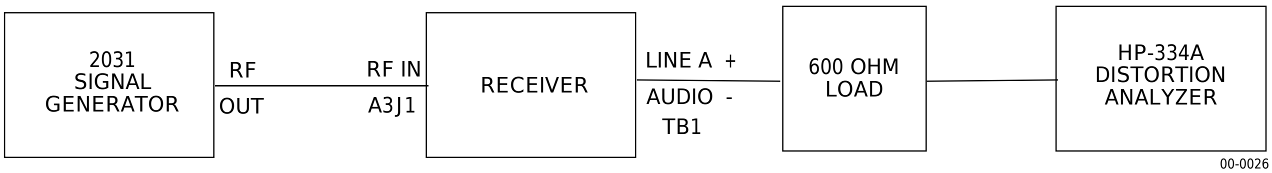

Figure 7-5. Audio Distortion Performance Test Equipment Connection

2. Set the signal generator to produce a 15.0000 MHz AM modulated signal at an output level of -50 dBm. Set the AM modulation to 400 Hz, at 30 %.

3. Preset the distortion analyzer as follows:

Mode:	Manual
Frequency Range:	X10
Function:	Voltmeter
Meter Range:	1 Volt

4. Set the WJ-8710A Receiver as follows:

Tuned Frequency:	15.000000 MHz	FRQ 15 <Return>
Detection Mode:	AM	DET 1 <Return>
IF Bandwidth:	6.0 kHz	BWS 4 <Return>
Gain Mode:	AGC Slow	AGC 1 <Return>
Gain Setting:	Mid-Range 060	RFG 60 <Return>
RF Input Path	Normal	RFP 1 <Return>
Squelch:	Off	SQL 136 <Return>

5. Verify that the detected audio level is 0 dBm ±3 dB, as indicated on the analyzer voltmeter.

NOTE

Due to a +10 dB offset on the distortion analyzer voltmeter, the +10 dB scale is used for a 0 dBm reading.

6. Reset the distortion analyzer meter range to the 3 volt scale and increase the signal generator modulation level to 50%.

7. Set the distortion analyzer function control and meter range to the SET LEVEL positions. Adjust the distortion analyzer sensitivity control for a 100% indication on the meter (an indication of "1" on the 0-1 scale).

8. Set the distortion analyzer function control to the Distortion position. Slowly adjust the distortion analyzer Frequency control for a minimum indication on the meter. Reset the meter range as required for the best meter resolution. Verify that the total harmonic distortion measured does not exceed 5%.

9. Set the receiver detection mode to ISB [DET 6 <Return>], and select the 3.2 kHz IF bandwidth [BWS 3 <Return>].

10. Reset the distortion analyzer as follows:

Mode:	Manual
Frequency Range:	X100
Function:	Voltmeter
Meter Range:	3 Volt

11. Reset the signal generator to produce a 15.0010 MHz CW signal at a -50 dBm output level (modulation off, frequency 1.0 kHz greater than the receiver tuned frequency).

12. Verify that the detected audio level indicated on the distortion analyzer voltmeter is 0 dBm ±3 dB.

13. Set the distortion analyzer function control and meter range to the SET LEVEL positions. Adjust the distortion analyzer sensitivity control for a 100% indication on the meter.

14. Set the distortion analyzer function control to the Distortion position. Slowly adjust the distortion analyzer Frequency control for a minimum indication on the meter. Reset the meter range as required for the best meter resolution. Verify that the total harmonic distortion measured does not exceed 5%.

7.6.7 SQUELCH/MUTE PERFORMANCE TEST

1. Connect the WJ-8710A Receiver and test equipment as illustrated in **Figure 7-6**.

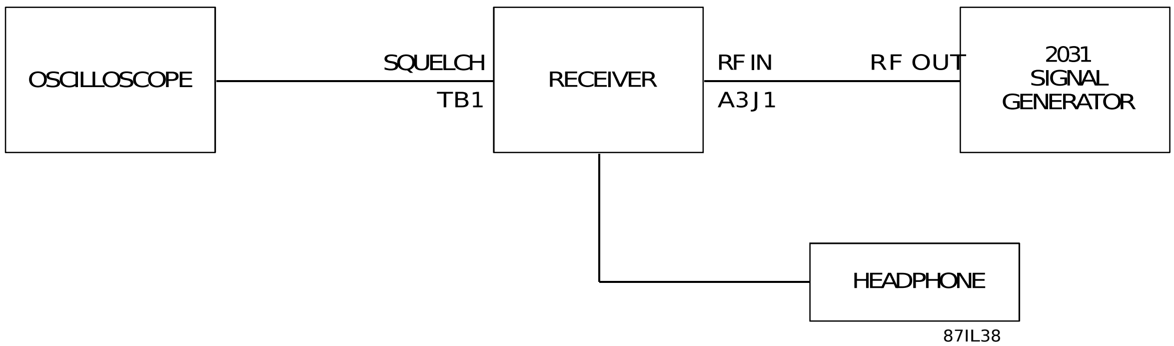

Figure 7-6. Squelch/Mute Performance Test Equipment Connection

2. Set the WJ-8710A Receiver as follows:

Tuned Frequency:	15.000000 MHz	FRQ 15 <Return>
Detection Mode:	AM	DET 1 <Return>
IF Bandwidth:	6.0 kHz	BWS 4 <Return>
Gain Mode:	AGC Fast	AGC 2 <Return>
RF Input Path	Normal	RFP 1 <Return>
Squelch:	-120	SQL 120 <Return>

3. Set the signal generator to produce a 15.0000 MHz CW output at a level of -130 dBm.

4. Observe that a steady logic "1" level (+5V) is present at the Squelch terminal of the rear panel terminal bus (TB1), as indicated on the oscilloscope.

5. While observing the oscilloscope trace, slowly increase the signal generator output level until the trace indicates a logic "0" (0V) level. Note the signal generator output level at which the squelch output switches. Verify that the signal generator output level is within ±10 dB of the receiver squelch setting.

6. Increase the receiver squelch threshold in 10 dB increments, up to 0 dBm. At each increment, increase the signal generator output level until the oscilloscope displays a logic "0" level, indicating that the squelch has turned off. Note the signal generator output level at each switchpoint. Verify that at each level tested, the signal generator output level is within ±10 dB of the receiver squelch setting.

7. Set the squelch to -100 dBm [SQL 100 <Return>] and set the signal generator to produce a 15.0000 MHz AM modulated output, at a level of -40 dBm. Set the modulation to 400 Hz, 50%.

8. Observe that a clear 400 Hz tone is present in the headphones, and the oscilloscope indicates a logic "0" at the squelch output terminal.

9. While monitoring the headphone audio and the oscilloscope display, connect a short jumper between the MUTE terminal of TB1 and ground. Observe that the audio cuts off and after a slight delay, the squelch line switches to Logic "1".

10. Remove the jumper and verify that the audio, and the squelch logic level return to the state observed in step 8.

7.6.8 RECONSTRUCTED IF OUTPUT PERFORMANCE TEST

1. Connect the WJ-8710A Receiver and test equipment as illustrated in **Figure 7-7**.

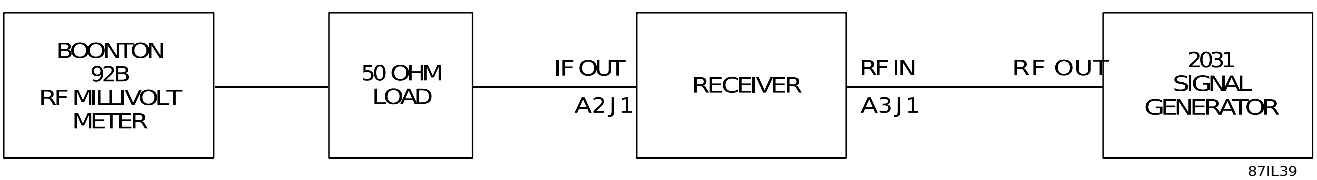

Figure 7-7. Reconstructed IF Output Performance Test Equipment Connection

2. Set the signal generator to produce a 15.0000 MHz CW output at a level of -100 dBm.

3. Set the RF millivoltmeter to the -20 dBm range.

4. Set the WJ-8710A Receiver as follows:

Tuned Frequency:	15.000000 MHz	FRQ 15 <Return>
Detection Mode:	AM	DET 1 <Return>
IF Bandwidth:	16.0 kHz	BWS 5 <Return>
Gain Control:	AGC Slow	AGC 1 <Return>
RF Input Path	Normal	RFP 1 <Return>
Squelch:	Off	SQL 136 <Return>

5. Note the IF Output signal level, as indicated on the RF millivoltmeter. Verify that the output level is -20 dBm ±3 dB (-23 to -17 dBm).

6. While observing the signal level on the RF millivoltmeter, increase the signal generator output level, in 10 dB increments, to an output level of 0 dBm. Verify that throughout the 100 dB change in the RF input signal level, the IF output level -20 dBm ±3 dB is maintained.

7. Decrease the signal generator output level to -115 dBm.

8. Set the receiver to the Manual Gain mode [AGC 0 <Return>] and set the manual gain to maximum [RFG 127 <Return>].

9. Adjust the signal generator output level to produce a -20 dBm reference level, as displayed on the RF millivoltmeter (Typical signal generator output level of -112 dBm).

10. Set the receiver manual gain to minimum [RFG 0 <Return>].

11. Increase the signal generator output level to +12 dBm and note the signal level indicated on the RF millivoltmeter. Verify that the RF millivoltmeter indication is less than the -20 dBm reference set in step 9, indicating greater than 100 dB of manual gain control.

12. Adjust the signal generator output level to -55 dBm.

13. Set the receiver manual gain to approximately mid-range [RFG 60 <Return>].

14. Increase the signal generator output level until a -20 dBm signal level reference is indicated on the RF millivoltmeter. Typically a signal generator output level of approximately -50 dBm is required.

15. While observing the RF millivoltmeter, slowly increase the signal generator frequency until the RF millivoltmeter indication decreases by 3 dB from the reference set in step 14. Note the signal generator frequency at this point.

16. Slowly decrease the signal generator frequency past the 15.0000 MHz tuned frequency and continue until the RF millivoltmeter again displays a 3 dB decrease from the reference level set in step 14. Note the signal generator frequency at this point.

17. Determine the 3 dB bandwidth of the reconstructed IF output by subtracting the value obtained in step 16 from the value obtained in step 15. The calculated bandwidth should be within ±10% of the selected IF bandwidth, as indicated in **Table 7-3**.

Table 7-3. Selected IF Bandwidth Frequency Ranges

IF BW (kHz)	CONTROL COMMAND	BW Min. (kHz)	BW Max. (kHz)
0.30	BWS 1 <Return>	0.270	0.330
1.00	BWS 2 <Return>	0.900	1.100
3.20	BWS 3 <Return>	2.880	3.502
6.00	BWS 4 <Return>	5.400	6.600
16.0	BWS 5 <Return>	14.400	17.600

18. Set the WJ-8710A Receiver to each of the IF bandwidths listed in **Table 7-3**, and repeat steps 14 through 17 for each selection.

7.6.9 RF/IF SIGNAL PATH PERFORMANCE TEST

1. Connect the WJ-8710A Receiver and test equipment as illustrated in **Figure 7-8**.

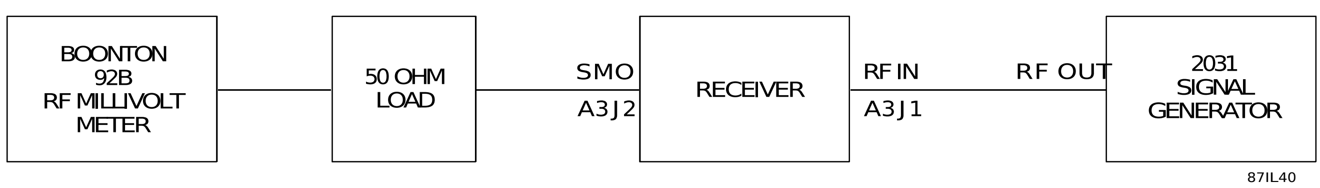

Figure 7-8. RF/IF Signal Path Performance Test Equipment Connection

2. Set the signal generator to produce a 10.0000 MHz CW output at a level of -70 dBm.

3. Set the RF millivoltmeter to the -30 dBm range.

4. Set the WJ-8710A Receiver as follows:

Tuned Frequency:	10.000000 MHz	FRQ 10 <Return>
Detection Mode:	AM	DET 1 <Return>
IF Bandwidth:	16.0 kHz	BWS 5 <Return>
Gain Control:	Manual Gain	AGC 0 <Return>
Gain Setting	Mid Range 060	RFG 60 <Return>
RF Input Path	Normal	RFP 1 <Return>
Squelch:	Off	SQL 136 <Return>

5. Adjust the signal generator output level as required to produce a -30 dBm reference level, as indicated on the RF millivoltmeter.

6. Determine the RF Assembly gain by comparing the signal generator output level with the SMO signal level indicated on the RF millivoltmeter. Typically, the signal gain ranges between 25 and 35 dB.

7. While observing the signal level on the RF millivoltmeter, slowly increase the signal generator frequency until decrease of 3 dB, from the reference set in step 5, is observed. Note the signal generator output frequency at this point.

8. Slowly decrease the signal generator frequency past the 10.0000 MHz tuned frequency and continue until the RF millivoltmeter again displays a 3dB decrease in signal level from the reference set in step 5. Note the signal generator output frequency at this point.

9. Determine the 3 dB bandwidth of the RF signal path by subtracting the frequency value obtained in step 8 from the value obtained in step 7. The calculated bandwidth should be at least 0.0300 MHz (30.0 kHz).

10. Return the signal generator output frequency to 10.0000 MHz and adjust the output level as required to obtain a -30 dBm reference level on the RF millivoltmeter.

11. Set the RF Input path of the receiver to the ATTENUATED selection. [RFP 2 <Return>]

12. Note the signal level indicated on the RF millivoltmeter. The signal level should decrease by 15±3 dB from the reference level set in step 10.

13. Set the RF millivoltmeter to the -20 dBm range and set the receiver RF Input path to the PREAMPLIFIED selection. [RFP 3 <Return>]

14. Note the signal level indicated on the RF millivoltmeter. The signal level should increase by 10±3 dB from the reference set in step 10.

7.7 CORRECTIVE MAINTENANCE PROCEDURES

Procedures for removal and replacement of faulty subassemblies and selected components are documented in the following paragraphs. Contact your supervisor or Signia-IDT, Inc. prior to breaking any factory applied inspection seals on the unit to avoid the possibility of voiding the warranty. The normal repair procedure while the unit is under warranty is to return the entire unit to the factory for warranty repair.

7.7.1 DC/DC POWER SUPPLY PC ASSEMBLY (A1) REMOVAL PROCEDURES

1. Remove the receiver main chassis from the enclosure. (Refer to **paragraph 2.2.2** and **Figures 2-2** and **2-3**).

2. Refer to **Figure 7-9**.

3. Remove plug A1P1 (2) from connector A2J5 on the Digital Control PC Assembly (1).

4. Remove plug P1 (6) from connector A1J1 on the DC/DC Power Supply PC Assembly (5).

5. Remove plug W1P2 (4) from connector A1J2 on the DC/DC Power Supply PC Assembly (5).

6. Remove ten screws (3) from the DC/DC/ Power Supply PC Assembly (5) and lift the DC/DC Power Supply PC Assembly (5) from the unit.

7.7.2 DC/DC POWER SUPPLY PC ASSEMBLY (A1) REPLACEMENT PROCEDURES

1. Refer to **Figure 7-9**.

2. Attach the DC/DC Power Supply PC Assembly (5) to the receiver chassis using ten screws (3).

3. Connect plug W1P2 (4) to connector A1J2 on the DC/DC Power Supply PC Assembly (5).

4. Connect plug P1 (6) to connector A1J1 on the DC/DC Power Supply PC Assembly (5).

5. Connect plug A1P1 (2) to connector A2J5 on the Digital Control Assembly (1).

6. Replace the receiver main chassis inside the enclosure. (Refer to **paragraph 2.2.2** and **Figures 2-2** and **2-3.)**

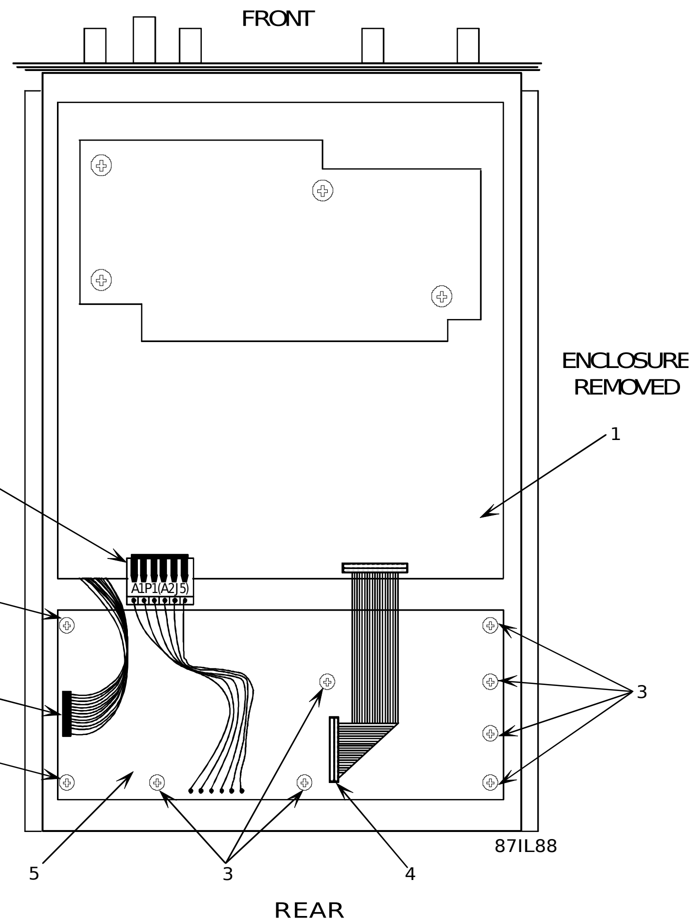

Figure 7-9. DC/DC Power Supply PC Assembly (A1) Remove and Replace Procedures

7.7.3 DIGITAL EXPANSION ASSEMBLY (A2A1) REMOVAL PROCEDURES

1. Remove the Receiver main chassis form the enclosure. (Refer to **paragraph 2.2.2** and **Figures 2-2** and **2-3**.)

2. Refer to **Figure 7-10**.

3. Remove four screws (4) from the Digital Expansion Board (2).

4. Carefully lift the board from the standoffs and Digital Control PC Assembly (1) connectors.

5. Remove the plug (4) from J1 on the Digital Expansion Board (3) if the installed option uses this connection.

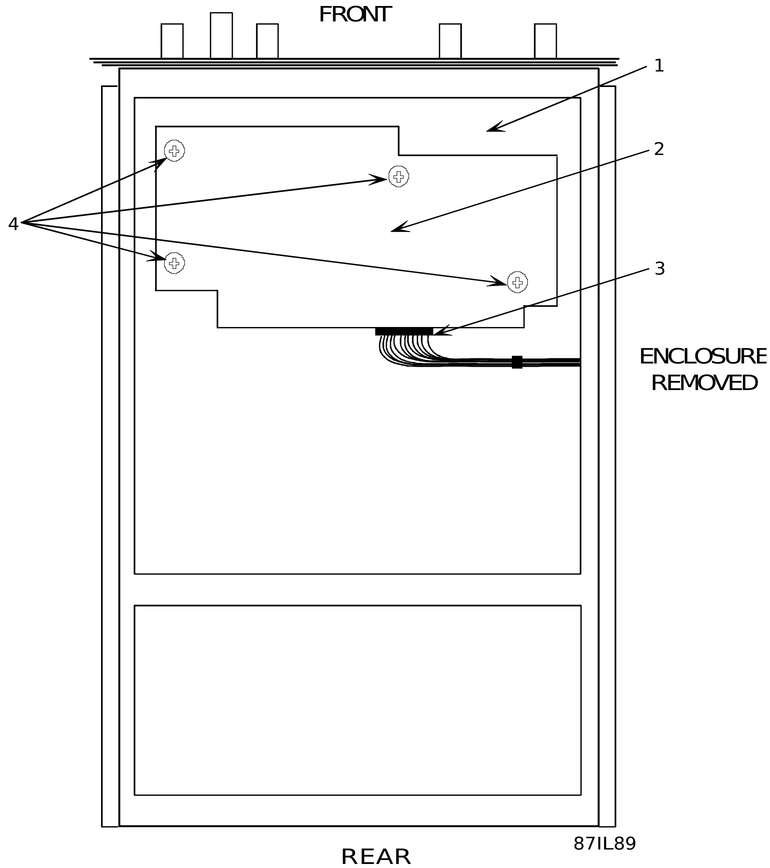

Figure 7-10. Digital Expansion Assembly (A2A1) Remove and Replace Procedures

7.7.4 DIGITAL EXPANSION ASSEMBLY (A2A1) REPLACEMENT PROCEDURES

1. Refer to **Figure 7-10**.
2. If the installed option uses the connection to J1 on the Digital Expansion Board connect the plug (3) to J1 on the Digital Expansion Board (2).
3. Carefully connect the Digital Expansion Board (2) to the Digital Control PC Assembly (1) connectors.
4. Replace four screws (4) in the Digital Expansion Board (2).
5. Replace the receiver main chassis inside the enclosure. (Refer to **paragraph 2.2.2** and **Figures 2-2** and **2-3**.)

7.7.5 DIGITAL CONTROL PC ASSEMBLY (A2) REMOVAL PROCEDURES

1. Remove the receiver main chassis from the enclosure. (Refer to **paragraph 2.2.2** and **Figures 2-2** and **2-3**.)

2. If installed, remove the Digital Expansion Assembly (A2A1). (Refer to **paragraph 7.7.3** and **Figure 7-10**.

3. Refer to **Figure 7-11** and **Figure 7-12**.

4. Remove the nut and washer from connector A2J1 (1) IF OUT on the receiver front panel (2).

5. Remove the two screwlocks (4) from the RS-232 connector on the receiver front panel (2).

6. Remove the Terminal Block (3) from TB1 on the receiver front panel (2).

7. Remove W1P1 (7) from J7 on the Digital Control PC Assembly (8).

8. Remove A3P1 (6) from J4 on the Digital Control PC Assembly (8).

9. Remove A1P1 (9) from J5 on the Digital Control PC Assembly (8).

10. Remove six screws or standoffs (5) from the Digital Control PC Assembly (8) and lift the Digital PC Control PC Assembly from the receiver.

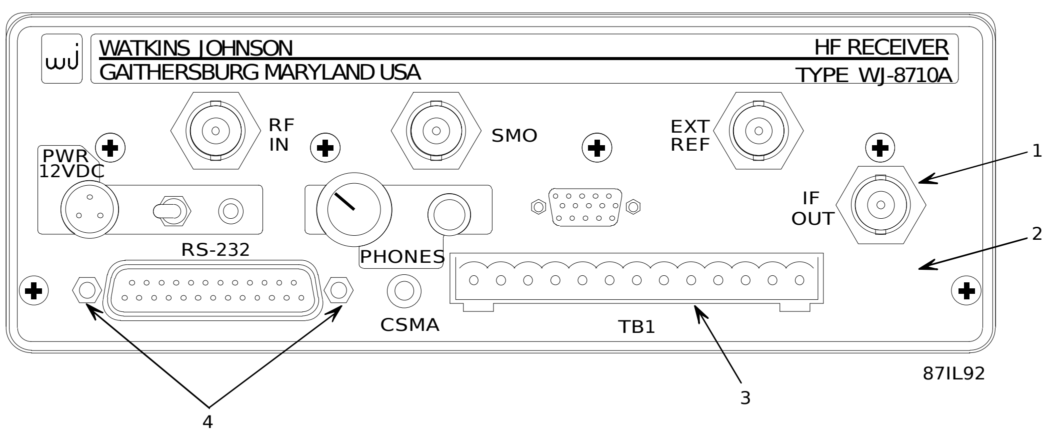

Figure 7-11. Digital Control PC Assembly (A2) Remove and Replace Procedures (Part 1)

7.7.6 DIGITAL CONTROL PC ASSEMBLY (A2) REPLACEMENT PROCEDURES

1. Refer to **Figure 7-11** and **Figure 7-12**.

2. Secure the Digital Control PC Assembly (8) to the receiver by attaching six screws or standoffs (5) securely.

3. Connect W1P1 (7) to J7 on the Digital Control PC Assembly (8).

4. Connect A1P1 (9) to J5 on the Digital Control PC Assembly (8).

5. Connect A3P1 (6) to J4 on the Digital Control PC Assembly (8).

6. Replace the washer and nut on connector A2J1 (1) IF OUT on the front panel of the receiver (2). Tighten the nut securely.

7. Replace the Terminal Block (3) on TB1 on the front panel of the receiver (2).

8. Replace the two screwlocks (4) on the front panel of the receiver (2). Tighten securely.

9. If used, replace the Digital Expansion Assembly (A2A1). (Refer to **paragraph 7.7.4** and **Figure 7-10**.)

10. Replace the receiver main chassis inside the enclosure. (Refer to **paragraph 2.2.2** and **Figures 2-2** and **2-3**.)

7.7.7 RF TUNER ASSEMBLY (A3) REMOVAL PROCEDURES

1. Remove the receiver main chassis from the enclosure. (Refer to **paragraph 2.2.2** and **Figures 2-2** and **2-3**.

2. If installed, remove the Digital Expansion Assembly (A2A1). (Refer to **paragraph 7.7.3** and **Figure 7-10**.)

3. Remove the Digital Control PC Assembly (A2). (Refer to **paragraph 7.7.5**, **Figure 7-11** and **Figure 7-12**.)

4. Refer to **Figure 7-13** and **Figure 7-14**.

5. Remove the nut and washer from connectors A3J1, A3J2, and A3J3 (1) on the front panel of the receiver (2).

6. Remove four screws (3) from the front panel of the receiver (2).

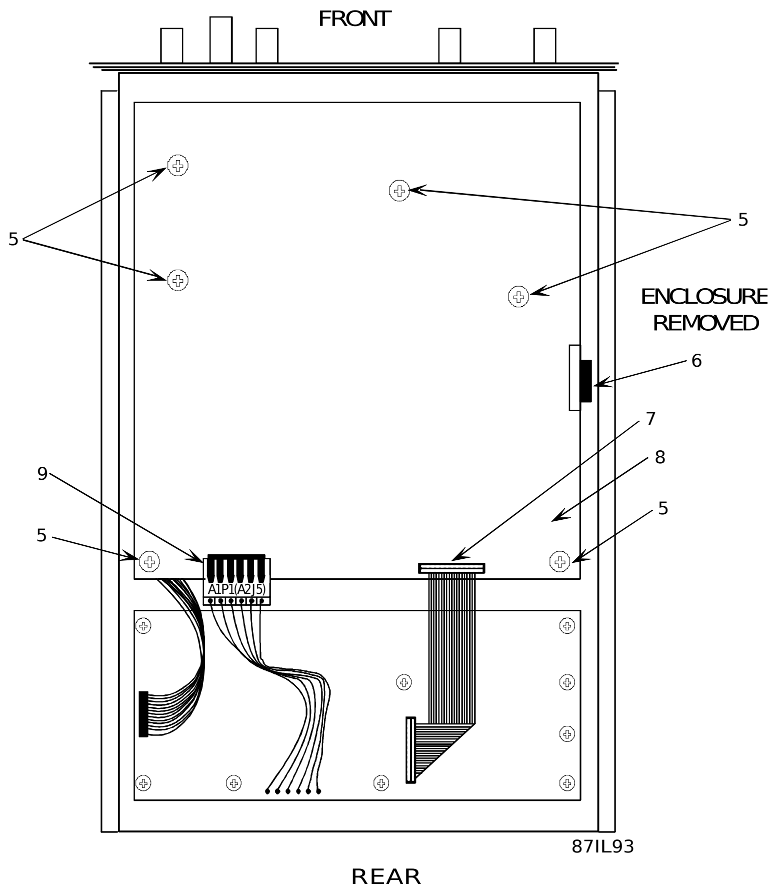

Figure 7-12. Digital Control PC Assembly (A2) Remove and Replace Procedures (Part 2)

7. Remove six screws (5) from the RF Tuner Assembly (4).

8. Lower the receiver front panel (2) from the chassis and lift the RF Tuner Assembly (4) from the unit.

7.7.8 RF TUNER ASSEMBLY (A3) REPLACEMENT PROCEDURES

1. Refer to **Figure 7-13** and **Figure 7-14**.

2. Secure the RF Tuner Assembly (4) to the receiver by attaching six screws (5) securely.

3. Place the front panel (2) in position on the unit and secure the front panel with four screws (3). Tighten screws securely.

4. Replace the nut and washer on connectors A3J1, A3J2, and A3J3 (1) on the front panel of the receiver (2).

5. Replace the Digital Control PC Assembly (A2). (Refer to **paragraph 7.7.5**, **Figure 7-12** and **Figure 7-13**.

6. If used, replace the Digital Expansion Assembly (A2A1). Refer to **paragraph 7.7.3** and **Figure 7-11**.)

7. Replace the receiver main chassis inside the enclosure. (Refer to **paragraph 2.2.2** and **Figures 2-2** and **2-3**.)

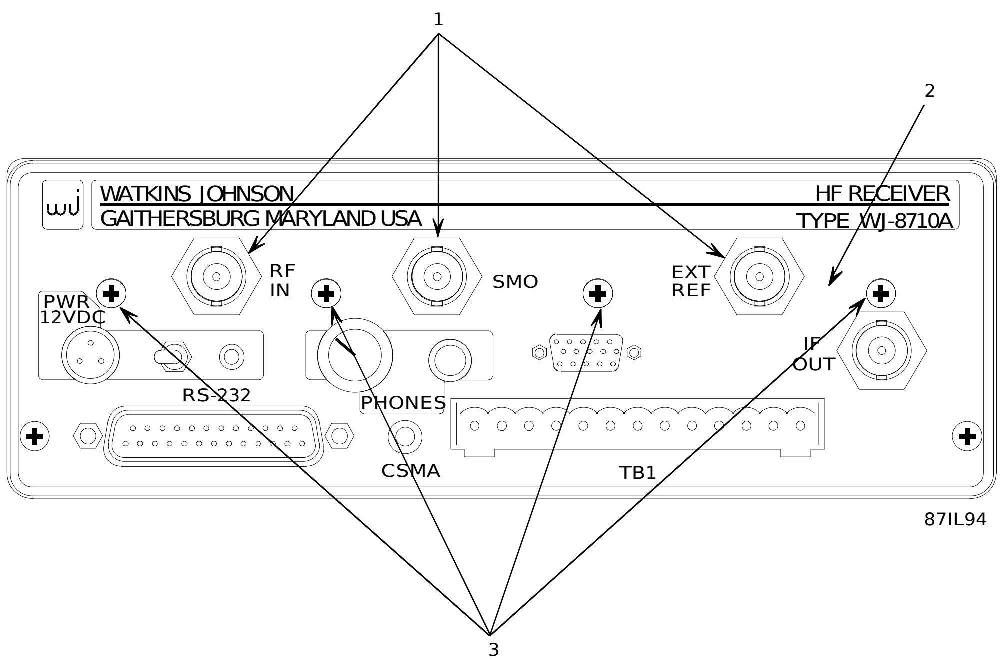

Figure 7-13. RF Tuner Assembly (A3) Remove and Replace Procedures (Part 1)

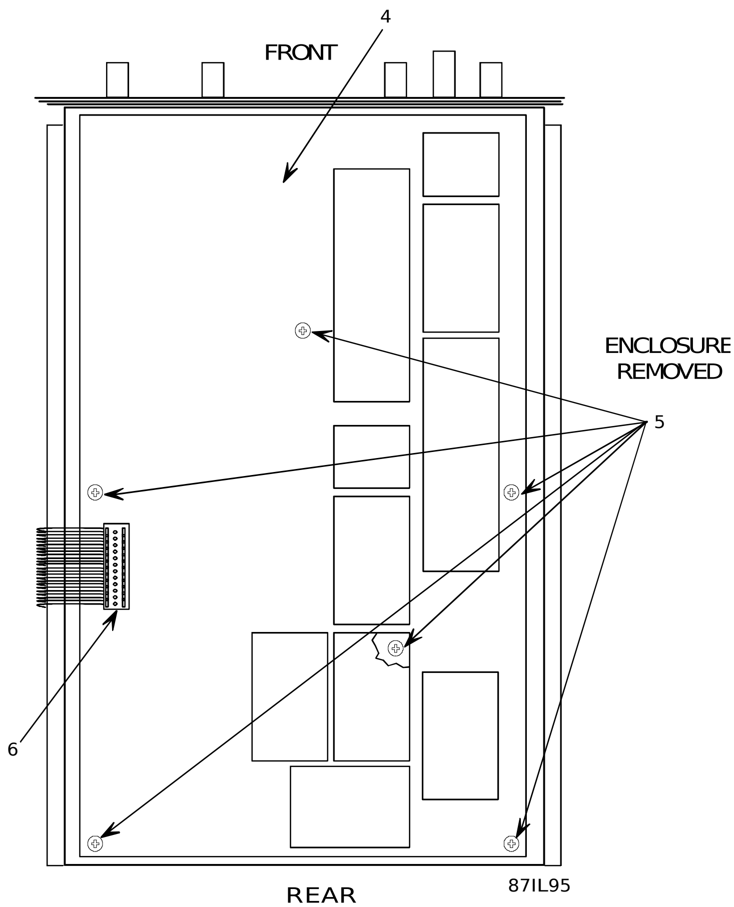

Figure 7-14. RF Tuner Assembly (A3) Remove and Replace Procedures (Part 2)

7.7.9 RAM/BATTERY (A2U5) REMOVAL/REPLACEMENT PROCEDURES

Component A2U5 is a plug-in chip that furnishes battery power (V Batt) for the Digital Control PC Assembly (A2). U5 may require replacement as a result of failure of the battery, failure of the other functions of the chip, or as a result of preventive maintenance activities designed to periodically replace the battery.

Refer to **Figure 7-15** for the approximate location of U5 on the Digital Control PC Assembly. If your receiver contains a Digital Expansion Assembly (Options) Board A2A1, the Digital Expansion Assembly (Options) A2A1 must be removed for access to the A2U5 component. (**Note:** Observe proper Electro Static Discharge (ESD) procedures when removing and replacing A2U5.)

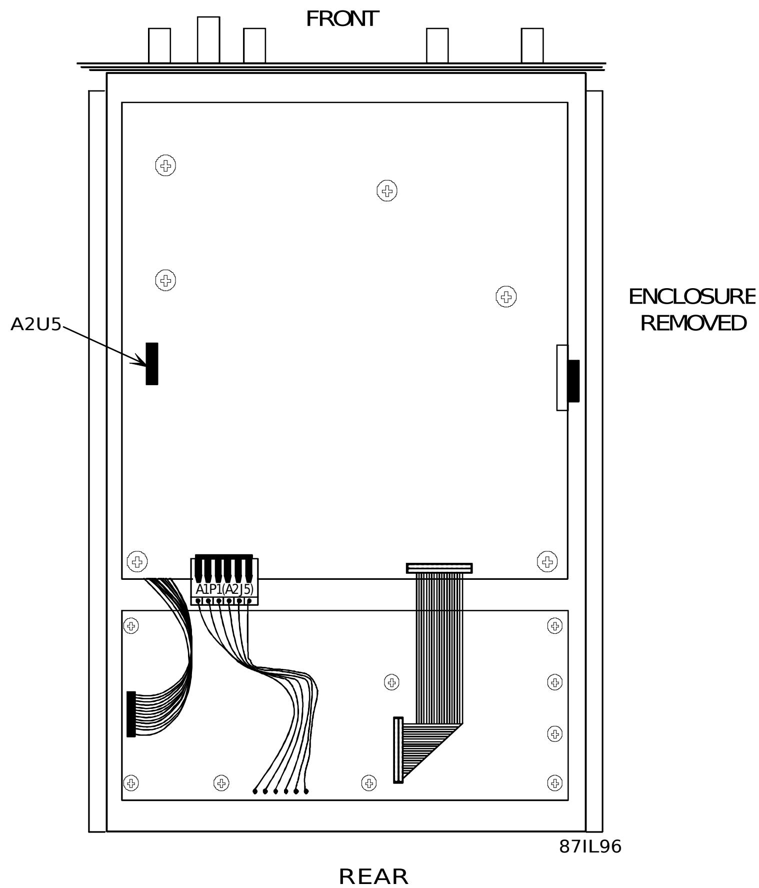

Figure 7-15. RAM/BATTERY (U5) Removal and Replacement Procedures

SECTION VIII

REPLACEMENT PARTS LIST

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SECTION VIII

REPLACEMENT PARTS LIST

8.1 UNIT NUMBERING METHOD

The method of numbering used throughout the unit is assigning reference designations (electrical symbol numbers) to identify: assemblies, subassemblies, modules within a subassembly, and discrete components. An example of the unit numbering method used is as follows:

Subassembly Designation A1	R1 Class and No. of Item
Identify from right to left as:	First (1) resistor (R) of first (1) subassembly (A)

On the main chassis schematic, components which are an integral part of the main chassis have no subassembly designations.

8.2 REFERENCE DESIGNATION PREFIX

The use of partial reference designations are used on the equipment and on the manual illustrations. This partial reference designation consists of the component type letter(s) and the identifying component number. The complete reference designation may be obtained by placing the proper prefix before the partial reference designation. Reference designation prefixes are included on the drawings and illustrations in the figure titles (in parenthesis).

8.3 PROVISIONING NOTE - INCONSISTENCIES IN PART NUMBERING CONVENTIONS

The internal computer applications at Signia-IDT, Inc. have undergone upgrades to better serve our customers. With this upgrade came alterations to the numbering scheme for parts reporting to an end item. Due to these alterations, minor inconsistencies may exist between identifying parts numbers found on drawings, piece parts, or other documentation. No form fit and function specifications have been altered due to this change in the numbering scheme.

The inconsistencies take two forms. New part number conventions mandate the use of three-digit suffixes for part numbers used within computer applications. Part numbers having single-digit suffixes have been altered by the addition of leading zeroes. Therefore, a piece part with an identifying number having a suffix of "-2" may be represented in a computer-generated document with a part number having a suffix of "-002". Also the new part numbering convention requires that the base portion of a part number be made up of six digits. Part numbers with base portions with less than six digits are expressed with leading zeroes to meet this requirement. Accordingly, a part number having a base of "34456" may appear as "034456". If you have questions or concerns regarding the configuration identification of piece parts, contact the plant for additional information at 1-800-954-3577.

8.4 LIST OF MANUFACTURERS

Mfr. Code	Name and Address	Mfr Code	Name and Address
0B0A9	Dallas Semiconductor Corp. 4350 Beltwood Pky S Dallas, TX 75244	14778	Renco Electronics Incorporated 60 Jefryn Blvd., E. Deer Park, NY 11729
00779	AMP, Inc. P.O. Box 3608 Harrisburg, PA 17150	15542	Mini-Circuits Laboratories 2625 E. 14th Street Brooklyn, NY 11235
01295	Texas Instruments, Inc. 13500 No. Central Express Way Dallas, TX 75231	17856	Siliconix Incorporated 2201 Laurelwood Road Santa Clara, CA 95050
04713	Motorola, Inc. 5005 East McDowell Road Phoenix, AZ 85008	18324	Signetics Corporation 4130 So. Market Court Sacramento, CA 95834
04713	Motorola, Inc. Semiconductor Products Sector 5005 E. McDowell Rd. Phoenix, AZ 85008-4229	2P953	LEMO USA, Inc. 335 Tesconi Circle P.O. Box 11006 Santa Rosa, CA 95406
06665	Analog Devices 1500 Space Park Dr. Santa Clara, CA 95050	20462	Prem Magnetics Incorporated 3521 No. Chapel Hill Road McHenry, IL 60050
06665	Precision Monolithics, Inc. 1500 Space Park Drive Santa Clara, CA 95050	22526	Dupont Electronics Department Route 83 New Cumberland, PA 17070
09021	Airco Electronics Bradford, PA 17055	24355	Analog Devices Incorporated Route 1, Industrial Park P.O. Box 280 Norwood, MA 02062
12697	Clarostat Mfg. Co., Inc. Lower Washington Street Dover, NH 03820	25088	Siemens America Incorporated 186 Wood Avenue So. Iselin, NJ 08830
14632	Signia-IDT, Inc. 700 Quince Orchard Road Gaithersburg, MD 20878	26742	Methode Electronics, Inc. 7447 W. Wilson Avenue Chicago, IL 60658-4548

Mfr. Code	Name and Address
27014	National Semi-Conductor Corp. 2950 San Ysidro Way Santa Clara, CA 95051
27264	Molex Incorporated 2222 Welington Court Lisle, IL 60532
28480	Hewlett-Packard Company 1501 Page Mill Road Palo Alto, CA 94304
30149	Standard Crystal Corporation 9940 E. Baldwin Place El Monte, CA 91731
34371	Harris Corp. Semiconductor Sector 200 Palm Bay Blvd. P.O. Box 883 Melbourne, FL 32902-0883
51406	Murata Erie North America, Inc. 1148 Franklin Road, S.E. Marietta, GA 30067
52648	Plessey Semiconductors 1641 Kaiser Avenue Irvine, CA 92714
54473	Panasonic Industrial Company One Panasonic Way P.O. Box 1501 Secaucus, NJ 07094
54583	TDK Electronics Corporation 12 Harbor Park Drive Port Washington, NJ 11550
55322	Samtec Incorporated 810 Progress Boulevard P.O. Box 1147 New Albany, IN 47150

Mfr Code	Name and Address
58982	Precision Connector Designs, Incorporated Centennial Park 2 Technology Dr. Peabody, MA 01960
61271	Fujitsu Microelectronics, Inc. 2985 Kifer Road Santa Clara, CA 95051-0802
61638	Advanced Interconnections Corporation 5 Division Street West Warwick, RI 02818-3842
62786	Hitachi America, LTD. 1800 Bering Drive San Jose, CA 95122
6Y440	Micron Semiconductor, Inc. 2805 E. Columbia Rd. Boise, ID 83706-9698
7J069	TDK Corp. of America 4015 W. Vincennes Rd. Indianapolis, IN 46268-3008
80294	Bourns Incorporated 6135 Magnolia Avenue Riverside, CA 92506
9AA37	JST Corporation 1200 Business Center Drive Mt. Prospect, IL 60056
91802	Industrial Devices, Inc. 260 Railroad Avenue Hackensack, NJ 07601
95146	Alco Electronics Products, Inc. 1551 Osgood Street North Andover, MA 01845
99800	Delivan Electronics Div. 270 Quaker Road East Aurora, NY 14052-2114

8.5 PARTS LIST

The following parts lists contain all the electrical components used in the unit, along with mechanical parts which may be subject to unusual wear or damage. When ordering replacement parts from Signia-IDT, Inc., specify the unit type, the serial number, and the option configuration. Also include the reference designation and the description of each item ordered. The list of manufacturers, provided in **paragraph 8.4**, and the manufacturer's part number, provided in **paragraph 8.6**, are supplied as a guide to aid the user of the equipment while in the field. The parts listed may not necessarily be identical with the parts installed in the unit. The parts listed in **paragraph 8.6** will provide for satisfactory unit operation.

Replacement parts may be obtained from any manufacturer provided that the physical characteristics and electrical parameters of the replacement item are compatible with the original part. In the case where components are defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

NOTE

As improved semiconductors become available, it is the policy of Signia-IDT, Inc. to incorporate them in proprietary products. For this reason some transistors, diodes and integrated circuits installed in the equipment may not agree with those specified in the parts lists and schematic diagrams of this manual. However, the semiconductors designated in the manual may be substituted in every case with satisfactory results.

8.6 WJ-8710A DIGITAL HF RECEIVER — MAIN CHASSIS

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
	Revision C1				
A1	DC/DC Power Supply PC Assembly	1	766027-1	14632	
A2	Digital Control PC Assembly	1	797214-1	14632	
A3	RF Tuner Assembly	1	797006-5	14632	
B1	Fan, DC Brushless	1	P003-12D-1B-3	14632	
DS1	Lamp Assembly, LED, Red	1	5111F1-5V	91802	
J1	Connector, Receptacle	1	ECG0B303CNL	2P953	
J2	Connector, Phone Jack	1	841209	14632	
P1	Connector, 14 Pin	1	87456-9	00779	
R1	Resistor, Variable	1	GA2G048F103UA	12697	
S1	Switch, Toggle	1	TTE13D-2T	95146	
W1	Cable Assembly	1	HCSD-12-D-3-01-G	55322	
1	WJ-8710 Accessor Kit	1	8710/AI	14632	

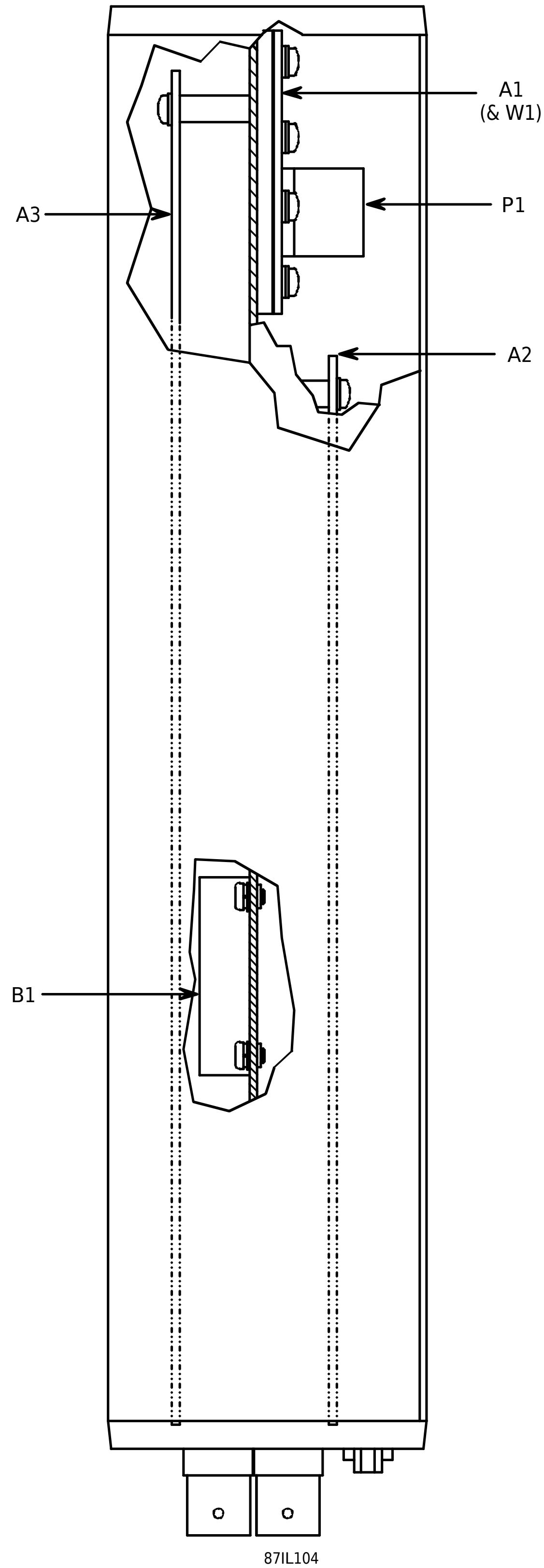

Figure 8-1. WJ-8710A Side View (Module Location)

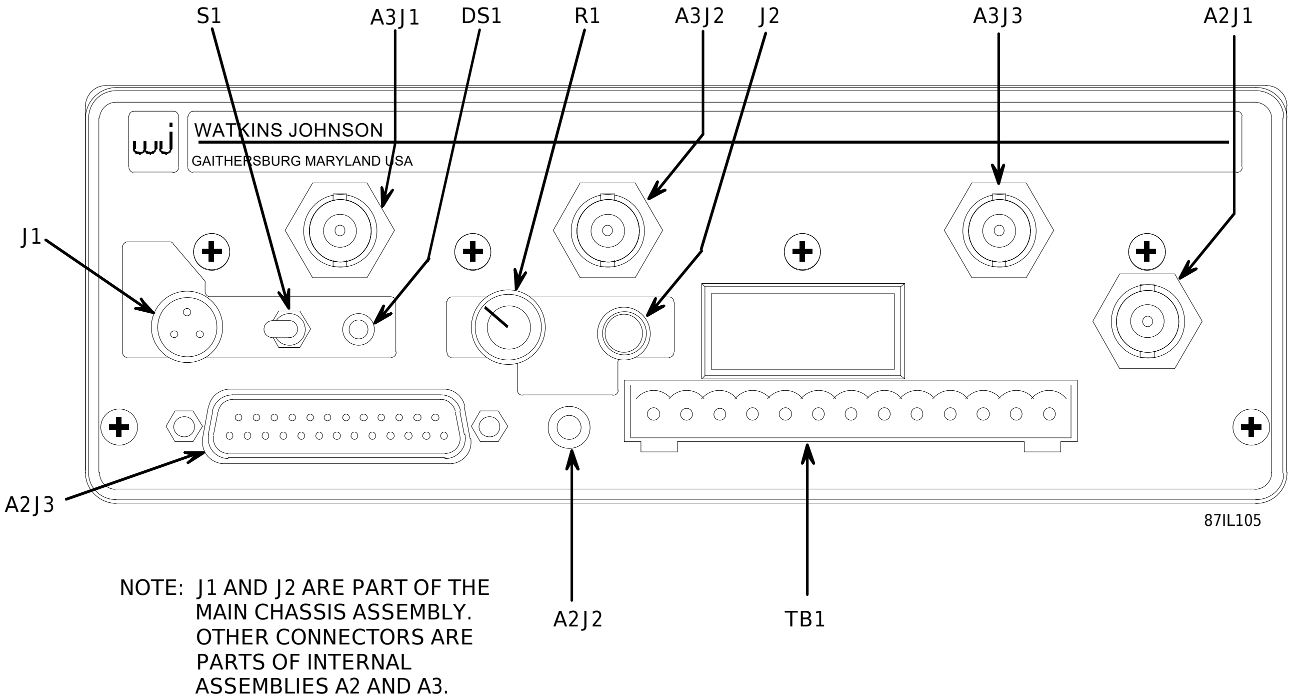

Figure 8-2. WJ-8710A Front View

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

8.6.1 TYPE 766027-1 DC/DC POWER SUPPLY PC ASSEMBLY — REF DESIG PREFIX **A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
	Revision B1				
C1	Capacitor, Ceramic: DISC .47 µF, 20%, 50 V	4	34452-1	14632	
C2	Capacitor, Electrolytic: Tantalum 15 µF, 20%, 35 V	9	199D156X0035EE4	56289	
C3 Thru C5	Same as C2				
C6 Thru C8	Same as C1				
C9	Same as C2				
C10	Capacitor, Electrolytic: Aluminum 6800 µF, 6.3 V, ±20%	1	ECE-B0JGE682	54473	
C11 Thru C14	Same as C2				
CR1	Diode Rectifier 400 PRV, 1.0 AMP	1	1N4004	80131	
E1	Terminal	6	42658-3	00779	
F1	Fuse 3 AMP	1	273003	75915	
J1	Connector, 14 Pin	1	65610-214	22526	
J2	Connector 24-Pin	1	79223-624	22526	
L1	Choke, Filter, 150 µH	2	20681-331		
L2	Same as L1				
L3	Choke, Filter 580 µH	3	20681-332		
L4	Same as L3				
L5	Same as L3				
P1	Connector, Housing, 6 POS	1	09-50-3061	27264	
R1	Resistor, Fixed, Composition: 270 kΩ, 5%, 1/4 W	1	RCR07G274JS	81349	
R2	Resistor, Trim, Film: 500 kΩ, 10%, 1/2 W	1	62PR500K	72138	
R4	Resistor, Fixed, Composition: 10 kΩ, 5%, 1/4 W	2	RCR07G103J6	81349	
R5	Same as R4				
R6	Resistor, Fixed, Composition: 47Ω, 5%, 1/4 W	2	RCR076470JS	81349	
R7	Same as R6				
R8	Resistor, Trim, Film: 10 kΩ, 10%, 1/2 W	1	62PR10K	73138	
U1	Integrated Circuit: OP/AMPL TO-5 CASE	1	LM158H	27014	
U2	Converter, DC-DC 10 WATT 9-18 VDC INPUT 5 VDC OUTPUT	1	UWR-5/2000-D12	50721	
U3	Converter, DC-DC 20 WATT DUAL OUTPUT 9-18 VDC INPUT ±12 VDC	1	BWR-12/830-D12	50721	

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

8.6.2 **TYPE 797214-1 DIGITAL CONTROL PC ASSEMBLY** REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
	Revision A				
BT1	Not Used				
XBT1	Not Used				
BT2	Not Used				
XBT2	Not Used				
C1	Capacitor, Ceramic, .01µF, 10%	118	841415-019	14632	
C2	Same as C1				
C3	Same as C1				
C4	Capacitor, Ceramic, .033µF, 10%	17	841415-022	14632	
C5 Thru C10	Same as C4				
C11	Same as C1				
C12	Capacitor, Ceramic, .1µF, 10%, >/=50VDC	8	841250-25	14632	
C13	Same as C1				
C14	Capacitor, Ceramic, 75pF, ±2%	1	841416-046	14632	
C15	Capacitor, Tantalum, 3.3µF, 20%, 16V	10	841293-10	14632	
C16	Same as C12				
C17	Capacitor, Ceramic, 22pF, 5%	3	841415-003	14632	
C18	Same as C1				
C19	Same as C1				
C20	Capacitor, Ceramic, 100pF, 5%	9	841415-007	14632	
C21	Same as C20				
C22	Same as C20				
C23	Same as C20				
C24	Same as C1				
C25	Capacitor, Electrolytic, Aluminum, 470 µF, 16V	1	ECE-A1CU471	54473	
C26	Same as C1				
C27	Capacitor, Ceramic, .047µF, 10%	9	841415-023	14632	
C28	Same as C27				
C29	Same as C1				
C30	Same as C4				
C31	Same as C4				
C32	Same as C1				
C33	Same as C4				
C34	Same as C1				
C35	Same as C15				
C36	Same as C1				
C37	Same as C1				
C38	Same as C12				
C39	Same as C1				
C40	Capacitor, Tantalum, 10µF, 20%, 16V	2	841293-16	14632	

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
C41	Same as C17				
C42	Same as C17				
C43	Same as C12				
C44	Same as C1				
C45	Same as C12				
C46	Same as C40				
C47	Same as C1				
C48	Same as C12				
C49	Capacitor, Ceramic, 470pF, 5%	8	841415-011	14632	
C50	Same as C49				
C51	Same as C49				
C52	Same as C49				
C53	Same as C49				
C54	Same as C1				
C55	Same as C1				
C56	Capacitor, Ceramic, 1000pF, 10%	4	841415-013	14632	
C57	Capacitor, Ceramic, 47pF, 2%	4	841416-041	14632	
C58	Same as C1				
C59	Same as C1				
C60	Same as C1				
C61	Same as C15				
C62	Same as C15				
C63	Same as C15				
C64	Same as C1				
C65	Same as C1				
C66	Same as C1				
C67	Same as C1				
C68	Same as C1				
C69	Same as C1				
C70	Same as C1				
C71	Same as C15				
C72	Same as C56				
C73	Same as C56				
C74	Same as C49				
C75	Same as C27				
C76	Same as C27				
C77	Capacitor, Ceramic, 1500pF, 10%,	3	841415-014	14632	
C78	Same as C27				
C79	Same as C77				
C80	Same as C77				
C81	Capacitor, Ceramic, 820pF, ±2%	3	841416-071	14632	
C82	Same as C49				
C83	Same as C1				
C84	Same as C1				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A2**

C85	Same as C1				
C86	Same as C49				
C87					
Thru	Same as C1				
C95	Same as C1				
C96	Capacitor, Ceramic, 2200pF, 10%	4	841415-015	14632	
C97	Same as C57				
C98					
Thru	Same as C1				
C100					
C101	Same as C27				
C102	Same as C1				
C103	Same as C15				
C104	Same as C15				
C105	Same as C4				
C106	Capacitor, Ceramic, 220pF, 5%	1	841415-009	14632	
C107	Same as C1				
C108	Same as C27				
C109					
Thru	Same as C1				
C111					
C112	Same as C15				
C113	Capacitor, Ceramic, 330pF, 5%	1	841415-010	14632	
C114	Same as C27				
C115	Same as C57				
C116	Same as C1				
C117	Same as C1				
C118	Same as C96				
C119	Same as C1				
C120	Same as C1				
C121	Same as C15				
C122	Same as C57				
C123	Same as C4				
C124	Same as C96				
C125	Capacitor, Ceramic, 180pF, 2%	1	841416-055	14632	
C126	Capacitor, Ceramic, 470pF, 2%	1	841416-065	14632	
C127	Same as C27				
C128	Capacitor, Ceramic, 68pF, ±2%	1	841416-045	14632	
C129	Same as C1				
C130	Same as C1				
C131	Not Used				
C132					
Thru	Same as C1				
C134					

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A2**

C135	Not Used				
C136	Same as C1				
C137	Same as C1				
C138	Same as C81				
C139 Thru C141	Same as C1				
C142	Not Used				
C143	Same as C1				
C144	Same as C81				
C145 Thru C147	Same as C1				
C148	Capacitor, Ceramic, 100pF, 2%	4	841416-049	14632	
C149 Thru C151	Same as C148				
C152 Thru C154	Same as C1				
C158	Capacitor, Ceramic, 1000pF, 2%	1	841416-073	14632	
C159	Capacitor, Ceramic, 56pF, 2%	1	841416-043	14632	
C160	Same as C1				
C161	Same as C1				
C162	Capacitor, Ceramic, 1200pF, 2%	1	841416-075	14632	
C163	Capacitor, Tantalum, 68µF, 20%, 6.3V	1	841293-24	14632	
C164 Thru C170	Same as C1				
C171	Same as C56				
C172 Thru C174	Same as C1				
C175	Capacitor, Tantalum, 33µF, 20%, 16V	9	841293-22	14632	
C176	Same as C175				
C177	Same as C96				
C178	Same as C1				
C179	Same as C175				
C180	Capacitor, Tantalum, 6.8µF, 20%, 6.3V	2	841293-14	14632	
C181	Same as C180				
C182	Same as C1				
C183	Not Used				
C184	Same as C1				
C185	Same as C12				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A2**

C186	Same as C12				
C187 Thru C189	Same as C1				
C190	Not Used				
C191	Same as C1				
C192	Same as C4				
C193 Thru C197	Same as C1				
C198	Not Used				
C199	Not Used				
C200	Same as C1				
C201	Same as C1				
C202 Thru C204	Same as C175				
C205	Same as C1				
C206	Same as C20				
C207 Thru C213	Same as C1				
C214	Same as C20				
C215	Same as C20				
C216	Same as C1				
C217	Same as C20				
C218	Same as C1				
C219 Thru C221	Same as C175				
C222	Same as C1				
C223	Same as C20				
C224 Thru C228	Same as C1				
C229	Same as C4				
C230	Same as C1				
C231	Same as C1				
C232	Not Used				
C233	Same as C4				
C234	Not Used				
C235	Same as C1				
C236	Same as C4				
C237	Same as C4				

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
C238	Not Used				
C239	Not Used				
CR1	Not Used (SOT-23)				
CR2	Diode/Swpin Dual Swithcing Diode Reverse Volltage	2	MMBD7000LT1	04713	
CR3	Not Used				
CR4	Same as CR2				
CR5	Not Used				
FL1	Filter, 455 kHz Precision Ladder Type	1	CFS-455B	51406	
J1	Connector, Jack, BNC BNC Rt Ang , PCB/Panel MT W/SLDR Mt Posts	1	227677-1	00779	
J2	Phone Jack, 3.5 Dia Mini Phone Jack, RES=3OM	1	SJ360	53337	
J3	Connector, 25-Pin D-Sub RT Ang, PC MT	1	DMRSTR25RA05Cg	05574	
J4	CONN 24-Pin Term Strip Gold Flash .100CTRS	4	79223-624	22526	
J5	Connector, Header,6 Pos Pin Friction Lock .156 CTRS	1	26-48-2066	27264	
J6	Not Used				
J7 Thru J9	Same as J4				
J10	Not Used				
J11	Connector, PC,BD 3 Pin SHRD HDR	1	3-102202-4	00779	
J12	Not Used				
J13	Not Used				
J14	Connector, Header,10 Pin HDR .025SQ X.230 X.10CTR SGLD PLTD	1	TSW105-07-G-D	55322	
J15	Not Used				
J16	Not Used				
JW1	Not Used				
L1	Inductor, 10µH, Surface MT	3	RL-1500-10	14778	
L2	Same as L1				
L3	Same as L1				
L4	Inductor, 1.0µH, ±20%,@7.96MHZ QMIN-25 370MA Ferrite 1210	9	B82422-A1102-M	25088	
L5 Thru L10	Same as L4				
L11	Not Used				
L12	Inductor, 2.2µH	1	841444-009	14632	
L13	Inductor, 4.7µH	1	B82422-A1472-M	25088	
L14	Inductor, 150nH	1	841438-029	14632	
L15	Inductor, 68nH	1	841438-021	14632	
L16	Inductor, 2.7µH	1	841444-011	14632	
L17	Not Used				
L18	Inductor, 1000µH	2	NLF453232-102K	7J069	
L19	Same as L18				

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
L20	Same as L4				
L21	Same as L4				
L22	Not Used				
L23	Not Used				
Q1	Not Used				
Q2	Transistor	3	MMBT2222ALT1	04713	
Q3	Same as Q2				
Q4	Not Used				
Q5	Not Used				
Q6	Transistor	2	2N7002-LT1	17856	
Q7	Same as Q2				
Q8	Transistor	2	MMBT-3906	04713	
Q9	Same as Q6				
Q10	Transistor	2	MMBT3904LT1	04713	
Q11	Same as Q8				
Q12	Same as Q10				
R1	Resistor, Fixed, 100kΩ, 5%	110	841414-121	14632	
R2	Resistor, Fixed, 47Ω, 5%	20	841414-041	14632	
R3	Resistor, Fixed, 47kΩ, 5%	7	841414-113	14632	
R4	Same as R3				
R5	Resistor, Fixed, 100Ω, 5%	16	841414-049	14632	
R6	Same as R3				
R7	Resistor, Fixed, 10kΩ, 5%	43	841414-097	14632	
R8	Resistor, Fixed, 4.7kΩ, 5%	7	841414-089	14632	
R9	Resistor, Fixed, 2.2kΩ, 5%	8	841414-081	14632	
R10	Same as R2				
R11	Resistor, Fixed, 820Ω, 5%	1	841414-071	14632	
R12	Resistor, Fixed, 680Ω, 5%	1	841414-069	14632	
R13	Same as R5				
R14	Same as R5				
R15 Thru R17	Not Used				
R18	Resistor, Fixed, 1.0kΩ, 5%	23	841414-073	14632	
R19	Jumper .05 Ω MAX 1A MIN@70C	26	841417	14632	
R20	Same as R19				
R21	Same as R18				
R22	Same as R19				
R23	Not Used				
R24	Same as R18				
R25	Same as R19				
R26	Resistor, Fixed, 1.5kΩ, 5%	5	841414-077	14632	
R27	Same as R19				
R28	Same as R18				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
R29	Resistor, Fixed, 2.7Ω, 5%	4	841414-011	14632	
R30	Resistor, Fixed, 22kΩ, 5%	4	841414-105	14632	
R31	Same as R5				
R32	Same as R30				
R33	Same as R5				
R34	Same as R1				
R35	Same as R19				
R36	Resistor, Fixed, 2.7kΩ, 5%	2	841414-083	14632	
R37	Same as R18				
R38	Same as R19				
R39	Same as R7				
R40	Same as R7				
R41	Same as R18				
R42	Same as R7				
R43	Same as R19				
R44	Not Used				
R45	Same as R18				
R46	Same as R36				
R47	Same as R2				
R48	Same as R1				
R49	Same as R1				
R50	Resistor, Fixed, 470Ω, 5%	10	841414-065	14632	
R51	Not Used				
R52	Resistor, Fixed, 75kΩ, 5%	2	841414-118	14632	
R53	Same as R52				
R54	Same as R1				
R55	Resistor, Fixed, 33kΩ, 5%	5	841414-109	14632	
R56	Resistor, Fixed, 220kΩ, 5%	6	841414-129	14632	
R57	Same as R55				
R58	Same as R56				
R59	Resistor, Fixed, 68kΩ, 5%	4	841414-117	14632	
R60	Same as R18				
R61	Same as R1				
R62	Same as R1				
R63	Same as R50				
R64 Thru R66	Same as R1				
R67	Same as R2				
R68	Same as R56				
R69	Same as R56				
R70	Same as R2				
R71	Same as R56				
R72	Same as R56				

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
R73	Same as R2				
R74	Same as R59				
R75	Same as R18				
R76	Same as R1				
R77	Same as R1				
R78	Same as R9				
R79	Same as R1				
R80	Same as R1				
R81	Same as R18				
R82 Thru R84	Same as R1				
R85	Not Used				
R86	Same as R1				
R87	Same as R2				
R88	Same as R18				
R89	Same as R9				
R90 Thru	Same as R1				
R92	Same as R1				
R93	Same as R50				
R94	Resistor, Fixed, 18kΩ, 5 %	4	841414-103	14632	
R95	Same as R2				
R96	Same as R94				
R97	Same as R2				
R98	Same as R3				
R99	Same as R3				
R100	Same as R55				
R101	Same as R8				
R102 Thru R104	Same as R1				
R105	Not Used				
R106	Same as R9				
R107	Same as R94				
R108	Same as R9				
R109	Same as R94				
R110	Same as R18				
R111	Same as R7				
R112	Resistor, Fixed, 8.2kΩ, 5%	2	841414-095	14632	
R113	Same as R112				
R114	Same as R7				
R115	Same as R1				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A2**

R116	Not Used				
R117 Thru R119	Same as R7				
R120 Thru R123	Same as R1				
R124	Same as R2				
R125	Same as R1				
R126	Same as R18				
R127	Same as R59				
R128	Same as R7				
R129	Same as R2				
R130 Thru R132	Same as R1				
R133	Resistor, Fixed, 150kΩ, 5%	2	841414-125	14632	
R134	Same as R50				
R135	Same as R7				
R136	Same as R26				
R137	Same as R26				
R138	Same as R30				
R139	Same as R2				
R140	Same as R1				
R141	Same as R1				
R142	Same as R18				
R143	Same as R18				
R144	Same as R1				
R145	Same as R18				
R146	Same as R55				
R147	Resistor, Fixed, 150Ω, 5%	1	841414-053	14632	
R148	Resistor, Fixed, 3.3kΩ, 5%	9	841414-085	14632	
R149	Same as R1				
R150	Same as R1				
R151	Resistor, Fixed, 10Ω, 5%	5	841414-025	14632	
R152	Same as R18				
R153	Same as R18				
R154	Same as R133				
R155	Resistor, Fixed, 4.7Ω, 5%	1	841414-017	14632	
R156	Not Used				
R157 Thru R159	Same as R7				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A2**

R160	Same as R26				
R161	Same as R26				
R162	Same as R30				
R163	Same as R2				
R164	Same as R3				
R165	Same as R1				
R166	Same as R7				
R167	Same as R7				
R168	Same as R18				
R169	Resistor, Fixed, 220Ω, 5%	3	841414-057	14632	
R170	Same as R7				
R171	Same as R1				
R172	Same as R151				
R173	Same as R7				
R174	Same as R7				
R175	Not Used				
R176	Same as R29				
R177	Same as R1				
R178	Same as R7				
R179	Same as R1				
R180	Same as R2				
R181	Not Used				
R182	Not Used				
R183	Same as R2				
R184	Same as R29				
R185	Same as R7				
R186	Same as R19				
R187	Same as R2				
R188	Same as R151				
R189	Not Used				
R190	Same as R29				
R191	Same as R19				
R192	Not Used				
R193	Same as R1				
R194	Same as R1				
R195	Same as R7				
R196	Same as R7				
R197	Same as R148				
R198	Same as R148				
R199	Same as R151				
R200	Same as R18				
R201	Same as R19				
R202	Same as R148				

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
R203	Same as R148				
R204	Not Used				
R205	Same as R19				
R206	Same as R151				
R207	Same as R1				
R208	Same as R1				
R209	Same as R19				
R210	Same as R1				
R211	Same as R19				
R212	Same as R1				
R213	Not Used				
R214	Same as R19				
R215	Same as R1				
R216	Same as R19				
R217	Resistor, Fixed, 5.6kΩ, 5%	1	841414-091	14632	
R218	Same as R148				
R219	Same as R9				
R220	Same as R5				
R221	Same as R5				
R222	Same as R9				
R223	Same as R7				
R224	Same as R1				
R225	Not Used				
R226	Same as R8				
R227	Same as R3				
R228	Same as R8				
R229	Same as R1				
R230	Same as R1				
R231	Same as R19				
R232	Same as R1				
R233	Same as R1				
R234	Not Used				
R235	Same as R1				
R236	Not Used				
R237	Same as R1				
R238	Not Used				
R239	Same as R1				
R240	Same as R7				
R241	Same as R8				
R242	Same as R8				
R243	Same as R7				
R244	Same as R1				
R245	Same as R7				

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
R246	Same as R1				
R247	Resistor, Fixed, 1.0 MΩ 5%	4	841414-145	14632	
R248	Same as R2				
R249	Same as R1				
R250	Same as R7				
R251	Same as R7				
R252	Same as R2				
R253	Same as R1				
R254	Same as R1				
R255	Same as R7				
R256 Thru R261	Same as R1				
R262 Thru R264	Not Used				
R265	Same as R5				
R266 Thru R268	Same as R1				
R269	Not Used				
R270	Same as R7				
R271	Same as R19				
R272	Same as R1				
R273	Same as R7				
R274	Same as R7				
R275 Thru R277	Same as R1				
R278	Same as R7				
R279	Not Used				
R280	Same as R19				
R281	Same as R1				
R282	Same as R1				
R283	Same as R7				
R284	Not Used				
R285	Not Used				
R286	Same as R247				
R287	Not Used				
R288	Same as R1				
R289	Same as R19				
R290	Same as R1				
R291	Not Used				
R292	Same as R1				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A2**

R293	Same as R19				
R294	Same as R19				
R295	Not Used				
R296	Same as R19				
R297	Same as R55				
R298	Same as R7				
R299	Not Used				
R300	Not Used				
R301	Same as R19				
R302	Same as R5				
R303	Same as R7				
R304	Same as R1				
R305	Same as R1				
R306	Same as R18				
R307	Same as R59				
R308	Same as R7				
R309	Not Used				
R310	Same as R7				
R311	Same as R7				
R312	Same as R1				
R313	Same as R1				
R314	Same as R5				
R315	Same as R7				
R316	Same as R5				
R317	Same as R1				
R318	Same as R5				
R319	Same as R1				
R320	Same as R5				
R321	Same as R1				
R322	Same as R1				
R323	Same as R18				
R324	Same as R5				
R325	Same as R1				
R326	Same as R1				
R327	Same as R18				
R328	Same as R7				
R329	Same as R1				
R330	Same as R9				
R331	Same as R1				
R332	Same as R1				
R333	Resistor, Fixed, 6.8 kΩ, 5%	2	841414-093	14632	
R334	Same as R8				
R335	Not Used				
R336	Same as R1				

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
R337	Same as R333				
R338	Same as R148				
R339	Same as R148				
R340	Resistor, Fixed, 68Ω, 5%	2	841414-045	14632	
R341	Same as R247				
R342	Same as R247				
R343	Same as R2				
R344 Thru R359	Same as R1				
R360	Same as R7				
R361	Same as R340				
R362	Not Used				
R363	Same as R19				
R364	Not Used				
R365	Not Used				
R366	Same as R50				
R367 Thru R369	Same as R5				
R370	Same as R50				
R371	Same as R50				
R372	Same as R169				
R373	Same as R50				
R374	Same as R50				
R375	Same as R169				
R376	Same as R19				
R377	Same as R148				
R378	Same as R2				
R379	Not Used				
S1	Switch/Dip SPST Side Actuated Dip	2	ADP-08S	95146	
S2	Same as S1				
T1	Transformer CPLG Audio 600CT/500CT IMP=10%,	2	SPT-130	20462	
T2	Same as T1				
U1	Integrated Circuit, Microcontroller,Microcontroller Unit 16-BIT Timer 8 Channel 8-BIT	1	MC68GC11A0FN	04713	
XU1	Socket 52-POS PLCC .050CTRS 1.050 X .20HT Polarized Surf	1	213-052-601	26742	
U2	Integrated Circuit,TRI-State Octal D-Type Latch SOL-20 Wide Pkg	1	74HC373SOL20	02735	
U3	Integrated Circuit,Octal TRI-State B!uffer, SOL-20 Wide Pkg	4	74HC244 SOL20	04713	
U4	Integrated Circuit,Quad 2-Input NAND Gate S0-14N	1	74HC00 SO14	02735	

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
U5	Integrated Circuit, RAM,8K X 8 Nonvolatile Time Keeping RAM 120NS=AT 28-Pin	1	DS1643-120	0B0A9	
XU5	Socket, IC 28 Pin .600 Row Spacing On .100 CTRS Gold Contact	2	O-628-SGT	S5322	
U6	Integrated Circuit, CMOS,Triple Three Input OR Gate SO-14 PLSTC PKG	1	74HC4075 SO14	02735	
U7	Integrated Circuit,TRIPLE 3-Input NOR Gates	1	74HC27 SO14	02735	
U8	Integrated Circuit,3-TO-8 Line Decoder	1	74HC138 SO16	02735	
U9	Integrated Circuit, CMOS,Quad Buffer/Line Driver	2	74HC125 SO14	34371	
U10	Integrated Circuit,Triple 3-Input AND Gate	1	74F11 SO14	04713	
U11	Integrated Circuit,1-OF-8 Decoder/Demultiplexer	1	74F138 SO16	04713	
U12	EPROMProgrammed	1	842032	14632	
XU12	socket, IC 32-PIN LOW PROFILE DIP Socket .600 Row Slpace Gold	1	O-632-SGT	S5322	
U13	Integrated Circuit,16-BIT A/D Converter 20-Pin PLSTC DIP	1	DSP56ADC16S	04713	
U14	Same as U3				
U15	Integrated Circuit,Octal D Flip-Flops With Clear SOL-20 Wide Pkg	1	74HC273 SOL20		
U16	Same as U9				
U17	Same as U3				
U18	Not Used				
U19	Same as U3				
U20	Integrated Circuit,Line Driver and Receiver Monolithic 8 Pin PKS	2	SN75155D	01295	
U21	Integrated Circuit, CMOS,Hex Inverters Active Outputs	3	74AC04 SO14	04713	
U22	Amplifier Ultra-High Frequency Op. Amp Gain Bandwidth 1.	1	NE5539D	18324	
U23	Integrated Circuit,Dual D Flip-Flop With Preset and Clear	3	74HC74 SO14	04713	
U24	Integrated Circuit, CMOS,14-Stage Binary Ripple Counter	2	74HC4020 SO16	34371	
U25	Integrated Circuit, CMOS,Parallel-In/Serial-OUT 8-BIT Shift Register SO-1	1	74HC165 SO16	02735	
U26	Integrated Circuit, /INV Hex Inverter	1	74HC04 SO14	04713	
U27	Integrated Circuit,SYN Presettable Binary Counter	2	74AC161 SO16	34371	
U28	Same as U27				
U29	Same as U23				
U30	Integrated Circuit,Synchronous Binary Counter with Asynchronous Clear SO	1	74HC161 SO16	02735	
U31	Same as U23				
U32	Same as U21				
U33	Integrated Circuit, CMOS,Dual D Flip-Flop With PRESET AND CLEAR	1	74AC74CO14	02735	
U34	Voltage Regulator3 TERM NEG Volt Regulator -5V	1	MC79M05CDT	04713	

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
U35	Same as U24				
U36	Same as U21				
U37	Integrated Circuit,40 MHZ DSP Microprocessor with PLL 24-BIT 132-PIN PQF	1	DSP56002FC40	04713	
U38	Same as U20				
U39	Integrated Circuit, /SRAMCMOS,32K X 8 20NS Access Time 28PIN SOJ	6	MT5C2568DJ-20	6Y440	
U40	Same as U39				
U41	Same as U39				
U42	Integrated Circuit, /Sensing Undervoltage Sensing Rest Operation W/1V Input	1	MC34064D-5	04713	
U43	Not Used				
U44	Integrated Circuit, Differential Bus Transceiver	2	SN75176AD	01295	
U45 Thru U47	Same as U39				
U48	Integrated Circuit, Octal D Flip-Flop with RESET SOL-20 PKG	2	74HCT273 SOL20	02735	
U49	Integrated Circuit, Dual D Flip-Flop with SET and RESET	1	74HCT74 SO14	34371	
U50	Same as U48				
U51	Integrated Circuit, /CONV D/A Monolithic 8-BIT HS Current Output	2	DAC0800LCM	27014	
U52	Amplifier JFET-Input Dual OP AMP	7	MC34002D	04713	
U53	Integrated Circuit, Quad 2-Input AND Gate	1	74HC08 SO14	02735	
U54	Same as U52				
U55	Same as U51				
U56	EPROM Programmed	1	842033	14632	
XU56	Same as XU5				
U57	Same as U44				
U58	Integrated Circuit, Dual 1-OF-4 Decoder/Demultiplexer	1	74F139 SO16	04713	
U59	Integrated Circuit, /CONV D/A 16 Bit Audio D/A Converter	1	AD1851R	24355	
U60	Integrated Circuit, CMOS,Triple 2-Channel Analog Multiplexer/Demultiplexer	3	74HC4053 SO16	02735	
U61	Same as U52				
U62	Same as U60				
U63	Same as U52				
U64	Same as U52				
U65	Amplifier Single Low Noise OP AMP SO 8 PIN	3	NE5534D	18324	
U66	Same as U65				
U67	Integrated Circuit, Dynamic Range Processor Dual VCA 16-Pin DIP	1	SSM-2122P	06665	
U68	Same as U60				

REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
U69	Amplifier JFET-Input Operational Amplifier	2	MC34001D	04713	
U70	Same as U69				
U71	Same as U52				
U72	Integrated Circuit, /AMP 1.5W Audio Power AMP 14-PIN DIP	1	LM388N-1	27014	
U73	Not Used				
U74	Same as U52				
U75	Same as U65				
VR1	Not Used				
XTB1	Connector, Header,13-POS Shrouded PC MT	1	ELFH13210	58982	
Y1	Not Used				

8.6.3 TYPE 797006-1/-2/-3/-4/-5 RF TUNER PC ASSEMBLY — REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
	Revision D1				
	See Note*				
C1	Not Used				
C2	Not Used				
C3	Capacitor, Ceramic: .01 µF, 10%, 50 V	140	841415-019	14632	
C4	Same as C3				
C5	Same as C3				
C6	Not Used				
C7 Thru C10	Same as C3				
C11	Capacitor, Ceramic: 56 pF, 2%, 50 V NPO	4	841416-043	14632	
C12	Capacitor, Ceramic: .1 µF, 10% 50 VDC	80	841250-25	14632	
C13	Same as C12				
C14	Same as C12				
C15	Same as C3				
C16	Same as C12				
C17 Thru C22	Same as C3				
C23	Capacitor, Ceramic: 160 pF, 2%, 50 V NPO	2	841416-054	14632	
C24	Not Used				
C25	Capacitor, Ceramic: 8.2 pF,±.25 pF, 50 V	1	8414116-023	14632	
C26	Same as C23				
C27	Capacitor, Ceramic: 27 pF, 2%, 50 V NPO	3	841416-035	14632	
C28	Same as C11				
C29	Capacitor, Ceramic: 82 pF, ±2%, 50 V NPO	3	841416-047	14632	
C30	Not Used				
C31	Same as C3				
C32	Same as C3				
C33 Thru C37	Same as C12				
C38	Capacitor, Ceramic: 22 pF, 5%, 50 V NPO	6	841415-003	14632	
C39 Thru C41	Same as C3				
C42	Same as C38				
C43	Capacitor, Ceramic: 91 pF, ±2%, 50 V NPO	2	841416-048	14632	
C44	Capacitor, Ceramic: 33 pF, ±2%, 50 V NPO	1	841416-037	14632	
C45	Capacitor, Ceramic: 130 pF, 2%, 50 V NPO	1	841416-052	14632	

*Note: The differences between the RF Assembly versions are as follows:
- Type 797006-1 Standard, .7 PPM Stability
- Type 797006-2 8712/REF, .2 PPM Stability
- Type 797006-3 Conformal Coated, .7 PPM Stability
- Type 797006-4 Conformal Coated, .2 PPM Stability
- Type 797006-5 Standard, with covers.

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

C46	Same as C43				
C47	Capacitor, Ceramic: 100 pF, 2%, 50 V NPO	9	841416-049	14632	
C48	Capacitor, Ceramic: 1500 pF, 10%, 50 V	3	841415-014	14632	
C49	Capacitor, Ceramic: 470 pF, 5%, 50 V NPO	3	841415-011	14632	
C50	Not Used				
C51	Same as C47				
C52	Same as C3				
C53	Same as C3				
C54	Same as C12				
C55	Same as C12				
C56	Same as C3				
C57	Same as C38				
C58	Same as C3				
C59	Same as C38				
C60	Same as C3				
C61	Capacitor, Tantalum: 2.2 µF, 20%, 20 V	4	841293-09	14632	
C62	Same as C3				
C63	Capacitor, Tantalum: 3.3 µF, 20%, 16 V	13	841293-10	14632	
C64	Same as C3				
C65	Same as C3				
C66	Same as C61				
C67	Same as C3				
C68	Capacitor, Tantalum: 33 µF, 20%, 16 V	15	841293-22	14632	
C69 Thru C75	Same as C12				
C76	Same as C61				
C77	Same as C61				
C78	Capacitor, Ceramic: 1000 pF, 10%, 50 V	10	841415-013	14632	
C79	Same as C68				
C80 Thru C84	Same as C3				
C85	Capacitor, Tantalum: 4.7 µF, 20%, 25 V	2	841293-13	14632	
C86 Thru C89	Same as C12				
C90	Same as C68				
C91	Same as C12				
C92	Not Used				
C93	Same as C3				
C94	Capacitor, Ceramic: 2200 pF, 10%, 50 V	7	841415-015	14632	
C95	Same as C78				
C96	Same as C78				
C97	Same as C94				
C98	Same as C3				
C99	Same as C3				

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
C100	Not Used				
C101	Same as C3				
C102 Thru C110	Same as C12				
C111 Thru C113	Same as C3				
C114	Capacitor, Tantalum: 6.8 µF, 20%, 6.3 V	2	841293-14	14632	
C115 Thru C118	Same as C3				
C119	Capacitor, Ceramic: 68 pF, 5%, 50 V NPO	2	841415-006	14632	
C120	Same as C114				
C121	Same as C12				
C122	Same as C12				
C123	Same as C63				
C124 Thru C126	Same as C3				
C127 Thru C131	Same as C12				
C132	Same as C3				
C133	Same as C12				
C134	Same as C12				
C135	Same as C3				
C136	Same as C3				
C137	Same as C63				
C138	Same as C12				
C139	Same as C3				
C140	Same as C47				
C141	Same as C3				
C142	Same as C47				
C143	Same as C3				
C144	Capacitor, Ceramic: 47 pF, 5%, 50 V NPO	3	841415-005	14632	
C145	Same as C63				
C146	Same as C12				
C147 Thru C154	Same as C3				
C155	Same as C12				
C156	Same as C3				
C157	Same as C144				
C158	Same as C3				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

C159	Same as C3				
C160	Same as C12				
C161	Same as C12				
C162	Not Used				
C163	Same as C3				
C164	Same as C3				
C165	Not Used				
C166	Same as C3				
C167	Same as C68				
C168	Same as C3				
C169	Same as C3				
C170	Same as C47				
C171 Thru C173	Same as C3				
C174	Not Used				
C175	Same as C49				
C176	Same as C78				
C177	Same as C63				
C178	Same as C78				
C179	Same as C119				
C180	Capacitor, Ceramic: 39 pF, 2%, 50 V NPO	1	841416-039	14632	
C181	Same as C12				
C182	Same as C12				
C183	Same as C3				
C184	Not Used				
C185	Same as C47				
c186	Same as C3				
C187	Same as C94				
C188	Same as C144				
C189	Same as C47				
C190 Thru C192	Same as C3				
C193	Not Used				
C194	Same as C78				
C195 Thru C197	Same as C3				
C198	Same as C85				
C199	Same as C3				
C200	Same as C68				
C201	Same as C49				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

C202	Not Used				
C203	Same as C47				
C204	Same as C12				
C205	Capacitor, Tantalum: .33 µF, 20%, 35 V	8	841293-01	14632	
C206	Same as C12				
C207 Thru C211	Not Used				
C212	Same as C78				
C213	Same as C47				
C214	Same as C3				
C215	Same as C3				
C216	Capacitor, Ceramic: .033 µF, 10%, 50 V	8	841415-022	14632	
C217	Same as C63				
C218	Same as C38				
C219	Same as C216				
C220	Same as C3				
C221	Not Used				
C222	Same as C3				
C223	Same as C3				
C224	Not Used				
C225	Not Used				
C226	Same as C3				
C227	Same as C3				
C228	Same as C216				
C229	Same as C3				
C230	Same as C216				
C231	Same as C3				
C232	Not Used				
C233	Same as C3				
C234 Thru C240	Not Used				
C241 Thru C245	Same as C3				
C246 Thru C249	Same as C68				
C250	Same as C216				
C251	Same as C3				
C252	Same as C38				
C253 Thru C255	Same as C3				

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
C256	Capacitor, Tantalum: 68 µF, 20%, 6.3 V	2	841293-24	14632	
C257	Same as C68				
C258	Same as C216				
C259	Same as C78				
C260	Same as C78				
C261	Same as C3				
C262	Same as C3				
C263	Same as C94				
C264	Capacitor, Ceramic: 330 pF, 5%, 50 V NPO	2	841415-010	14632	
C265 Thru C267	Not Used				
C268	Same as C48				
C269	Same as C94				
C270	Same as C63				
C271	Same as C63				
C272	Same as C3				
C273	Same as C12				
C274	Same as C12				
C275	Same as C63				
C276	Same as C3				
C277	Same as C63				
C278	Same as C205				
C279	Same as C12				
C280	Same as C3				
C281	Same as C68				
C282	Same as C256				
C283	Same as C68				
C284	Same as C68				
C285	Same as C3				
C286	Same as C3				
C287	Same as C78				
C288	Same as C3				
C289	Same as C3				
C290	Same as C12				
C291	Same as C3				
C292	Capacitor, Ceramic: 2.2 pF, ±.1 pF, 50 V NPO	3	841416-009	14632	
C293	Same as C292				
C294	Same as C3				
C295	Same as C27				
C296 Thru C298	Same as C3				

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
C299	Same as C11				
C300	Same as C3				
C301	Same as C11				
C302 Thru C304	Same as C3				
C305	Same as C68				
C306	Same as C3				
C307	Same as C3				
C308	Not Used				
C309	Not Used				
C310 Thru C312	Same as C3				
C313	Same as C68				
C314	Not Used				
C315	Same as C27				
C316	Same as C292				
C317	Same as C12				
C318	Capacitor, Ceramic: 22 pF, 2%, 50 V NPO	2	841416-033	14632	
C319	Same as C318				
C320 Thru C325	Same as C3				
C326	Same as C12				
C327	Same as C12				
C328	Same as C48				
C329	Same as C264				
C330 Thru C334	Same as C3				
C335	Same as C29				
C336 Thru C338	Same as C3				
C339	Same as C12				
C340	Same as C29				
C341	Same as C12				
C342	Same as C63				
C343	Same as C12				
C344	Same as C63				
C345	Same as C12				
C346	Same as C205				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

C347 Thru C350	Same as C12				
C351	Same as C205				
C352 Thru C354	Same as C12				
C355	Same as C205				
C356	Same as C12				
C357	Same as C3				
C358	Same as C205				
C359	Same as C3				
C360	Same as C94				
C361	Same as C216				
C362	Same as C94				
C363	Same as C3				
C364 Thru C366	Same as C12				
C367	Same as C63				
C368 Thru C370	Same as C12				
C371	Same as C205				
C372	Same as C12				
C373	Same as C12				
C374	Same as C205				
C375 Thru C377	Same as C12				
C378	Same as C216				
CR1	Dual Switching Diode	17	MMBD7000LT1	04713	
CR2	Diode	6	BB620(Q62702-B403)	25088	
CR3 Thru CR10	Same as CR1				
CR11	Same as CR2				
CR12	Same as CR2				
CR13	Same as CR1				
CR14	Same as CR1				
CR15	Same as CR2				
CR16	Same as CR2				
CR17	Same as CR1				
CR18	Diode	6	FDSO1503	27014	

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
CR19 Thru CR23	Same as CR18				
CR24	Diode	6	HSMP-3800-T31	28480	
CR25 Thru CR29	Same as CR24				
CR30	Same as CR1				
CR31	Same as CR2				
CR32 Thru CR35	Same as CR1				
E1	Cable Assembly	1	IDMD-12-T-4-C	55322	
FB1	Ferrite Bead: 120Ω, ±25%	10	CB30-453215T	54583	
FB2 Thru FB10	Same as FB1				
FL1	Filter, BP: 40.455 MHz	1	92609	14632	
FL2	Filter: 455 kHz	1	CFS-455B	51406	
J1	Connector, Jack, BNC	3	227677-1	00779	
J2	Same as J1				
J3	Same as J1				
J4	Not Used				
J5	Connector	1	79223-610	22526	
L1	Inductor: 1000 µH, 10%	6	841699-037	14632	
L2	Inductor: 10 µH, 10%	2	841699-013	14632	
L3	Inductor: 22 nH, ±5%	1	841438-009	14632	
L4	Inductor: 15 nH, ±5%	1	841438-005	14632	
L5	Inductor: 4700 nH, 10%	12	841698-033	14632	
L6	Inductor: 47 µH, ±10%	2	NL322522-470K	54583	
L7	Inductor: 150 nH, ±5%	2	841438-029	14632	
L8	Inductor: 68 nH, ±5%	2	841438-021	14632	
L9	Inductor: 4.7 µH, ±20%	4	B82422-A1472-M	25088	
L10	Same as L6				
L11	Same as L7				
L12	Same as L8				
L13	Same as L9				
L14	Same as L9				
L15 Thru L17	Same as L5				
L18	Inductor: 270 µF, ±5%	2	841438-035	14632	
L19	Inductor: 330 nH, ±5%	1	841438-037	14632	
L20	Inductor: 220 nH, ±5%	4	841438-033	14632	

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
L21	Inductor: 160 nH, ±5%	1	841438-030	14632	
L22	Inductor: 180 nH, ±5%	1	841438-031	14632	
L23	Inductor: 240 nH, ±5%	1	841438-034	14632	
L24	Same as L1				
L25	Inductor: 150 µH, 10%	2	841699-027	14632	
L26	Same as L25				
L27	Same as L1				
L28	Same as L1				
L29	Inductor: 270 µH, 10%	13	841699-030	14632	
L30	Same as L29				
L31	Inductor: 47 µH, 10%	4	841699-021	14632	
L32	Same as L31				
L33	Same as L31				
L34	Same as L9				
L35	Same as L29				
L36	Same as L20				
L37	Inductor: 100 nH, ±5%	2	841438-025	14632	
L38	Same as L37				
L39	Inductor: 4700 nH, 10%	1	841698-033	14632	
L40	Same as L5				
L41	Same as L5				
L42	Same as L18				
L43 Thru L45	Same as L29				
L46 Thru L48	Same as L5				
L49 Thru L52	Same as L29				
L53	Not Used				
L54	Same as L29				
L55 Thru L57	Not Used				
L58	Same as L29				
L59	Same as L29				
L60	Inductor: 470 nH, ±5%	2	841438-041	14632	
L61	Same as L60				
L62	Same as L20				
L63	Same as L20				
L64	Same as L1				
L65	Same as L1				

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
L66	Same as L2				
L67	Same as L31				
L68	Same as L5				
L69	Same as L5				
L70	Not Used				
L71	Same s L5				
Q1	Transistor	1	MMBR2857	04713	
Q2	Transistor	15	MMBT3904LT1	04713	
Q3	Same as Q2				
Q4	Transistor	18	MMBT-3906	04713	
Q5	Same as Q4				
Q6	Transistor	3	OST310	17856	
Q7	Transistor	6	MMBTH69LT1	04713	
Q8	Same as Q7				
Q9 Thru Q12	Same as Q2				
Q13	Same as Q4				
Q14	Same as Q2				
Q15	Transistor	1	2N7002	17856	
Q16	Same as Q6				
Q17	Same as Q7				
Q18	Same as Q7				
Q19	Same as Q4				
Q20	Same as Q7				
Q21	Same as Q7				
Q22	Same as Q2				
Q23	Transistor	1	841381-2	14632	
Q24	Same as Q4				
Q25	Same as Q2				
Q26	Same as Q4				
Q27	Same as Q2				
Q28	Same as Q4				
Q29	Same as Q2				
Q30	Same as Q4				
Q31	Same as Q4				
Q32	Transistor	4	MRF5812	04713	
Q33 Thru Q35	Same as Q32				
Q36	Same as Q2				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

Q37	Transistor	2	MMBT3960A	04713	
Q38	Same as Q37				
Q39	Same as Q6				
Q40	Same as Q4				
Q41	Transistor	2	MTD10N05E	04713	
Q42	Same as Q4				
Q43	Transistor	1	MTD4P05	04713	
Q44	Same as Q41				
Q45	Same as Q2				
Q46	Same as Q2				
Q47	Same as Q4				
Q48	Same as Q2				
Q49 Thru Q54	Same as Q4				
R1	Resistor, Fixed: 1.0 kΩ, 5%, 1/10 W	29	841414-073	14632	
R2	Resistor, Fixed: 680Ω, 5%, 1/10 W	22	841414-069	14632	
R3	Same as R1				
R4	Jumper	26	841417	14632	
R5	Same as R4				
R6	Same as R2				
R7	Same as R4				
R8	Resistor, Fixed: 100 kΩ, 5%, 1/10 W	14	841414-121	14632	
R9	Same as R2				
R10	Resistor, Fixed: 10Ω, 5%, 1/10 W	35	841414-025	14632	
R11	Resistor, Fixed: 10 kΩ, 5%, 1/10 W	19	841414-097	14632	
R12	Same as R11				
R13	Same as R1				
R14	Same as R8				
R15	Resistor, Fixed: 1.5 MΩ, 5%, 1/10 W	5	841414-149	14632	
R16	Same as R10				
R17	Resistor, Fixed: 680 kΩ, 5%, 1/10 W	5	841414-141	14632	
R18	Resistor, Fixed: 6.8 kΩ, 5%, 1/10 W	5	841414-093	146732	
R19	Resistor, Fixed: 120 kΩ, 5%, 1/10 W	2	841414-123	14632	
R20	Resistor, Fixed: 12 kΩ, 5%, 1/10 W	6	841414-099	14632	
R21	Resistor, Fixed: 4.7 kΩ, 5%, 1/10 W	16	841414-089	14632	
R22	Same as R10				
R23	Same as R20				
R24	Resistor, Fixed: 27 kΩ, 5%, 1/10 W	6	841414-107	14632	
R25	Same as R20				
R26	Same as R24				
R27	Same as R21				
R28	Same as R10				
R29	Resistor, Fixed: 68 kΩ, 5%, 1/10 W	2	841414-117	14632	

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
R30	Same as R15				
R31	Same as R29				
R32	Same as R15				
R33	Same as R10				
R34	Resistor, Fixed: 2.2 kΩ, 5%, 1/10 W	8	841414-081	14632	
R35	Same as R15				
R36	Same as R15				
R37	Same as R17				
R38	Not Used				
R39	Same as R11				
R40	Resistor, Fixed: 330Ω, 5%, 1/10 W	7	841414-061	14632	
R41	Same as R8				
R42	Resistor, Fixed: 3.3 kΩ, 1/10 W	10	841414-085	14632	
R43	Same as R1				
R44	Resistor, Fixed: 470Ω, 5%, 1/10 W	19	841414-065	14632	
R45	Same as R1				
R46	Resistor, Fixed: 15 kΩ, 5%, 1/10 W	5	841414-101	14632	
R47	Not Used				
R48	Same as R11				
R49	Same as R19				
R50	Same as R10				
R51	Same as R42				
R52	Resistor, Fixed: 100Ω, 5%, 1/10 W	17	841414-049	14632	
R53	Same as R52				
R54	Same as R10				
R55	Same as R8				
R56	Resistor, Fixed: 22 kΩ, 5%, 1/10 W	3	841414-105	14632	
R57	Same as R8				
R58	Same as R56				
R59	Resistor, Variable: 10 kΩ	1	3269X-1-103	80294	
R60	Same as R11				
R61	Same as R10				
R62	Same as R46				
R63	Same as R1				
R64	Same as R1				
R65	Not Used				
R66	Resistor, Fixed: 470 kΩ, 5%, 1/10 W	2	841414-137	14632	
R67	Same as R10				
R68	Same as R11				
R69	Same as R18				
R70	Same as R44				
R71	Same as R10				
R72	Same as R10				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

R73	Same as R1				
R74	Same as R52				
R75	Same as R34				
R76	Same as R8				
R77	Same as R11				
R78	Same as R11				
R79	Same as R10				
R80	Resistor, Fixed: 1.5 kΩ, 5%, 1/10 W	12	841414-077	14632	
R81	Resistor, Fixed: 150Ω, 5%, 1/10 W	6	841414-053	14632	
R82	Resistor, Fixed: 470Ω, 5%, 1/8 W	3	841296-057	14632	
R83	Same as R44				
R84	Same as R82				
R85	Same as R82				
R86	Same as R24				
R87	Resistor, Fixed: 120Ω, 5%, 1/10 W	4	841414-051	14632	
R88	Resistor, Fixed: 270Ω, 5%, 1/10 W	2	841414-059	14632	
R89	Same as R24				
R90	Same as R21				
R91	Same as R66				
R92	Same as R44				
R93	Same as R2				
R94	Same as R81				
R95	Resistor, Fixed: 22Ω, 5%, 1/10 W	7	841414-033	14632	
R96	Same as R52				
R97	Same as R34				
R98	Same as R80				
R99	Resistor, Fixed: 120Ω, 5%, 1/8 W	5	841296-043	14632	
R100	Same as R99				
R101	Same as R99				
R102	Same as R81				
R103	Same as R99				
R104	Resistor, Fixed: 180Ω, 5%, 1/10 W	5	841414-055	14632	
R105	Same as R52				
R106	Same as R10				
R107	Same as R99				
R108	Same as R95				
R109	Same as R10				
R110	Same as R87				
R111	Same as R52				
R112	Same as R10				
R113	Same as R24				
R114	Resistor, Fixed: 220Ω, 5%, 1/10 W	10	841414-057	14632	
R115	Same as R114				
R116	Same as R2				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

R117	Resistor, Fixed: 47Ω, 5%, 1/10 W	15	841414-041	14632	
R118	Same as R87				
R119	Same as R1				
R120	Same as R1				
R121	Same as R87				
R122	Same as R1				
R123	Resistor, Fixed: 68Ω, 5%, 1/10 W	5	841414-045	14632	
R124	Same as R123				
R125 Thru R127	Same as R44				
R128	Same as R123				
R129	Same as R80				
R130	Same as R1				
R131	Same as R44				
R132	Same as R21				
R133	Resistor, Fixed: 33 kΩ, 5%, 1/10 W	3	841414-109	14632	
R134	Same as R21				
R135	Same as R44				
R136	Same as R21				
R137	Same as R133				
R138	Same as R21				
R139	Same as R21				
R140	Same as R114				
R141	Same as R21				
R142	Same as R133				
R143	Same as R21				
R144	Same as R10				
R145 Thru R147	Same as R8				
R148	Same as R114				
R149	Resistor, Fixed: 2.7 kΩ, 5%, 1/10 W	8	841414-083	14632	
R150 Thru R152	Same as R21				
R153	Same as R24				
R154	Same as R20				
R155	Same as R8				
R156	Same as R10				
R157	Same as R11				
R158	Same as R149				
R159	Same as R11				
R160	Same as R21				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
R161	Same as R21				
R162	Same as R52				
R163	Same as R42				
R164	Same as R44				
R165	Same as R10				
R166	Same as R88				
R167	Same as R149				
R168	Same as R42				
R169	Same as R10				
R170	Same as R1				
R171	Same as R149				
R172	Same as R42				
R173	Resistor, Fixed: 560Ω, 5%, 1/10 W	5	841414-067	14632	
R174	Same as R42				
R175	Not Used				
R176	Same as R4				
R177	Same as R114				
R178	Same as R149				
R179	Same as R10				
R180	Same as R2				
R181	Same as R117				
R182	Same as R80				
R183	Same as R2				
R184	Same as R10				
R185	Not Used				
R186	Same as R81				
R187	Same as R40				
R188	Same as R81				
R189	Same as R117				
R190	Same as R2				
R191	Resistor, Fixed: 3.3Ω, 5%, 1/10 W	2	841414-013	14632	
R192	Same as R191				
R193	Same as R4				
R194	Resistor, Fixed: 33Ω, 5%, 1/10 W	4	841414-037	14632	
R195	Same as R34				
R196	Same as R8				
R197	Same as R10				
R198	Same as R10				
R199	Same as R2				
R200	Same as R2				
R201	Same as R1				
R202	Same as R46				
R203	Same as R52				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

R204	Same as R117				
R205	Same as R44				
R206	Same as R8				
R207	Same as R40				
R208	Same as R44				
R209	Same as R4				
R210	Same as R194				
R211	Same as R117				
R212	Same as R2				
R213	Same as R42				
R214	Same as R2				
R215	Same as R42				
R216 Thru R218	Same as R4				
R219	Same as R10				
R220	Same as R114				
R221	Same as R42				
R222	Same as R4				
R223	Same as R2				
R224	Same as R4				
R225	Same as R4				
R226	Same as R10				
R227	Same as R10				
R228	Same as R2				
R229	Same as R1				
R230	Same as R1				
R231	Same as R10				
R232	Same as R42				
R233	Same as R80				
R234	Same as R10				
R282	Same as R117				
R283	Same as R1				
R284	Same as R95				
R285	Same as R1				
R286	Same as R18				
R287	Same as R80				
R288	Same as R249				
R289	Same as R173				
R290	Resistor, Fixed: 2.7Ω, 5%, 1/10 W	2	841414-011	14632	
R291	Same as R11				
R292	Same as R11				
R293	Same as R10				

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR

REF DESIG PREFIX **A3**

R294	Same as R4
R295	Same as R44
R296	Same as R4
R297	Same as R114
R298	Same as R11
R299	Same as R34
R300	Same as R52
R301	Same as R52
R302	Same as R123
R303	Same as R123
R304	Same as R104
R305	Same as R104
R306	Same as R40
R307	Same as R117
R308	Same as R1
R309	Same as R117
R310	Same as R40
R311	Same as R149
R312	Same as R95
R313	Same as R117
R314	Same as R80
R315	Same as R18
R316	Same as R117
R317	Same as R1
R318	Same as R117
R319	Same as R40
R320	Same as R117
R321	Same as R149
R322	Same as R4
R323	Same as R20
R324	Same as R52
R325	Same as R4
R326	Same as R20
R327	Same as R80
R328	Same as R52
R329	Same as R173
R330	Same as R173
R331	Same as R95
R332	Same as R52
R333	Same as R95
R334	Same as R249
R335	Same as R1
R336	Same as R173

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
R337	Same as R52				
R338	Same as R104				
R339	Same as R114				
R340	Same as R44				
R341	Same as R117				
R342	Same as R290				
R343	Same as R44				
R344	Same as R44				
R345	Same as R18				
R346	Same as R80				
R347	Same as R1				
R348	Same as R149				
R349	Same as R44				
R350	Same as R52				
R351	Same as R34				
R352	Same as R2				
R353	Same as R44				
R355	Same as R52				
R355	Same as R11				
R356	Same as R1				
R357	Same as R1				
R358	Same as R80				
R359	Same as R80				
R360	Same as R114				
R361	Same as R117				
R362	Same as R81				
R363	Same as R249				
R364	Same as R104				
R365	Same as R46				
R366	Same as R194				
R367	Same as R10				
R368	Same as R249				
R369	Same as R194				
R370	Same as R40				
R371	Same as R10				
R372	Same as R95				
R373	Same as R2				
R374	Resistor, Fixed: 180Ω, 5%, 1/8 W	1	841296-047	14632	
T1	Transformer	1	841709-1	14632	
T2	Transformer	2	458DB-1011=P1	9AA39	
T3	Same as T2				
T4	Transformer	1	458PS-1007=T1	9AA39	
U1	Integrated Circuit	1	8674HC08SO14U	14632	

REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
U2	Integrated Circuit	2	8674HC32SO14U	14632	
U3	Integrated Circuit	1	8674HC138SO16U	14632	
U4	Integrated Circuit/CMOS	1	8674HC4094SO16U	14632	
U5	Integrated Circuit	2	8674HC00SO14U	14632	
U6	Amplifier	1	86062SO8	14632	
U7	Integrated Circuit	3	MC145158DW-2	04713	
U8	Integrated Circuit	1	8674HC02SO14U	14632	
U9	OSC/TCVXO, ±0.6 PPM*	1	92658	14632	
U9	TCXO/XTAL 10.000 MHz**		92549	14632	
U10	Integrated Circuit/CMOS	3	8674AC00SO14U	14632	
U11	Integrated Circuit	1	TL431CD	04713	
U12	Same as U2				
U13	Integrated Circuit/CMOS	1	MB87086APF	61271	
U14	Amplifier	10	NE5534D	18324	
U15	Same as U7				
U16	Same as U14				
U17	Integrated Circuit	1	MB504PF	61271	
U18	Integrated Circuit	1	SP8792/MP	52648	
U19	Integrated Circuit/CMOS	1	8674AC74S014	14632	
U20	Same as U5				
U21 Thru U25	Same as U14				
U26	Mixer, Balanced	1	NE602D	18324	
U27	Same as U10				
U28	Integrated Circuit	1	SD5400CY	17856	
U29	Amplifier	1	LH2422AJ	27014	
U30	Mixer	1	LRMS-1-TR	15542	
U31	Integrated Circuit/CMOS	1	8674HC4053SO16U	14632	
U32	Same as U14				
U33	Integrated Circuit/CMOS	1	8674AC86S014	14632	
U34	Same as U10				
U35	Same as U7				
U36	Same as U14				
U37	Integrated Circuit	1	8674HC74SO14U	14632	
U38	Not Used				
U39	Amplifier	3	86061SO08	14632	
U40	Same as U39				
U41	Same as U39				
U42	Same as U14				
VR1	Diode, Zener	2	MMBZ5231BLT1	04713	
UR2	Same as VR1				
VR3	Diode, Zener	1	MMBZ5235BLT1	04713	

* Note: *Type 797006-1/-3/-5
**Type 797006-2/-4

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURERS PART NO.	MFR. CODE	RECM VENDOR
8.6.4	**WJ-8710/AI ACCESSORY ITEMS**				
AI-1	Connector, Plug, Multi	1	FGG.0B.303.C.L.A.D52	2P953	
AI-2	Fuse, Plug-In, 3 AMP Microfuse	1	273003	75915	
AI-3	Bumper	4	8710/AI	06540	
AI-4	Screw, Mach	4	AN500C6RA	70318	
AI-5	Washer, Lock	4	MS35338-136	96906	
AI-6	Terminal Block 13 Position	1	ELFP132210	58982	
AI-7	Cover Removal Tool	1	283269-1	14632	

NOTES

SECTION IX

SCHEMATIC DIAGRAMS

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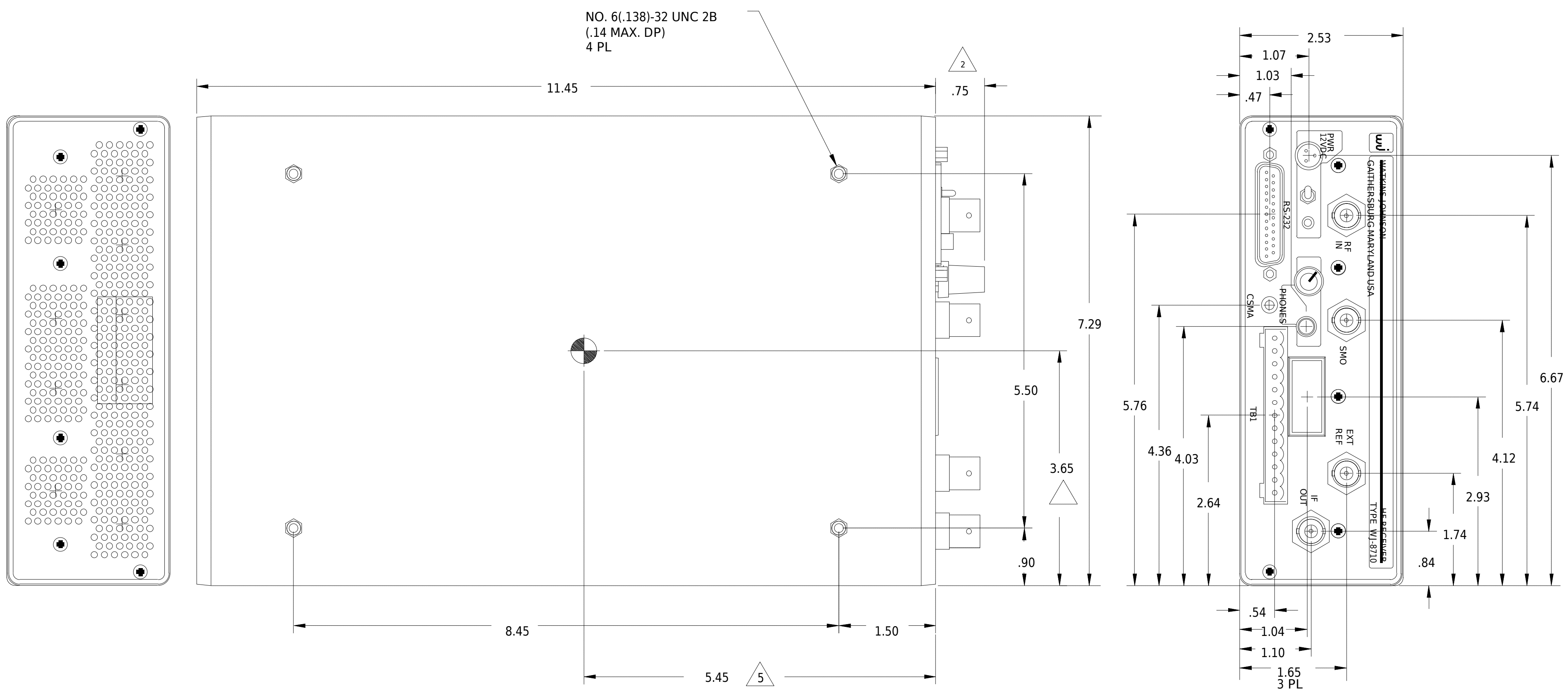


NOTES

1. POWER RQUIREMENTS:
   - INPUT POWER 18 WATTS
   - INPUT VOLTAGE 12 VDC

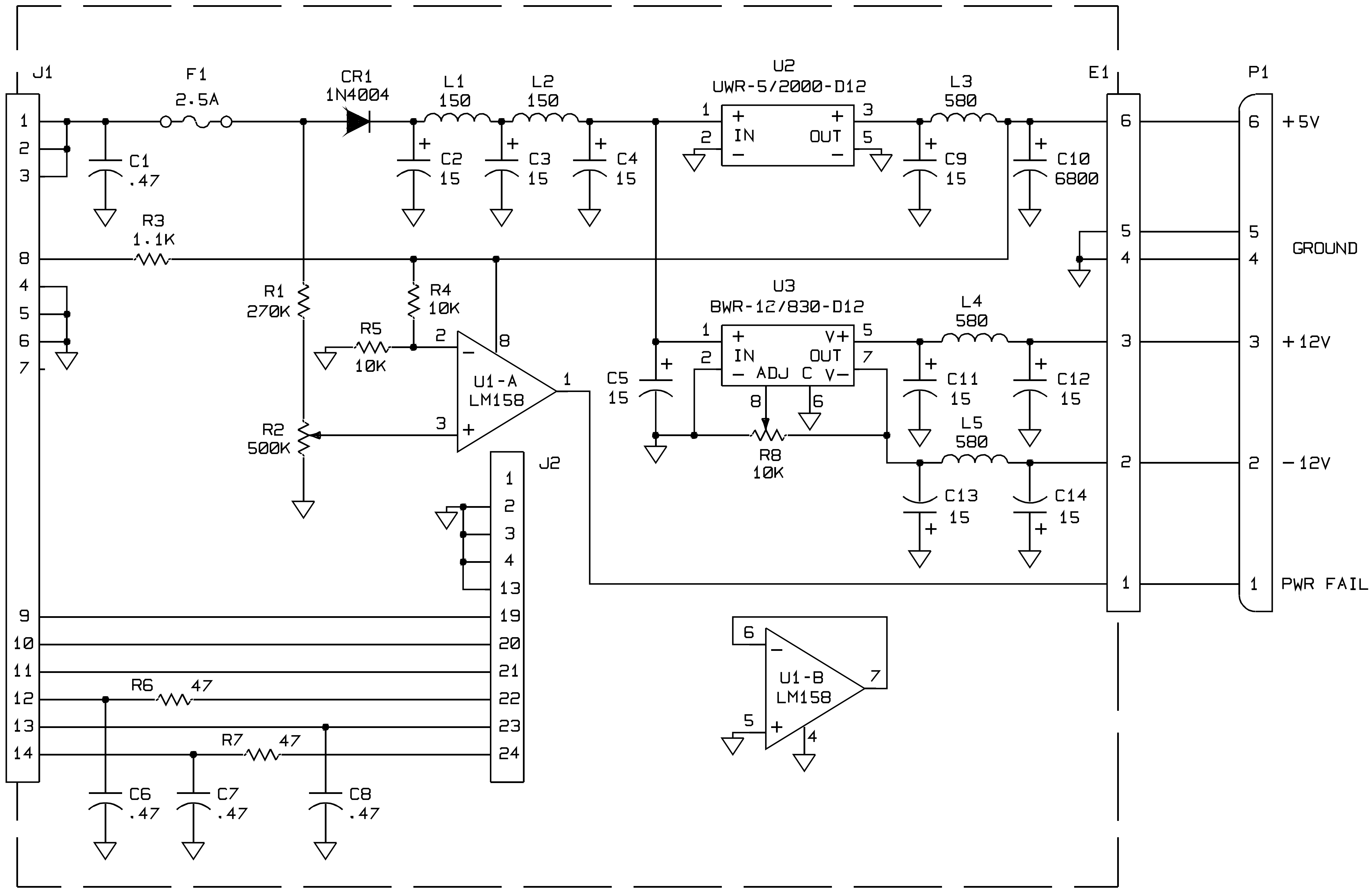
2. IDENTIFIES MAXIMUM PROTRUSION OF FRONT PANEL ITEMS.

3. THE EQUIPMENT WILL OPERATE IN A FREE AIR AMBIENT AT SEA LEVEL FROM -10°C TO +55°C WITH COMPLETE PERFORMANCE SPECIFICATIONS BEING MET FROM 0°C TO 50°C. WHERE THE ENVIROMENT VARIES FROM FREE AIR AMBIENT AT SEA LEVEL SUFFICIENT AIR SPACE AND/OR VOLUME OF COOLING AIR MUST BE PROVIDED AROUND THE UNIT TO DISSIPATE THE HEAT DEVELOPED.

4. WEIGHT 7 LBS

5. APPROX CENTER OF GRAVITY IDENTIFIED BY

FO-1. WJ-8710A Digital HF Receiver
Critical Dimension Diagram 482311 (C)



NOTES:

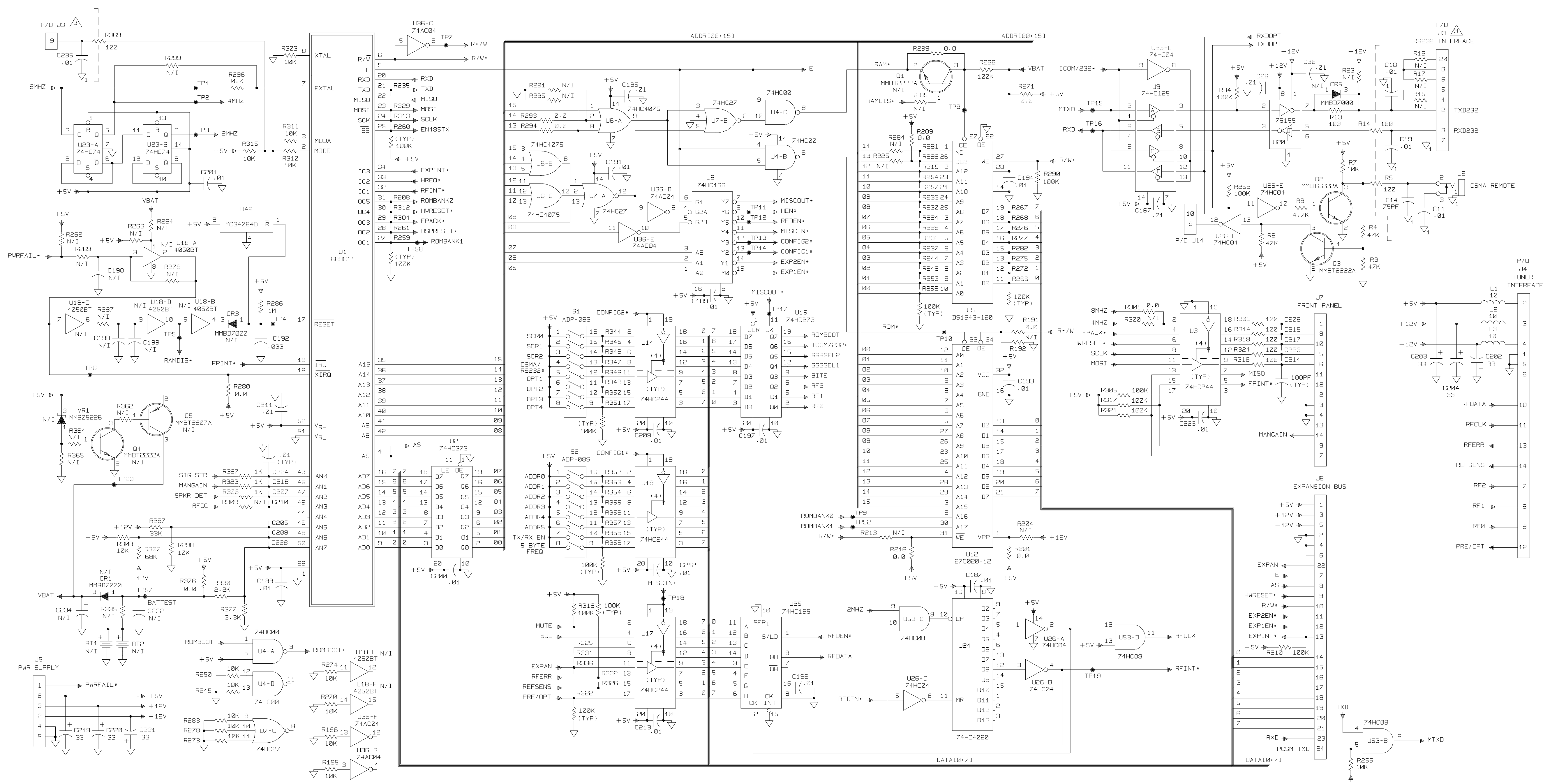
1. UNLESS OTHERWISE SPECIFIED:

A) RESISTANCE IS IN OHMS, ±5%, 1/4W.

B) CAPACITANCE IS IN μF.

C) INDUCTANCE IS IN μH.

FO-2. Type 766027-1 DC/DC Power Supply (A1), Schematic Diagram 383216



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A) RESISTANCE IS IN OHMS, ±5%, 1/10W.
   - B) CAPACITANCE IS IN μF.
   - C) INDUCTANCE IS IN μH.

2. PIN/ADDRESS NUMBERS SHOWN ARE FOR MICRON SEMICONDUCTOR PARTS. ADDRESS NUMBERS MAY DIFFER ON ALTERNATE MFG. PARTS, HOWEVER THEY ARE FUNCTIONALLY EQUIVALENT.

△3 DIFFERENCE BETWEEN TYPES IS LISTED IN TABLE 1.

TABLE 1

TYPE	J3	J2
797214-1	USED	USED
797214-2	N/I	USED
797214-3	USED	N/I
797214-4	△5	

NOTES: (CONTINUED)

4. IT IS POSSIBLE TO USE VARIOUS DENSITY MEMORY CHIPS FOR U39, U40, U41, U45, U46, U47 & U56. THE FOLLOWING TABLE 2 LISTS EACH ASSY DASH NO. (TYPE). IT'S MEMORY CONFIGURATION, AND WHICH 0-OHM RESISTORS MUST BE INSTALLED.

TABLE 2

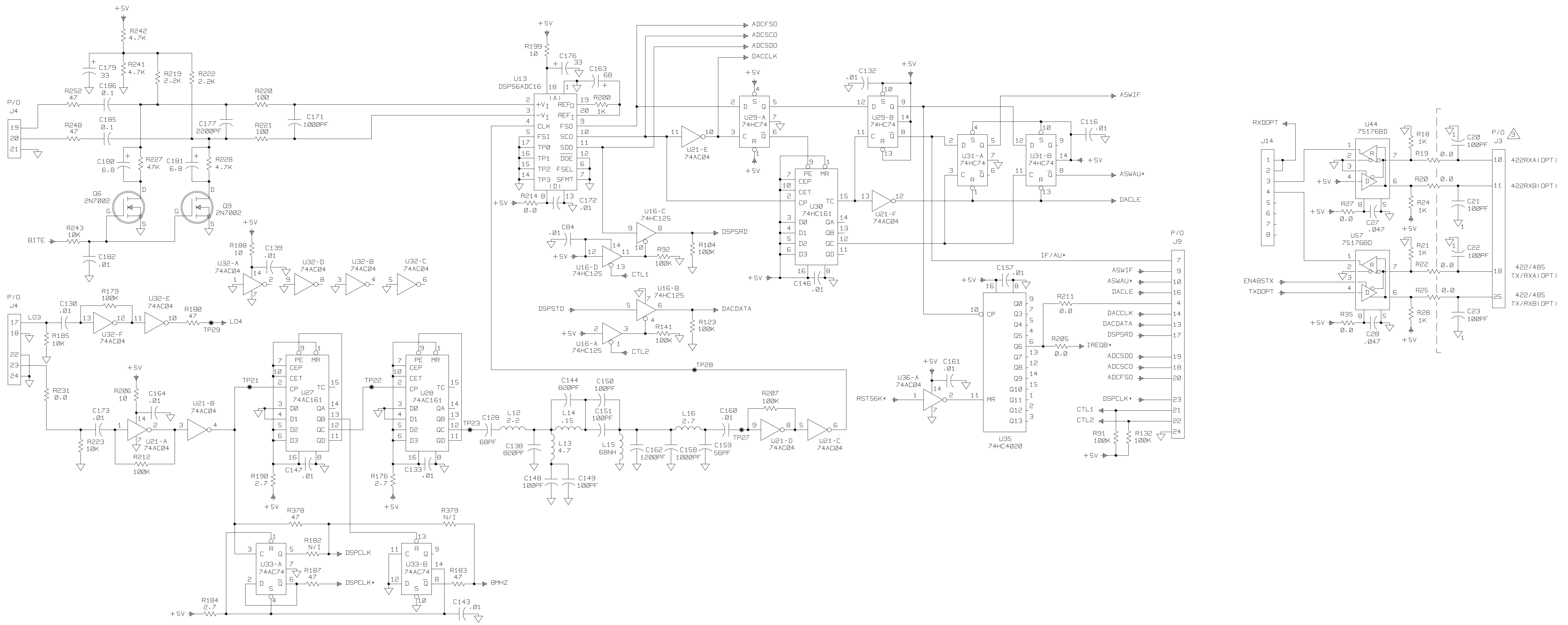
TYPE	REF DES	DESCRIPTION	PART NO.	R43	R44	R38	R156
797214-1, -2	U56 U45, U46, U47, U39, U40, U41	64K X 8 EPROM 32K X 8 SRAM ** 32K X 8 SRAM ***	27C512 MT5C2568 MT5C2568	0.0	N/I	0.0	N/I

** A 28-PIN 32K X 8 SRAM IS SHOWN ON THE SCHEMATIC. WHEN A 28-PIN 8K X 8 SRAM IS INSTALLED, PIN 26 IS CE2 (VS. A13) AND PIN 1 IS NC (VS. 141).

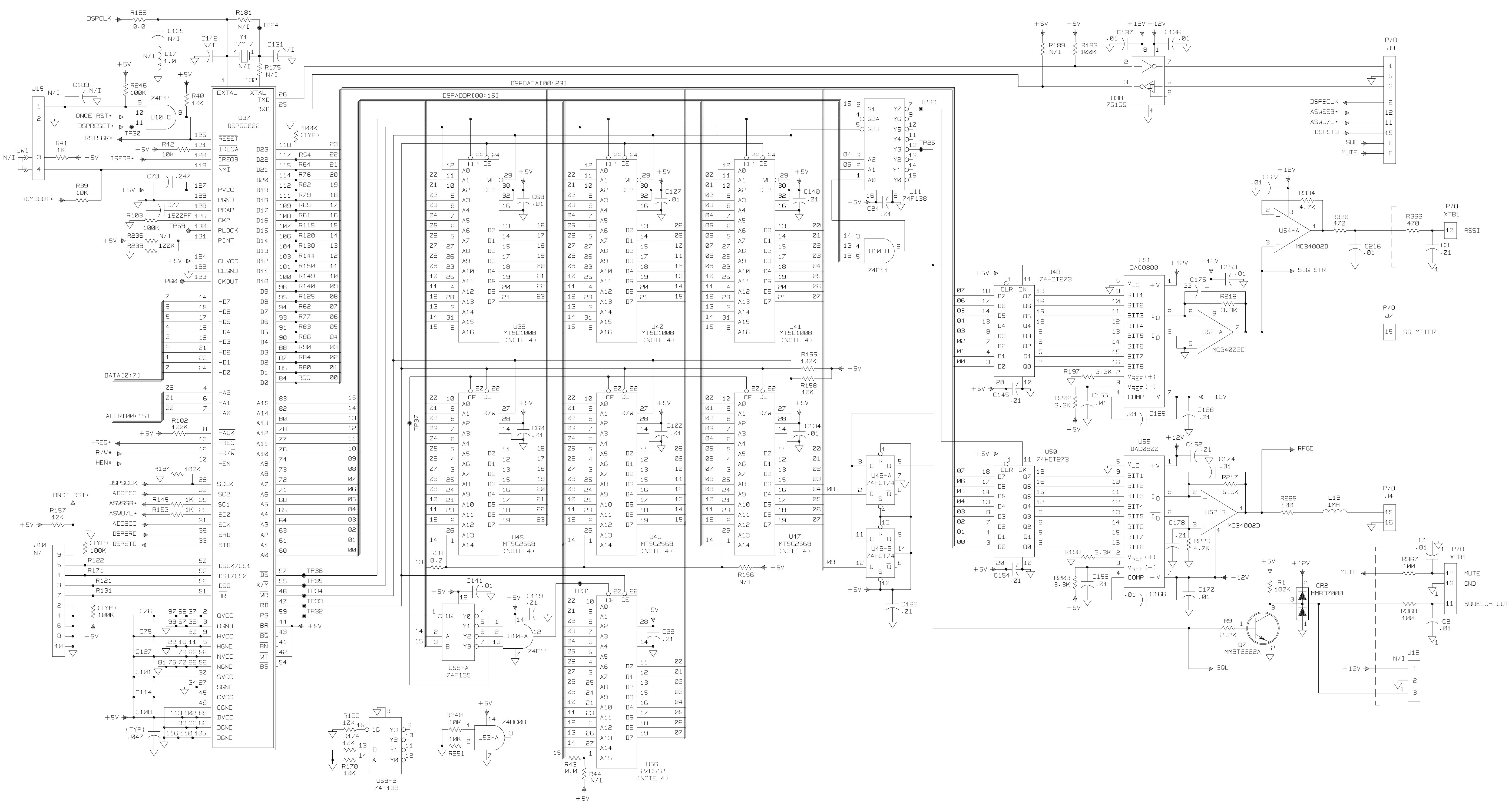
*** A32-PIN 128K X 8 SRAM IS SHOWN ON THE SCHEMATIC. WHEN A 28-PIN 32K X 8 IS INSTALLED, PINS 1 THRU 28 CORRESPOND TO PINS 3 THRU 30 ON THE 32-PIN CHIP.

△5 -4 SAME AS -1, EXCEPT CONFORMAL COATED.

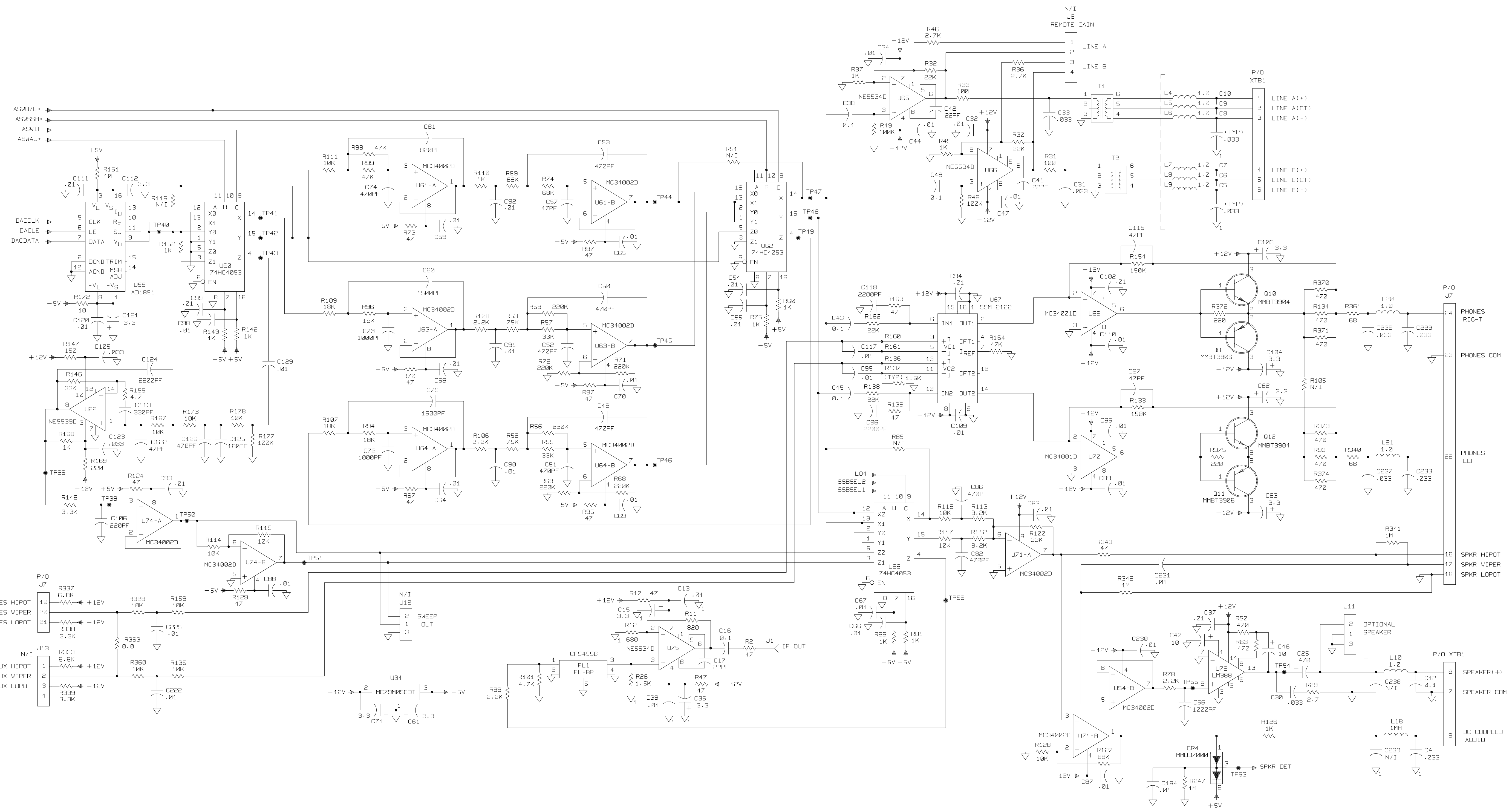
FO-3. Type 797214-1 Digital Control Assembly (A2), Schematic Diagram 581839 (Sheet 1 of 4) (B)



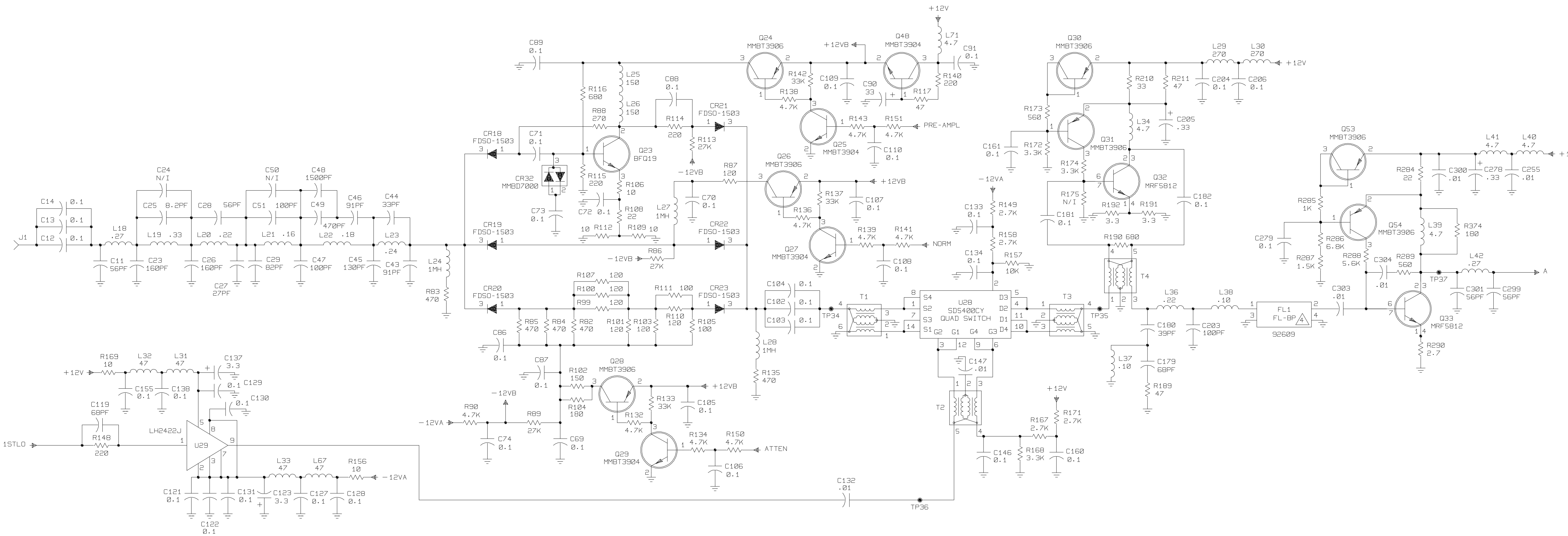
FO-3. Type 797214-1 Digital Control Assembly (A2),
Schematic Diagram 581839 (Sheet 2 of 4) (B)



FO-3. Type 797214-1 Digital Control Assembly (A2), Schematic Diagram 581839 (Sheet 3 of 4) (B)



FO-3. Type 797214-1 Digital Control Assembly (A2), Schematic Diagram 581839 (Sheet 4 of 4) (B)



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A) RESISTANCE IS IN OHMS, ±5%,1/10W.
   B) CAPACITANCE IS IN μF.
   C) INDUCTANCE IS IN μH.
2. PADDLE-STRIP 'E1' HAS A PLUG LABELED 'P1'(NOT-SHOWN) WITH IDENTICAL PINS.

⚠3 -3 AND -4 ARE CONFORMAL COATED VERSIONS OF -1 AND -2, RESPECTIVELY.

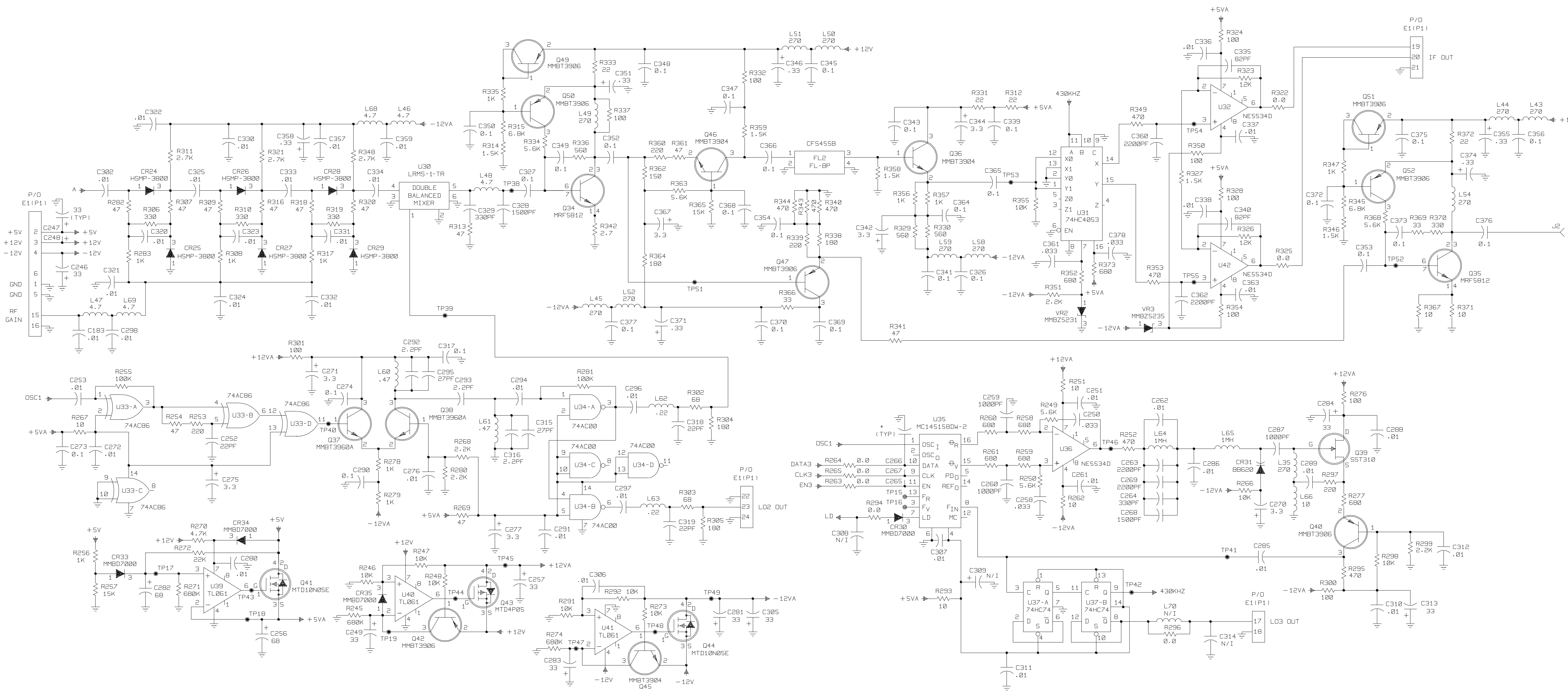
⚠4 SEE TABLE 'A' FOR DIFFERENCE BETWEEN DASH NUMBERS.

⚠5 NOMINAL VALUE. FINAL VALUE FACTORY SELECTED.

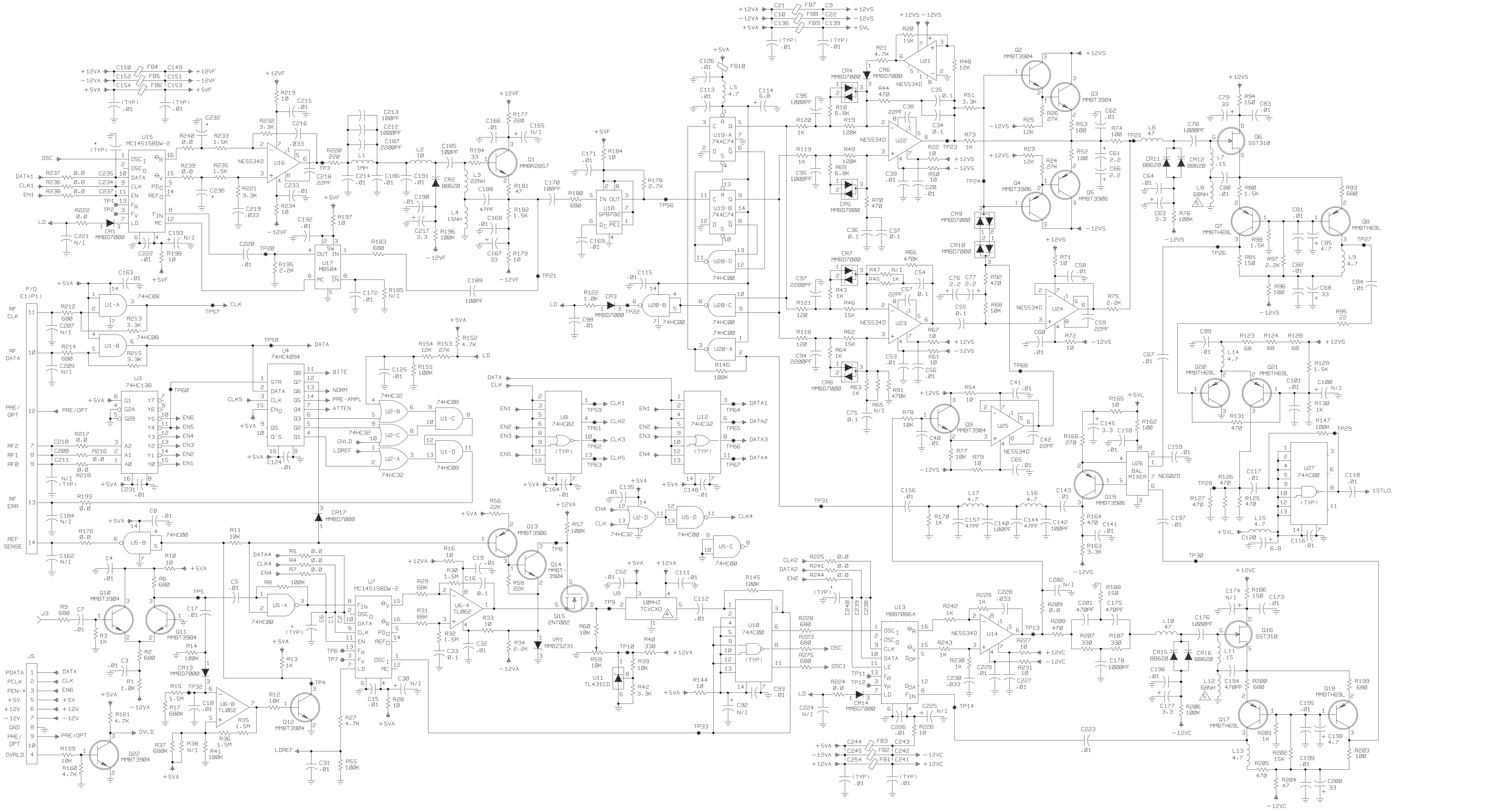
TABLE A

TYPE(DASH)NO.	U9	FL1
797006-1	92658	92609
797006-2	92549	92609
797006-3	⚠3	
797006-4		
797006-5	92698	92699
797006-6	92731	92727
797006-7	92658	92727

FO-4. Type 797006-X RF Tuner Assembly (A3), Schematic Diagram 581274 (Sheet 1 of 3) (R)



FO-4. Type 797006-X RF Tuner Assembly (A3), Schematic Diagram 581274 (Sheet 2 of 3) (R)



FO-4. Type 797006-X RF Tuner Assembly (A3),
Schematic Diagram 581274 (Sheet 3 of 3) (R)

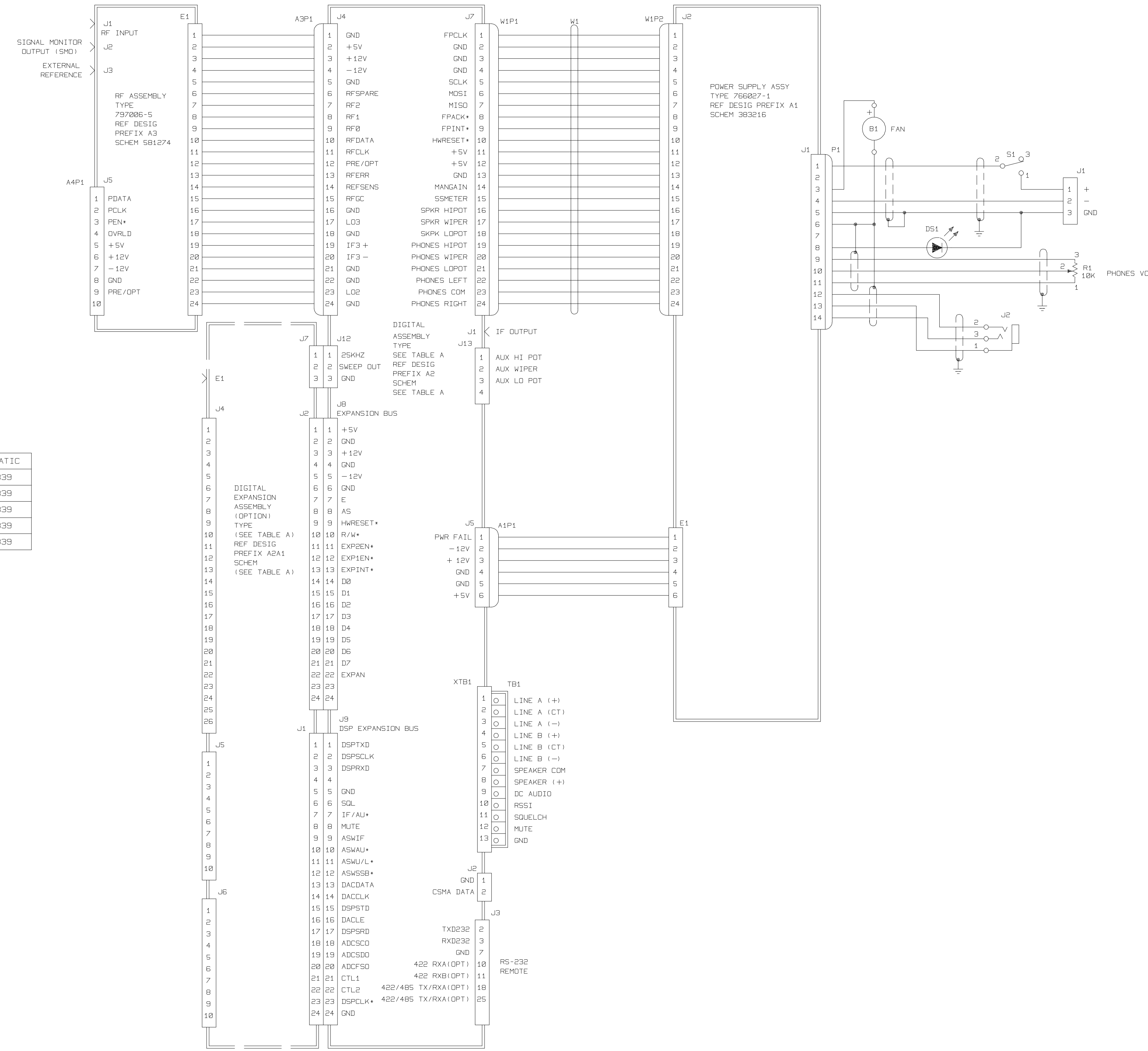
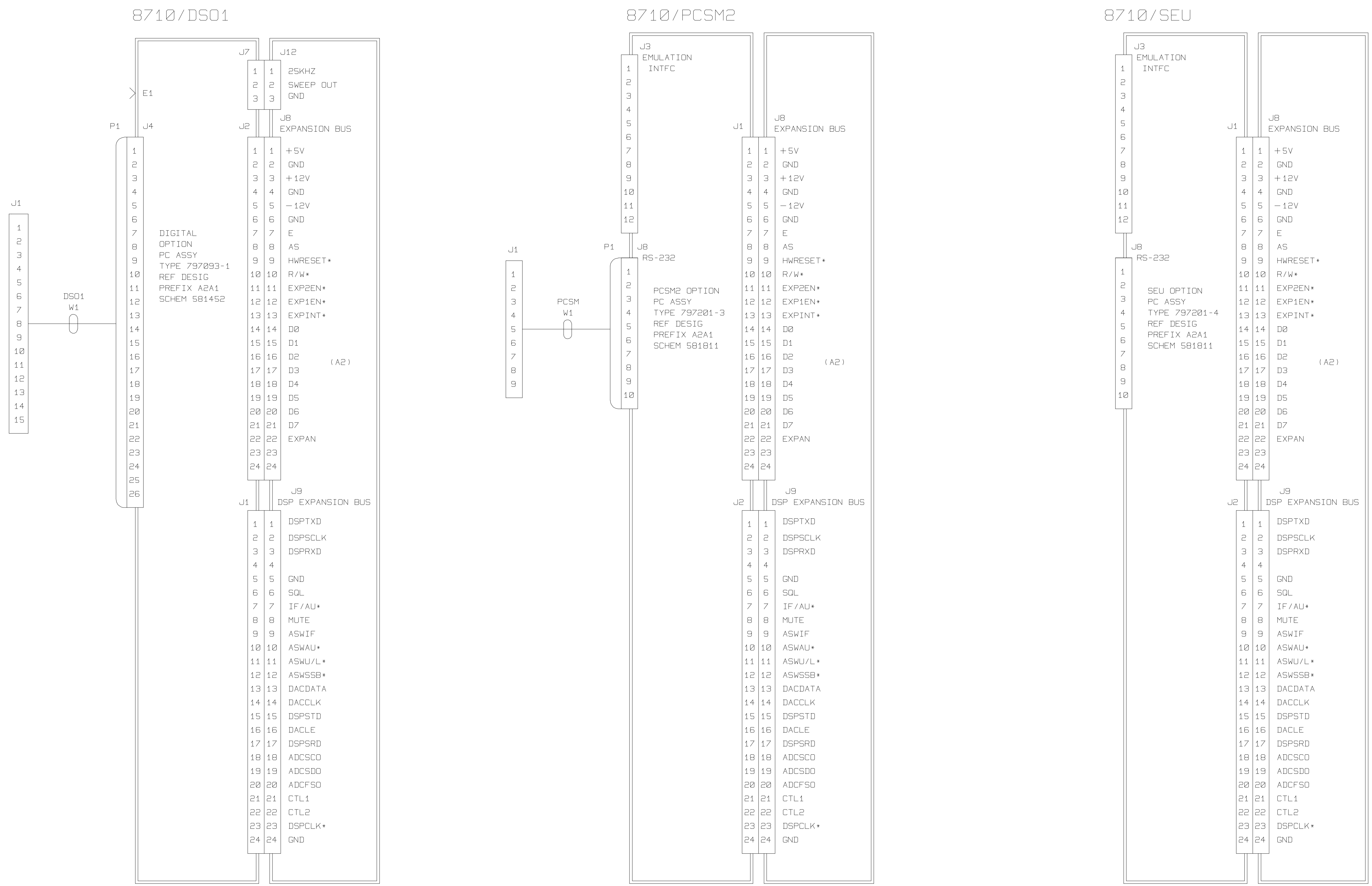


TABLE A

	A2A1		A2	
APPLICATION	TYPE	SCHEMATIC	TYPE	SCHEMATIC
871Y/485	———	———	797214-3	581839
8710/DSO1	797093-1	581453	797214-1	581839
WJ-8710A	———	———	797214-1	581839
8710/SEU	797201-4	581811	797214-1	581839
8710/PCSM2	797201-3	581811	797214-1	581839

FO-5. Type WJ-8710A Digital HF Receiver, Main Chassis, Schematic Diagram 581652 (Sheet 1 of 2) (B)



FO-5. Type WJ-8710A Digital HF Receiver, Main Chassis, Schematic Diagram 581652 (Sheet 2 of 2) (B)