INSTRUCTION MANUAL

FOR

WJ-8628-4 VHF/UHF RECEIVER

WATKINS-JOHNSON COMPANY
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GAITHERSBURG, MARYLAND 20878

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WARNING

This equipment employs dangerous voltages which may be fatal if contacted. Exercise extreme caution in working with this equipment with any of the protective covers removed.

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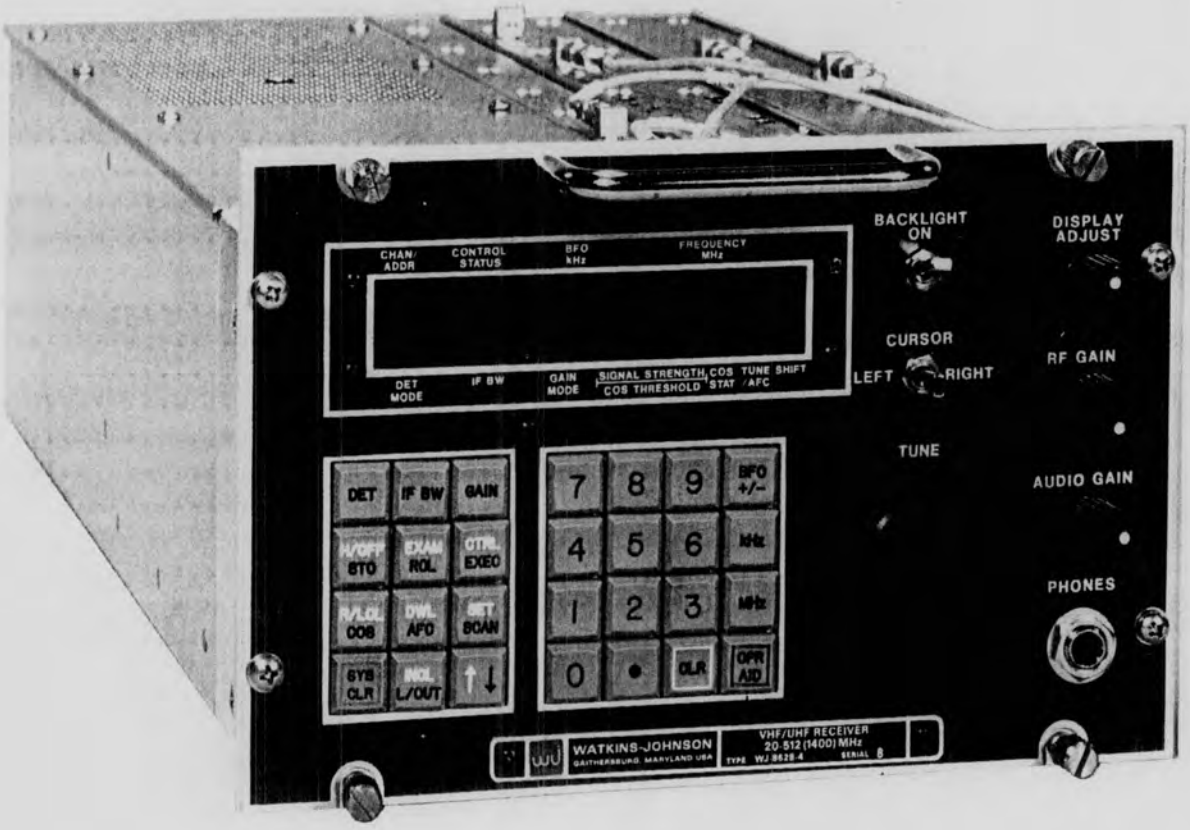


Figure 1-1. WJ-8628-4 VHF/UHF Receiver

SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The WJ-8628-4 VHF/UHF Receiver (**Figure 1-1**) is a fully synthesized, microprocessor-controlled VHF/UHF receiver that operates in the frequency range of 20 to 512 MHz, tunable to 100 Hz resolution. The receiver is compatible with the WJ-9040 Receiving System Family, functioning both as a receiver and a receiver controller with the Master Handoff Option (MH Option). The receiver shares the WJ-9040 System characteristics of low power consumption, modular construction and high performance. The WJ-8628-4 operates in both a local and remote control mode. Variable tuning resolution to 100 Hz is provided by phase lock loop frequency synthesizers stabilized by a 50 MHz reference frequency normally provided by a FRM150 or SRM105A module located in the WJ-9040 EFR100 Equipment Frame. For stand-alone applications, a dedicated power supply module (MPS Option) provides the reference signal.

The WJ-8628-4 can demodulate AM, FM, CW, SSB and Pulse signals. Four customer selectable IF bandwidths are available that can be changed in the field for added versatility. The 3 dB IF bandwidth options range from 3.2 kHz to 4 MHz. Simultaneous AM and FM audio, selectable AM or FM video output, signal monitoring and a 21.4 MHz IF output are also available.

The receiver front panel includes both a general purpose keypad for direct entry of all parameters, and a tuning knob for manual tuning of frequency, COS threshold and BFO offset. Front panel versatility is enhanced with dedicated control of detection mode, IF bandwidth, gain mode, RF and audio gain. Additional dual purpose keys facilitate control of the WJ-8628-4's memory in both the stand alone and Handoff Option (MH Option) applications with a minimum of operator training.

The microprocessor-controlled liquid crystal display (LCD) provides a 48-character alphanumeric and graphic display of operating status. In the normal mode, all receiver parameters are indicated, including an easy-to-read bar graph comparison of the relative signal strength versus the squelch threshold. A tuning indicator with 13 discreet positions provides an aid for accurate centering of signals. The versatile display also permits special setup modes such as Scan Set, where easy, comprehensive messages provide all pertinent information regarding step channel scanning (standard feature) or optional f1/f2 sector scanning (SCAN Option).

Operator training time is minimized with the front panel ability to display error conditions using clear, concise phrases. Interactive prompting and corrective procedures written on the display greatly enhance the user's confidence in the receiver.

The standard memory configuration of the WJ-8628-4 provides up to 56 kilobytes of ROM and 8 kilobytes of RAM with battery backup for all memory channels. The basic receiver uses approximately 2/3 of this capacity, supporting additional software for special applications. For expanded data collection requirements, 8 kilobytes of RAM may be substituted for ROM in the unit's memory.

The WJ-8628-4 is capable of remote talk-listen communication when installed in a properly configured WJ-9040 equipment frame, or as a stand-alone unit with the I/O Option.

An external controller (i.e., terminal or computer) can interrogate the receiver's status at any time. When the receiver is in the Remote mode, either from a front panel key entry or a remote command, the controller can send a new status to the WJ-8628-4. The controlling device also has the ability to store and recall any of the 99 memory channels, and perform scan functions.

When used as a Master Receiver Controller (MH Option), the receiver generates a high-speed WJ-9040 System I/O data stream. Connecting this 50-ohm link to a properly configured equipment frame achieves direct control of all the 1/4 rack (HF or VHF/UHF) receivers in that frame.

Maintenance operations are straightforward due to clean mechanical packaging and placement of nearly all components on plug-in circuit boards. These circuit boards mount on motherboards with most pins accessible from the bottom of the receiver. Removing the top cover exposes the assemblies, which may be unplugged from their sockets or freed from the main chassis by quick disconnect plugs.

1.2 MECHANICAL CHARACTERISTICS

The receiver is normally mounted in a 19-inch WJ-9040 EFR100 Equipment Frame and occupies one half the width of the frame. The main chassis, front, rear, and top internal compartment panels are nickel plated brass. All operating controls and indicators are on the front panel, while all input and output lines are routed through the rear panel (except for the PHONES jack).

The front panel is overlaid with a black bezel etched with control markings. The keypads are mounted on a printed circuit board and extend through cutouts in the front panel. The alphanumeric display is mounted on a circuit card positioned behind a cutout in the front, over which a polarized filter is installed. The PHONES jack, RF GAIN and AUDIO GAIN controls are also mounted on the front panel.

The rear panel mounts all input and output connectors. A 25-pin D series connector interfaces the required control I/O, DC supply voltages and polled I/O signals between the receiver and the EFR100 Equipment Frame. Five SMA coaxial connectors interface the RF input, 50 MHz reference input, signal monitor, selected video, and IF outputs. A nine-pin SRE series connector interfaces the auxiliary output signals.

Removing eight screws from the rear panel mounting bracket allows each of the four main compartments to be separated from the receiver. The RF Tuner, IF Demodulator, Synthesizer and Digital Control Sections are each mounted in separate enclosures for mechanical support and shielding. Most of the interconnections are made with push-on multi-pin plugs.

1.3 OPERATIONAL OVERVIEW

The following paragraphs describe the WJ-9040 operational environment in terms of its interaction with the WJ-8628-4 VHF/UHF Receiver. Included are definitions of the hardware interface between the receiver and the WJ-9040 System and an overview of the data interchanges that occur.

1.3.1 BASIC SYSTEM ORGANIZATION

The WJ-8628-4 VHF/UHF Receiver is part of the WJ-9040 Receiving System Family and will typically be operated in a WJ-9040 System environment. The receiver is designed to plug into the WJ-9040 EFR100 Equipment Frame. This frame defines the interface point between the receiver and the WJ-9040 System. The receiver receives all DC power, control instructions and commands via a 25-pin D type connector that mates with a counterpart on the equipment frame. The WJ-9040 System is designed to communicate with the receiver from two primary sources: a WJ-9040 System Receiver Controller or an external control device via an RS-232/IEEE-488 Interface. Both sources interface with the receiver through the IOM108 I/O Control Module on the equipment frame. Actual communication with the receiver is via a 54-bit serial data stream connecting the IOM108 and the receiver. In addition, a FRM150 Frequency Reference Module, or SRM105A Site Reference Module, supplies a 50 MHz signal to the receiver synthesizers. **Figure 1-2** is a simplified block diagram showing the relationship between the major elements in the WJ-9040 System.

1.3.2 EQUIPMENT REQUIRED BUT NOT SUPPLIED

The following items are a minimum complement necessary to obtain use of the receiver if it is to be configured as a component in a WJ-9040 Receiving System.

- EFR100 Equipment Frame
- EPS100 Power Supply
- SRM105A Site Reference Module (or FRM150 Frequency Reference Module)
- IOM108 I/O Control Module with DIO232 or DIO488 Interface (necessary only for interface with external controller)
- Antenna, 50 ohms
- Audio Monitoring Equipment:

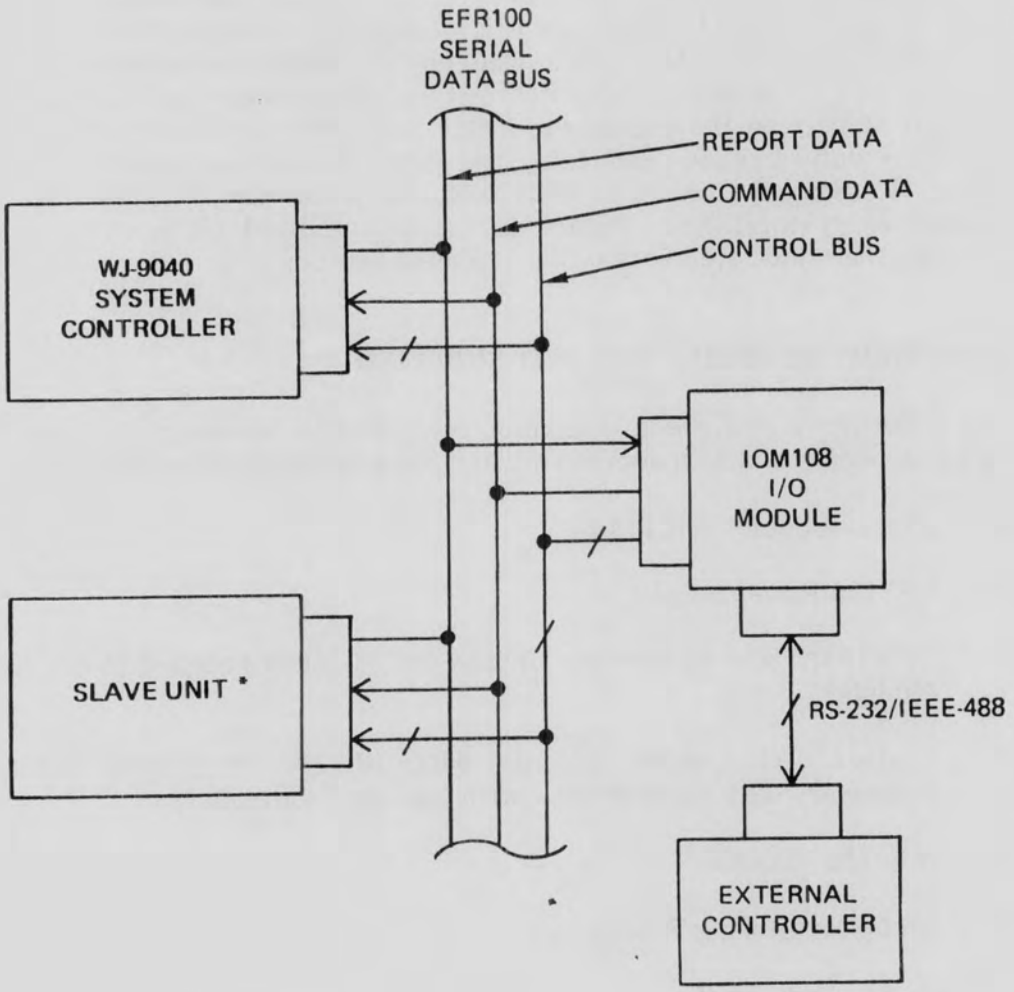
  a. Speaker panel
  b. Headphones
  c. Tape recorder

For stand-alone use, a dedicated power supply and frequency reference module are available.

1.3.3 OPTIONAL EQUIPMENT

The following equipment is available for use with the WJ-8628-4 Receiver. For additional information, contact the Watkins-Johnson Company, Gaithersburg, Maryland or your Watkins-Johnson representative.

- 500-1400 MHz Frequency Extender



*HF SLAVE RECEIVER DEMODULATOR

Figure 1-2. WJ-9040 System Configuration

- Dual RF Antenna Inputs (20-500 MHz and 500-1400 MHz with FE Option)
- Digitally Refreshed Display Output

1.4 EQUIPMENT SPECIFICATIONS

See **Table 1-1** for receiver specifications and **Table 1-2** for IF bandwidth options and sensitivity levels.

Table 1-1. WJ-8628-4 VHF/UHF Receiver Specifications

Tuned Frequency	20 to 512 MHz (20 to 1400 MHz with FE Option)
Tuning Resolution	100 Hz
Synthesizer Tuning Speed	10 ms, typical
Input Impedance	50 ohms, unbalanced, nominal
IF Bandwidths (3 dB)	Four (4), customer selectable from 10 kHz to 4 MHz and SSB
Detection Modes	Standard: FM, AM, CW, Pulse, SSB
Gain Control Modes	Manual, AGC
AGC and Manual Range	90 dB, minimum
Synthesized BFO	±4.0 kHz in 10 Hz steps
IF Rejection	Greater than 90 dB
Image Rejection	Greater than 90 dB
Sensitivity	See **Table 1-2**
IF Output	-20 dBm at sensitivity level, 21.4 MHz
Signal Monitor Output	21.4 MHz, 6 MHz bandwidth
Third Order Input Intercept Point	0 dBm, minimuum
Video Amplifier Response	Within 3 dB from 20 Hz to 1/2 IF Bandwidth
Video Output Level	350 mV rms into 75 ohms
Video Distortion	Less than 5% total Harmonic Distortion in AGC or Manual Gain Modes
Phones Output	10 mW minimum into 600 Ω phones
Signal Strength Output	Shaped DC AM Detector output, 0 to +10 Vdc
Squelch/COR	Adjustable threshold from noise level to 50 dB above noise. COR holds a nominal 4 seconds after carrier disappears.
Digital Control	72 Bit Serial Word (WJ-9040 System compatible)
Temperature, Operating	0° to +50° C
Size	5.2 inches (132 mm) high, 8.0 inches (203 mm) wide and 14.38 inches (365 mm) deep
Weight	Approximately 17 lbs (7.7 kg)
Power Consumption	Approximately 15 watts (From +8.2, -18.3, +18.3, +29 Vdc)

Table 1-2. IF Bandwidth Options and Sensitivity Levels

IF Bandwidth	RF Input Sensitivity (dBm)
10 kHz	-105
20 kHz	-102
50 kHz	-98
100 kHz	-95
200 kHz	-92
500 kHz	-88
1 MHz	-85
2 MHz	-82
4 MHz	-79

SECTION II

INSTALLATION AND OPERATION

2.1 UNPACKING AND INSPECTION

Examine the shipping carton for damage prior to unpacking the equipment. If the carton appears to be damaged, have the carrier's agent present when the equipment is unpacked. If this is not possible, retain all packaging material and shipping containers for the carrier's inspection to verify damage to the equipment after unpacking. Also verify that the equipment shipped corresponds to the packing slip. Contact the Watkins-Johnson Company, CEI Division, or your Watkins-Johnson representative for any discrepancies or shortages.

The unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. It is, therefore, ready for use upon receipt. After uncrating and checking the contents against the packing slip, visually inspect all exterior surfaces for dents and scratches. If external damage is visible, remove the dust covers and inspect the internal components for apparent damage. Then check the internal cables for loose connections, and plug-in items such as printed wiring boards, which may have been loosened from their receptacles.

2.2 REPACKING

If the equipment must be prepared for reshipment, the packing methods should follow the pattern established in the original shipment. If retained, the original materials can be reused to a large extent or at least provide guidance for the repackaging effort. Conditions during storage and shipment should be limited as follows:

Maximum humidity: 95% (no condensation)
Temperature Range: - 40°C to 85°C

2.3 INSTALLATION PROCEDURES

The WJ-8628-4 VHF/UHF Receiver is designed to mount in the EFR100 Equipment Frame. Specific installation procedures for the EFR100 are covered in the WJ-9040 System Common Equipment Instruction Manual. However, the following general guidelines should be observed when using the receiver in the WJ-9040 Operational Environment:

1. Operating temperature range should be from 0°C to +50°C.

2. Free air circulation should be allowed between equipment frames. Multiple stacking significantly increases ambient temperatures.

3. Use only stable, properly grounded AC power for the WJ-9040 equipment.

4. Secure the receiver in the frame by rotating the four front panel locking screws clockwise until tight.

2.3.1 INPUT/OUTPUT CONNECTORS

The receiver's input/output connectors are shown in **Figure 2-1.** These connectors are physically mounted on the receiver rear panel. Two 25-pin D type connectors (J1 and A3J1) mate with a counterpart in the EFR100 Equipment Frame to provide DC power and control signals to the receiver and status indication outputs. Five SMA female connectors provide signal input and output connections. A nine-pin SRE female connector (J4) provides auxiliary outputs from the demodulator. These connectors are described individually in the following paragraphs.

2.3.1.1 Power, Command/Control (J1)

The Power Command/Control 25-pin D type connector mates with the stand-alone power supply (MPS Option) or any one of connectors J1-J8 on the EFR100 to supply DC voltage and I/O command and control signals to the receiver. Status conditions, including signal strength, squelch status, AFC Voltage and synthesizer lock, are polled by the IOM108 via this connector.

2.3.1.2 50 MHz Reference Input (J2)

The 50 MHz Reference Input SMA connector must be connected to either J1, J2, J3, or J4 on the FRM150 or other highly stable 50 MHz signal (50 ohm, 0 dBm), to provide a reference for the receiver's synthesizers.

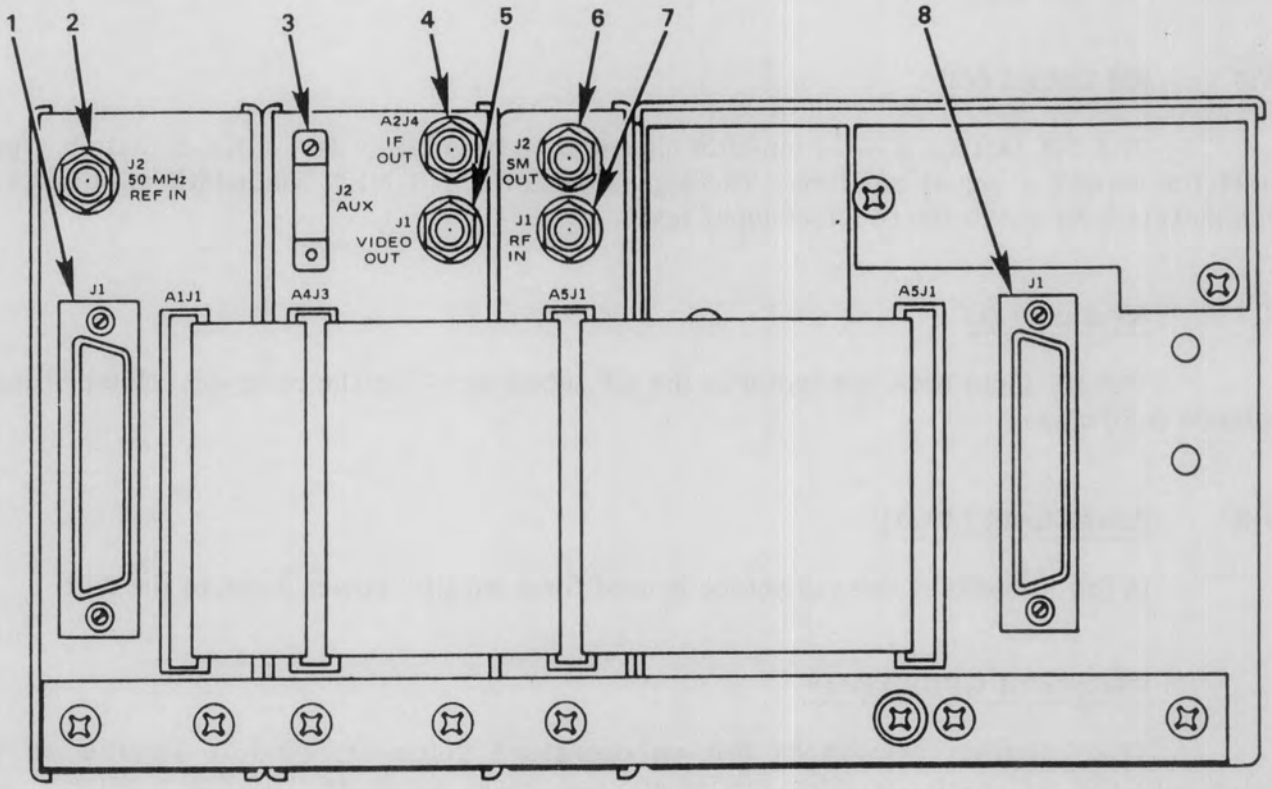
2.3.1.3 Auxiliary Output (J2)

The Auxiliary Output nine-pin SRE female connector provides outputs from the receiver's demodulator section. These outputs are for connection to user-selected interface devices. The pin assignments are as follows:

A - Ground
B - FM Audio Output (5 kΩ impedance)
C - AM/CW/SSB Audio Output (5 kΩ impedance)
D - Signal Strength Output (analog 0 to +10 Vdc, 10 kΩ)
E - Carrier Operated Relay (open collector, 30 mA sink to ground, +24 Vdc max)
F - Carrier Operated Squelch (0 or + 5 Vdc CMOS driver)
H - Sweep REV (+10V to +15V = non-inverted spectrum, OPEN = inverted spectrum)
J - Squelched Audio Output (600 ohm impedance)
K - AFC Voltage (±2.5V for IF BW) (10 kΩ)

2.3.1.4 IF Output (A2J4)

The IF Output SMA connector supplies an IF bandwidth limited 21.4 MHz IF output signal. The level will be 20 mVrms minimum into 50 ohms with an input signal level equivalent to AGC threshold.



1. Power, Command/Control (J1)
2. 50 MHz Reference Input (J2)
3. Auxiliary Output (J2)
4. IF Output (A2J4)
5. Video Output (J1)
6. SM Output (J2)
7. RF Input (J1)
8. Power (A3J1)

Figure 2-1. Receiver Input/Output Connectors

2.3.1.5 **Selected Video Output (J1)**

The Selected Video Output SMA connector supplies a bandwidth limited video output signal from the AM, FM, CW or SSB detector as selected. The AC coupled signal has a bandwidth from 20 Hz to one-half the IF bandwidth at a level of 350 mVrms into 75 ohms.

2.3.1.6 **SM Output (J2)**

The SM Output SMA connector provides a broadband 21.4 MHz IF output signal suitable for driving a signal monitor. The signal occupies a 6 MHz bandwidth at a level of approximately 5 dB above the receiver input level.

2.3.1.7 **RF Input (J1)**

The RF Input SMA connector is the RF signal input for the receiver. Nominal input impedance is 50 ohms.

2.3.1.8 **Power Input (A3J1)**

In the WJ-8628-4 this connector is used for a parallel power input to the unit.

2.4 RECEIVER OPERATION

The following paragraphs are an operator's guide designed to familiarize the operator with the different operating modes and sequences available with the receiver. The function and use of the front panel controls and indicators are explained and detailed receiver operating instructions are provided.

2.4.1 INTRODUCTION

The WJ-8628-4 VHF/UHF Receiver incorporates the following operational features:

- Local receiver control through momentary contact keypad switches and a tuning knob on the front panel.
- Ninety-nine discretely addressed and one implicitly addressed memory channels. The channels are utilized to store front panel data. They may be accessed individually or scanned.
- A memory scan mode in which the receiver scans a selected group of channels.
- An F1/F2 frequency sector scan mode in which the receiver scans an operator programmed frequency sector (Scan Option).

- Remote control capability through the IOM108 interface or stand-alone I/O interface.
- Software flexibility allowing implementation of customer enhancements.

2.4.2 CONTROLS AND INDICATORS

The purpose and function of the front panel controls, keypad switches and displays are explained in the following paragraphs.

2.4.2.1 Front Panel Controls

Refer to **Figure 2-2** for the location of each of the following front panel controls.

2.4.2.1.1 BACKLIGHT ON Switch

When lifted to the ON position, the BACKLIGHT ON Switch energizes the illuminated backlight in the LCD display. This backlight enhances display readability when a low ambient light level is present. The intensity of the backlight illumination is adjustable inside the unit. See **paragraph 4.6.7.**

2.4.2.1.2 DISPLAY ADJUST Potentiometer

The DISPLAY ADJUST Potentiometer adjusts the vertical viewing angle of the LCD display characters. The characters are invisible at maximum CCW and the display is totally illuminated at maximum CW. The operator may adjust this control for optimum display contrast.

2.4.2.1.3 RF GAIN Control

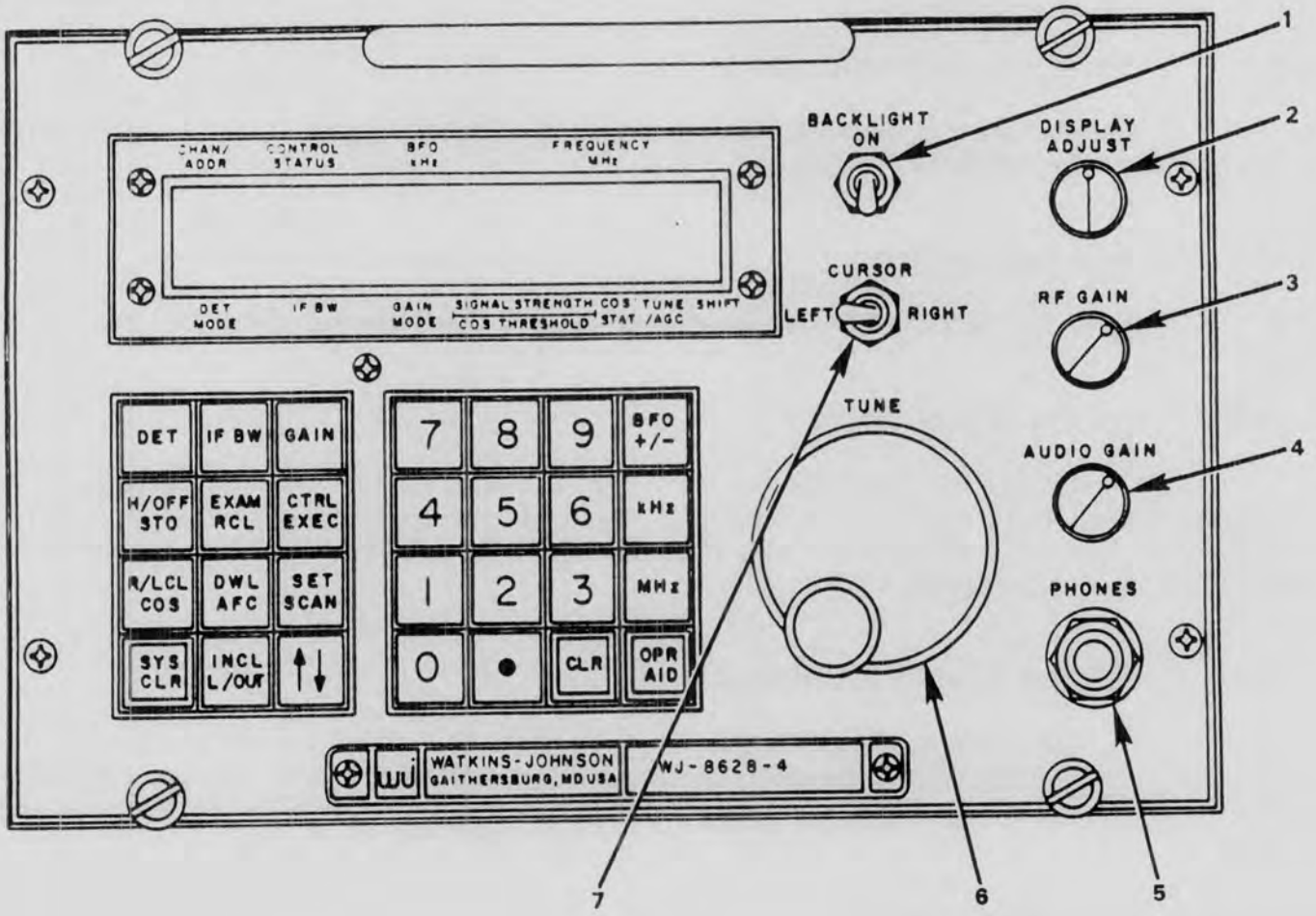
When in the Manual (MAN) gain mode, rotating the RF GAIN Control potentiometer clockwise approximates a logarithmic increase in receiver gain. The RF GAIN control is inoperative when any AGC mode is selected.

2.4.2.1.4 AUDIO GAIN Potentiometer

Rotating the AUDIO GAIN Potentiometer clockwise increases the output of the phone audio signal from the front panel PHONES jack.

2.4.2.1.5 PHONES Jack

The PHONES output is intended to drive a 600 ohm or greater headphone set. An output level of 10 milliwatts, minimum, into 600 ohms is available when the AUDIO GAIN control is at maximum clockwise.



1. BACKLIGHT ON Switch
2. DISPLAY ADJUST
3. RF GAIN
4. AUDIO GAIN
5. PHONES Jack
6. TUNE Knob
7. Cursor Control Switch

Figure 2-2. Receiver Front Panel Controls

2.4.2.1.6 TUNE Knob

The TUNE Knob is used to manually set the receiver's tuned frequency, BFO frequency or COS (Carrier Operated Squelch) threshold. When used for frequency setting, the knob is rotated clockwise to numerically increase the receiver's tuned frequency or BFO frequency. When used for COS threshold setting, the knob is rotated clockwise to numerically increase the receiver's squelch threshold (0 minimum, 63 maximum, software controlled).

2.4.2.1.7 Cursor Control Switch

The Cursor Control Switch is used to position the LCD display cursor (underscore) to permit the TUNE knob to control tuned frequency, BFO frequency or COS threshold. The switch is toggled either left or right to move the cursor to the desired position. When the cursor is in the proper position, the TUNE knob may be rotated to adjust the desired parameter. The cursor can also be moved to the far right edge of the screen where the TUNE knob is disabled, dictated by a left-pointing arrow adjacent to the frequency display.

2.4.2.2 Front Panel Keypad Switches

Refer to **Figure 2-3** for the location of each of the following front panel keypad switches.

2.4.2.2.1 BFO +/- Switch

In the CW mode, the BFO +/- Switch is used for direct entry of BFO offset frequencies. Numeric data in kHz (**paragraph 2.4.2.2.6**) is entered followed by the BFO +/- switch as a termination command. If no data is entered, the switch will toggle the offset from "+" (above the tuned signal) to "-" (below the signal).

2.4.2.2.2 kHz Switch

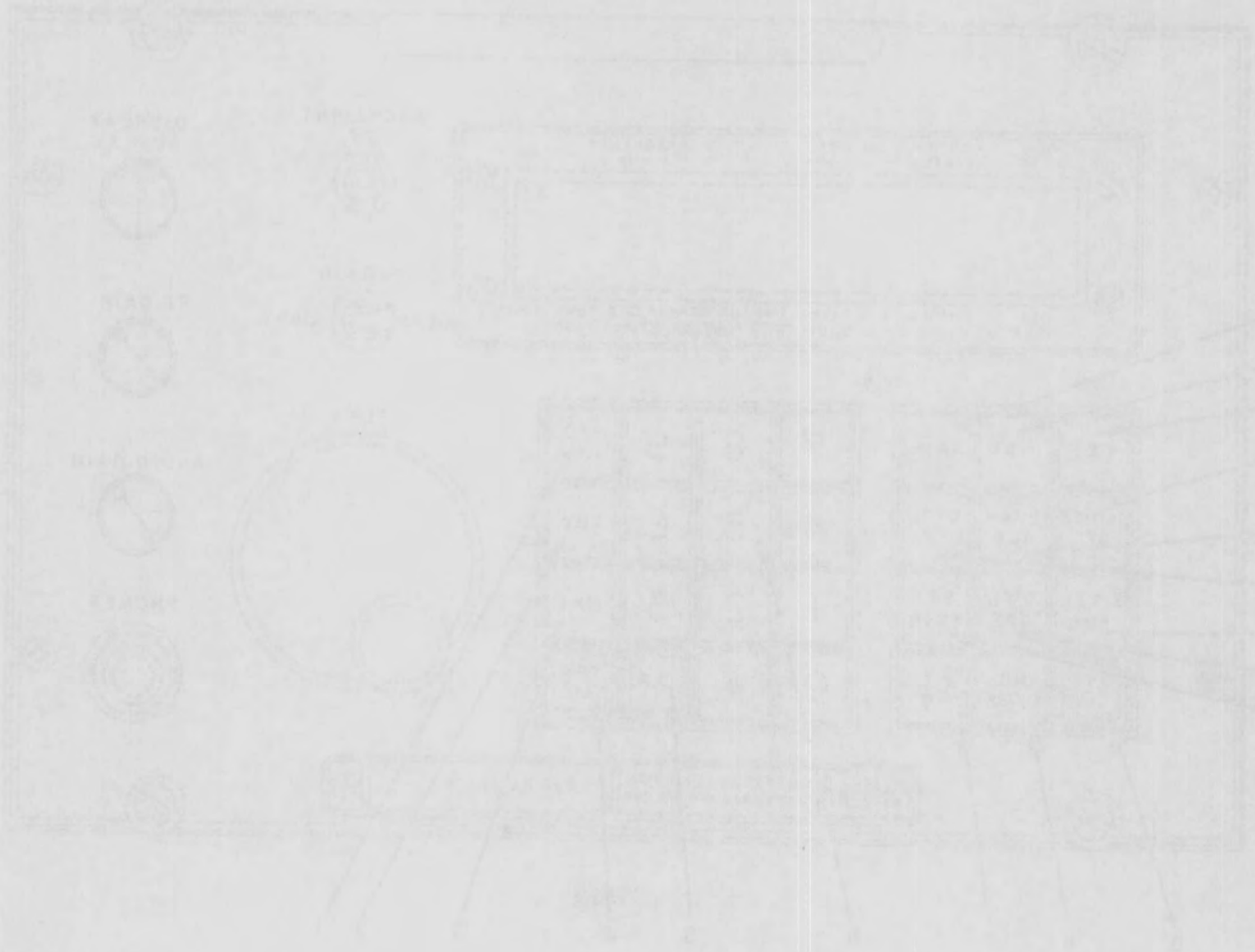
The kHz Switch is used for direct entry of the receiver tuned frequency. Numeric data is entered followed by the kHz switch as a termination command. This key is allowed only when controlling a HF or VHF receiver when the MHO Option is installed.

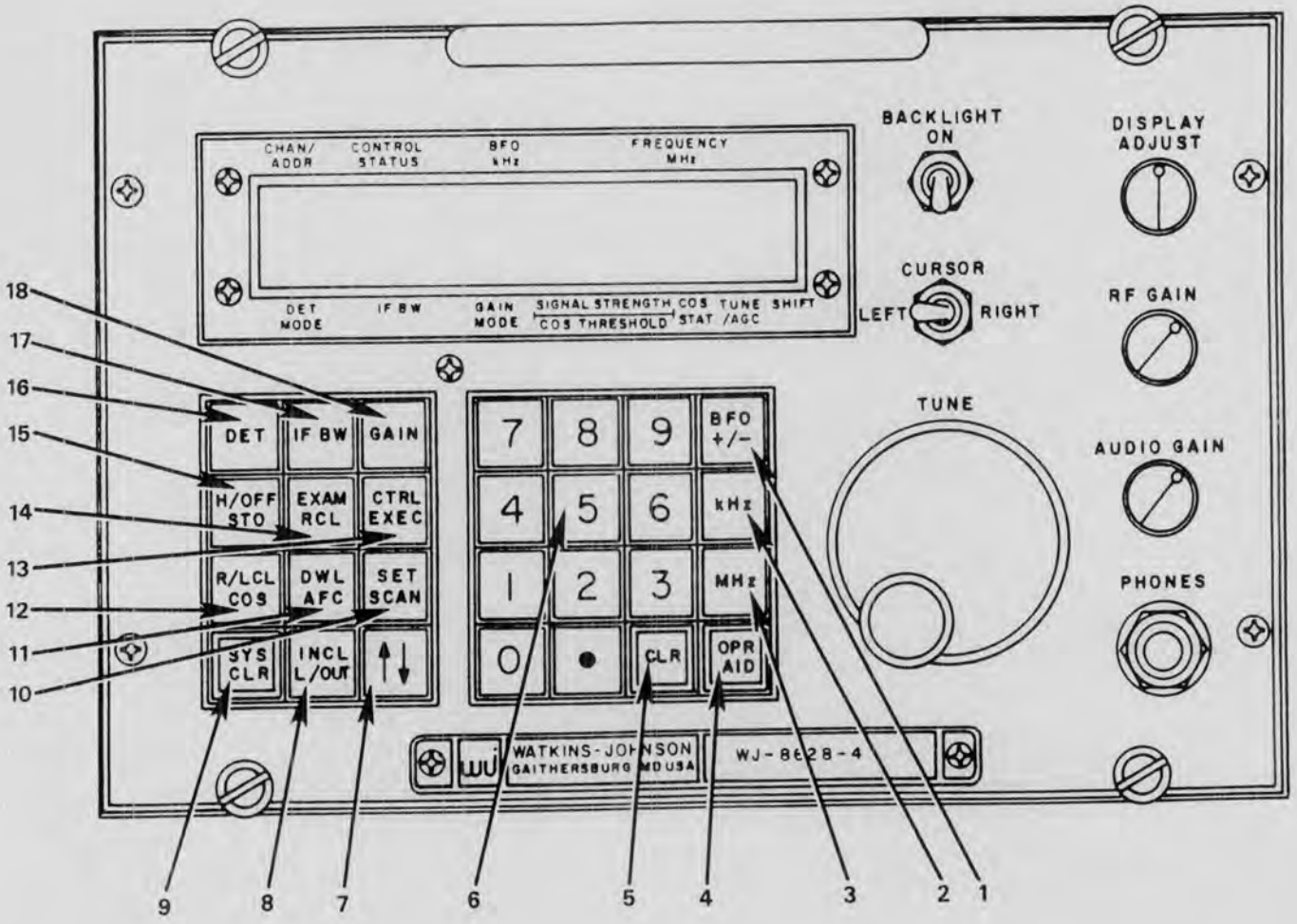
2.4.2.2.3 MHz Switch

The MHz Switch is used for direct entry of the receiver tuned frequency. Numeric data is entered followed by the MHz switch as a termination command.

2.4.2.2.4 OPR AID Switch

The OPR AID Switch accesses software designed to aid the operator in understanding the sequences and functions available with the receiver.





1. BFO +/- (BFO Offset Entry Switch)
2. kHz Tuned Frequency Entry
3. MHz Tuned Frequency Entry
4. OPR AID (Operator Aid Switch)
5. CLR (Numeric Entry CLEAR Switch)
6. Numeric Entry Switches 0-9
7. (Lower Case/Upper Case Selection)
8. INCL L/OUT (Include/Lock Out Memory Channels), (SCAN function)
9. SYS CLEAR (System Clear)
10. SET SCAN (SCAN/SCAN SET select)
11. DWL (Dwell select), (SCAN function)
12. L/LCL COS (COS Threshold Set/ Remote and Local Select)
13. EXEC (Execute Select)
14. RCL (Recall Select)
15. STO (Store Select)
16. DET (Detection Mode Select)
17. IF BW (IF Bandwidth Select)
18. GAIN (Gain Mode Select)

Figure 2-3. Front Panel Keypad Switches

2.4.2.2.5 CLR Switch

The CLR (CLEAR) Switch, when pressed after a numeric data entry, clears the display of the numeric data and returns the display to normal status. The entered numeric data is not processed by the receiver. This switch also clears any error messages and restores the previous display.

2.4.2.2.6 Numeric Switches 0–9

The Numeric Switches are used for direct entry of numeric data required for tuned frequency, BFO offset, COS threshold, memory channel access, dwell time, etc.

2.4.2.2.7 Upper Case/Lower Case Switch

This switch is the upper case/lower case access switch. Some of the keypad switches are dual function, as indicated on the face of the switches. The upward pointing arrow is used to access the upper case functions on these switches, and the downward pointing arrow is used to access the lower case functions. The switch toggles the arrow shown in the lower right corner of the LCD.

2.4.2.2.8 INCL/L-OUT Switch

The INCL/L-OUT Switch is a dual function switch. The upper case INCL function is used as a termination command to INCLUDE a memory channel or string of channels in a scan. The lower case L/OUT function is a termination command to LOCK OUT a memory channel or string of channels from a scan.

2.4.2.2.9 SYS CLR Switch

The SYS CLR Switch accesses the SYSTEM CLEAR routine which allows the operator to empty all memory channel locations and reinitialize the receiver. The IOM108 units connected via the frame or WJ-9040 Serial I/O can also be cleared by following the prompts.

2.4.2.2.10 SET/SCAN Switch

The SET/SCAN Switch is a dual function switch. The upper case SET function is the SCAN SET mode which allows the operator to review and modify parameters associated with SCANNING. Pressing SET again terminates this mode. The lower case SCAN function is the SCAN mode which performs a scan of selected memory channels. Pressing the SCAN key again terminates the scan.

2.4.2.2.11 DWL Switch

The DWL Switch is the DWELL mode select which allows the operator to program the various dwell times associated with scan functions, or examine the current dwell time values.

2.4.2.2.12 **R/LCL COS Switch**

The R/LCL COS Switch is a dual function switch. The upper case R/LCL function toggles the receiver between the REMOTE and LOCAL modes of operation. The lower case COS (Carrier Operated Squelch) function is used as a termination command for direct entry of COS threshold data, or to examine the numeric value of COS threshold.

2.4.2.2.13 **EXEC Switch**

The EXEC Switch is a termination command for the EXECUTE mode. The function is used to directly control the status of the receiver section of the WJ-8628-4 from channel 0 or any of the 99 stored memory channels.

2.4.2.2.14 **RCL Switch**

The RCL Switch is a termination command which changes the CONTROL STATUS to RCLm (RECALL MEMORY). The contents of one of the stored memory channels is displayed without changing the receiver status.

2.4.2.2.15 **STO Switch**

The STO Switch is a termination command which stores all the currently displayed parameters into the designated memory channel.

2.4.2.2.16 **DET Switch**

The DET Switch is used to select one of the available detection modes and is repeatedly pressed until the desired detection mode is displayed.

2.4.2.2.17 **IF BW Switch**

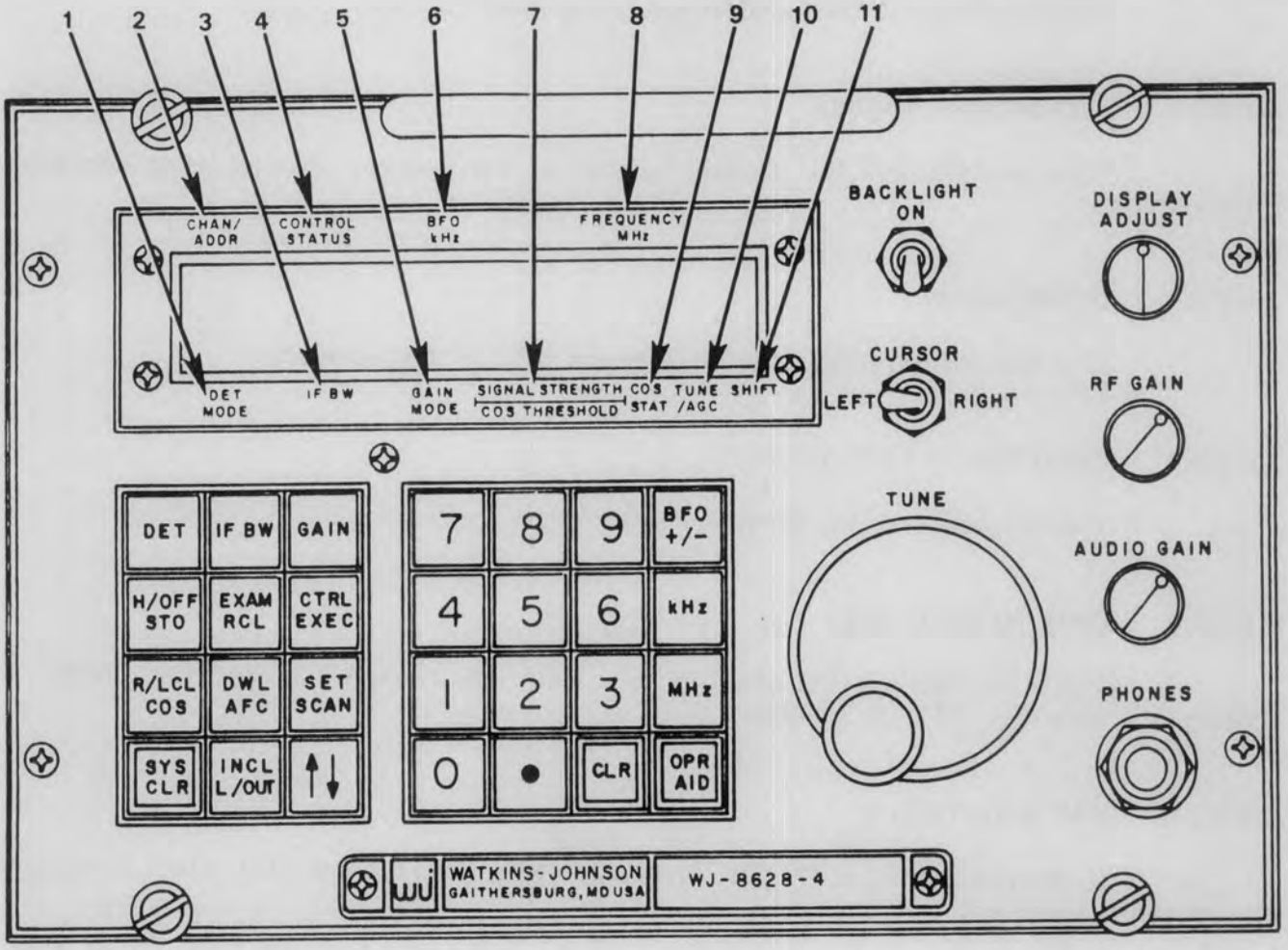
The IF BW Switch is used to select one of the available IF bandwidths and is repeatedly pressed until the desired bandwidth is displayed.

2.4.2.2.18 **GAIN Switch**

The GAIN Switch is used to select one of the available gain modes and is repeatedly pressed until the desired gain mode is displayed.

2.4.2.3 **Front Panel Display**

Refer to **Figure 2-4** to locate the display areas described in the following paragraphs.



1. DET MODE (Detection Mode)
2. CHAN/ADDR (Channel/Address)
3. IF BW (IF Bandwidth)
4. CONTROL STATUS
5. GAIN MODE
6. BFO Offset
7. SIGNAL STRENGTH/COS THRESHOLD
8. FREQUENCY (MHz), (Receiver Tuned Frequency)
9. COS STAT (Carrier Operated Squelch Status)
10. TUNE/AFC (AFC Tuning Indicator)
11. SHIFT (upper/lower case functions)

Figure 2-4. LCD Parameter Display Locations

2.4.2.3.1 **DET MODE Display**

This area displays the selected detection mode for the receiver.

2.4.2.3.2 **CHAN/ADDR Display**

This area displays the channel number of the memory channel being accessed by the receiver.

2.4.2.3.3 **IF BW Display**

This area displays the selected IF bandwidth for the receiver.

2.4.2.3.4 **CONTROL STATUS Display**

This area displays the specific control mode the front panel is executing.

2.4.2.3.5 **GAIN MODE Display**

This area displays the specific gain mode the receiver is operating under. The three gain modes are: FST, SLO, and MAN.

2.4.2.3.6 **BFO (kHz) Display**

If the receiver is in the CW mode, this area displays the BFO offset frequency in kHz currently selected.

2.4.2.3.7 **SIGNAL STRENGTH/COS THRESHOLD Display**

This is a dual purpose display area. It gives a graphic comparison of relative signal strength vs. COS threshold. The upper bar shows signal strength. The length of the upper bar increases from left to right as the signal strength increases. The lower bar shows the COS threshold. The length of the lower bar corresponds to the magnitude of COS threshold entered. A COS of 0 is shown as no bar length (bar completely collapsed at the left). A COS of 63 is shown by maximum bar length. The COS threshold is exceeded when the signal strength bar exceeds the length of the COS bar. The numeric value of the COS threshold appears in place of the bars when the COS key is pressed with no previous data entry.

2.4.2.3.8 **FREQUENCY (MHz) Display**

If no numeric data is entered, this area shows the tuned frequency of the receiver in MHz. When numeric keys are pressed, the frequency information is erased and the data is entered calculator style in the frequency area. Data entry is identified by the flashing arrow symbol in the upper right corner of the display.

2.4.2.3.9 COS STAT Display

This area displays a star (*) when the received signal strength exceeds the COS threshold.

2.4.2.3.10 TUNE/AFC Display

This area serves as a visual tuning indicator for the receiver. When the receiver is exactly tuned on a signal, the tuning indicator is displayed as a vertical bar. Mistuning of the receiver is displayed as a right or left deflection of the tuning indicator. On receivers equipped with AFC, this indicator is replaced by the letter "A" when AEC is selected. The correct tuning is then handled by the digital AFC circuitry.

2.4.2.3.11 SHIFT Display

This area displays an upward pointing arrow when the upper case key functions with white lettering have been selected, and displays a downward pointing arrow when lower case key functions with black lettering have been selected. Single-color labels positioned in the center of the 'key' buttons are active in either upper or lower case.

2.4.3 OPERATING PROCEDURES

The following paragraphs are a detailed description of the techniques required to correctly operate the receiver. The operating procedures are provided in five separate units: Initializing, Local Mode, Remote Mode, Memory Functions and Scanning. The operator should first become familiar with the functions of the controls and indicators (**paragraph 2.4.2**) before proceeding.

The mode currently in use by the receiver is indicated in the CONTROL STATUS area of the display (**paragraph 2.4.2.3.4**). The CONTROL STATUS indications are briefly explained as follows:

1. EXEC

   The EXEC (EXECute) mode directly controls the status of the receiver section of the WJ-8628-4. All keys are enabled. Any activated key which alters receiver parameters causes this information to be immediately transferred to the receiver.

2. RCLm

   The RCLm (Recall memory) mode displays the contents of the selected memory channel 1 to 99 without causing a change to the receiver section. Any change made to a parameter during RCLm mode changes only the LCD, and is not immediately restored in memory. The display status changes to MODm (MODified memory), prompting the operator to use the STO key (**paragraph 2.4.2.2.15**) if the changes are desired.

3. SCANNING

The SCAN key is used to activate the SCAN MODE. In this mode, SCANNING is displayed in the control status area and the selected channels are successively executed by the receiver and tested for a signal presence above the selected COS threshold. When a signal is found above threshold, the complete status of that channel is displayed and the dwell time begins.

4. RMT

In the RMT (Remote) mode, all receiver operations are under the control of an external device. All front panel keys (except R/LCL) are locked out. Pressing the R/LCL switch changes the Control Status to EXEC.

2.4.3.1 Initializing the Receiver

Whenever power is applied to the WJ-8628-4, an initialization sequence is performed. Depending upon the hardware and software options installed, and the associated WJ-9040 System components connected to the WJ-8628-4, some initialization steps may or may not be executed. In all cases, the following tests and commands are performed.

1. The I/O interface is initialized and enabled for communication with an external controller.

2. The main 8 kilobytes of RAM used by the microprocessor are write/read tested. Any error found is displayed.

3. All IF Bandwidth modules are identified for display and SSB offset purposes. The presence of certain receiver options is also checked.

4. The previous tuning status (frequency, detection mode, etc., retained in battery-backed memory) is sent to the receiver.

5. The previous front panel CONTROL STATUS, also retained by the battery, is enabled. The receiver's operating mode is now either RMT or EXEC, and the initialization is finished.

The configuration of the Master/Handoff Subsystem (MHO Option) also takes place on power-up. Refer to **paragraph 2.4.3.6.3**, Initialization on Power Up.

2.4.3.2 Local Mode Operation (EXEC)

The following paragraphs describe the basic local mode operating procedures for the receiver. Local mode procedures permit the operator to set the receiver's tuned frequency, BFO offset, detection mode, IF bandwidth, gain mode and COS (Carrier Operated Squelch) threshold level. Direct control over the local receiver using these procedures can only be achieved when the receiver is in the EXEC (EXECUTE) CONTROL STATUS mode with lower

case key functions selected. To ensure this condition, each of the following procedure examples is first preceded by three keypad entries:

lower case arrow Ø EXEC

If the receiver is already in this mode (hereafter called EXEC mode), these three keypad entries may be ignored. The local mode procedures are also used in the RECALL mode, as explained in **paragraph 2.4.3.3.4.**

2.4.3.2.1 **Detection Mode**

When depressed, if no numeric entries are present, the DET keypad steps the receiver through the available Detection Modes. In the EXEC mode, the current receiver Detection Mode is changed to agree with the Mode being displayed. The available Detection Modes are AM, FM, Pulse and CW. LSB and USB are options if the appropriate IF BW is installed. If a numeric entry precedes the DET keypad, the error message "Not expecting # before DET" appears and remains as long as the DET keypad is depressed. **Example 1** illustrates the method of selecting the Detection Mode.

- Det Mode Selection - Procedure

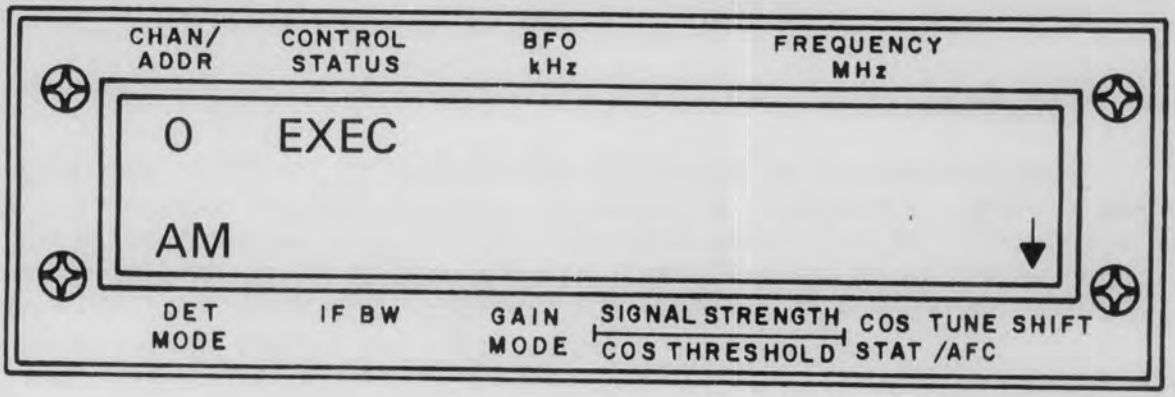
  1. If the Control Status is not "EXEC", press the lower case, 0 and EXEC keypads.

  2. Repeatedly press the DET keypad until desired DET mode is displayed.

Example 1. Select AM Detection Mode.

↓ 0 EXEC ..... (1) This places the receiver in EXEC mode as required for local operation.

DET ..... (2) Repeatedly press the DET keypad until AM is displayed as shown below.



2.4.3.2.2 IF Bandwidth

When depressed, if no numeric entries are present, the IF BW keypad steps through the IF bandwidths installed in the unit. In the EXEC mode, the current receiver bandwidth is changed to agree with the bandwidth being displayed. The available bandwidths are listed in **Table 1-2.** If a numeric entry precedes the IF BW keypad, the error message "Not expecting # before IF BW" appears and remains as long as the IF BW key is depressed. **Example 2** illustrates the method of selecting the IF Bandwidth.

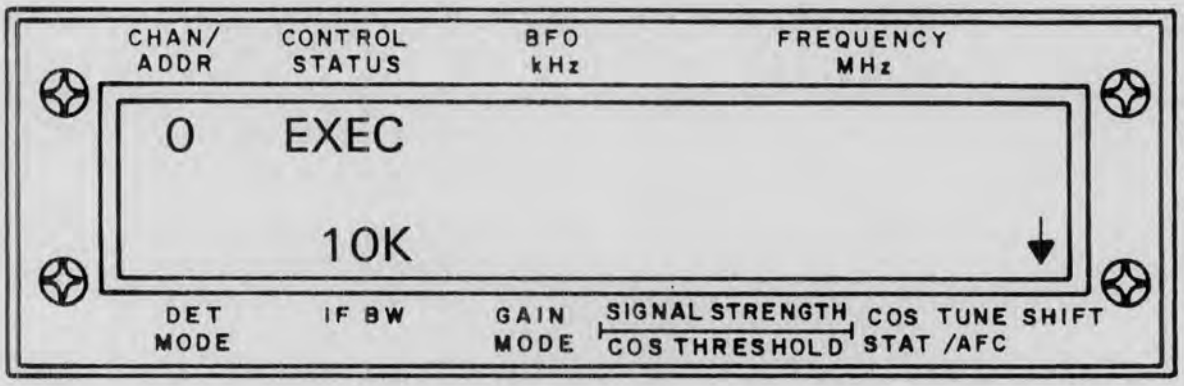
- IF Bandwidth Selection - Procedure

  1. If the Control Status is not EXEC, press the lower case, 0 and EXEC keypads.

  2. Repeatedly press the IF BW keypad until the desired BW is displayed.

Example 2. **Select 10 kHz Bandwidth.**

[↓] [0] [EXEC]	(1)	This places the receiver in EXEC mode as required for local operation.
[IF BW]	(2)	Repeatedly press the IF BW keypad until 10 is displayed as shown below.



2.4.3.2.3 GAIN Mode

When depressed, if no numeric entries are present, the GAIN Mode keypad steps through the available Gain Modes. In the EXEC mode, the current receiver Gain Mode is changed to agree with the mode being displayed. The available Gain Modes are MANUAL and AGC. The response time of the AGC circuit is automatically set by the selected detection mode and will be displayed as FST or SLO. If a numeric entry precedes the GAIN keypad, the

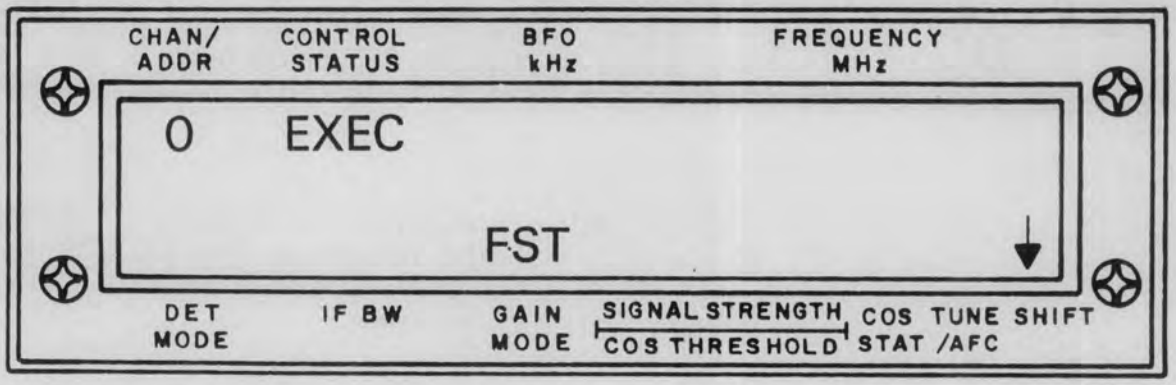
error message "Not expecting # before GAIN" appears and remains as long as the GAIN keypad is depressed. **Example 3** illustrates the method of selecting the Gain Mode.

- Gain Mode Selection - Procedure

  1. If the Control Status is not EXEC, press the lower case, 0 and EXEC keypads.
  2. Repeatedly press GAIN until the desired Gain Mode is displayed on the LCD display.
  3. When the MAN (Manual) Gain Mode is selected, the front panel RF Gain Control is activated. Rotating the control counterclockwise reduces the receiver gain, and clockwise rotation increases the gain.

Example 3. Select FST Gain Mode.

[↓] [0] [EXEC]	(1)	This places the receiver in EXEC mode as required for local operation.
[GAIN]	(2)	Repeatedly press the GAIN Mode keypad until FST is displayed as shown below.



2.4.3.2.4 **COS (Carrier Operated Squelch) Threshold**

When preceded by a numeric entry, depression of the COS keypad results in the processing of the numeric entry as a COS threshold level. If in the EXEC mode, the current receiver COS level is changed to agree with the level entered. When depressed, when no numeric entries are present, the COS keypad causes the LCD display to show the numeric value of the threshold level. This display remains as long as the COS keypad is depressed. The range of COS levels are from 0 to 63. **Examples 4** and **5** illustrate the use of the COS keypad.

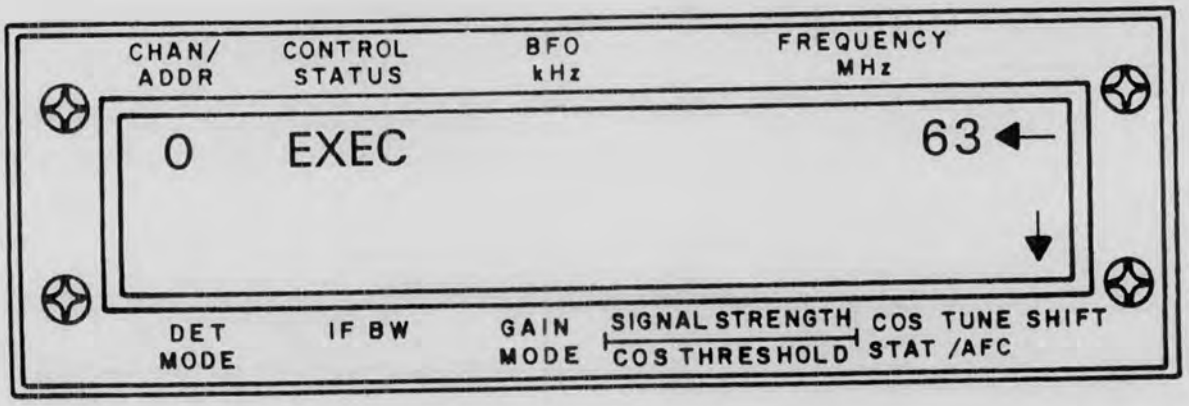
- COS Threshold Entry - Procedure

1. If the Control Status is not EXEC, press the lower case, 0 and EXEC keypads.
2. Enter desired 1 or 2 digit COS threshold.
3. Terminate by pressing COS keypad.

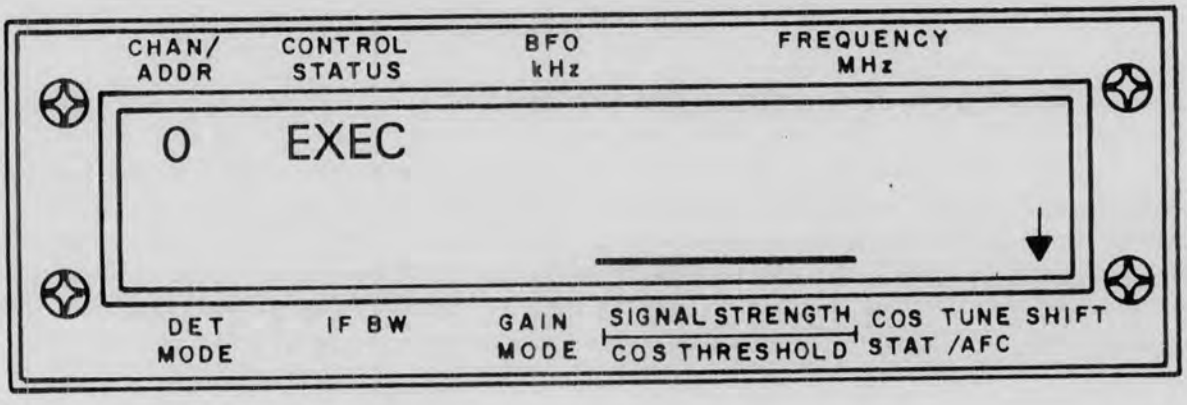
Example 4. Set COS Threshold Level to 63.

[↓] [0] [EXEC] ..... (1) This places the receiver in EXEC mode as required for local operation.

[6] [3] ..... (2) Desired threshold data entry, "63" is displayed in FREQUENCY (MHz) area of display as shown below.



[COS] ..... (3) Termination command: FREQUENCY (MHz) returns to normal, COS threshold bar shows maximum deflection to right as shown below.



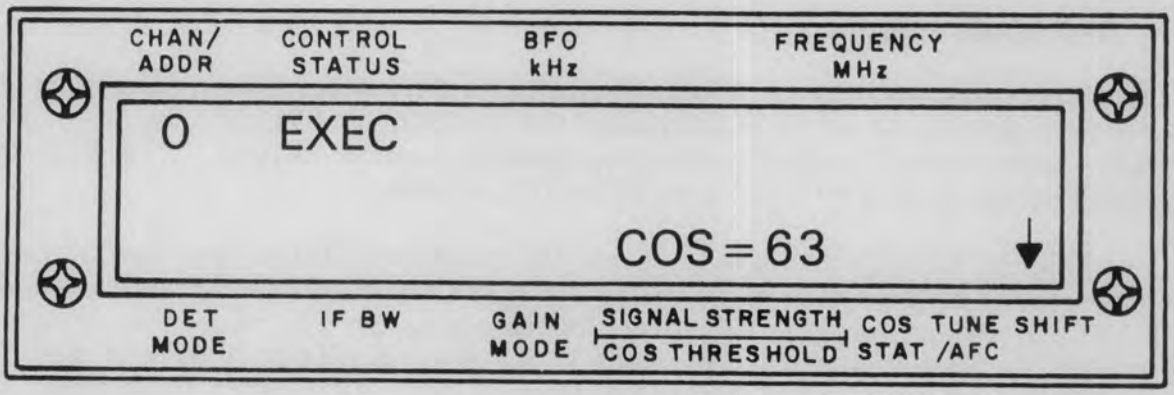
- COS Threshold Level Check - Procedure

  1. If the Control Status is not EXEC, press the lower case, 0 and EXEC keypads.

  2. Press the COS keypad and hold to display the data.

Example 5. Check the Current COS Threshold Level.

[↓] [0] [EXEC]	(1)	This places the receiver in EXEC mode as required for local operation.
[COS]	(2)	Termination command: the SIG STR and COS THRS bar displays are removed and current COS level is displayed as analog number as shown below.



2.4.3.2.5 **RF Tuned Frequency**

Setting the receiver tuned frequency is accomplished either by utilization of the TUNE knob and CURSOR or by directly entering the desired tuned frequency via the general purpose keypad. The RF Tuned Frequency is displayed in the FREQUENCY (MHz) area of the LCD display.

When the TUNE knob is used to tune the receiver, tuning the knob clockwise increases the tuned frequency while turning counterclockwise decreases it. Selection of tuning step size is accomplished by toggling the CURSOR switch to position the display CURSOR (or Underscore) under the desired digit in the FREQUENCY (MHz) area of the display. Digits to the right of the selected digit are not altered by the TUNE knob. The selected digit and all digits to the left of the selected digit are incremented or decremented by the TUNE knob in decade ripple counting fashion.

The frequency can also be set by entering the desired frequency, in MHz, on the general purpose keypad. When preceded by a numeric entry, depression of the MHz keypad results in the processing of the numeric entry as an RF Tuned Frequency. If in the EXEC mode, the current receiver tuned frequency changes to agree with the frequency entered. When depressed, when no numeric entries are present, the error message "Expecting # before MHz" appears and remains as long as the MHz keypad is depressed. The range of available tuned frequencies is 20.00000 to 512.0000 or 20.0000 to 1400.0000 if the FEU Option is installed. **Example 6** illustrates the use of the MHz keypad.

- RF Tuned Frequency Entry - Procedure

  1. If the Control Status is not EXEC, press the lower case, 0 and EXEC keypads.
  2. Enter the desired numerical frequency data.
  3. Terminate by pressing MHz or kHz keypad.

2.4.3.2.6 BFO Offset Frequency

When the receiver is in the CW detection mode, setting the receiver BFO Offset Frequency is accomplished either by utilization of the CURSOR and TUNE knob or by directly entering the desired offset frequency via the general purpose keypad. The BFO Offset Frequency is displayed in the BFO (kHz) area of the LCD display.

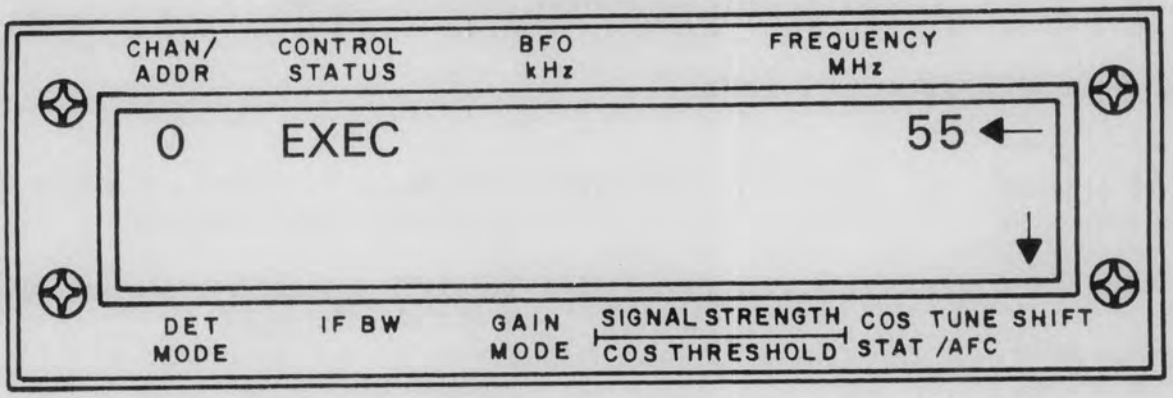
When the TUNE knob is used to set the receiver's BFO offset, turning the knob clockwise numerically increases the offset while tuning counterclockwise decreases the offset. The TUNE knob is enabled for BFO offset by first selecting the CW mode, then toggling the CURSOR switch to position the display cursor under the 0.1 kHz or 0.01 kHz BFO digit. Rotating the TUNE knob changes the BFO offset from +4.00 to -4.00 kHz in 10 Hz steps. In the LSB or USB mode, the offset range is +1.00 to -1.00 kHz.

The BFO offset can also be set by entering the desired offset in kHz on the general purpose keypad. If the BFO +/- key is depressed while the receiver is not in the CW detection mode, the error message "BFO Det Mode is not CW" is displayed and remains as long as the BFO +/- key is depressed. During CW mode, when preceded by a numeric entry, depression of the BFO keypad results in the processing of the numeric data as a BFO offset. If in the EXEC mode, the current receiver BFO offset is changed to agree with the offset entered. Whendepressed, when no numeric entries are present, the polarity sign of the displayed offset is changed. The range of available offsets is 0.0 to 4.0 kHz. **Example 7** illustrates the use of the BFO keypad.

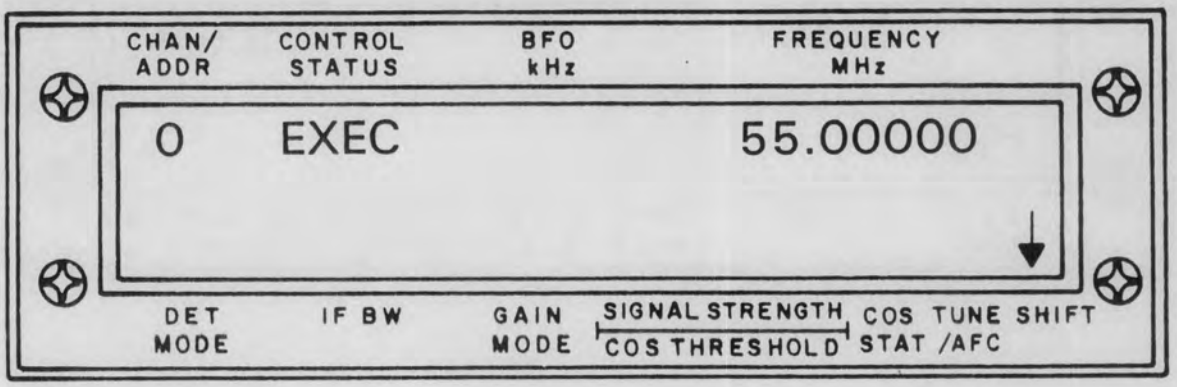
Example 6. Tune the Receiver to 55 MHz.

[↓] [0] [EXEC] ..... (1) This places the receiver in EXEC mode as required for local operation.

[5] [5] ..... (2) Desired tuned frequency data entry, "55" is displayed in FREQUENCY (MHz) area as shown below.



[MHz] ..... (3) Termination command: new tuned frequency is displayed as shown below.

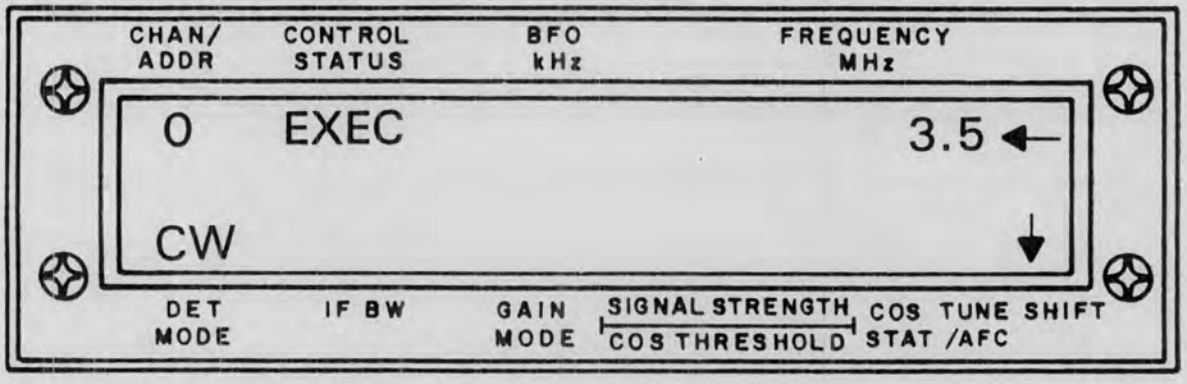


- BFO Offset Frequency Entry - Procedure

1. If the Control Status is not EXEC, press the lower case, 0 and EXEC keypads.
2. Select CW mode using the DET keypad.
3. Enter the desired numerical offset data.
4. Terminate by pressing the BFO keypad.
5. If offset polarity is incorrect, press BFO again.

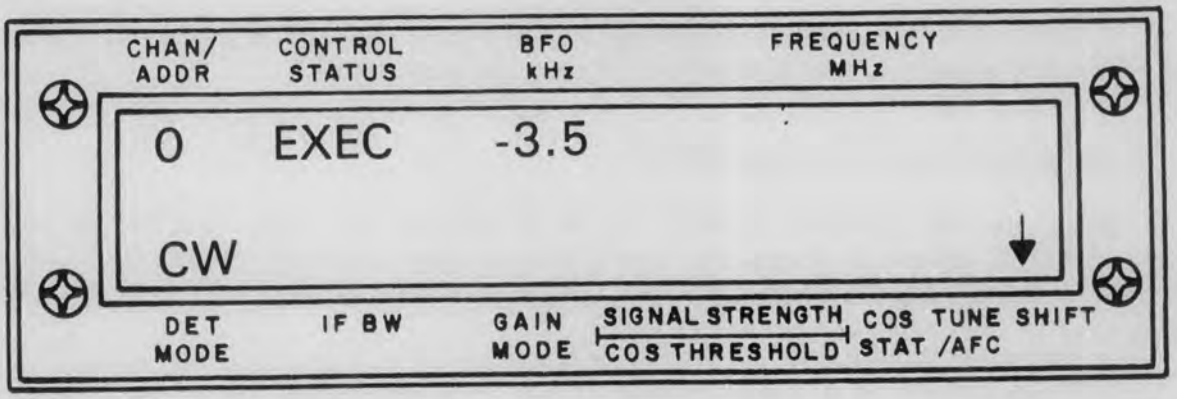
Example 7. Set BFO Offset to +3.5 kHz.

[↓] [0] [EXEC]	(1)	This places the receiver in EXEC mode as required for local operation.
[DET]	(2)	The DET keypad is repeatedly depressed until CW is displayed.
[3] [•] [5]	(3)	Desired BFO offset data entry, "3.5" is displayed in FREQUENCY (MHz) area and CW is displayed in DET MODE area as shown below.



Example 7. Set BFO Offset to +3.5 kHz (Continued).

BFO +/-	.....	(4) Termination command: new BFO offset is displayed as shown below.



BFO +/-	.....	(5) The BFO keypad is pressed again to change the offset polarity from "-" to "+".

2.4.3.3 **Memory Functions (RCLm)**

The following paragraphs describe the basic memory storage and recall procedures for the receiver. The memory functions permit the operator to store receiver front panel parameters in a memory channel, and then recall and execute receiver parameters from a memory channel. Memory functions also permit the operator to program the receiver to scan a selected group of memory channels.

There are 100 available memory channels (99 discrete and one implicitly addressed) for storage of receiver parameter data. Each memory channel is used to store the following receiver parameters: RF tuned frequency, BFO offset, detection mode, IF bandwidth, gain mode and COS threshold. Dwell time is a separate parameter that is used in conjunction with scanning.

Some memory functions are lower case, some are upper case. To ensure that the correct case is selected, each procedure example given is first preceded by a lower case or upper case entry as required for that example. If the receiver is already in the correct state, the lower/upper case entry may be ignored.

2.4.3.3.1 **Memory Channel 0**

Memory channels in the range 1 through 99 have the ability to maintain setup parameters without affecting the receiver status. Memory Channel 0, however, always contains the current active receiver status regardless of the front panel Channel/Address number.

As shown in **paragraph 2.4.3.2**, the EXEC (EXECUTE) Control Status with a channel address of 0 is the most commonly used mode during local operation. By ensuring this condition, stored data in other memory channels is not accidentally altered. Also, any change to the receiver (i.e., frequency, IF bandwidth) during this mode is stored automatically in channel 0. The STO key may not be used to place new data into channel 0. If the STO key is used without entering data beforehand, the message "Expecting data entry before STO" appears. If the STO key is used as a termination command after a data entry of 0, the message "STO range: 1-99" is displayed.

If the RCL key is used as a terminator for a data entry of 0, the result is the same as for the EXEC key sequence, and the Control Status becomes 0 EXEC.

2.4.3.3.2 Numbered Memory Storage (STO)

Each memory channel from 1 to 99 is utilized to store one set of receiver parameters. Storable parameters are RF Tuned Frequency, Detection Mode, Gain Mode, IF Bandwidth, BFO Offset and Threshold Level. Entry of these parameters was explained in **paragraph 2.4.3.2.**

When preceded by a numeric entry from 1 to 99, depression of the STO keypad results in the processing of the numeric entry as a memory channel. All currently displayed receiver parameters are stored in the designated memory channel. The front panel responds with the complete status still displayed, a Control Status of "Stored" and the designated memory channel in the CHAN/ADDR display area. Note that this Control Status is displayed only until the next keystroke. **Example 8** illustrates numbered memory storage.

- Numbered Memory Storage - Procedure

  1. Enter the desired 1 or 2 digit memory channel digits.

  2. Terminate by pressing STO keypad.

2.4.3.3.3 Single Keystroke Memory Storage (STO)

If the Control Status is MODm (Modified Memory, **paragraph 2.4.3.3.4**) the currently displayed CHAN/ADDR may be used to automatically re-store the new setup into that memory channel. This is accomplished by pressing the STO key as a terminator with no data entered. The front panel responds by displaying the complete status of that channel and changing the Control Status back to RCLm (**paragraph 2.4.3.3.4**).

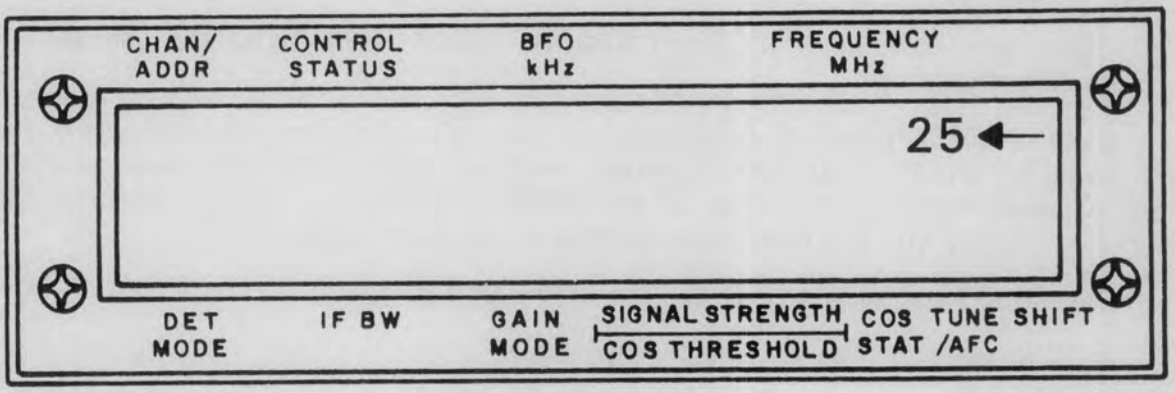
2.4.3.3.4 Numbered Memory Recall (RCL)

When preceded by a numeric entry from 1 to 99, depression of the RCL keypad results in the processing of the numeric entry as a memory channel. The contents of the designated memory channel are displayed and the Control Status becomes RCLm (Recall Memory). Current receiver operating parameters are maintained in channel 0 and are not changed. When depressed, when no numeric entries are present, the RCL keypad causes the contents of the currently displayed channel number to be recalled and displayed. Repeated depressions of the RCL keypad, without numeric entry, causes successive memory channels to be recalled and displayed. This feature allows a rapid examination of a group of memory channels.

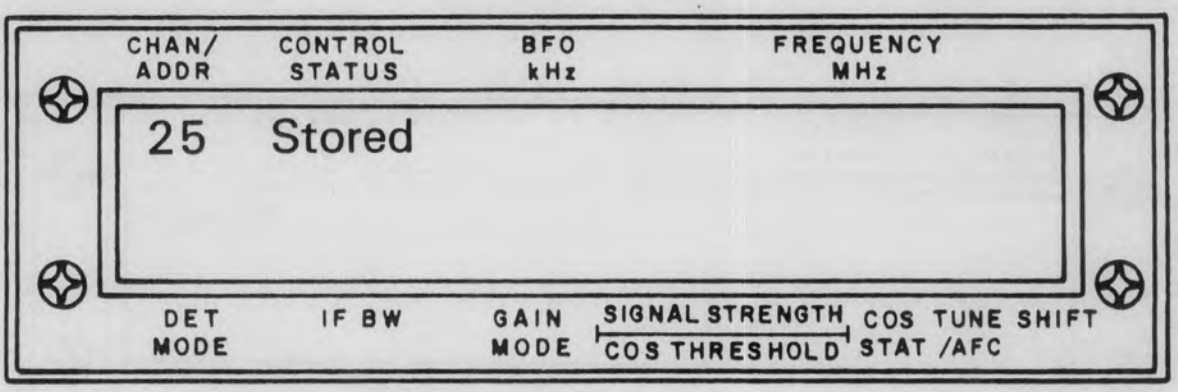
Example 8. Store Receiver Parameters in Channel 25.

[↓] [0] [EXEC] ..... (1) This places the receiver in EXEC mode as required for local operation.

[2] [5] ..... (2) Desired numbered channel data entry, "25" is displayed in FREQUENCY (MHz) area of display as shown below.



[STO] ..... (3) Termination command: FREQUENCY (MHz) returns to normal, "25" is displayed in CHAN/ADDR window, STORED is displayed in CONTROL STATUS window as shown below.



If any of the displayed memory setup parameters are changed while in RCLm mode, the changes are not automatically re-stored into the memory channel. The CONTROL STATUS display area changes to MODm (Modified Memory) indicating that the currently displayed receiver parameters do not match the parameters stored in the designed memory channel. This avoids accidental changes to a memory channel. Depressing the STO keypad stores the changed parameters in the designated memory channel.

If the modified parameters are not to be stored, depressing the RCL key with no data entered discards the changes. The Control Status returns to RCLm (Recall Memory) with the original contents of the memory channel displayed.

If, during a Control Status of MODm, a new front panel mode is desired (i.e., 0 EXEC, **paragraph 2.4.3.2**), the operator is prompted to save the new data in the memory channel. The display reads:

"Store new data in ? Use CURSOR: NO ? YES" (with the channel number indicated).

If the CURSOR switch is pressed to the left, the changed parameters for the channel are discarded and the next control mode is entered. If the switch is moved to the right, the new setup parameters are re-stored in the designated memory channel and the Control Status returns to RCLm, with the new memory channel contents displayed.

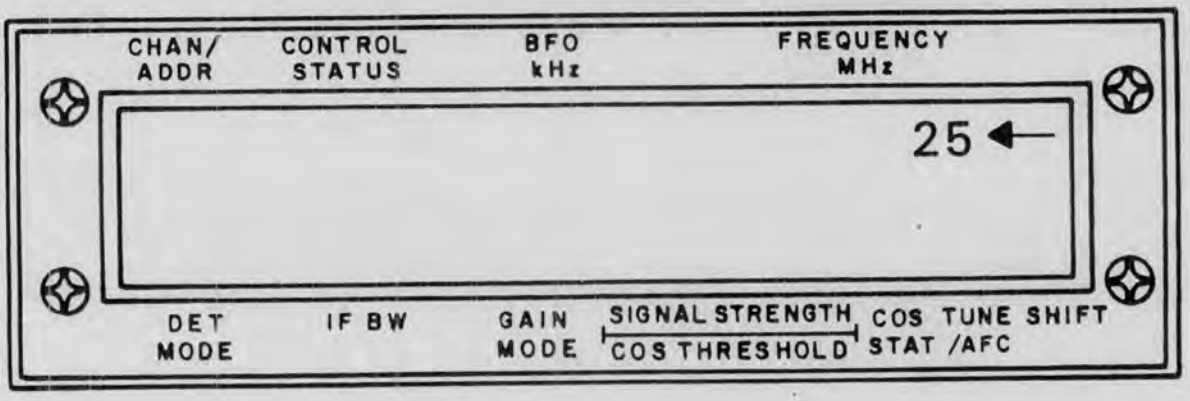
Examples 9 and **10** illustrate the use of the RCL keypad.

o Numbered Memory Recall - Procedure

1. Enter the desired 1 or 2 digit memory channel digits.
2. Terminate by pressing the RCL keypad.

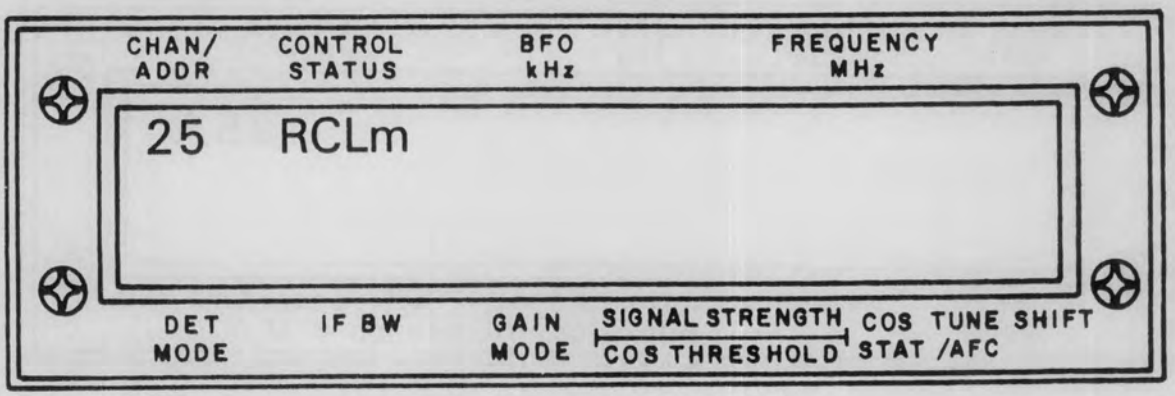
Example 9. Recall Receiver Parameters in Channel 25.

[↓] [0] [EXEC]	(1)	This places the receiver in EXEC mode as required for local operation.
[2] [5]	(2)	Desired numbered channel data entry, "25" is displayed in FREQUENCY (MHz) area of display as shown below.



Example 9. Recall Receiver Parameters in Channel 25 (Continued).

RCL ..... (3) Termination command: FREQUENCY (MHz) returns to normal, "25" is displayed in CHAN/ADDR window, RCLm is displayed in CONTROL STATUS window, contents of channel are displayed as shown below.



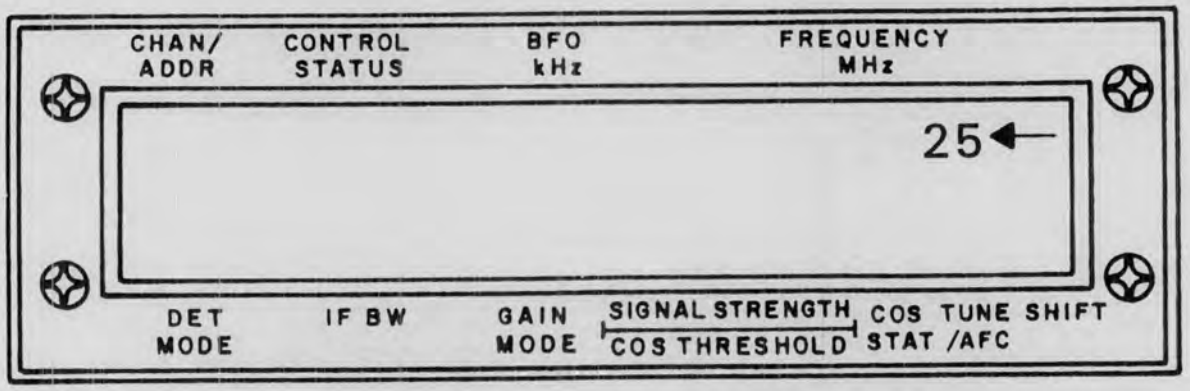
- Numbered Memory Updating - Procedure

  1. Enter the desired 1 or 2 digit memory channel digits.
  2. Terminate by pressing the RCL keypad.
  3. Update desired individual receiver parameters (**paragraph 2.4.3.2**).
  4. Terminate by pressing the STO keypad.

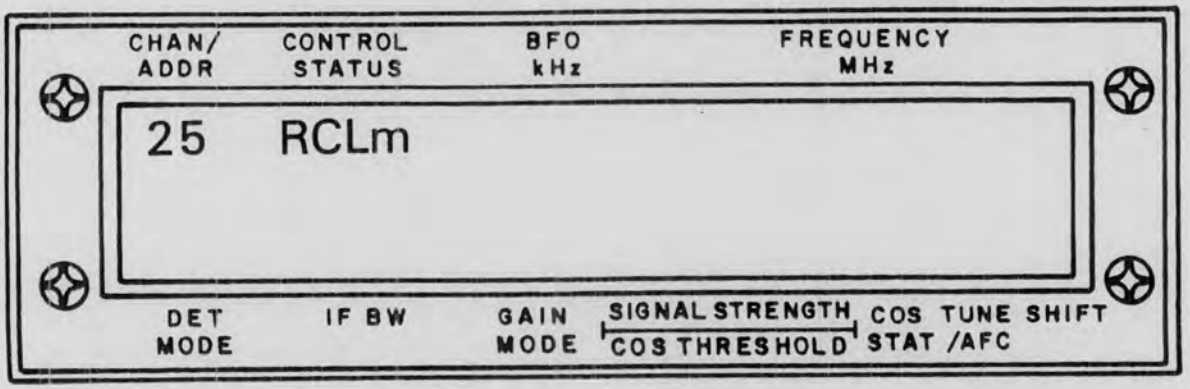
Example 10. Change IF Bandwidth Stored In Channel 25 From 50 kHz to 10 kHz.

[↓] [0] [EXEC] ..... (1) This places the receiver in EXEC mode as required for local operation.

[2] [5] ..... (2) Desired numbered channel data entry, "25" is displayed in FREQUENCY (MHz) area of display as shown below.

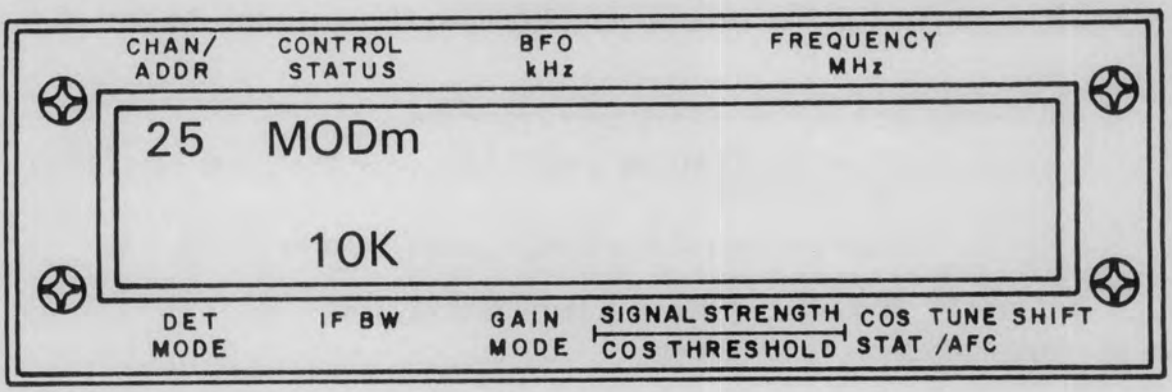


[RCL] ..... (3) Termination command: FREQUENCY (MHz) returns to normal, "25" is displayed in CHAN/ADDR window, RCLm is displayed in CONTROL STATUS window, contents of channel are displayed as shown below.

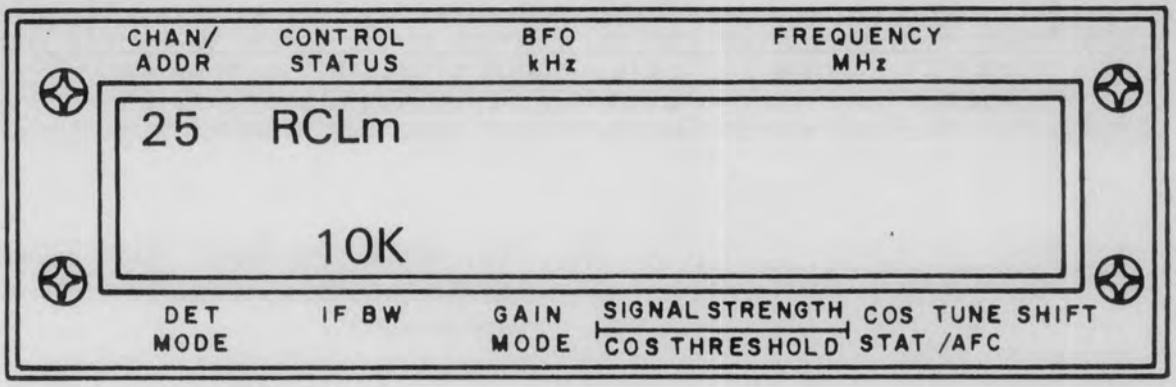


Example 10. Change IF Bandwidth Stored In Channel 25 From 50 kHz to 10 kHz (Continued).

IF BW ..... (4) Depress IF BW keypad repeatedly until 10 kHz is displayed; MODm is displayed in CONTROL STATUS window, other receiver parameter displays remain unchanged as shown below.



STO ..... (5) Termination command: RCLm is displayed in CONTROL STATUS window as shown below. Displayed status is shown in CHAN 25.



2.4.3.3.5 **Numbered Memory Execution (EXEC)**

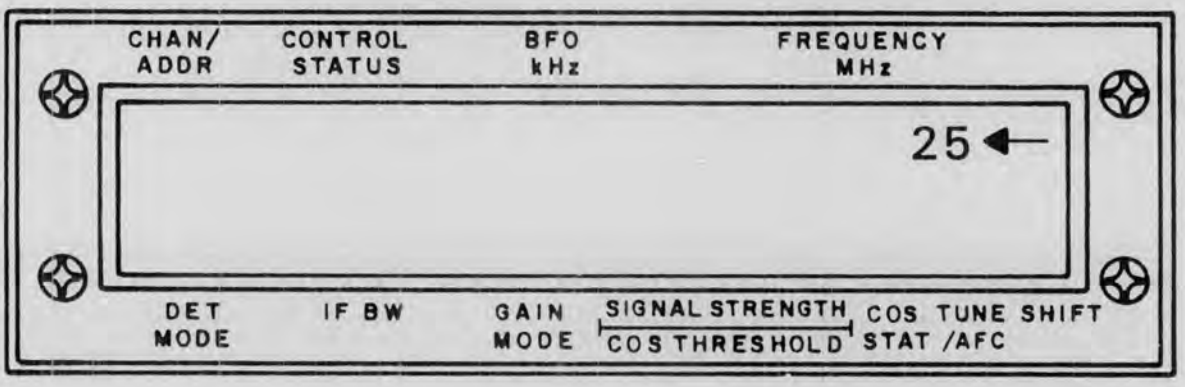
When preceded by a numeric entry from 1 to 99, pressing the EXEC keypad results in the processing of the numeric entry as a memory channel. The contents of the designated memory channel are displayed and current receiver operating parameters are changed to the parameters in the designated memory channel. When pressed during the Control Status RCLm (Recall memory) when no numeric data entries are present, the EXEC keypad causes the contents of the currently displayed memory channel number to be executed. If the Control Status is EXEC with a CHAN/ADDR display of 1-99, repeated pressing of the EXEC keypad, without numeric data entry beforehand causes successive memory channels to be executed. This allows rapid manual scanning of a group of memory channels. If any of the displayed receiver parameters are changed following execution of a numbered memory channel, the actual receiver tuning status is changed and the contents of that channel are updated to agree with the newly displayed receiver parameters. **Example 11** illustrates the use of the EXEC keypad.

- Numbered Memory Execution - Procedure
  1. If the Control Status is not EXEC, press the lower case, 0 and EXEC keypads.
  2. Enter the desired 1 or 2 digit memory channel digits.
  3. Terminate by pressing the EXEC keypad.

Example 11. Numbered Memory Execution.

[↓] [0] [EXEC] ..... (1) This places the receiver in EXEC mode as required for local operation.

[2] [5] ..... (2) Desired numbered channel data entry, "25" is displayed in FREQUENCY (MHz) area of display as shown below.



[EXEC] ..... (3) Termination command: "25" is displayed in CHAN/ADDR window, receiver operands are changed.

2.4.3.4 Scanning

2.4.3.4.1 Numbered Memory Scanning

The receiver's memory scan capability sequentially scans an operator selected group of memory channels. During scan operation, the stored parameters of each memory channel are automatically recalled and transferred to the receiver. As each channel is recalled, the received signal strength is compared to an operator selected threshold level stored in that channel (**paragraph 2.4.3.2.4**). When a channel is located where signal strength equals or exceeds the threshold level, the scanning operation stops for an operator selected dwell time, and then restarts automatically. The following is a summary of the functions of the various keypads associated with memory scanning.

1. SCAN: When pressed, after storing a desired group of memory channels (any or all of 1 through 99), the SCAN keypad starts or ends the CHANNEL SCAN mode.

2. L/OUT: When pressed, following numeric data entry of 1 to 99, the L/OUT keypad deletes the designated memory channel from the CHANNEL SCAN list. When pressed, following numeric data entry of two digits separated by a decimal point, the L/OUT keypad deletes all channels between the two digits from the CHANNEL SCAN list.

3. INCL: When pressed, following numeric data entry of 1 to 99, the INCL keypad adds the designated memory channel to the CHANNEL SCAN list. When pressed, following the numeric data entry of two digits separated by a decimal point, the INCL keypad adds all channels between the two digits to the CHANNEL SCAN list.

4. DWL: When pressed, following numeric data entry, the DWL keypad processes the numeric entry as a DWELL TIME for the CHANNEL SCAN mode. Three dwell time entries are required: The first dwell time is the time in milliseconds that the receiver remains on a new channel waiting for energy to appear (Pre-Hit). This is useful when scanning channels with pulse signals. The second dwell time is the time in seconds the receiver remains on a hit channel after exceeding COS threshold (On-Hit). This is useful for automatically continuing the SCAN when a signal remains active for a long period. Entry range is 0-9, where 9 is infinite. The third dwell time is the time in seconds the receiver remains on a hit channel after the signal drops below threshold (After-Hit). Entry range is 1-9, where 9 is infinite. When the DWL key is pressed with no data entered beforehand, the present dwell times are displayed as long as the key is held.

5. SET: When pressed, the SET keypad displays the total number of channels in the SCAN list. The three dwell times are also displayed. Individual channel numbers are displayed in the screen area labeled "LIST:" This list can be scrolled by the cursor control switch.

2.4.3.4.2 **RF GAIN Control During Scan Mode**

The software program which scans the WJ-8628-4 is optimized for use in the AGC mode. Each memory channel contains an operator-entered COS (Carrier Operated Squelch) threshold. When stepping through the included channels, this threshold level is used to convert the receiver to a preset manual gain level which causes only those signals above the threshold to be detected. Thus, in the AGC mode, the COS threshold is used to adjust the sensitivity of the scan for that channel.

If an included channel has been stored in memory with the MAN (Manual) Gain selected, the digital manual gain word is not stored. Instead, the RF GAIN Control on the frontpanel of the WJ-8628-4 is tested. Each time a channel is found in the manual mode, the potentiometer position is read and sent to the receiver as the RF Gain Setting. In the manual gain mode, therefore, the COS threshold and the RF Gain Control affect the sensitivity of the scan. (This applies only to the front panel scan mode.) Under remote control the digital manual gain word is stored in each memory channel (refer to **Examples 12** through **16**).

- Dwell Time Entry - Procedure

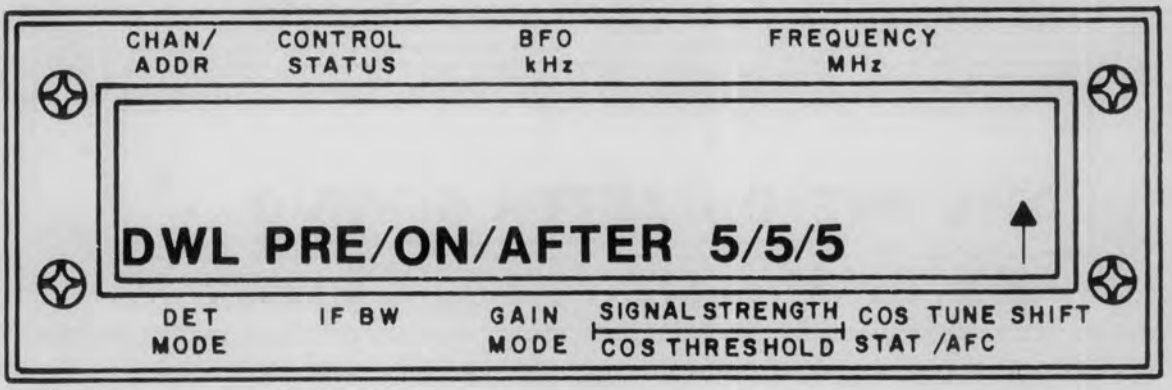
1. Enter all desired dwell times on keypad.

2. Terminate by pressing the DWL keypad.

Example 12. **Enter Pre-Hit Dwell Time of 5 Milliseconds, and On-Hit and After-Hit Dwell Times of 5 Seconds Each.**

[5] [•] [5] [•] [5] ..... (1) Desired numeric entry: On-Hit and After-Hit times separated by decimal point, "5.5.5" is displayed on the FREQUENCY (MHz) area.

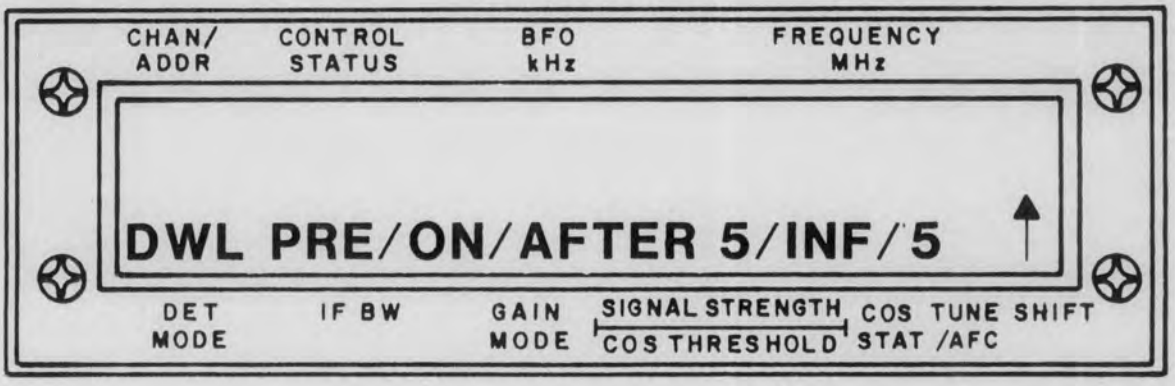
[DWL] ..... (2) Termination command: FREQUENCY (MHz) area returns to normal, DWELL times displayed as shown below.



Example 13. **Enter On-Hit Dwell Time of Infinite.**

[5] [•] [9] [•] [5] ..... (1) Desired numeric entry: On-Hit and After-Hit times separated by decimal point, "5.9.5" is displayed on the FREQUENCY (MHz) area.

[DWL] ..... (2) Termination command: FREQUENCY (MHz) area returns to normal, DWELL times are displayed as shown below.



Example 14. Enter After-Hit Dwell Time of 0 Seconds.

[5] [•] [9] [•] [0] ..... (1) Desired numeric entry: After-Hit time is preceded by a decimal point, "5.9.0" is displayed in the FREQUENCY (MHz) area.

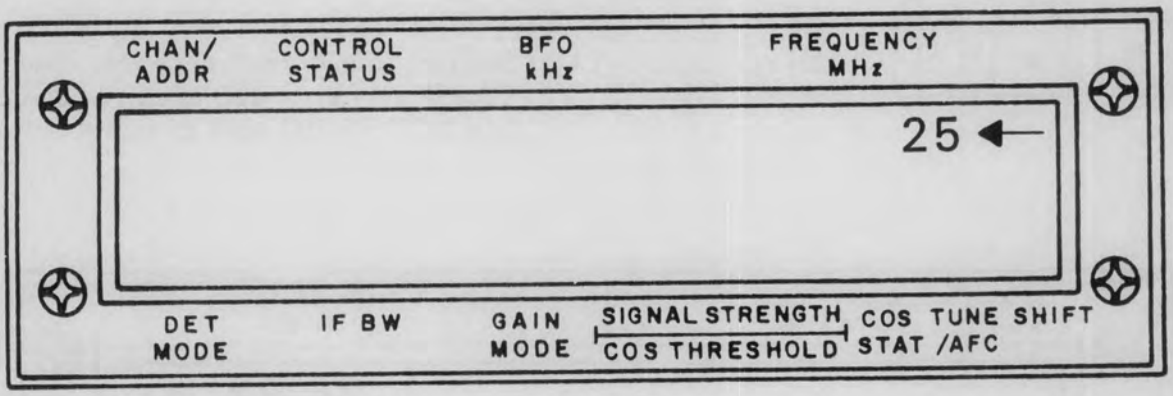
[DWL] ..... (2) Termination command: FREQUENCY (MHz) area returns to normal, DWELL times displayed as shown below.

- Single Channel Lockout - Procedure

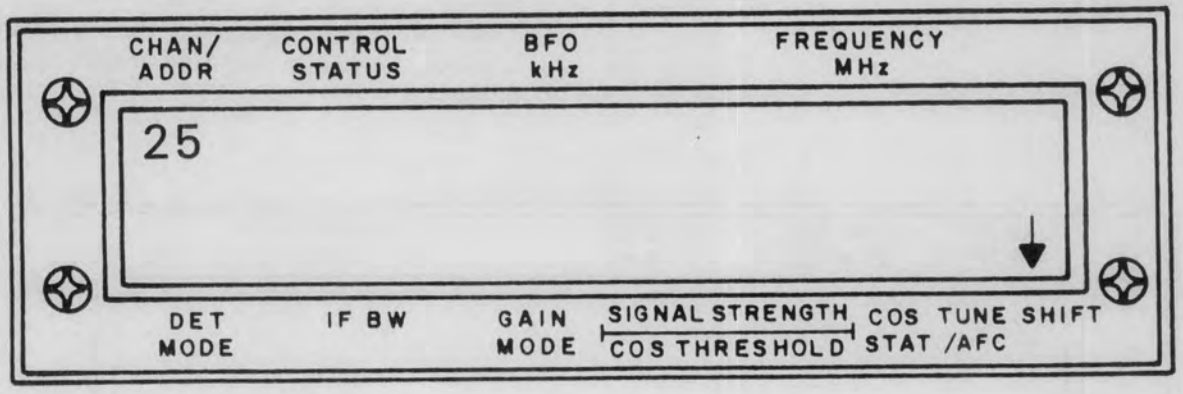
  1. Enter the desired 1 or 2 digit memory channel digits.
  2. Terminate by pressing the lower case and L/OUT keypads.

Example 15. Lockout Memory Channel 25.

[2] [5] ..... (1) Desired numeric entry: After-Hit time is preceded by a decimal point, "25" is displayed in FREQUENCY (MHz) area as shown below.



[↓] [L/OUT] ..... (2) Termination command: FREQUENCY (MHz) returns to normal. If any string channel was displayed, the "i" (included) symbol next to CHAN/ADDR number is erased.



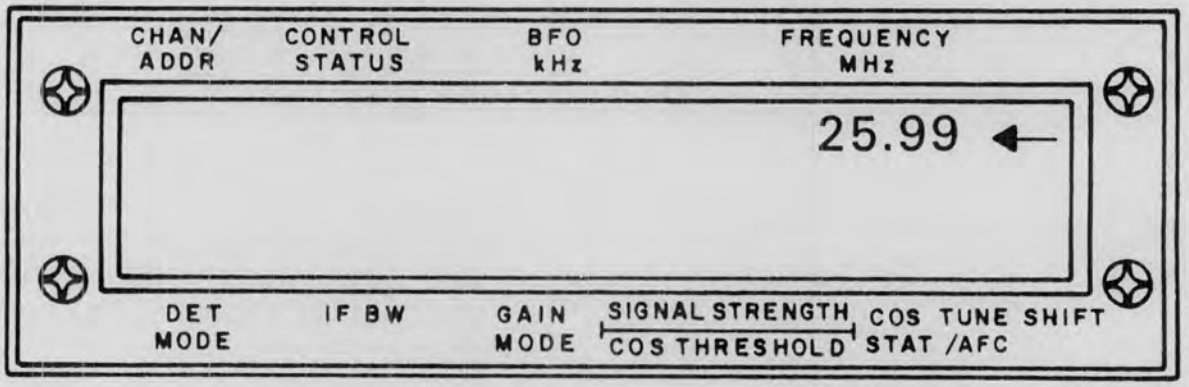
- Channel Group Lock Out - Procedure

  1. Enter first and last memory channel digits of the group separated by a decimal point.

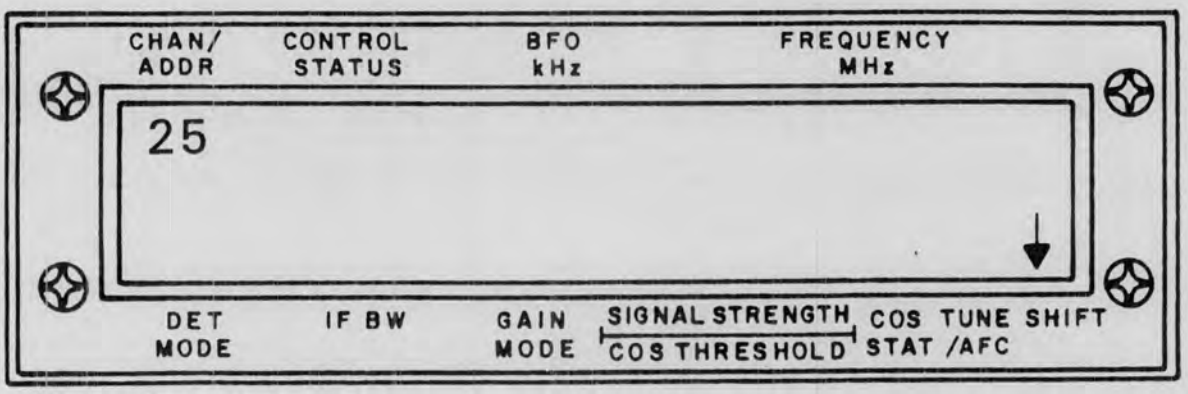
  2. Terminate by pressing the lower case and L/OUT keypads.

Example 15. Lockout Memory Channel 25 (Continued).

[2] [5] [•] [9] [9] ..... (1) Desired numbered channel data entry, "25.99" is displayed in FREQUENCY (MHz) area as shown below.



[↓] [L/OUT] ..... (2) Termination command: FREQUENCY (MHz) returns to normal. If any string channel was displayed, the "i" (included) symbol next to CHAN/ADDR number is erased.

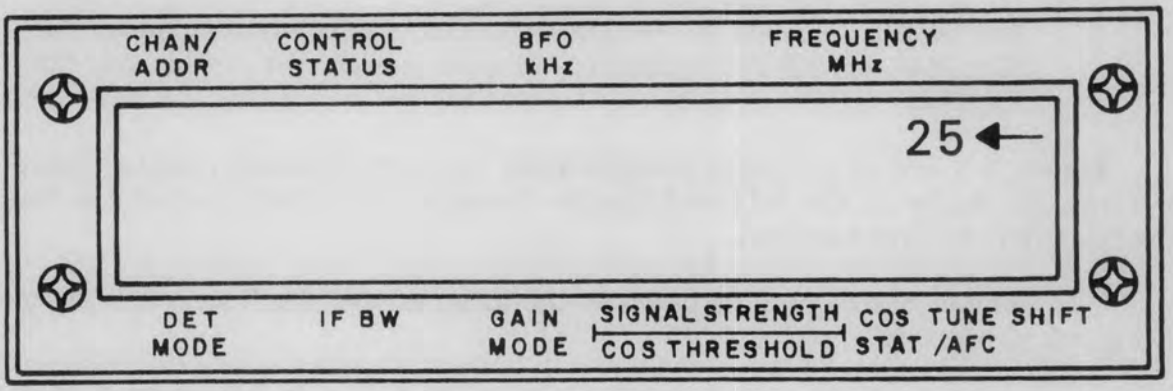


- Add Memory Channel to Scan List - Procedure

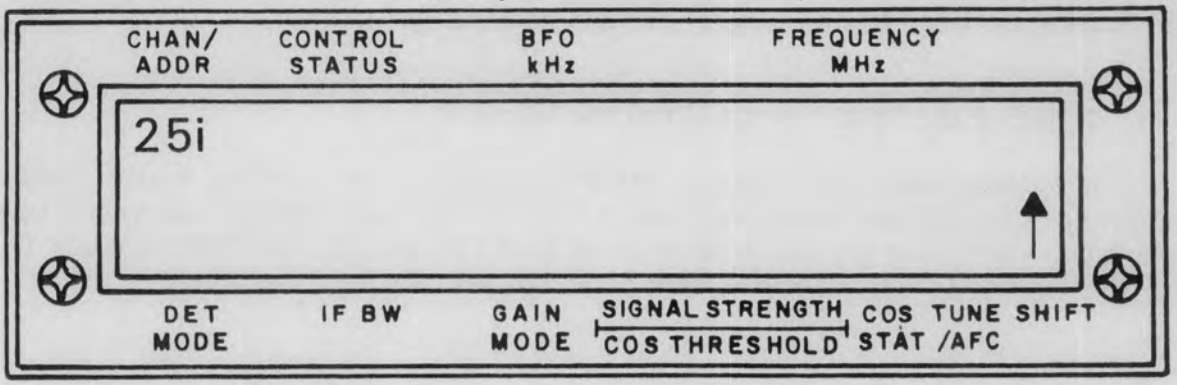
1. Enter the desired 1 or 2 digit memory channel digits.
2. Terminate by pressing the upper case and INCL keypads.

Example 16. Add Channel 25 to Channel Scan List.

[2] [5] ..... (1) Desired numbered channel data entry, "25" is displayed in FREQUENCY (MHz) area as shown below.



[↑] [INCL] ..... (2) Termination command: FREQUENCY (MHz) returns to normal as shown below. If channel indicated is "25" an "i" appears after channel indicating it has been "included" into scan list.



2.4.3.5 Remote Control Mode

This section describes the remote control operation of the WJ-8628-4 receiver. Remote operation requires the following minimum hardware configuration:

1. One EFR-100 Equipment Frame
2. One EPS-100 Power Supply
3. One IOM108 I/O Interface module with either IEEE-488 or RS-232 option
4. One WJ-8628-4 Receiver/Controller
5. One ASCII Terminal or computer (Customer Supplied) equipped for IEEE-488 or RS-232 operation (Should match the option in the IOM108.

Figure 2-5 shows a typical configuration for implementing remote control by a computer terminal. Refer to the WJ-9040 System Common Equipment manual for details on connecting the IOM108 to the terminal.

The communication process between the terminal and the Receiver is described in the following two paragraphs.

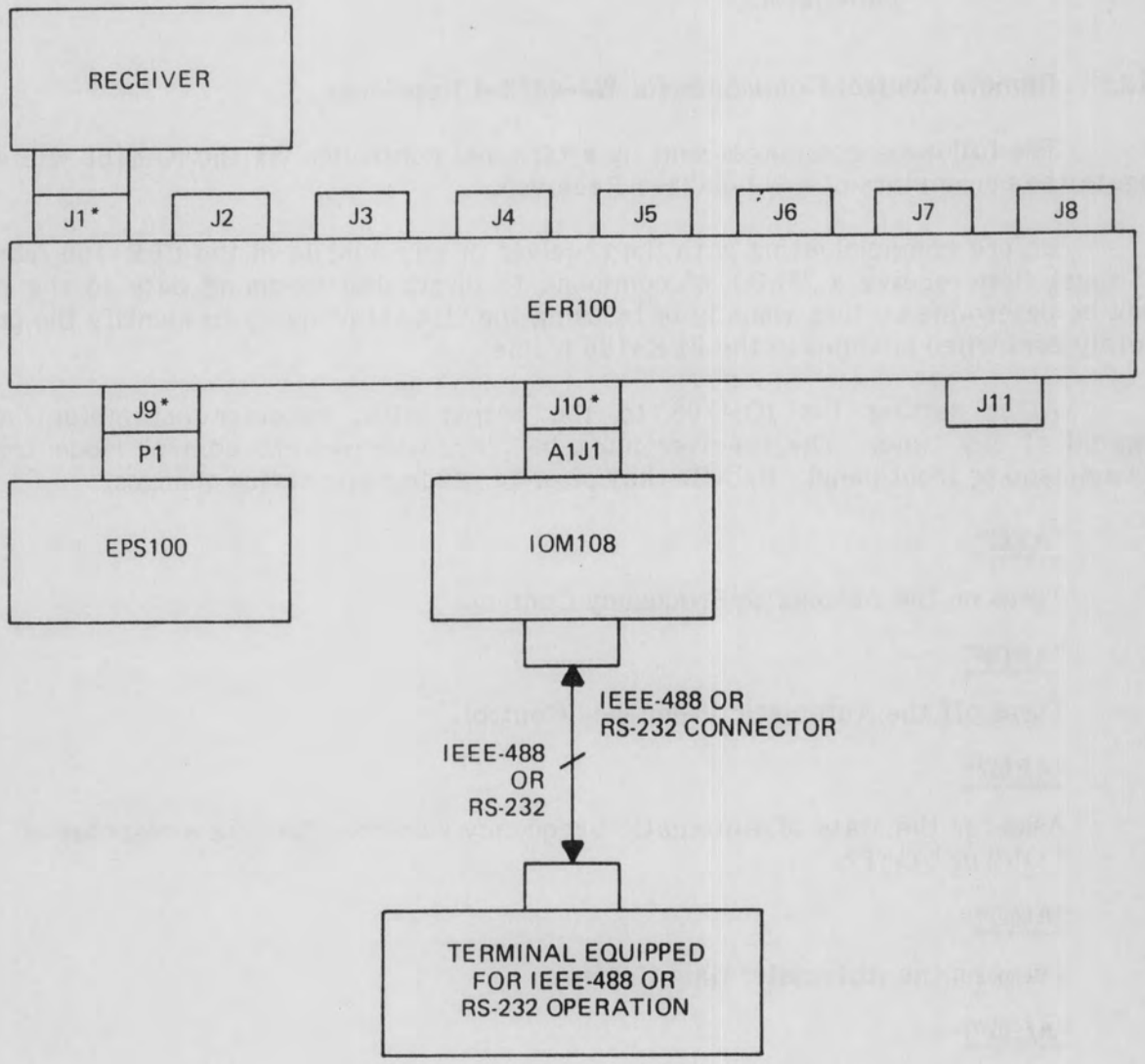
Using the valid mnemonic ASCII commands found in **paragraph 2.4.3.5.1** and **paragraph 2.4.3.5.2**, the external controller communicates with the IOM108 via the IEEE-488 or RS-232 interface. The IOM108 decodes the ASCII commands and converts them to binary data which is sent to the designated slot in the backplane of the EFR-100 frame via the **Command/Control** data line.

If the terminal sends a query type command such as **"FRQ?"**, the IOM checks for changes in the module's status and interrogates it via the Report Data line, if required, to obtain its current status. The IOM08 converts the binary information into an ASCII string and sends it to the terminal.

The Receiver must first be configured for Remote control before any change command is accepted from the terminal. This can be done by:

1) Depressing the R/LCL key on the Receiver front panel or
2) Issuing the **"RMT"** command on the terminal.

In either case, the message **"RMT"** appears in the Control Status field of the Receiver Front Panel display indicating that it is in the Remote Control and ready to accept status changes. The Remote/Local state may be found by sending the **"RMT?"** query from the terminal. Neither the terminal nor the front panel has priority over the other.



* = ACTIVE

Figure 2-5. Remote Control Hardware Configuration

NOTE

Any of the query commands found in **paragraph 2.4.3.5.1** or **2.4.3.5.2** can be sent to the Receiver in Remote Local mode, since these commands do not alter the Receiver's parameters.

2.4.3.5.1 **Remote Control Commands for WJ-8628-4 Receivers**

The following commands sent by a terminal controller via the IOM108 will alter or interrogate the parameters of a WJ-8628-4 Receiver.

Before communicating with the receiver or any module in the EFR-100 frame, the IOM108 must first receive a "SLOT n" command to direct the incoming data to the module. This may be determined either visually or by using the "EXAM n" query to identify the presence of remotely controlled modules in the EFR-100 frame.

After setting the IOM108 to the proper slot, receiver parameters may be interrogated at any time. The receiver must be placed in Remote control mode using the **"RMT"** command or front panel **R/LCL** key prior to sending any status changes.

"AFC"

Turns on the Automatic Frequency Control.

"AFC/"

Turns off the Automatic Frequency Control.

"AFC?"

Asks for the state of Automatic Frequency Control. Returns a response of " ON" or " OFF".

"AGC"

Turns on the Automatic Gain Control.

"AGC/"

Turns off the Automatic Gain Control.

"AGC?"

Asks for the state of Automatic Gain Control. Returns a response of " FAST", " SLOW", or " OFF".

"AM"

Sets the detection mode to AM.

"AUD n"

Polled Audio to slot **n** is enabled.

"AUD?"

Asks which Slot has the Polled Audio enabled. Returns "AUD n" where **n** is the Slot number.

"BFO [+/-] f"

Sets the Beat Frequency Oscillator to a frequency offset of "f" kHz, positive or negative. Ranges:
+/-4.00 kHz for CW
+/-1.00 kHz for LSB and USB

ERRORS: If **n** is outside of the range, the command is ignored.

"BFO?"

Asks for the BFO frequency. Returns the BFO frequency in kHz.

"BW n"

Selects bandwidth number n, where n is in the range of 1 to 4. The value **n** represents the position of the hardware in the receiver. The actual bandwidth is determined by the type of IF card installed. See **"BWC?"**

ERRORS: If **n** is outside the range, the command is ignored.

"BW?"

Asks for the bandwidth number. Returns a number 1 through 4. For the actual IF bandwidth in kHz or MHz, see **"BWC?"**

"BWC?"

Asks for the actual bandwidth. Returns the bandwidth in kHz or MHz. Examples: " 3 kHz", " 1.4 MHz".

"CLR"

Clears the tuned status of the Receiver and sets the unit to a default state.

"CONT* "

Continues a scan from the point it stopped (i.e. to continue a scan during a dwell or hit).

"COR n" or **"COS n"**

Sets the Carrier Operated Squelch level to n, n must be in the range of 0 to 63.

ERRORS: If **n** is outside the range 0 to 63, the command is ignored.

"COR?" or **"COS?"**

Asks for the level of Carrier Operated Squelch. Returns the COS level setting.

"CST?"

Asks for the state of COS. Returns " ON" if the signal strength is greater than the COS setting. Returns " OFF" otherwise.

"CW"

Sets the detection mode to CW.

"DET?"

Asks for the detection mode. Returns the selected detection mode.

"DWL* n,m"

Sets the dwell times for a scan. The value of **n** is the On-hit dwell time, and m is the After-hit time in the range 0 to 9. See the receiver operating manual for details on scanning and dwell times.

Note: The value 9 sets an infinite dwell time.

"DWL*?"

Asks for the dwell times. Returns " DWL n,m", where **n** is the On-hit dwell, and m is the After-hit dwell.

"EXAM"

Asks for a description of the unit. Returns the receiver type and identifies certain options.

"FM"

Sets the detection mode to FM.

"FRQ f"

Sets the tuned frequency, where **f** is the frequency in MHz. Refer to the receiver manual for frequency ranges.

"FRQ?"

Asks the frequency of a receiver. Returns the tuned frequency in MHz. Example " 23.4500 MHz"

"HIT*?"

Asks the hit status. Returns one of the following responses:

" n,m,f" — if a hit has occurred during a scan, where **n** is the Channel number or Band number, **m**, is the signal strength, and **f** is the frequency in MHz. Data may be read by the controller only once, and is overwritten by successive hits.

" **LOCAL**" — if the receiver is in local control

" **NH**" — if no hit has occurred since the previous "HIT?" request

" **MAN***" — if the receiver is not scanning

INL* n,[m],[o-p]"

Includes the specified Memory Channels for step scanning. The parameters are in the range 1 to 99. The dash or hyphen may be used to include a string. The comma may be used to create a discreet list. Examples:

"INL* n"
"INL* n,m,o,p"
"INL* n-p"
"INL* n,m-p"

"INL* n?"

Asks the include status of the Receiver's Memory Channel n. Range is 1 to 99. Returns:

" **D**" — Disabled; if the Channel IS NOT included.
" **E**" — Enabled; if the Channel IS included.
" **U**" — Undefined; if the receiver has software dated before 12/86.

"LCK* n,[m],[o-p]"

Locks out the specified Memory Channels for step scanning. Range is 1 to 99. The dash or hyphen may be used to include a string. The comma may be used to create a discreet list. Examples:

"LCK* n"
"LCK* n,m,o,p"
"LCK* n-p"
"LCK* n,m-p"

"LCL"

Sets the receiver to Local front panel control.

"LSB"

Sets the detection mode to **LSB.**

"MAN* "

Stops a scan. The control mode will become **RMT** allowing commands to change the receiver status.

"PLS"

Sets the detection mode to **PLS.**

"RCL* n"

Recall and execute the Memory Channel **n**, range 1 to 99.

"RFG n"

Sets the RF Gain level to **n**, range 0 to 63 where 0 is maximum gain, 63 is minimum. The data is placed in memory regardless of the receiver gain mode, but the mode must be manual ("AGC/") for the RFG level to be used.

ERRORS: The command is ignored if **n** is out of range.

"RFG?"

Asks for the RF Gain level. Returns the RF Gain level from 0 to 63. Data is returned regardless of receiver gain mode.

"RMT"

Sets the Receiver into Remote control.

"RMT?"

Asks the remote status of a unit. Returns:

" REMOTE" — if the unit is in Remote control
" LOCAL" — if the unit is in Local control

"SCN* " or **"STP* "**

Starts a Channel scan, or Step scan. The scan will start with the lowest included Memory Channel, and continue until a hit and dwell begins or until instructed to stop using the **MAN*** or **LCL** commands, or the front panel [**R/LCL**] key.

ERRORS: If there are no included Memory Channels the command is ignored

"SCN*?" or **"STP*?"**

Asks the status to verify the receiver is scanning. Returns:

" **STP***" — if Channel (Step) scanning
" **SWP***" — if Sweep (Band) scanning
" **MAN***" — if not scanning

Note: HIT data is not returned by this command.

"SLOT n"

Addresses Slot n, where **n** is 1 to 8, so that following commands will be sent to that Slot.

ERRORS: If **n** is out of range, the command will be ignored.

"SLOT?"

Asks for the addressed Slot. Returns the Slot number of the unit currently being controlled in the format **" Slot n".**

"SS?"

Asks for the relative signal strength of the tuned signal. Returns a value from 0 to 99, 0 is minimum and 99 is maximum.

STO* n"

Stores the complete tuned status of the receiver into Memory Channel n, range 1 to 99.

"USB"

Sets the detection mode to USB.

"VER?"

Asks for the software revision of the IOM. The response is in the this format " IOM108 vx.x.x", where x.x.x is the revision number.

"VIEW* [n]"

This command will return a compact form of the contents of Memory Channel n, range 1 to 99. If the n parameter is "0" or is not used (i.e. "VIEW*"), the current active tuned status will be returned. The individual fields are the same as the responses to separate interrogations. The return information is formatted as follows:

" frq,Det,COS level,BFO frq, BW #,AGC state,RFG level,Incl. Status **"

** Note: The include status is returned as a letter:

"E" indicates the Memory Channel is Enabled (included),
"D" indicates the Memory Channel is Disabled (locked out),
"U" indicates Undefined.

The "U" will appear if the **n** parameter was 0 or not used, since the currently tuned parameters of the receiver are neither included or locked out. The "U" will also appear if the Receiver has software dated before 12/86.

2.4.3.5.2 Remote Control Commands for WJ-8628-4 Receivers Sweep Scan

The following describes the commands recognized by the WJ-8628-4 receiver software to remotely edit a Scan Control Block (SCB) and start a Sweep Scan, sometimes called Band scan, F1-F2 or Sector scan.

The WJ-8628-4 receiver has five separately programmable bands for a Sweep Scan. Each F1-F2 band has an associated Scan Control Block (SCB) which contains all the necessary parameters (i.e., Start and Stop frequencies, Scanning increment, Detection mode, Squelch threshold, etc.). The receiver retains all five band scan setups in Battery-backed memory. Band parameters can be verified or altered remotely by first editing the Scan Control Block, reading or changing the Band parameters from the receiver, and then storing the new Band parameters in the receiver.

The following four commands are related to the edit mode of the Scan Control Block:

1) **"SCB* n"**
2) **"SCB*?", "SCB?"**
3) **"SCB*/", "SCB/"**
4) **"END n"**

Where n is the Band number from 1 to 5.

"SCB* n"

This command will cause the WJ-862X-4 to begin editing the Scan Control Block n, range 1 to 5.

During the edit mode, if another valid **"SCB* n"** command is issued, the new block will be edited and any changes to the previous SCB edit are lost. An invalid **"SCB* n"** command during the editing will terminate the editing and any new data will not be re-stored in the receiver memory.

Example: The command **"SCB* 3"** command is issued. The controller is now able to interrogate and modify the third F1-F2 setup in the receiver. While in the edit mode the **"SCB* 5"** command is issued. The fifth scan setup will be edited. Any changes made to the SCB for band 3 are lost. If the command **"SCB* 7"** were to be issued at this point, all editiing would be aborted since 7 is an invalid Band number.

"SCB*?" or **"SCB?"**

Either of these query commands will return one of two responses - **" SCB/"** if the receiver is not editing a Scan Control Block or **" SCB n"** where n is the SCB being edited.

"SCB*/" or **"SCB/"**

Either one of these commands will abort the editing of a Scan Control Block and any new parameters are not re-stored in the Receiver memory.

"END" or "END n"

This command will exit the edit mode and store the new SCB parameters in the Receiver. The n following the **"END"** command is optional. With no additional parameter, the modified SCB data will be re-stored in the same Band setup that was read from the receiver by the **"SCB* n"** command. If a number n (1 to 5) follows the **"END"** command, the new SCB data will be stored into that setup in the receiver regardless of which Band was originally edited. This allows copying one Band to another, or making small changes without the need to completely set up each of the five bands.

Example: To copy Band setup 2 to Band setup 5 the following sequence of commands should be issued: **"SCB* 2" "END 5"**. This reads in Band 2 from the receiver and ends the band editing sesion by placing the SCB parameters in Band 5 of the receiver.

2.4.3.5.3 Sweep Scan Remote Commands

The following commands will alter or verify the parameters of the Scan Control Block. Note that most commands and responses are the same as those for normal status changes. It should be emphasized that these commands are listed for the SCB Edit Mode. To verify that the SCB mode is active, use the **"SCB*?"** or **"SCB?"** interrogation.

"AFC" and "AFC/"

Enables or disables automatic frequency control during After-hit dwell times. AFC is always disabled during the sweep itself.

"AFC?"

Returns a response of " ON or " OFF" indicating whether AFC is enabled or disabled in the current SCB.

"AGC" and "AGC/"

Enables and disables automatic gain control during the sweep and post-hit dwell times.

"AGC?"

Returns a response of " FAST", " SLOW", or " OFF" indicating the gain mode in the current SCB.

"AM"

Sets the detection mode for the current SCB to AM.

"BFO f"

Sets the Beat Frequency Oscillator to a frequency offset of f kHz, positive or negative. Ranges:

+/- 4.00 kHz for CW
+/- 1.00 kHz for LSB and USB

The Beat Frequency Oscillator becomes active during a dwell after a hit if the detection mode is CW or SSB.

ERRORS: If **f** is outside the range, the command is ignored.

"BFO?"

Returns the BFO offset in kHz for the current SCB.

"BW n"

Sets the bandwidth number of the current SCB to IF filter **n**, range 1 to 4.

ERRORS: If **n** is outside the range, the command is ignored.

"BW?"

Returns the bandwidth number selected in the current SCB.

Note: The actual bandwidth in kHz or MHz is not available while editing an SCB.

"COR n" or **COS n"**

Sets the Carrier Operated Squelch level for the current sweep to n, range 0 to 63.

ERRORS: If **n** is outside the range 0 to 63, the command is ignored.

"COR?" or **"COS?"**

Returns the Carrier Operated Squelch level setting for the current SCB.

"CW"

Sets the detection mode for the current SCB to CW.

DET?"

Returns the detection mode for the current SCB.

"F1 f"

Sets the Start Frequency (F1) of the current SCB to f MHz.

Note: When increasing the Start frequency, all the previously stored lockout frequencies that are less than the new F1 will be set equal to F1.

ERRORS: If **f** is outside the frequency range of the current receiver, the command is ignored. If **f** is greater than the current Stop frequency (F2), the Stop frequency is set equal to the Start frequency (F1). This allows F1 to be altered without causing an "F1 greater than F2" error before F2 can be altered.

"F1?"

Returns the Start frequency of the current SCB in the format " xxxx.xxxx MHz" (no leading zeroes), or " INVALID: NOT IN SCB" if not editing an SCB.

"F2 f"

Sets the Stop frequency (F2) of the current SCB to f (in MHz).

Note: When decreasing the Stop frequency, all the previously stored lockout frequencies that are greater than the new F2 will be set equal to F2.

ERRORS: If **f** is outside the frequency range of the current receiver, the command is ignored. If **f** is less than the current Start frequency (F1), the command is ignored. In this case, F1 must be changed first.

"F2?"

Returns the Stop frequency of the current SCB in the format " xxxx.xxxx MHz" (no leading zeroes), or " INVALID: NOT IN SCB" if not editing an SCB.

"FM"

Sets the detection mode for the current SCB to FM.

"LSB"

Sets the detection mode for the current SCB to LSB.

"L1 f1,f2"

Sets the first of five possible lockout frequency ranges in the current SCB. f1 must be less than f2 and both must be within the range of the SCB's Start and Stop frequencies (F1 and F2). The two parameters are separated by a comma in the command string.

ERRORS: The command is ignored if:

(a) not editing an SCB,
(b) f1 or f2 are outside the F1-F2 Band range,
(c) f1 is greater than f2,
(d) improper format (i.e. no comma).

"L1?"

Returns the frequency range of the first lockout in the format " c,f1,f2 MHz". c is either "ON" or "OFF" signifying whether the lockout is enabled or disabled. f1 and f2 (leading zeroes are dropped) are the start and stop frequencies of the lockout region within the sweep band. The command will return " INVALID: NOT IN SCB" if not editing an SCB.

"L2 f1,f2"

Sets the second lockout range as above.

"L2?"

Returns the frequency range of the second lockout as above.

"L3 f1,f2"

Sets the third lockout range as above.

"L3?"

Returns the frequency range of the third lockout as above.

"L4 f1,f2"

Sets the fourth lockout range as above.

"L4?"

Returns the frequency range of the fourth lockout as above.

"L5 f1,f2"

Sets the fifth lockout range as above.

"L5?"

Returns the frequency range of the fifth lockout as above.

"L n D"

Disables lockout range **n**, where **n** is a number from 1 to 5 representing the five possible lockout ranges. The f1 and f2 data remains in the SCB, but the lockout region will NOT be skipped during the sweep scan. The

receiver will execute the scan throughout the lockout range and stop on any signals above threshold.

ERRORS: If an invalid value of **n** is received, the command is ignored. The command is also ignored when not editing an SCB.

"L n E"

Enables lockout **n**, where **n** is a number from 1 to 5 representing the five possible lockout ranges. During a sweep of this band, the receiver will skip over the range of lock out **n** without stopping on signals.

ERRORS: If an invalid value of **n** is received, the command is ignored. The command is also ignored when not editing an SCB.

"PLS"

Sets the detection mode for the current SCB to PLS.

"PRD"

Sets the Pre-Hit dwell time for the current SCB to **n**, range 0 to 9. The Pre-Hit dwell time is the inverse of the sweep speed; 9 causes the slowest sweep, 0 the fastest.

ERRORS: If an invalid value of **n** is received, the command is ignored. The command is also ignored when not editing an SCB.

"PRD?"

Returns the value or the Pre-Hit dwell time for the current SCB. Returns " INVALID: NOT IN SCB" if not editing an SCB.

"RFG n"

Sets the RF Gain level of the current SCB to **n**, where **n** is 0 to 63. 0 is maximum gain, 63 is minimum. The data is placed in memory regardless of the receiver gain mode, but the mode must be manual ("AGC/") for the RFG level to be used.

"RFG?"

Returns a number from 0 to 63 indicating the RF Gain level of the current SCB. Data is returned regardless of receiver gain mode.

"SWI f"

Sets the size of the sweep increment steps to **f**, expressed in MHz. The frequency, f, range is 0.0001 to 4 MHz.

ERRORS: The Command is ignored if not editing an SCB or if the value of f is out of range.

"SWI?"

Returns the sweep step increment in MHz for the current SCB. Returns " INVALID: NOT IN SCB" if not editing an SCB.

"USB"

Sets the detection mode for the current SCB to USB.

The following five commands control the execution of a Band Scan:

1) **"BND* <parameters>"**
2) **"BND*?"**
3) **"CONT* "**
4) **"SWP* "**
5) **"SWP*?"**

"BND* <parameters>"

Includes the bands specified by the parameter list. Band numbers not in the list are implicitly disabled. The parameter list must contain all the valid band number(s) to be included, and are separated by commas. The command is ignored if the receiver is already scanning.

Example: **"BND* 3,2,5"** (numbers need not be in order) will execute bands 2, 3, and 5 in the Band Scan, and disable bands 1 and 4. If a subsequent **"BND* 1,3"** command is issued, bands 1 and 3 will be executed and bands 2, 4 and 5 will be disabled.

ERRORS: The command will be ignored if the receiver is not in REMOTE control, if there is an invalid band number, if the receiver is already scanning, or if editing an SCB.

"BND*?"

Returns the message **" BAND a,b,c,d,e"**, where the variables represent the list of included bands similar to the **"BND * <parameters>"** command. The message **" BAND NONE"** is returned if no bands are included for the Band Scan.

Note: Receivers with software dated before December 1986 do not have the Band Scan capability, in this case the message returned is **" BAND NOT AVAIL"**. If the IOM108 has software dated before December 1986, **" INVALID READ"** is returned.

"CONT* "

Continues a scan from the point it stopped, such as during a dwell or hit.

ERRORS: The command is ignored if the receiver is not in a Remote Scan mode or already scanning.

"SWP* "

Starts or re-starts the receiver Band Scan. The bands which will be scanned are those which were included by the **"BND* <parameters>"** command. Prior to issuing the **"SWP*"** command the **"BND* <parameters>"** command should be issued to make sure that the correct Bands are set up.

If the receiver is already executing a sweep scan, the scan will begin again with **f1** of the lowest included band number.

ERRORS: The command is ignored if:
(a) the receiver is not in REMOTE control,
(b) there are no included Bands,
(c) the receiver is executing a step scan,
(d) editing an SCB.

"SWP*?"

Returns the scanning status of the receiver in the following messages:

" MAN*" — Receiver in Manual mode, not scanning.
" STP*" — Receiver in Channel scan.
" SWP*" — Receiver in Band scan (sweep scan).

2.4.3.6 Master/Handoff Option Operation

This section describes the front panel operation of the WJ-8628-4 Receiver equipped with the Master/Handoff Option. The master/handoff software increases the flexibility of the receiver controller by permitting it to directly control one or more slave receivers located in the local frame and in other frames. Any slave receiver in the WJ-9040 System Family can be monitored and controlled by the WJ-8628-4 Master Receiver/Receiver Controller. The direct handoff function, however, where the active status of the master unit is down-loaded to a slave receiver, is possible only between compatible types (HF to HF or VHF to VHF).

2.4.3.6.1 Master/Handoff Hardware Configuration

The minimally configured master/handoff system is structured around the EFR100 Equipment Frame. The EFR100 is designed to accept the various plug-in modules in the WJ-9040 System Family. These modules are available in three sizes: one-eighth, one-quarter and one-half rack width. The EFR100 has eight internal connectors which mate with counterparts on the rear panel of each plug-in module. Insertion of a module causes its mating EFR100 connector to become active via recognition software in the IOM108. To successfully implement the Master/Handoff Option, the following hardware items, as a minimum, must be present in the EFR100:

1. One WJ-8628-4 Receiver/Controller with MH Option
2. WJ-8628-1 Slave Receivers (one or more)
3. One IOM108 I/O Interface Module
4. One EPS100 Power Supply
5. One FRM150 Frequency Reference Module or SRM105A Site Reference Module

The Receiver/Controller can control slave receivers in more than one frame. The additional frames are connected via the WJ-9040 high speed data link. **Figures 2-6** and **2-7** depict simplified hardware interconnection requirements for implementing single frame and multi-frame master/handoff subsystems.

2.4.3.6.2 **Handoff Addressing Assignments**

Address assignments for handoff receivers are performed by the controller on power-up and are verified every 10 seconds. **Figure 2-8** shows one example of address assignments for a two-frame handoff subsystem consisting of a controller and three handoff receivers. The handoff address assignments are used by the operator in performing master/handoff operation sequences **(paragraph 2.4.3.6.4).**

NOTE

The WJ-9040 System is comprised of customer-selectable receiver modules and ancillary devices. The arrangement of modules within equipment frames is a matter of choice. For the purpose of this manual, the receivers are located as shown in **Figure 2-7** and **Figure 2-8.** The terms "slave" receiver and "handoff" receiver are used interchangeably regardless of their handoff compatibility with the master receiver **(paragraph 2.4.3.6).**

2.4.3.6.3 **Initialization on Power-Up**

When power is applied to the WJ-8628-4, the battery-backed memory attempts to restore the previous operating mode. If the previous mode was a remote control function such as an RMT or RMT scan, the WJ-8628-4 initializes itself only, and assumes the status RMT, waiting for instructions from the external controller.

If the power-down mode was any other than a remote control function, the WJ-8628-4 attempts to configure the Master/Handoff Subsystem. The handoff receivers in the subsystem are identified and addresses are assigned by the master receiver. No action is required by the operator to perform this function on power-up. When initialization is finished, the control status of the WJ-8628-4 is EXEC, the main local operating mode. If any subsystem configuration errors occurred, a message remains on the display **(paragraph 2.4.3.6.5).**

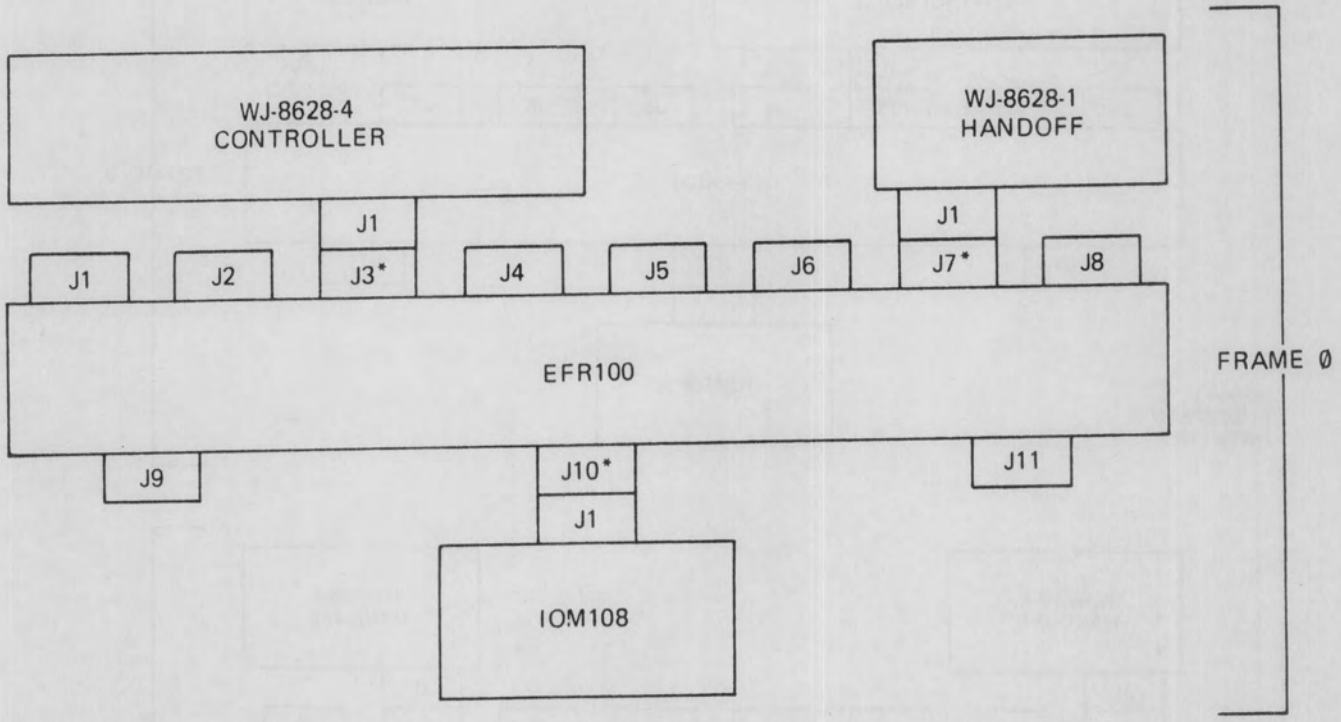


Figure 2-6. Single Frame Hardware Configuration

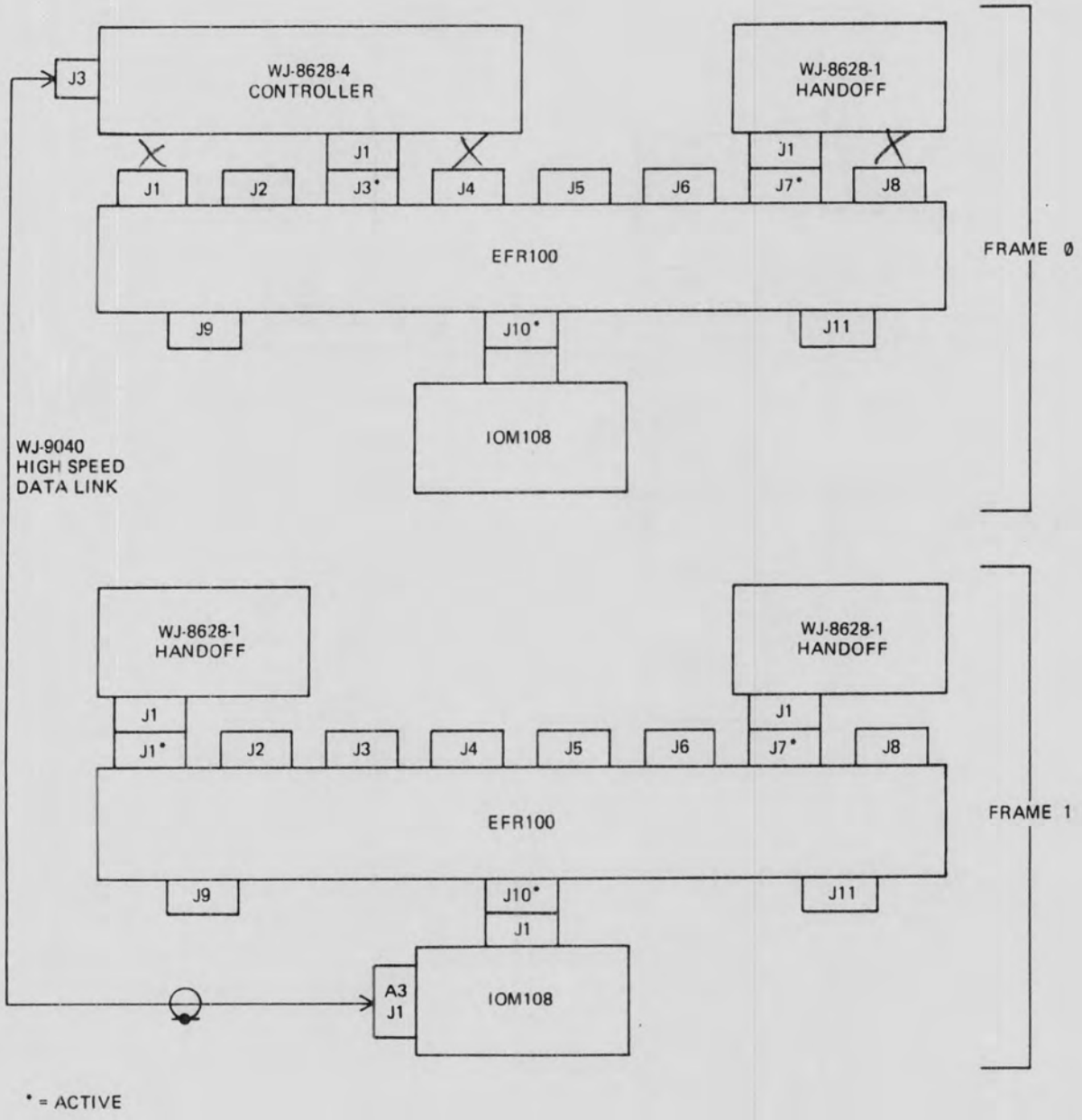


Figure 2-7. Multi-Frame Hardware Configuration

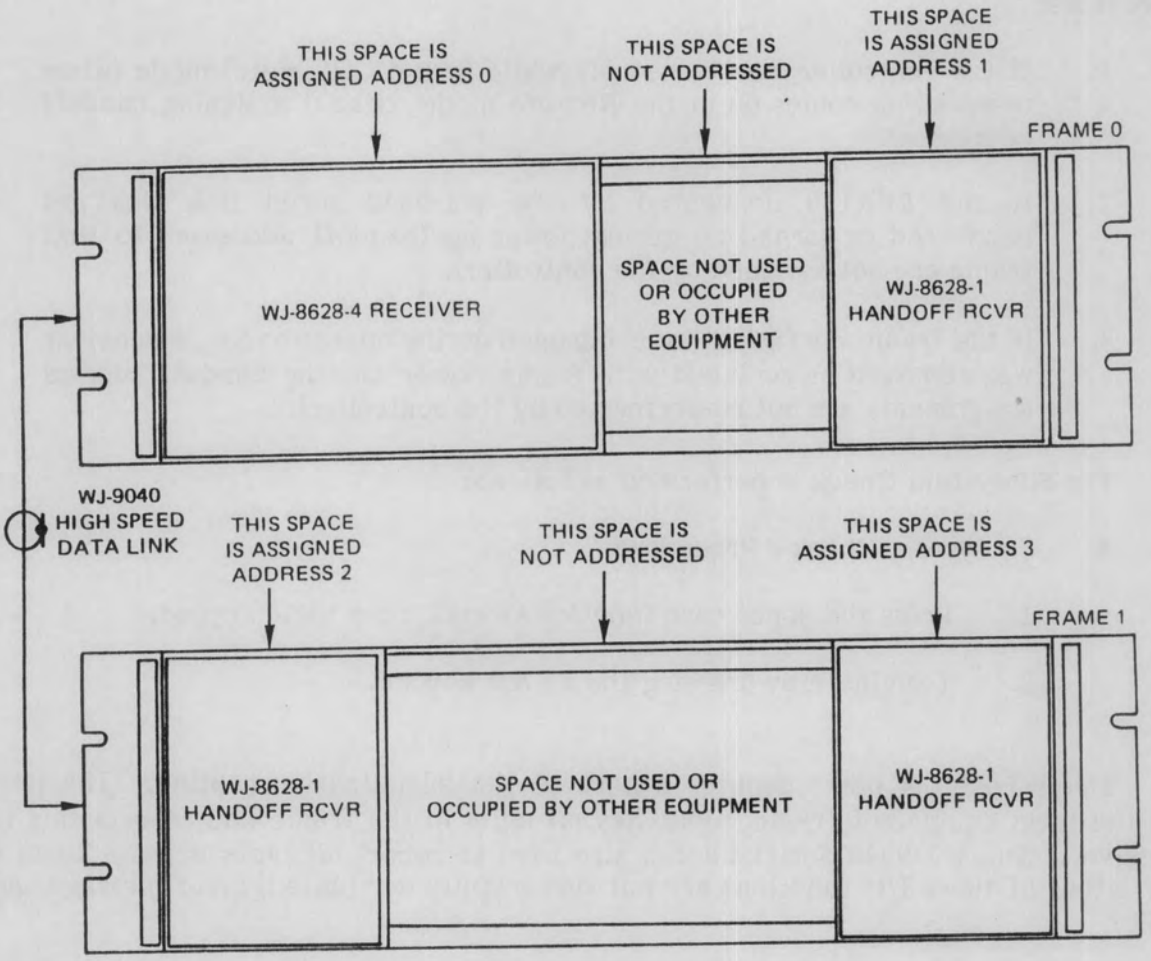


Figure 2-8. System Initialization Handoff Receiver Addressing

2.4.3.6.4 **Subsystem Check**

Prior to actually placing a handoff subsystem into operational service, it is recommended that a subsystem check be performed. This insures that all I/O functions are operational and informs the operator of the handoff address assignments. Additionally, the operator must use the subsystem check. A subsystem check would be necessary for one of the following reasons:

1. If the controller was turned off while in RMT (Remote) mode (when powered up comes on in the Remote mode .without assigning handoff addresses).

2. If the EFR100 connected by the WJ-9040 serial link was not connected or turned on during power up (handoff addresses to that frame are not assigned by the controller).

3. If the frame configuration is changed during operation i.e., a receiver was removed or replaced with frame power on (the handoff address assignments are not re-performed by the controller).

The Subsystem Check is performed as follows:

- Subsystem Check - Procedure

  1. Press the upper case function keypad, then the 0 keypad.

  2. Terminate by pressing the EXAM keypad.

The WJ-8628-4 now executes a part of the initialization routine. The IOM108, located in the local equipment frame, identifies all units in the frame and reports this to the master receiver. The WJ-9040 Serial Link is also used to report all units accessable in other frames. If either of these I/O functions are not successfully completed, error messages appear on the LCD.

Some WJ-9040 Receiving Systems may have more than one WJ-8628-4 receiver, or other units equipped with a front panel. While it is possible to have more than one master receiver in the subsystem, and for both of these to access the same handoff receivers, it is not possible to place a master receiver in a slave mode to another master receiver. If, during the subsystem check, more than one front-panel receiver is identified, the message, "Please Note.....1/2 Rack rcvrs are not configured as slaves" is displayed for a few seconds as a reminder to the operator.

After all I/O functions are completed and any messages have been cleared, the LCD displays the Frame 0 status as shown in **Figure 2-9.** Frame 1 status may be checked by stepping the cursor to the right. The LCD displays Frame 1 status as shown in **Figure 2-10.** Note the correlation between the LCD display areas and the hardware configuration shown in **Figure 2-7.** Additional frames, if connected, may be checked by stepping the cursor switch to the right.

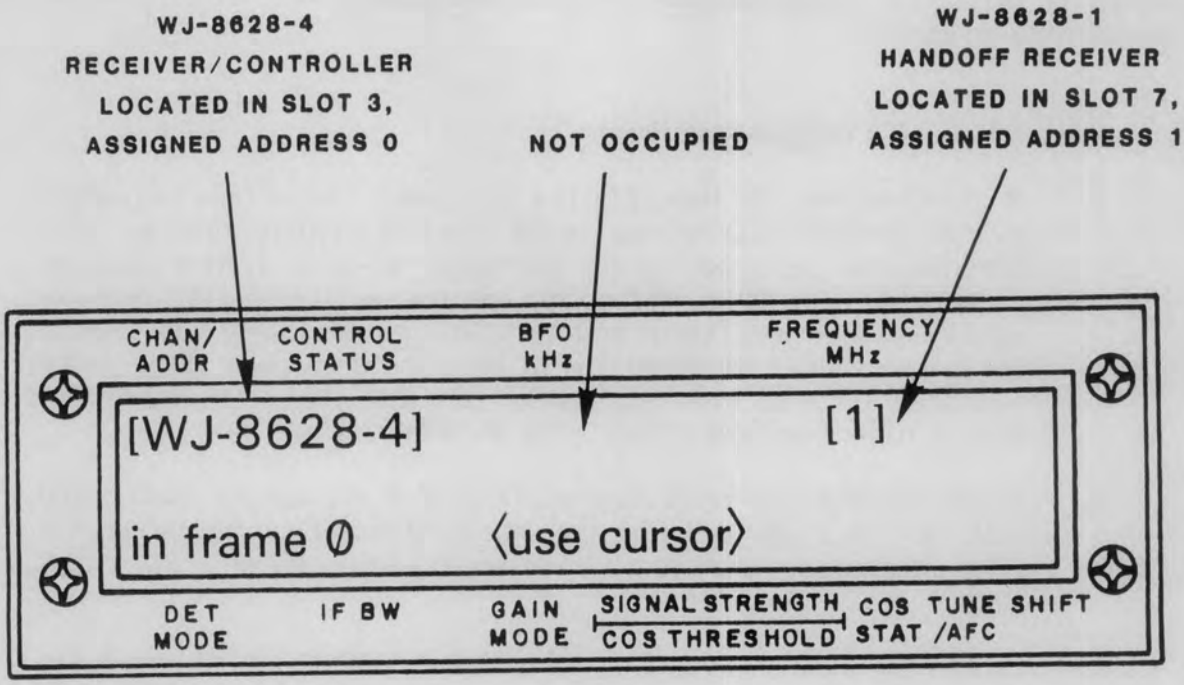


Figure 2-9. Subsystem Check, Frame 0 Status Display

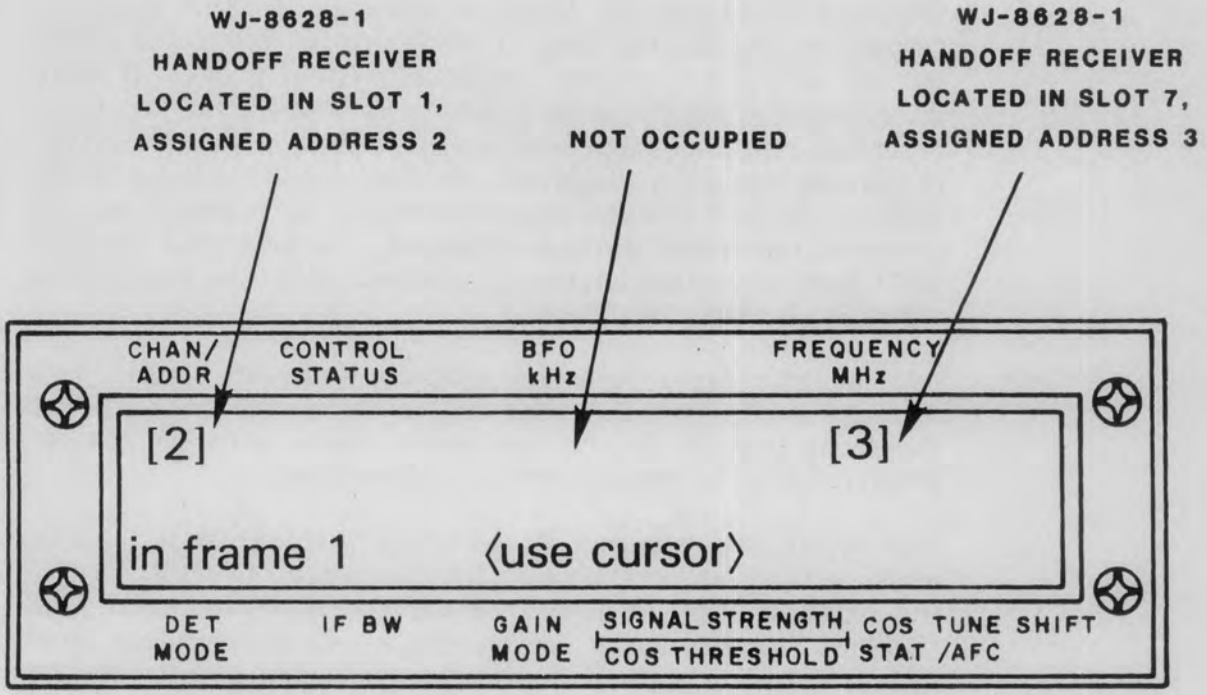


Figure 2-10. Subsystem Check, Frame 1 Status Display

To exit the subsystem check, press the CLR keypad to return to the previous display mode, or press the EXAM keypad for additional information about specific handoff receivers within the subsystem.

2.4.3.6.5 **Master/Handoff Configuration Errors**

1. If the IOM108 in the local EFR100 Equipment Frame fails to respond to the WJ-8628-4 during the Master/Handoff configuration, an error condition has occurred. If the particular WJ-9040 System does not contain an IOM108 in the equipment frame, the master receiver would also interpret this as an error. In response to any such fault in the local frame on power-up, the LCD on the front panel displays the message, "Error on Power-up Enter 11 OPR AID". The WJ-8628-4 then continues configuration via the WJ-9040 Serial Link.

2. If the IOM108 connected to the WJ-8628-4 via the WJ-9040 Serial Link fails to respond during the Master/Handoff configuration, the same message is displayed, "Error on Power-up Enter 11 OPR AID".

3. If both the local IOM108 and the external IOM108 fail to respond to the initialization commands, the same error message is displayed on the LCD.

4. Error Messages:

   A. "Error on power-up Enter 11 OPR AID". This message is displayed if either the local or external IOM108 failed to respond to the Master/Handoff configuration commands issued by the WJ-8628-4 on power-up or subsystem check. If more information about the error condition is desired, the keystroke described in the message may be entered and a second message (explained below) is displayed. If the second message is not desired, the next stroke of any key erases the message and the previous front panel status is displayed. The keystroke "11 OPR AID" may be entered later, if desired, with the appropriate secondary message displayed.

   B. "No Equip. Frame response; Possible hardware fault" This message is displayed following the keystroke "11 OPR AID" if the local IOM108 in the equipment frame with the master receiver failed to respond during configuration.

   C. "No Serial I/O response; Power? Coax? Hdwr? Busy?" This message is displayed following the keystroke "11 OPR AID" if the external IOM108 connected via the WJ-9040 Serial Link failed to respond during configuration. Causes for this error include no power applied to the external frame, disconnected or faulty coaxial cable, or the IOM108 is busy servicing another I/O such as IEEE-488.

D. "No Equip. Frame response; No Serial I/O response" This message is displayed following the keystroke "11 OPR AID" if both the local and external IOM108s fail to respond to the master receiver during configuration.

2.4.3.6.6 Master/Handoff Operating Procedures

The following paragraphs provide a detailed description of the techniques required to correctly operate the receiver in the master/handoff modes. The information provided is only applicable to properly configured subsystems as described in **paragraph 2.4.3.6.1.** The three basic master/handoff operations are:

- EXAM
- CTRL
- HANDOFF

2.4.3.6.7 Handoff Receiver Monitoring (EXAM)

The use of the EXAM keypad permits the receiver/controller to continuously monitor the status of any handoff receiver configured in its subsystem. The EXAM mode is a monitor mode only. All keys which cause the handoff receiver status to change are locked out from the receiver/controller front panel.

When preceded by a numeric data entry not greater than the highest handoff address, pressing the EXAM keypad results in the processing of the numeric entry as a handoff receiver address. The subsystem address, tuning range and frame location of the addressed receiver is displayed. Pressing the EXAM keypad a second time causes the handoff receiver's active status to be displayed, while the signal strength, COS status and center tuning are continuously updated on the master receiver's front panel.

When pressed, with no numeric data entries present, the EXAM keypad monitors each successive handoff receiver. After the last receiver, address 1, is selected the cycle may be repeated.

To exit the EXAM mode, the CTRL keypad may be used to directly enter the CTRL mode. The entry of 0, EXEC or 0, or CTRL returns the controller to the EXEC mode activating the local master receiver. **Example 17** illustrates the use of the EXAM keypad.

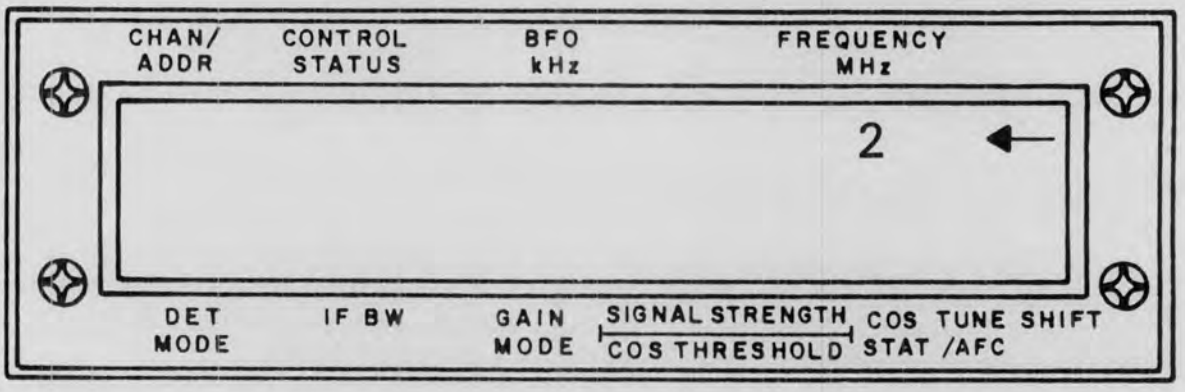
- Handoff Receiver Monitoring - Procedure

1. Press the upper case function keypad.
2. Enter the desired 1 or 2 digit handoff receiver address.
3. Terminate by pressing the EXAM keypad.
4. Press EXAM a second time to display handoff status.

Example 17. Monitor the Status of Handoff Receiver #2.

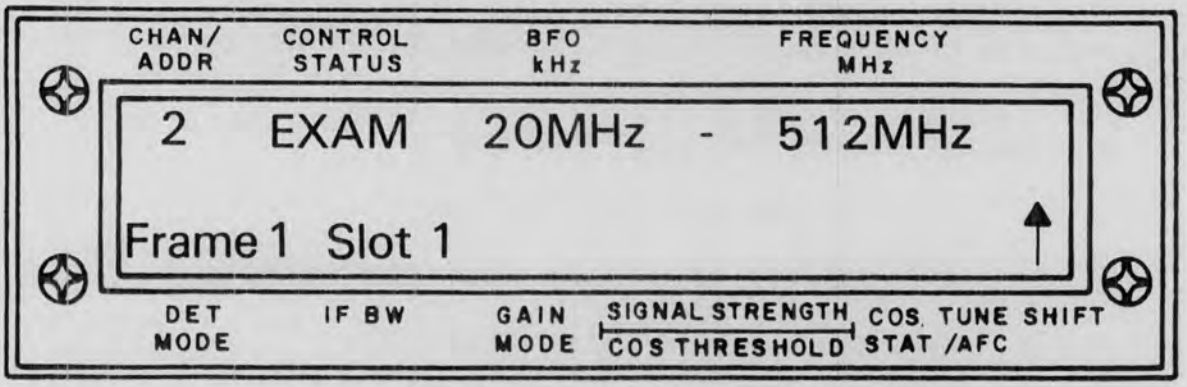
[↑] ..... (1) Sets the controller to respond to upper case functions.

[2] ..... (2) Desired handoff address data entry, "2" is displayed in FREQUENCY (MHz) window as shown below.

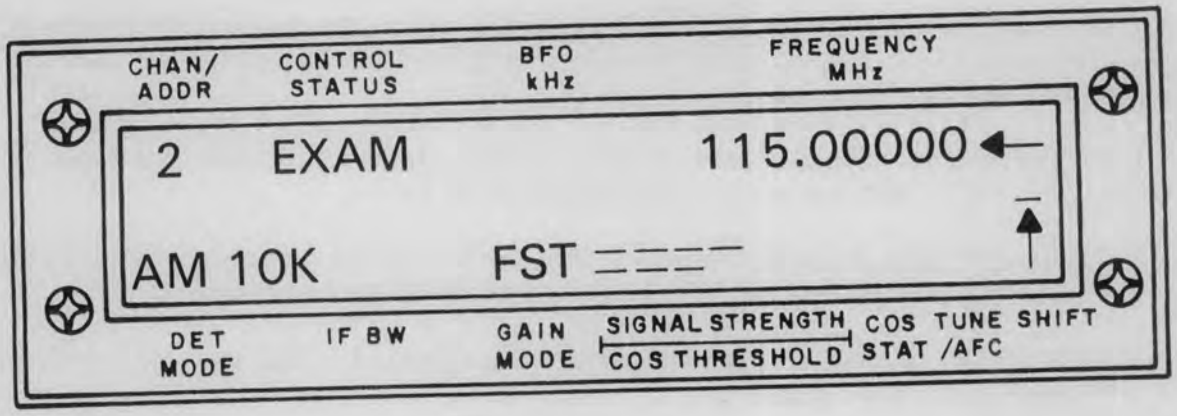


Example 17. Monitor the Status of Handoff Receiver #2 (Continued)

[EXAM] ..... (3) Termination command: FREQUENCY (MHz) returns to normal, "2" is displayed in CHAN/ADDR window. Handoff receiver address, tuning range and frame location are displayed as shown below.



EXAM ..... (4) Second termination command, addressed handoff receiver's status is displayed as shown below.



2.4.3.6.8 **Handoff Receiver Status Modification (CTRL)**

The use of the CTRL keypad permits the receiver/controller to modify the status of any handoff receiver configured in its subsystem. The CTRL mode is both a status modification and a status monitoring mode. Handoff receiver parameters (signal strength, COS status and center tuning) are continuously sampled and updated. The CTRL operation is similar to the EXAM operation except that the status change keys in CTRL are enabled on the receiver/controller front panel.

When preceded by a numeric data entry not greater than the highest handoff address, pressing the CTRL keypad results in the processing of the numeric entry as a handoff receiver address. The status of the addressed receiver is displayed and all receiver parameter keys are enabled. Addressed receiver parameters may be changed using procedures given in **paragraph 2.4.3.2**, but without entering the 0 EXEC keystroke.

When pressed, with no numeric entries present, the CTRL keypad accesses each successive handoff receiver. After the last receiver, address 1 is selected and the cycle may be repeated.

To exit the CTRL mode, the EXAM keypad may be used to directly enter the EXAM mode. The entry of 0, EXEC or 0, or CTRL returns the controller to the EXEC mode enabling the local master receiver. **Example 18** illustrates the use of the CTRL keypad.

- Handoff Receiver Status Modification -Procedure

  1. Press the upper case function keypad.
  2. Enter the desired 1 or 2 digit handoff receiver address.

3. Terminate by pressing the CTRL keypad.

4. Enter new handoff receiver parameters, as desired, directly through the controller keypad.

2.4.3.6.9 **Front Panel Status Transfer (H/OFF)**

The use of the H/OFF key permits the receiver/controller to perform a transfer of its front panel status to any similar handoff receiver configured in its subsystem. The use of H/OFF is subject to the following conditions:

1. The H/OFF keypad must not be used with receivers of different types (e.g., HF/VHF). Attempting to do so results in an error.

2. Handoff data transfer transmits only the IF BW slot number of the controller. The actual BW installed in the handoff receiver may be different.

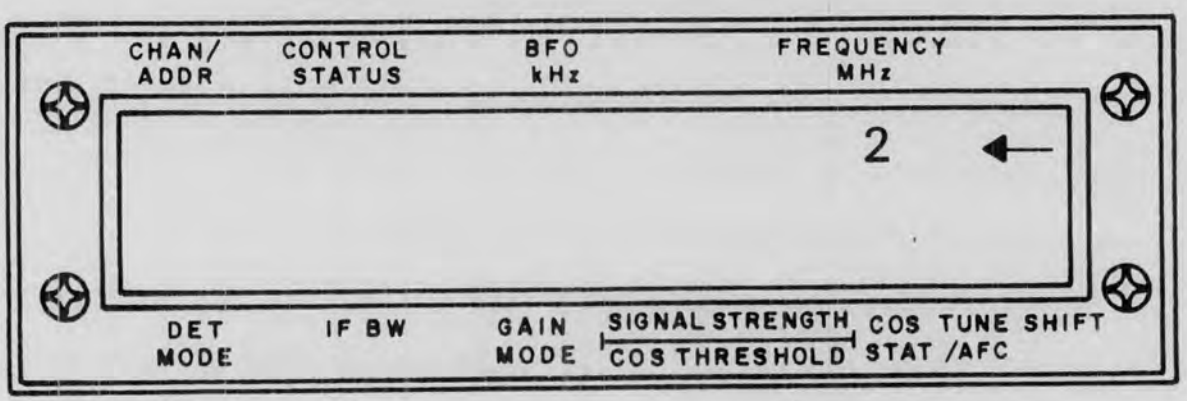
3. If an unavailable IF BW slot number is requested in the handoff receiver, it defaults to BW number 1.

4. If the controller has options which cannot be transferred, an appropriate message is displayed.

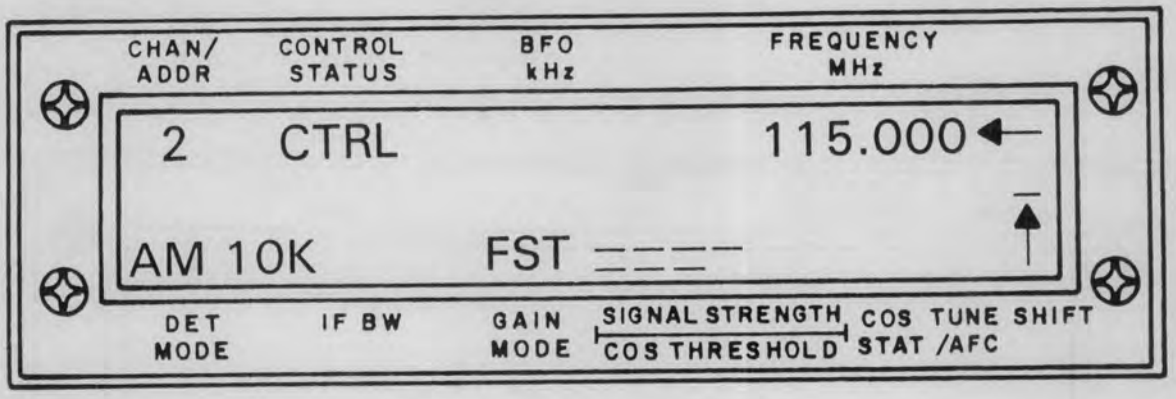
Example 18. Modify Status of Handoff Receiver #2.

[↑] ..... (1) Sets the controller to respond to upper case functions.

[2] ..... (2) Desired handoff address data entry, "2" is displayed in FREQUENCY (MHz) window as shown below.



CTRL ..... (3) Termination command: receiver parameter keys are enabled, addressed receiver status is displayed as shown below.



RECEIVER PARAMETER KEYS ..... (4) Parameter changes are entered as desired, addressed receiver status changes as parameters are entered, controller display immediately updates to new parameters.

When preceeded by a numeric data entry not greater than the highest handoff address, pressing the H/OFF keypad results in the processing of the numeric entry as a handoff receiver address. The handoff receiver's status is changed to agree with the parameters currently displayed on the controller front panel. The controller then acknowledges a correctly executed H/OFF by displaying the handoff address, subsystem location, IF BW slot number and actual handoff receiver bandwidth.

The handoff acknowledgement display is terminated by pressing any keypad.

Pressing EXAM or CTRL immediately after H/OFF causes the controller to enter the EXAM or CTRL mode for the designated handoff receiver. See **paragraphs 2.4.3.6.7** and **2.4.3.6.8** for information concerning the use of these two keypads. Any key other than EXAM or CTRL restores the Control Status to the previous mode (EXEC, RCLm). **Example 19** illustrates the use of the H/OFF keypad.

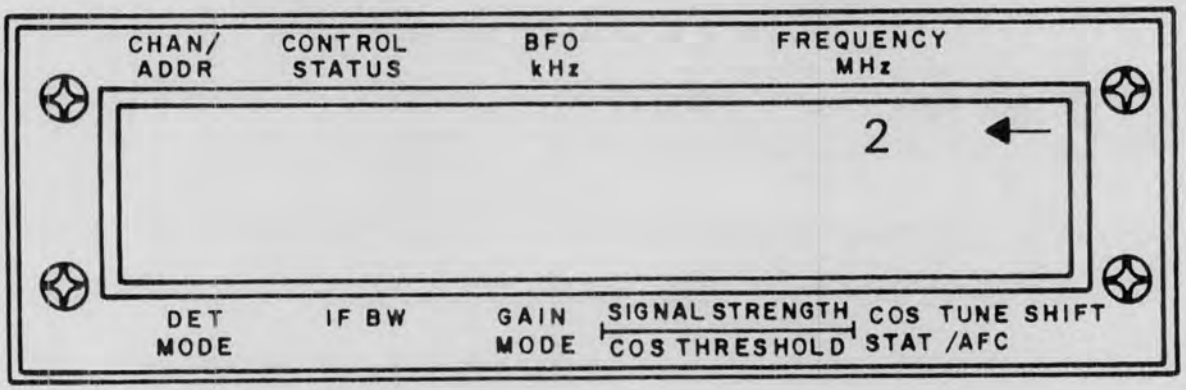
- Front Panel Status Transfer - Procedure

  1. Press the upper case function keypad.
  2. Enter the desired handoff receiver address.
  3. Terminate by pressing the H/OFF keypad.

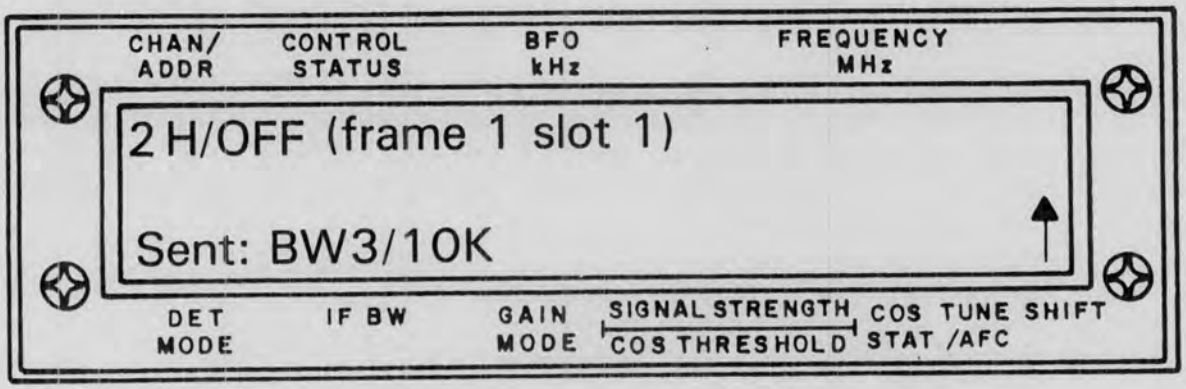
Example 19. Transfer Controller Parameters to Handoff Receiver #2.

[↑] ..... (1) Sets the controller to respond to upper case functions.

[2] ..... (2) Desired handoff address data entry, "2" is displayed in FREQUENCY (MHz) window as shown below.



[H/OFF] ..... (3) Termination command: handoff receiver status is changed to agree with controller. Handoff receiver address, subsystem location, IF BW slot number and actual bandwidth is displayed as shown below.



2.4.3.7 SCAN Option Operation

The WJ-8628-4 VHF/UHF Receiver equipped with the SCAN Option can be programmed to sweep up to five operator-entered frequency bands. Each of the five sweep bands has separate step increments which are adjustable from 100 Hz to 4 MHz. Each sweep band can also be set up with a different threshold, IF bandwidth and detection mode when searching more than one spectral region. Within each of the five sweep bands, up to five lockouts of variable width can be programmed.

- Programming the SCAN - Procedure

  1. Press the upper case function keypad.

  2. Press the SET keypad.

  The display will prompt with the following question: "SETUP which scan type use curs F1-F2 (?) CHAN"

Moving the cursor to the right provides setup information for the channel (or step) scan function. Move the cursor to the left to set up the sweep scan. The next prompt, "SET = next, SET = prev, SYSCLR = exit, OPRAID = info" reminds the operator of the most frequently used keys during the setup. Approximately ten display fields are interactively used to allow the operator to modify all scan parameters. The operator should remember these primary setup keys.

Help messages are also available to provide additional information when the OPR AID key is pressed and held.

To exit the setup mode, the SYS CLR key returns the receiver to the EXEC operating mode.

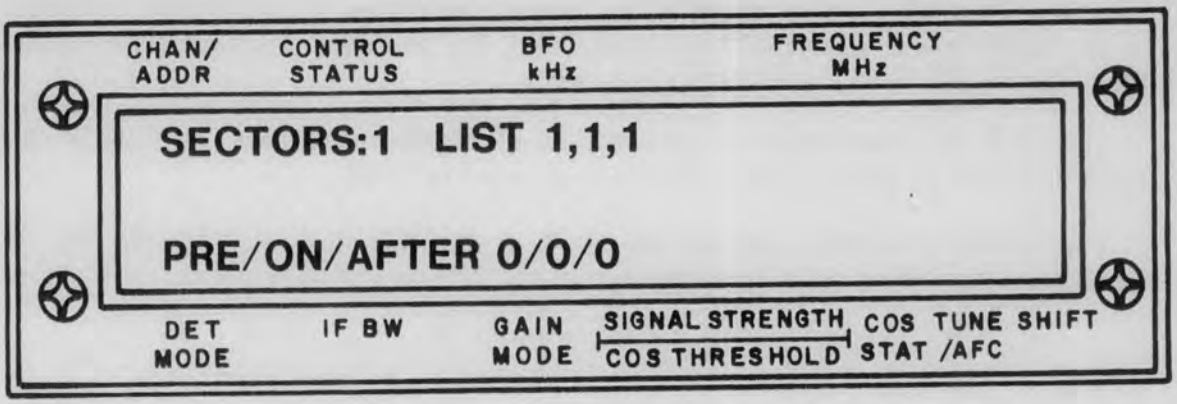
To advance to the next display field, press the SET key.

To return to the previous display, press . (decimal point), then SET.

This informational display is provided only once upon entering the setup mode.

To continue the setup, press the SET key.

Example 20, below, illustrates the main F1-F2 setup field.



Following the "SECTORS" label is the number (0 to 5) of frequency bands currently included (activated or enabled) for scanning. This does not indicate whether the setup contains valid information, only whether or not it will be executed.

To include a band in the active list for scanning, be sure the upper case is selected, then enter a number from 1 to 5 followed by INCL. Only one band may be included or locked out during each keystroke. To include band 3 type: "3, INCL".

To lockout (or deactivate) a band, be sure the lower case is selected, then enter a number from 1 to 5 followed by L/OUT.

The keypad entry, LIST, displays a string representing the frequency band numbers which are included (enabled). Each number in this area is separated by a comma, and scrolls horizontally when the CURSOR switch is pressed. This allows the operator to verify which bands are included. Each time a band is included or locked out, the list is updated.

The PRE/ON/AFTER field shows the dwell times currently entered. An explanation of their function follows. To set new dwell times, all three parameters must be entered. First, be sure the upper case is selected, then enter "x . y . z DWL" where x, y and z are number keys from 0-9.

2.4.3.7.1 Dwell Times

The pre-dwell time is the time in milliseconds (0-9) the receiver remains on each new frequency increment waiting for possible RF activity. A pre-dwell of 0 pauses until the synthesizer has settled before testing once for peak energy to determine if the signal level is above threshold. This gives the fastest scan possible. A pre-dwell of 9 pauses until the synthesizer has settled, then opens the peak sample circuit for 9 milliseconds and compares it to threshold. A longer pre-dwell increases the reliability of capture, especially if AM or pulse modulated signals are encountered.

The on-hit dwell time is the time in seconds (0-8 or infinite) the receiver remains on a signal above threshold. The on-hit dwell time is activated as soon as energy is detected and on all signal transitions from below threshold to above threshold. Most scanning receivers halt and stay on a signal as long as it is present. This is set on the WJ-8628-4 by entering an on-hit dwell time of 9, or infinite. In this condition the receiver remains on the signal as long as it is above threshold.

If signals with a constant carrier are expected, and the operator requires only a brief time to identify the signal and take appropriate action, the on-hit dwell time can be reduced. The WJ-8628-4 will time out, exit the dwell time and go to the next frequency while the first signal is still active. For example, if an on-hit dwell time of 5 seconds is selected and the scan passes through a commercial broadcast band, the receiver halts on each signal above threshold for five seconds before continuing the sweep.

The after-hit dwell time is activated on all signal transitions from above threshold to below threshold, such as when a push-to-talk transmission ends.

The after-hit dwell time is the time in seconds (0-8 or infinite) the receiver remains on a frequency where a hit has just occurred. If the signal is expected to return and

the operator wants to wait for it, the after-hit dwell time is set accordingly. If no waiting is desired, the after-hit dwell time is set to 0. If an infinite wait is desired, set this parameter to 9.

2.4.3.7.2 Selecting and Programming the Band

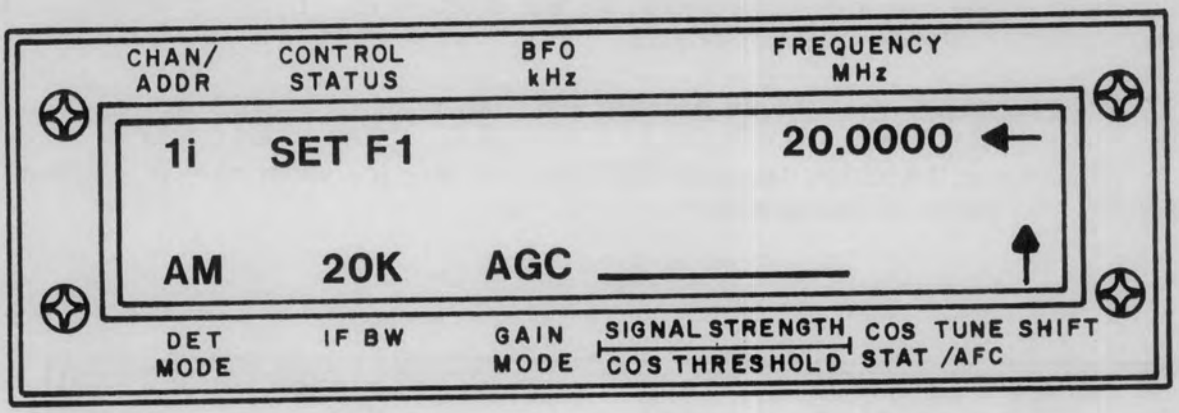
To proceed from the main setup display described in **paragraph 2.4.3.7.1**, a specific frequency band must now be entered for programming. The SET key is the terminator for data entry.

- Selecting and Programming the Band - Procedure

  1. Press the upper case function key.
  2. Eenter a band number from 1-5.
  3. Press the SET keypad.

A help display is available by pressing and holding the OPR AID key. **Example 21** illustrates the method of programing frequency band 1.

Example 21. Program Frequency Band 1.



The CHAN/ADDR area of the LCD indicates "1" for the band being programmed.

The "i" character next to the band number indicates the included status of the band, i.e. whether it is in the active list to be executed during a scan. A band not included would display a blank space. To include this band, simply press INCL. To lock it out (or deactivate), press L/OUT.

Programming the band can continue regardless of its include status. Bands can also be included or locked out in the main setup field.

The CONTROL STATUS is "SET F1", with all receive tuning parameters displayed. No signal strength or COS status is present because the receiver is not presently tuned to this setup.

Using conventional front panel keystrokes and tuning, select the start frequency of this band, COS threshold, and all other parameters applicable to the signals of interest. If the receiver halts on activity during the scan, these parameters will become the tuned status.

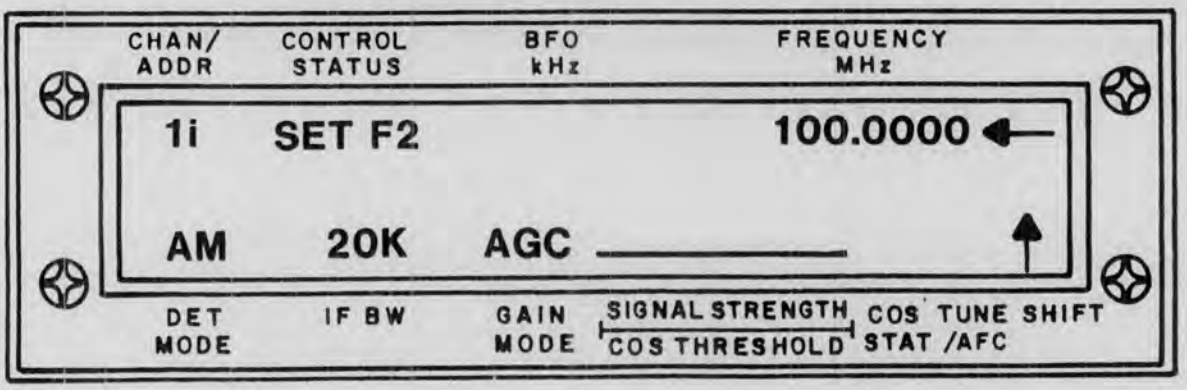
The COS threshold is particularly important since it is compared with the signal strength to determine whether or not a hit has occurred. Manual gain mode and AGC have different optimum settings.

If scanning in the manual gain mode, the COS threshold should be set to 20, or near the left edge of the dashed line in the LCD signal strength display area. The RF gain control on the front panel is then used to adjust the receiver gain during the scan.

If scanning in the AGC mode, the operator must use his experience to set the best threshold for the IF bandwidth and signals expected. If the threshold is very low, around 10 or less, the threshold triggers on noise and stops on all new frequencies. If the threshold is set too high, desired signals of interest might be missed.

A help display is available by pressing and holding the OPR AID key.

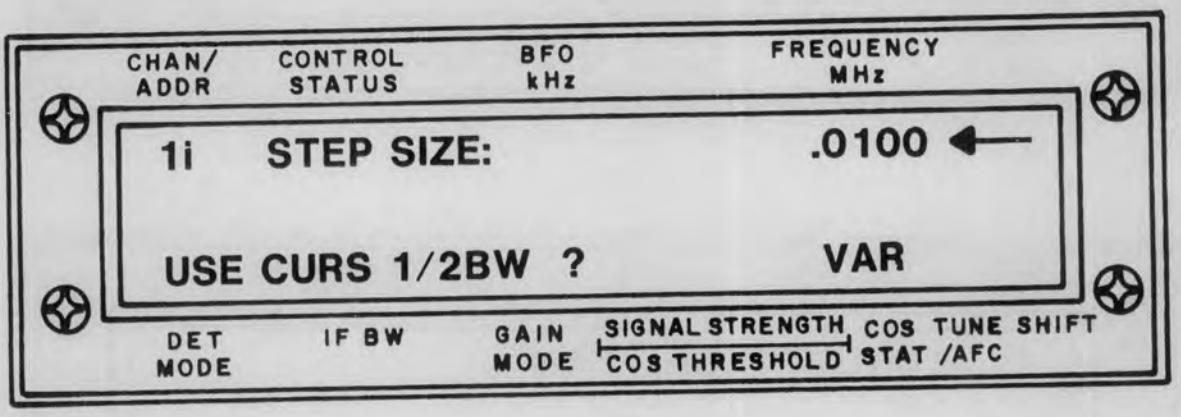
To continue the setup, press the SET key. Be sure the upper case is selected. The next display is shown below as **Example 22.**



The CONTROL STATUS is now "SET F2". Select the stop frequency of this band. All other parameters are re-displayed and may be changed if desired. The WJ-8628-4 program ensures that both the F1 and F2 displays are the same.

A help display is available by pressing and holding the OPR AID key.

To continue the setup, press the SET key. Be sure the upper case is selected. The next display is shown below as **Example 23.**



This display field indicates the frequency increment which the receiver will step.

IF the cursor is pressed to the left, the receiver automatically selects a step size equal to one-half the IF bandwidth selected during the SET F1 or SET F2 fields. In the example above, since the IF bandwidth was 20 kHz, the default step size is 10 kHz, displayed as 0.01 MHz.

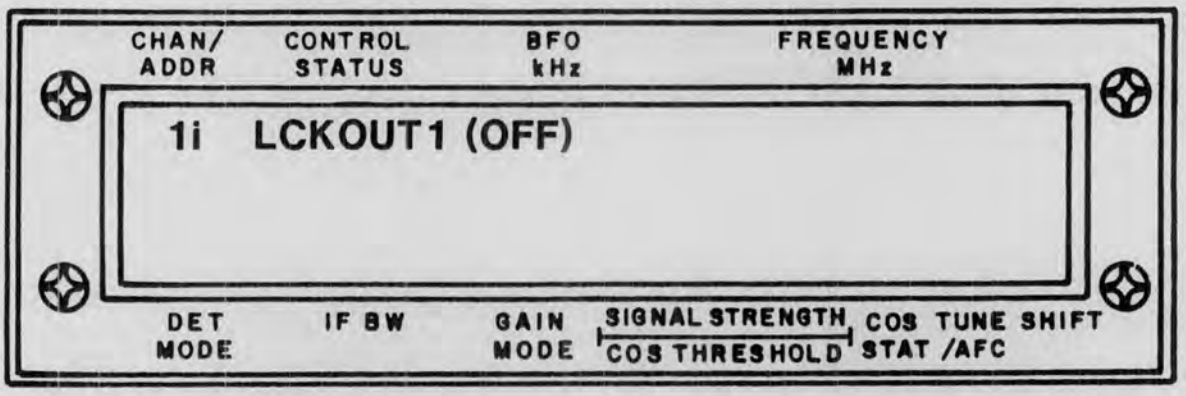
If the cursor is pressed to the right, the operator may key in a step size larger or smaller than the default value. To enter a step size, ensure that the cursor has been pressed toward the "VAR" symbol, enter keypad data and terminate with either the kHz or MHz key. (Date may be entered in kHz or MHz format but is displayed as MHz.)

The variable step feature is useful if a full IF bandwidth step will give an acceptable probability of intercept. This would double the scan rate. Another application is in wideband multi-channel group signals, where channel frequencies are known and could be visited in an interleaved sequence by properly selecting the IF bandwidth and a larger step size.

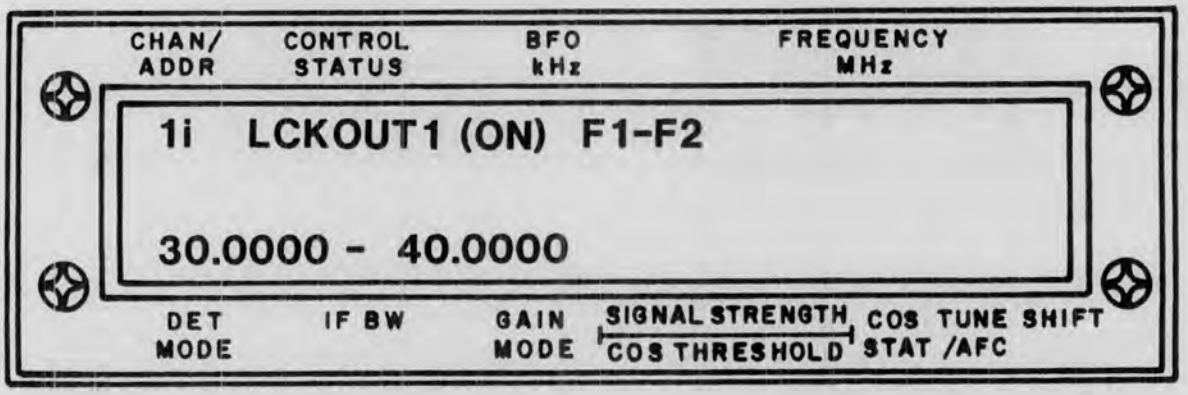
A help display is available by pressing and holding the OPR AID key.

2.4.3.7.3 **Programming Lockout Regions**

To continue the setup, press the SET key. Be sure the upper case is selected. The next display is shown below as **Example 24.**



or,



The next five fields program the lockout frequencies. The CHAN/ADDR is still band 1. The "i" indicates that this band will be executed during the scan.

The CONTROL STATUS is "LOCKOUT1", meaning that the first of five lockouts for this band is being entered.

If this lockout is NOT enabled, the word "OFF" is displayed. No frequency information is present since the lockout is not active. The lockout region, even if previously programmed with frequencies, is ignored and the scan then passes through that region normally, dwelling on any hit found.

If this lockout is activated, the word "ON" is displayed. The "F1-F2" is the format for programming the lockout. A sub-band from F1 to F2 will be locked out. The frequencies on the bottom line are the lower and upper limits of this lockout region. The receiver will pass over this range of frequencies without testing for signals.

To enable this lockout, use the INCL key. Be sure the shift arrow is up and press INCL. The "ON" indicator appears and the lockout frequency limits are displayed.

To disable this lockout, use the L/OUT key. The lower case must be selected, then press L/OUT. The "OFF" indicator appears and lockout frequencies are erased from the display, but retained in the receiver memory.

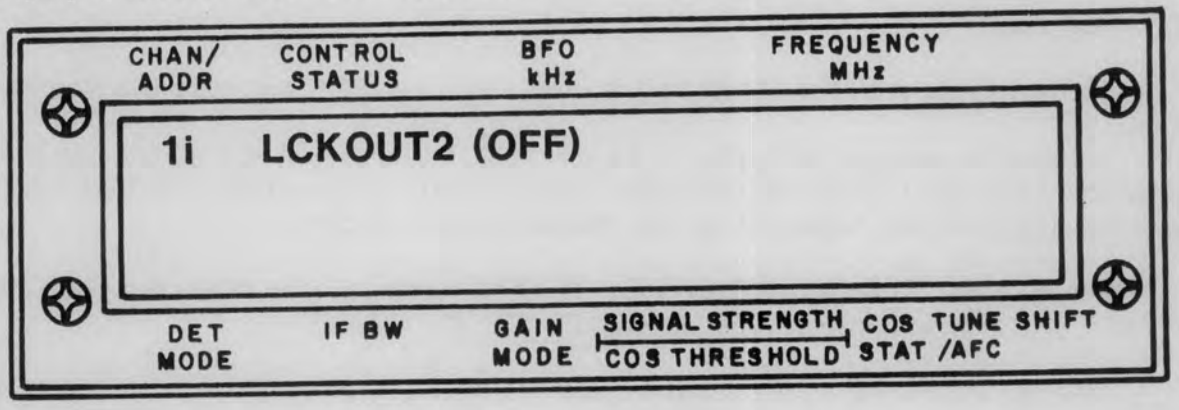
To set up an included or "ON" lockout, use the cursor switch to place the underscore below the desired frequency digit and use the tune wheel.

If the underscore is anywhere on the left side frequency (F1), the number keys and MHz may be used to enter a frequency. If the underscore is on the right side to tune F2, the number and MHz keys will enter the F2 frequency.

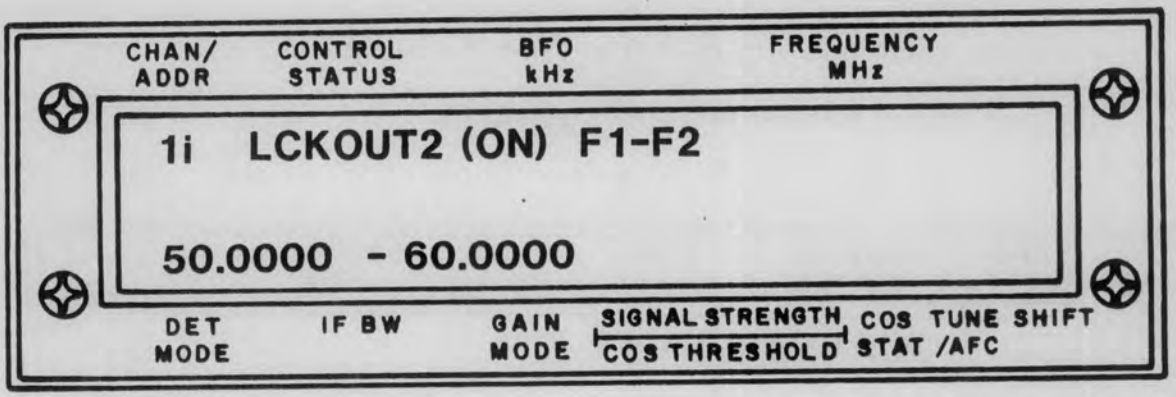
Range checking validates the data and allows frequencies only within the original F1 and F2 scan limits.

A help display is available by pressing and holding the OPR AID key.

To continue the setup, press the SET key. Be sure the upper case is selected. The next display is shown below as **Example 25.**



or



Continue setting lockout regions 2-5 as described in the previous paragraphs.

When all five lockout regions have been programmed, continue with the SET key. The main display showing the number of active sectors and the dwell times will be presented. In this field, and in the "SET F1" and "SET F2" fields, the INCL and L/OUT keys are used to enable and disable the entire band, not a lockout region.

From the main display, use the number keys to enter a band number from 2 thru 5, followed by the SET key to begin programming another scan band. If only one band is included in the active scan list, the others need not be set up.

The exit the scan setup mode, press SYS CLR once. If SYS CLR is pressed more than once, or from any control mode other than scan set, the memory clearing menu appears. This function is intended for emergency erasure of all receiver data, but the operator can easily escape if accidentally entered. Read the displayed instructions or press OPR AID for help. The WJ-8628-4 operating manual provides more information on using the SYS CLR.

2.4.3.7.4 Scanning

To begin scanning, the SCAN key is used. Be sure the lower case is selected, then press SCAN.

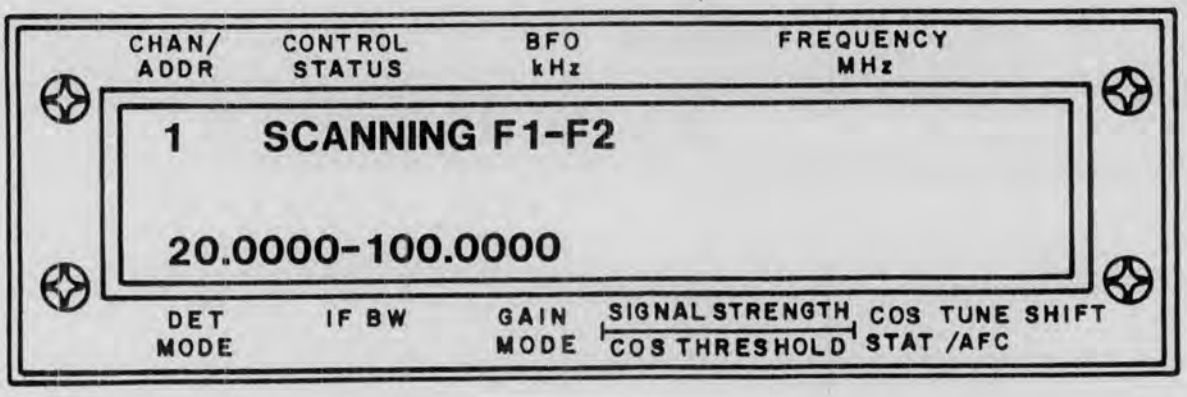
If the main scan setup display is on the LCD, the receiver begins scanning the type of scan previously set up. If in the F1-F2 setup mode, the SCAN key starts the F1-F2 scan. If the channel (or step) scan was being set up, the channel scan is started.

For all other front panel CONTROL STATUS modes, a scan menu is displayed with the prompt: "EXECUTE which scan type use curs F1-F2 ? CHAN"

Moving the cursor to the right begins the channel, or step scan, where up to 99 discreet memory channels are tested for signal presence. Refer to the section on channel scanning for more information.

Press the cursor switch to the left to begin the sweep scan.

The next display is shown below as **Example 26.**



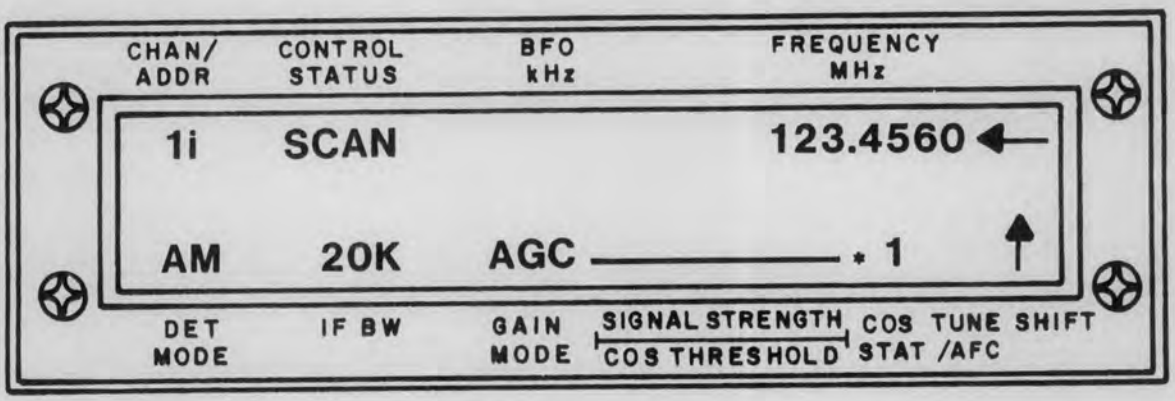
The "CHAN/ADDR" on the display is 1, indicating that band 1 is now active. The CONTROL STATUS is "SCANNING F1-F2". The start and stop frequencies of the band being scanned are shown on line 2.

If the scan was set up in the manual gain mode, the RF gain control on the front panel can be used to adjust the receiver gain to optimize the capture of signals, and avoid excessive unwanted signals.

The actual tuned frequency is not updated during scan because it is processed too fast to be meaningful to the operator and would require additional processor time to write to the LCD.

If a signal above threshold is found, and if the on-hit dwell and after-hit dwell times are greater than 0, the receiver steps and displays all tuned parameters. The dwell counters are initialized to the times programmed and the operator may take appropriate action while dwelling.

The display during a scan halted on energy is shown below as **Example 27.**



NOTE

If the signal level is exactly at COS threshold, it is possible that the squelch status will repeatedly toggle on and off. On each transition, the "on" and "after" dwell timers are reinitialized. If they are programmed to values greater than 0, the receiver may remain on the frequency for an indefinite time.

If the WJ-8628-4 is also equipped with the Master-Handoff Option, the tuned parameters can be passed to a properly configured WJ-8628-1 receiver. This is only allowed in a scan while the receiver is dwelling, and is done by keying in the handoff unit address from 1 to 34, then pressing H/OFF. The slave receiver tunes to the same status as the scanning receiver, the dwell will immediately end and the scan continues. For details on Master/Handoff operation, refer to the appropriate section of the operating manual.

The number keys, INCL, L/OUT, and DWL keys are enabled during scan so those parameters can be modified. If a band currently searching is locked out while executing, the search is completed but not re-entered for another sweep.

To halt the scan, either during a dwell or during a sweep, press the SCAN key. The CONTROL STATUS returns to EXEC with the most recent frequency step becoming the active tuned status.

Most keys are disabled during scan. An error message is displayed for most invalid key entries, and if OPR AID is pressed and held. The SYS CLR key can also be used to end the scan.

SECTION III

CIRCUIT DESCRIPTION

3.1 INTRODUCTION

This section describes the theory of operation of the receiver. A receiver simplified block diagram is provided to show overall functional partitioning of the receiver. Functional block diagrams are provided for each of the receiver's major sections to show functional signal flow through the receiver.

3.2 GENERAL DESCRIPTION

Figure 3-1 is a simplified block diagram of the receiver. The receiver is grouped into the following six major sections:

1. Frequency Extender (Option)
2. RF Tuner (A1)
3. 21.4 MHz IF Demodulator (A2)
4. Synthesizer Module (A3)
5. Digital Controller (A4)
6. Power Supply

3.2.1 FREQUENCY EXTENDER (OPTION)

A general discussion of the Frequency Extender functions and signal interfaces is provided in the following paragraphs.

3.2.1.1 Frequency Extender Functions

The Frequency Extender performs the following functions:

a. Down Conversion - The 500 to 1400 MHz RF input signals are converted to the 20 to 500 MHz range for processing by the RF Tuner.

b. RF Bypassing - The 20 to 512 MHz RF input signals are bypassed through the Frequency Extender and sent to the RF Tuner for processing.

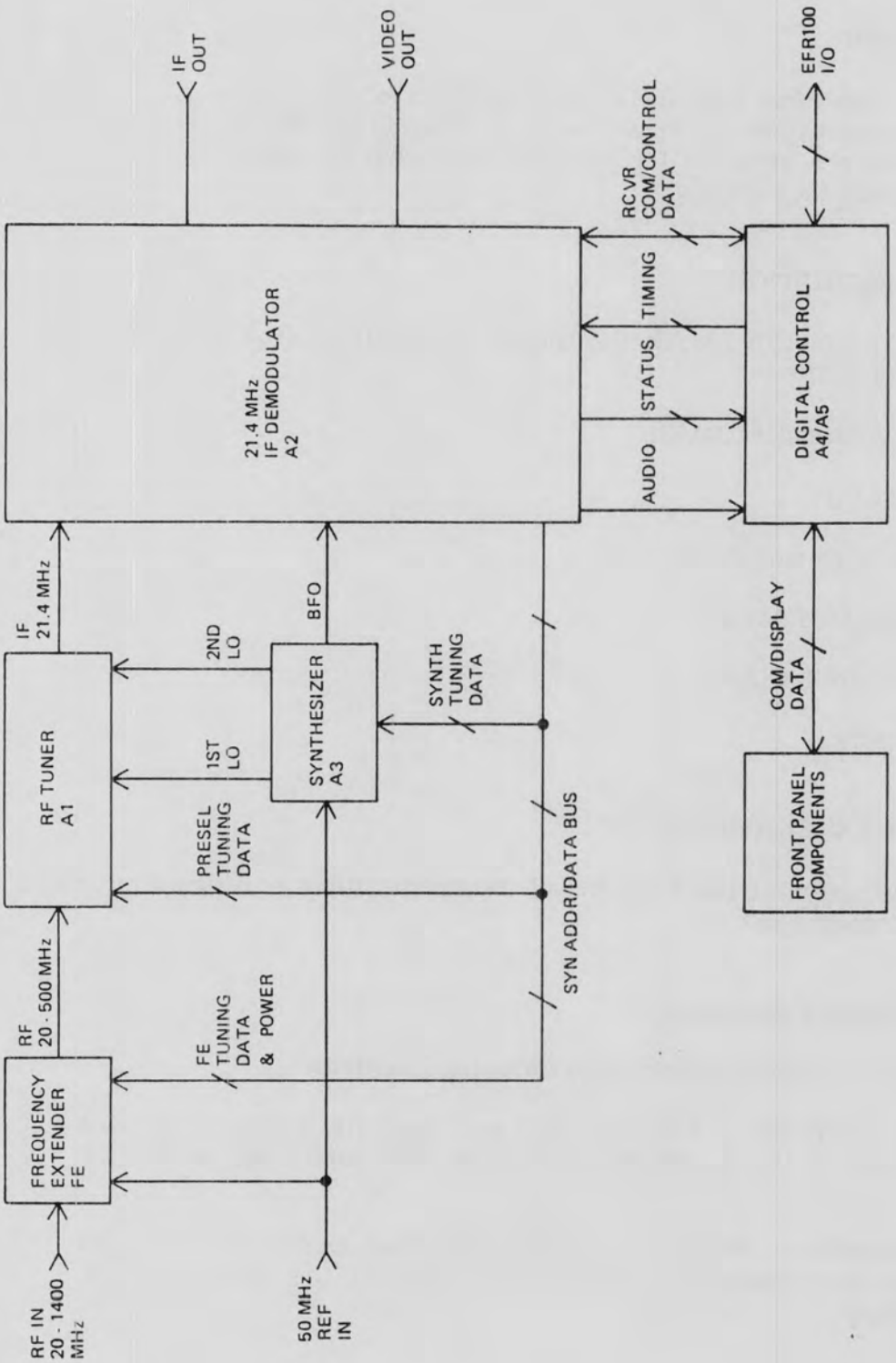


Figure 3-1. WJ-8628-4 VHF/UHF Receiver Block Diagram

3.2.1.2 **Frequency Extender Signal Interfaces**

The following input/output signals interface with the Frequency Extender:

a. RF Input - The 20 to 1400 MHz signals from an external source serve as the main signal input to the receiver. Input is 50 ohms impedance.

b. RF Output - The 20 to 500 MHz signals are sent to the RF Tuner for main receiver processing.

c. 50 MHz Ref. In - Rear panel connector, J2, provides the input for a highly stable 50 MHz reference signal. This signal is a sine wave at 0 dBm nominal into 50 ohms, and determines the effective tuning accuracy of the receiver.

d. FE Tuning Data - Three bits of SYN data and a strobe signal from the IF Demodulator are used to tune the RF and synthesizer circuits in the Frequency Extender.

3.2.2 **RF TUNER (A1)**

A general discussion of the RF Tuner functions and signal interfaces is provided in the following paragraphs.

3.2.2.1 **RF Tuner Functions**

The RF Tuner performs the following functions:

a. Preselection - The incoming 20-512 MHz spectrum is divided into four separate bands.

1. 20 to 59.999 MHz
2. 60 to 149.999 MHz
3. 150 to 274.999 MHz
4. 275 to 512 MHz

b. Frequency Translation - The selected portion of the incoming RF spectrum is translated to the 21.4 MHz 2nd IF by a double conversion process.

c. Bandlimiting - The bandwidth of the 21.4 MHz 2nd IF output is limited to 6 MHz.

3.2.2.2 **RF Tuner Signal Interfaces**

The following input/output signals interface with the RF Tuner:

a. RF Input - The 20 to 512 MHz RF signals, from an antenna or Frequency Extender Option, drive the input of the RF Tuner.

b. Tuning Data - Three bits of SYN data and a data strobe signal from the IF Demodulator are used to select the four preselector bands.

c. 1st LO - The Synthesizer sends the 1st LO signal to drive the 1st Mixer.

d. 2nd LO - The Synthesizer sends the 2nd LO signal to drive the 2nd Mixer.

e. IF Output - The 21.4 MHz IF output is provided as an input to the IF Demodulator section. This output is 50 ohms at 4 MHz and is nominally 15 dB above the RF input signal.

3.2.3 21.4 MHz IF DEMODULATOR (A2)

A general description of the 21.4 MHz IF Demodulator functions and signal interfaces is provided in the following paragraphs.

3.2.3.1 21.4 MHz IF Demodulator Functions

The 21.4 MHz IF Demodulator section performs the following functions:

a. Band Limiting - The 21.4 MHz IF signal is routed through one of four selectable bandpass filters. Available bandwidths are from SSB (2.85 kHz) to 4 MHz.

b. Signal Amplification - A combination of broadband and tuned high gain IF amplifier stages establish the overall gain of the receiver.

c. Gain Control - A series of AGC amplifiers adjust the overall receiver gain under conditions of varying input signal levels in the AGC mode. In the manual mode, the operator adjusts the gain with front panel controls.

d. Signal Demodulation - Three signal demodulators provide demodulated AM, FM, CW and SSB video outputs.

3.2.3.2 21.4 MHz IF Demodulator Signal Interfaces

The following input/output signals interface with the 21.4 MHz IF Demodulator:

a. IF Input - The RF Tuner sends the 21.4 MHz 2nd IF input signal. Signal bandwidth is 4 MHz and input impedance is 50 ohms.

b. BFO - The Synthesizer section sends the BFO signal, 21.4 MHz ± 4 kHz to operate the CW/SSB detector.

c. IF Out - A high level 21.4 MHz IF output is provided as a rear panel receiver output. This output is 50 ohms, bandlimited by the IF filter, and is nominally -13 dBm with a RF input signal equal to AGC threshold.

d. Video Out - A demodulated AM, FM or CW/SSB signal is provided as a rear panel receiver output. This output is 75 ohms and is nominally 1 Vpp or greater with an RF input signal level equal to the AGC threshold.

e. COM/CONTROL Data - Serial data, clock, strobe and enable lines are sent from the Digital Control section. These lines control the receiver operating parameters.

f. Status - The COS status, signal strength, AFC voltage, service request and polled audio signals are sent to the Digital Control (IOM108) for monitoring.

g. Audio - Low level audio is sent to the Digital Control for distribution to the front panel.

h. SYN Address/Data Bus - The 6-bit SYN bus is sent to the Synthesizer, RF Tuner and Frequency Extender to program the receiver operating frequency.

3.2.4 SYNTHESIZER MODULE (A3)

A general discussion of the Synthesizer functions and signal interfaces is provided in the following paragraphs.

3.2.4.1 Synthesizer Functions

The Synthesizer performs the following functions:

a. LO Signal Generation - The Synthesizer translates digital tuning data into the 1st, 2nd and BFO LO signals required for operation of the mixers in the RF Tuner and IF Demodulator sections.

b. External Reference Locking - Internal phase locked loops lock the accuracy of the three LO signals to an external frequency reference source.

3.2.4.2 Synthesizer Signal Interfaces

The following input/output signals interface with the Synthesizer section:

a. 50 MHz Ref. In - Rear panel connector, J2, provides the input for a highly stable 50 MHz reference signal. This signal is a sine wave at 0 dBm nominal into 50 ohms, and determines the effective tuning accuracy of the receiver.

b. Tuning Data - The IF Demodulator section sends a 6-bit word over the Synthesizer Address/Data Bus to program the output frequencies of the 1st, 2nd and BFO LO Synthesizers.

c. 1st LO - The 1st LO output is provided as an input to the RF Tuner. Frequency range is 346.6-638.6 MHz and level is +5±1 dBm.

d. 2nd LO - The 2nd LO output is provided as an input to the RF Tuner. Frequency range is 105.0-105.2/305.0-305.2 MHz and level is +5±1 dBm.

e. BFO - The BFO signal output is provided as an input to the IF Demodulator. Frequency range is 21.3960-21.4040 MHz and level is 100 mVrms minimum (high impedance 500Ω).

3.2.5 DIGITAL CONTROLLER (A4)

A general discussion of the Digital Control functions and signal interfaces is provided in the following paragraphs.

3.2.5.1 Digital Control Functions

The Digital Control section performs the following functions:

a. Receiver Control - The Digital Control generates the digital control words necessary to operate the signal processing sections of the receiver.

b. Front Panel Interface - Operator selected parameter inputs are from the front panel to the digital circuitry to generate receiver digital control words, store data in memory or perform special functions. Receiver status is also input and displayed on the display for monitoring purposes.

c. External Controller Interface - External controller commands are interfaced to the digital circuitry to generate receiver digital control words. The Digital Control section also sends receiver status words to the external controller. This would typically be an IOM108 connected through the backplane of an EFR100 Equipment Frame.

3.2.5.2 Digital Control Signal Interfaces

The following input/output signals interface with the Digital Control section:

a. Command/Control Data - Serial data, clock and enable lines are sent to the IF Demodulator to program all receiver operating parameters.

b. Status - DC voltages representing the status of COS, Signal Strength, AFC and selected IF Bandwidth are input to the Digital Control section for monitoring.

c. Audio - Low level audio is input from the IF Demodulator for distribution to the front panel.

d. Command/Display Data - Front panel select data is entered via the front panel to the Digital Control section to permit operator selection of the operating parameters. Also, display data is transferred from the Digital Control to the front panel for visual display.

e. EFR100 I/O - The EFR100 I/O permits an external control device to send parameter data to the receiver and also to receive status signals from the receiver.

3.2.6 POWER SUPPLY

The Power Supply section receives DC input voltages from either a bolt-on power supply unit (MPS Option) or from the EFR100 Equipment Frame and distributes the voltages to the receiver circuits. Module A4A1 regulates these voltages for the I/O control in the Digital Control section as shown below:

a. Input: +18 V, -18 V, +8 V (+20%, -0%)

b. Output: +12 V, -12 V, +5 V (+/- 10%)

3.3 RECEIVER FUNCTIONAL DESCRIPTION

3.3.1 FREQUENCY EXTENDER (OPTION)

Figure 3-2 is a block diagram of the Frequency Extender. As shown in **Figure 3-2,** the Frequency Extender consists of two major modules:

- 500-1400 MHz RF Assembly
- 800, 1000 MHz Synthesizer

3.3.1.1 500-1400 MHz RF Assembly

Refer to **Figure 3-3,** 500-1400 MHz RF Assembly Block Diagram. As shown in **Figure 3-3,** tuning data from the SYN Addr/Data Bus drives the bandswitch. The bandswitch decodes the tuning data and organizes the tuning of the 500-1400 MHz Assembly into five separate bands. These bands are summarized in **Table 3-1.**

Incoming RF signals are routed through the input switch. The input switch has five RF outputs corresponding to bands 1-5. If the receiver is tuned to the 20-500 MHz range, the band 5 command from the bandswitch directs the RF through the input switch, out the 20-500 MHz port and through the output switch to the 20-500 MHz output port. This effectively bypasses the 500-1400 MHz processing circuitry.

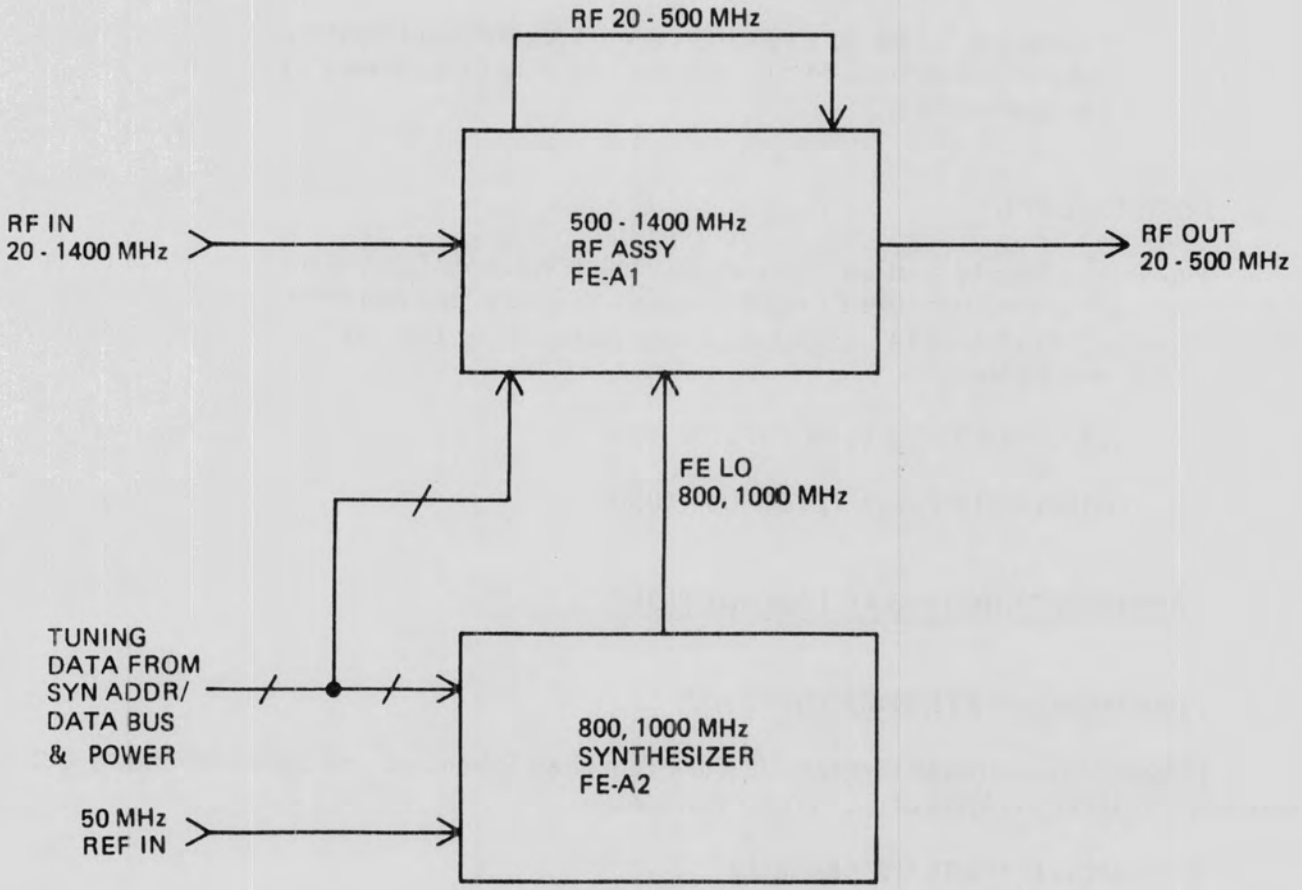


Figure 3-2. Frequency Extender Block Diagram

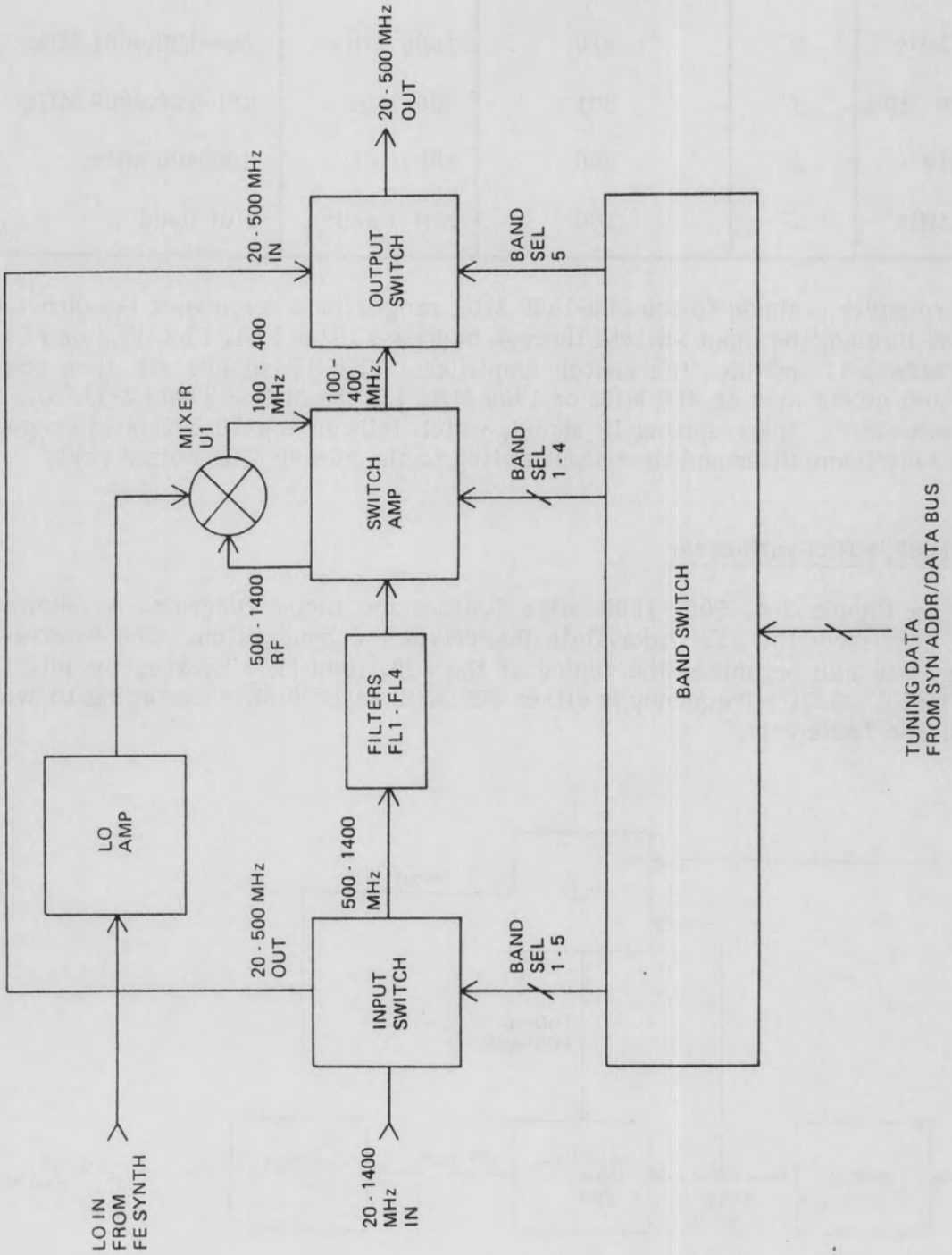


Figure 3-3. 500-1400 MHz RF Assembly Block Diagram

Table 3-1. Frequency Extender (FE) Bandswitching

Freq. Range	Band #	SYN Data Word	FE LO Freq.	FE IF Freq.
500-699.9999 MHz	1	011	800 MHz	300-100.0001 MHz
700-899.999 MHz	2	010	1000 MHz	300-100.0001 MHz
900-1099.9999 MHz	3	001	800 MHz	100-299.9999 MHz
1100-1400 MHz	4	000	1000 MHz	100-400 MHz
20-499.9999 MHz	5	100	Not Used	Not Used

If the receiver is tuned to the 500-1400 MHz range, band commands 1-4 direct the incoming RF signals through the input switch, through bandpass filter FL1, FL2, FL3 or FL4 as appropriate (see **Table 3-1**) and into the switch amplifier. The RF signals are then routed through mixer U1 and mixed with an 800 MHz or 1000 MHz LO signal (see **Table 3-1**) from the 800, 1000 MHz Synthesizer. The resulting IF signal, which falls in the 20-500 MHz range, is routed through the switch amplifier and the output switch to the 20-500 MHz output port.

3.3.1.2 800, 1000 MHz Synthesizer

Refer to **Figure 3-4**, 800, 1000 MHz Synthesizer Block Diagram. As shown in **Figure 3-4**, tuning data from the SYN Addr/Data Bus drives the bandswitch. The bandswitch decodes the tuning data and organizes the tuning of the 800, 1000 MHz Synthesizer into five separate bands. The FE LO OUT frequency is either 800 MHz or 1000 MHz according to which band is being tuned (see **Table 3-1**).

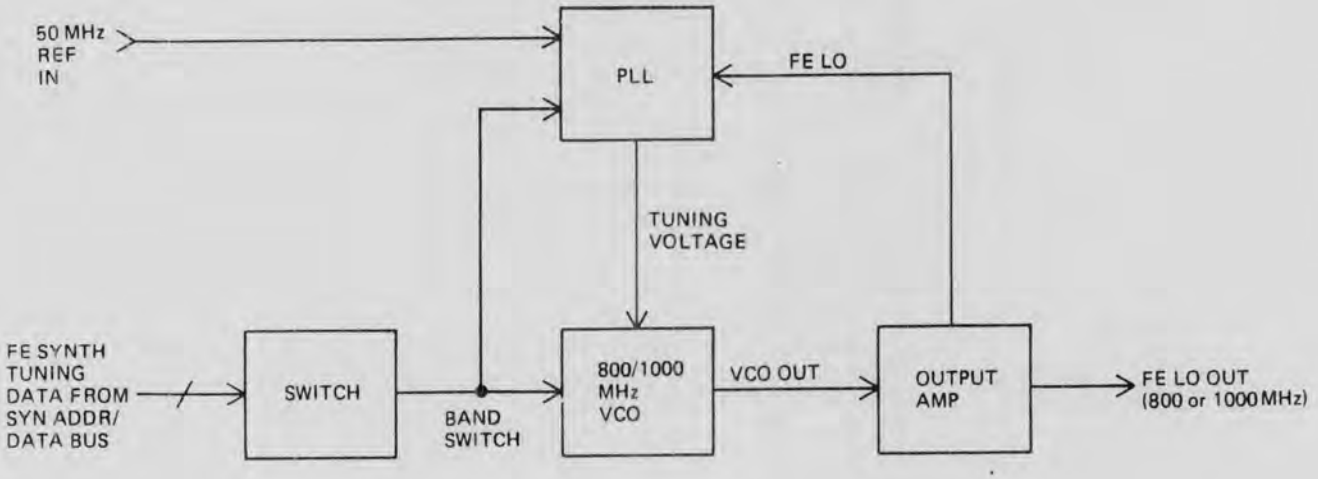


Figure 3-4. 800, 1000 MHz Synthesizer Block Diagram

The bandswitch output drives the 800/1000 MHz VCO and the PLL. The VCO is capable of oscillating at two frequencies: approximately 800 MHz and approximately 1000 MHz. The VCO output is amplified by the output amplifier to give the FE LO OUT signal. A sample of the VCO signal is fed to the PLL. An internal divider in the PLL, programmed by the bandswitch signal, compares the VCO sample with the 50 MHz reference signal from the rear. A correction tuning voltage is sent to the 800/1000 MHz VCO to force it to oscillate at exactly 800 or 1000 MHz as required (see **Table 3-1**).

3.3.2 RF TUNER (A1)

Figure 3-5 is a block diagram of the RF Tuner. As shown in **Figure 3-5**, the RF Tuner consists of five major modules:

- Input Preselector (A1A1)
- Dual RF Amplifier (A1A2)
- 1st IF Converter (A1A3)
- 2nd IF Converter (A1A4)
- Dual IF Filter (A1A6)

3.3.2.1 Input Preselector (A1A1)

Tuning data from the SYN Address/Data Bus drives the Input Preselector. A decoder decodes the tuning data and organizes the tuning of the preselector into a high band, 275-512 MHz, and a low band, 20-274.9999 MHz. The low band is additionally organized into three bands, 20-59.9999 MHz, 60-149.9999 MHz, and 150-274.9999 MHz. Incoming 20-512 MHz RF signals are routed through the Input Preselector. If the receiver is tuned to the 20-274.9999 MHz range, the RF is passed through the preselector to the lo-band output. If the receiver is tuned to the 275-512 MHz range, the RF is passed through the preselector to the hi-band output. The decoded hi-lo select signal is passed to the Dual RF Amplifier (A1A2) and the 1st IF Converter (A1A3) for band selection. The lo-band/hi-band RF output signals are sent to the Dual RF Amplifier (A1A2).

3.3.2.2 Dual RF Amplifier (A1A2)

The hi-lo select signal from the Input Preselector (A1A1) drives the Dual RF Amplifier. The select signal organizes the tuning of the amplifier into a lo-band, 20-275 MHz, and a hi-band, 275-512 MHz. If the receiver is tuned to the 20-275 MHz range, RF from the Input Preselector comes into the lo-band RF terminal and passes through the Dual RF Amplifier to the 20-512 MHz RF output terminal. If the receiver is tuned to the 275-512 MHz range, RF from the Input Preselector comes into the hi-band RF terminal and passes through the dual RF amplifier to an additional 275-512 MHz voltage tuned filter stage. From here it is switched to the RF output terminal. The 20-512 MHz output drives the input of the 1st IF Converter (A1A3).

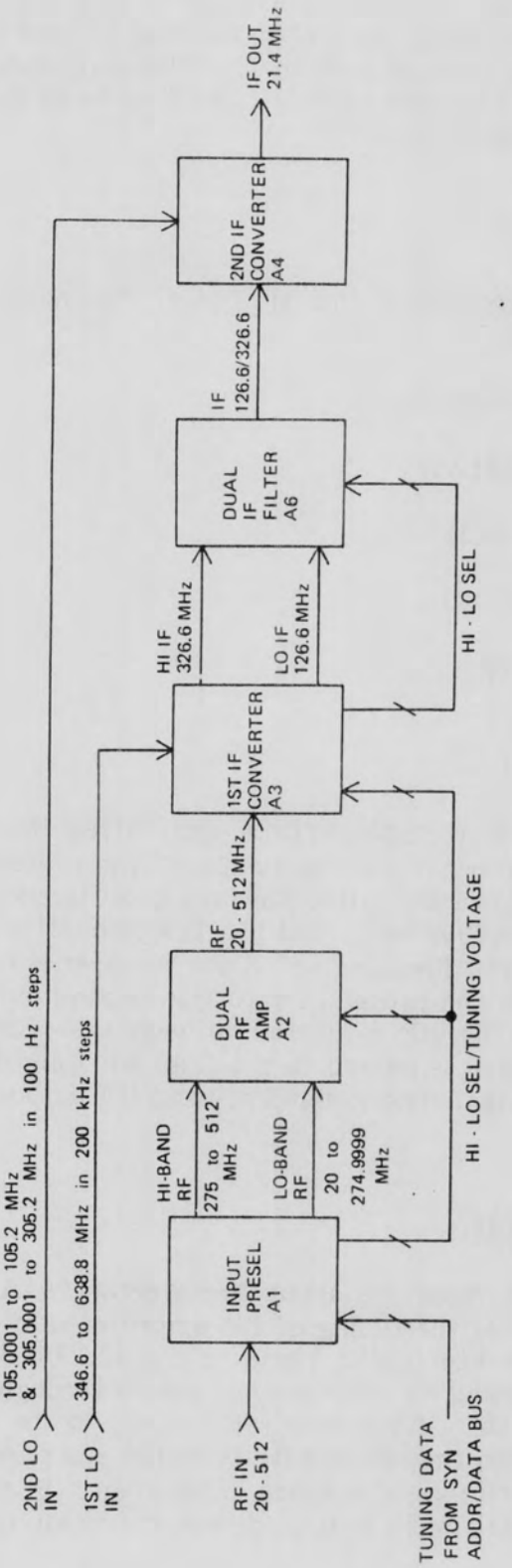


Figure 3-5. RF Tuner Block Diagram

3.3.2.3 1st IF Converter (A1A3)

The 20-512 MHz RF signal from the Dual RF Amplifier (A1A2) drives the input of the 1st IF Converter. The 1st IF Converter mixes the RF signal with the 1st LO signal to produce the 1st IF signal. When the receiver is tuning the low band frequency range (20-274.9999 MHz), the 1st LO frequency range is 346.6-601.4 MHz in 200 kHz steps and the resulting 1st IF frequency is 326.6 MHz to 326.401 MHz. When the receiver is tuning the high band frequency range (275-512 MHz), the 1st LO frequency range is 401.6-638.6 MHz and the resulting 1st IF frequency is 126.6 MHz to 126.401 MHz. The hi-lo select signal routes the lo-band IF, 326.6 MHz, out the low band output terminal and routes the hi-band IF, 126.6 MHz, out the high band output terminal to the Dual IF Filter (A1A6).

3.3.2.4 Dual IF Filter (A1A6)

The Dual IF Filter consists of two bandpass filters, one centered at 326.6 MHz and one centered at 126.6 MHz. When the receiver is tuning the low band frequency range (20-274.9999 MHz) the low band select signal energizes the low band input terminal. The 326.6 MHz 1st IF signal from the 1st IF Converter (A1A3) passes through the 326.6 MHz filter to the IF output terminal. When the receiver is tuning the high band frequency range (275-512 MHz), the high band select signal energizes the high band input terminal. The 126.6 MHz 1st IF signal from A1A3 passes through the 126.6 MHz filter to the IF output terminal. The IF output terminal drives the input of the 2nd IF Converter (A1A4).

3.3.2.5 2nd IF Converter (A1A4)

The 1st IF output from the Dual IF Filter (A1A6) drives the input to the 2nd IF Converter. The 1st IF signal is applied to the 2nd mixer. When the receiver is tuning the low band frequency range (20-274.9999 MHz), the mixer combines the 326.401 to 326.6 MHz 1st IF signal with a 305.0001 to 305.2 MHz (100 Hz steps) 2nd LO signal to produce the 21.4 MHz 2nd IF signal. When the receiver is tuning the high band frequency range (275-512 MHz), the mixer combines the 126.401 to 126.6 MHz 1st IF signal with a 105.0001 to 105.2 MHz (100 Hz steps) 2nd LO signal to produce the 21.4 MHz 2nd IF signal. The 21.4 MHz 2nd IF signal is sent to the IF Demodulator (A2).

3.3.3 21.4 MHz IF DEMODULATOR (A2)

Figure 3-6 is a block diagram of the 21.4 MHz IF Demodulator. As shown in **Figure 3-6**, the 21.4 MHz IF Demodulator consists of six major modules:

- 21.4 MHz Bandpass Amplifier (A2A1)
- AM/SSB/CW Demodulator (A2A2)
- Video/Audio/COS (A2A3)
- Digital Interface (A2A4)
- FM Demodulator Motherboard (A2A5)

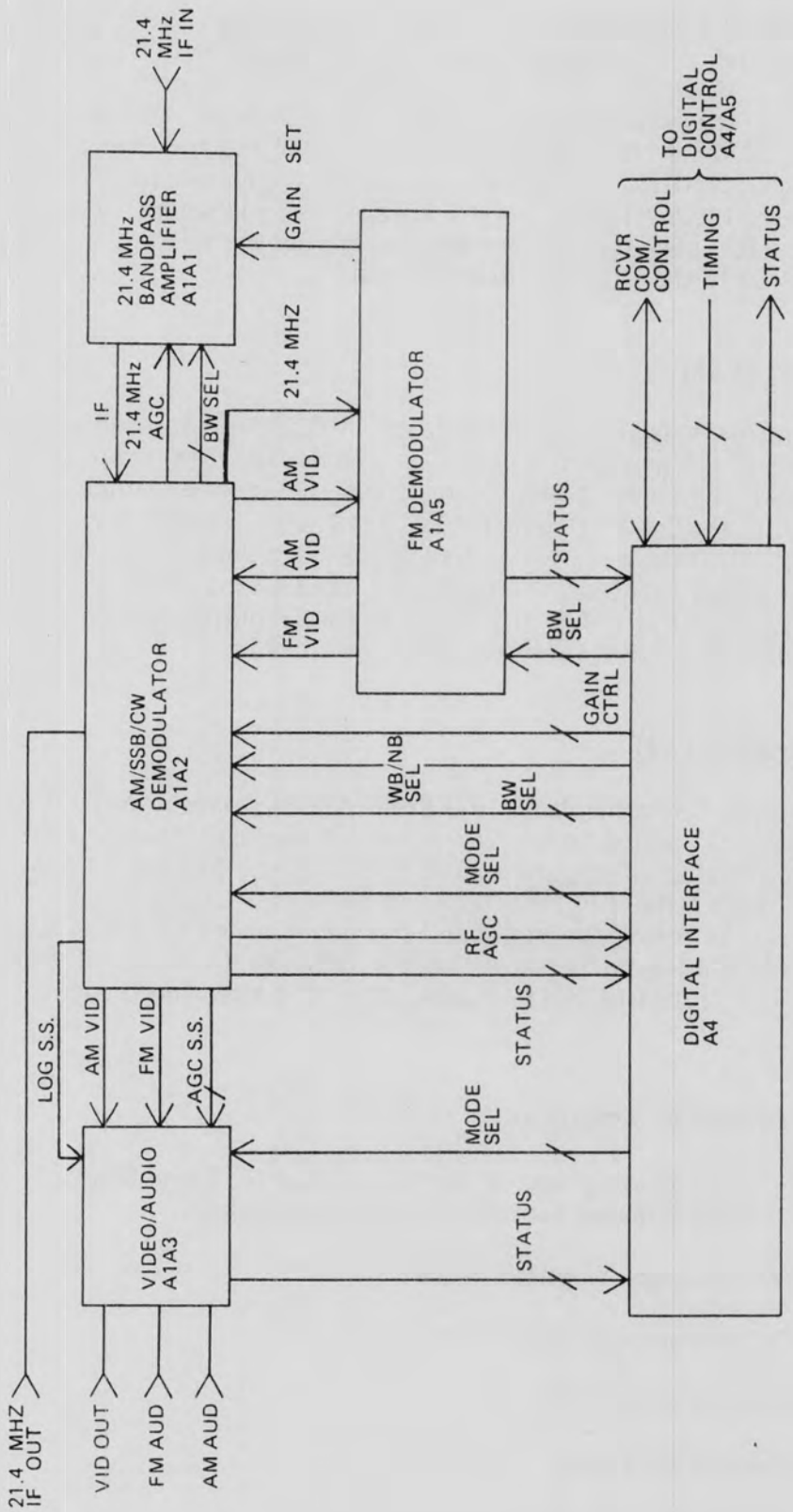


Figure 3-6. IF Demodulator Block Diagram

3.3.3.1 21.4 MHz Bandpass Amplifier (A2A1)

The 21.4 MHz IF signal from the RF Tuner (A1) is sent to the input of the 21.4 MHz Bandpass Amplifier. The signal is bandlimited by one of four IF bandpass filters selected by the BW SEL line from the AM/SSB/CW Demodulator (A2A2). The AGC voltage from A2A2 adjusts overall gain of the 21.4 MHz Bandpass Amplifier. The fixed gain set voltage from the FM Demodulator Motherboard (A2A5) adjusts the gain according to the bandwidth selected to provide a constant receiver gain-bandwidth product. The amplified bandlimited IF output drives the input to the AM/SSB/CW Demodulator (A2A2).

3.3.3.2 AM/SSB/CW Demodulator (A2A2)

The amplified bandlimited IF output from the 21.4 MHz Bandpass Amplifier (A2A1) drives the input of the AM/CW/SSB Demodulator. Mode, BW and AGC/MAN Select signals from the Digital Interface set the operating parameters of the demodulator. In AM and Pulse Modes, the IF signal is demodulated by an AM detector. The resulting AM video signal is routed through a video low pass filter on A2A5, then back through A2A2 to the Video/Audio/COS (A2A3). In CW/SSB modes, the IF signal is demodulated by a product detector driven by the BFO signal. The resulting video, also called AM video, is routed through a video low pass filter on A2A5, then back through A2A2 to the Video/Audio/COS (A2A3). In the FM mode, the 21.4 MHz IF signal is sent to A2A5 where it is demodulated by one of four FM detectors. The resulting FM video is routed through A2A2 to the Video/Audio/COS (A2A3). The A2A2 module requires an NB select line from the Digital Interface (A2A4) and switches in a double-tuned circuit for all BWs 200 kHz. The A2A2 module provides RF AGC to the RF Module via the Digital Interface (A2A4) and 40 pin interconnecting cable. The AM/CW/SSB Demodulator sends a BW Select line and an IF AGC line to the 21.4 MHz Bandpass Amplifier; and LOG Signal Strength and AGC Signal Strength to Video/Audio/COS (A2A3).

3.3.3.3 FM Demodulator Motherboard (A2A5)

The amplified bandlimited IF output signal from the AM/SSB/CW Demodulator (A2A2) drives the input of the FM Demodulator. The FM Demodulator consists of four separate FM demodulator modules, each corresponding to 1 of the 4 bandwidths available for the receiver. The BW Select signal from the Digital Interface (A2A4) selects 1 of the 4 demodulator modules according to which bandwidth has been selected for the receiver. The selected FM demodulator module demodulates the IF signal and sends the resulting video signal to A2A2. When the FM mode is selected, the FM video signal is routed through A2A2 to the Video/Audio/COS (A2A3).

Each FM demodulator module has a small resistor network which sends a small analog current to the 21.4 MHz Bandpass Amplifier (A2A1). This current, called the gain set current, has a specific value corresponding to the specific receiver bandwidth selected. The gain set current adjusts the gain of A2A1 according to the bandwidth to provide a constant receiver gain-bandwidth product.

3.3.3.4 Video/Audio/COS (A2A3)

The Video/Audio/COS consists of an AM video amplifier and an FM video amplifier. In the AM mode, the mode select line from the Digital Interface (A2A4) routes the AM video signal from the AM/SSB/CW Demodulator (A2A2) through the AM video amplifier to the video

output terminal. In the FM mode, the mode select line from the Digital Interface routes the FM video signal from the AM/SSB/CW Detector (A2A2) through the FM video amplifier to the video output terminal. AM and FM audio signals are separately and independently available in either the AM or FM mode.

The Video/Audio/COS also contains a signal strength processing circuit. LOG SS and AGC SS signals from A2A2 are processed to produce the signal strength voltage.

3.3.3.5 Digital Interface (A2A4)

The Digital Interface functions as the major interface point between the Digital Control (A4) and the receiver analog circuits. Receiver parameter data is transmitted from the Receiver/EF Interface (A4A5) as a 72-bit serial stream via the Receiver Command/Control line. This 72-bit serial stream completely defines all receiver operating parameters. The Digital Interface receives this parameter data and generates receiver operating commands. Gain control data is sent to the AM/SSB/CW Demodulator (A2A2), BW select data is sent to A2A2 and FM Demodulator Motherboard (A2A5), and mode select data is sent to A2A2 and the Video/Audio/COS (A2A3). Frequency tuning data is sent to the Frequency Extender and the Synthesizer via the SYN Address/Data Bus.

Status information from A2A2, A2A3 and A2A5 is read by the Digital Interface and sent back to A4A5 via the status line.

3.3.4 SYNTHESIZER MODULE (A3)

Figure 3-7 is a block diagram of the Synthesizer Module. As shown in **Figure 3-7**, the Synthesizer consists of nine major modules:

- Time Base (A3A2)
- 2nd LO VCO (A3A3)
- 2nd LO PLL (A3A4)
- AUX PLL/Phase Detector (A3A5)
- AUX VCO (A3A6)
- BFO Assembly (A3A7)
- Reference Mixer (A3A8)
- 1st LO Phase Detector/Divider (A3A9)
- 1st LO VCO (A3A10)

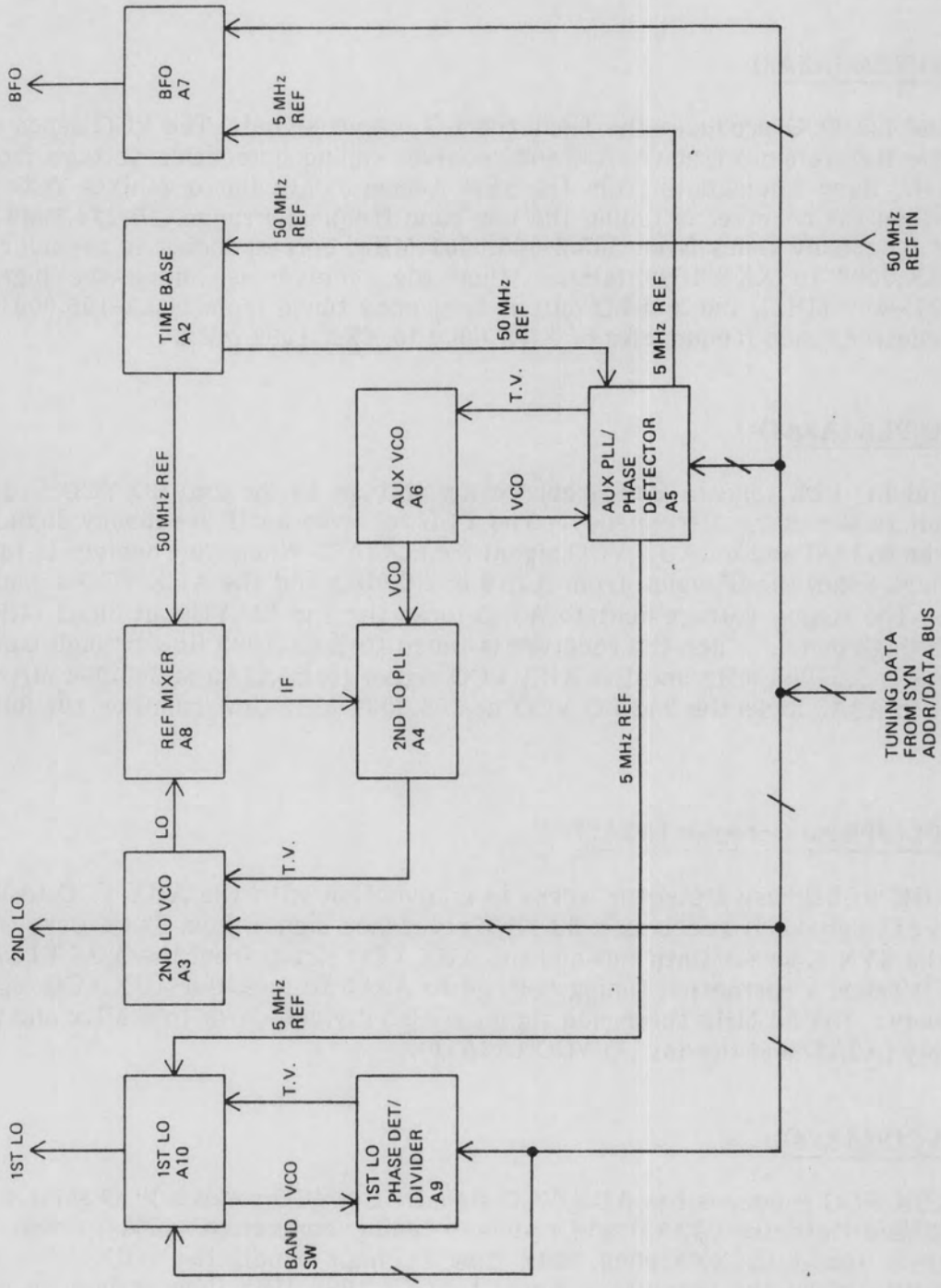


Figure 3-7. Synthesizer Block Diagram

3.3.4.1 Time Base (A3A2)

The Time Base is the heart of the Synthesizer section. The stable 50 MHz reference input from the rear panel is split and amplified by two buffer amplifiers to give two 50 MHz reference outputs. The two reference outputs drive the AUX PLL/Phase Detector (A3A5) and the Reference Mixer (A3A8).

3.3.4.2 2nd LO VCO (A3A3)

The 2nd LO VCO produces the final 2nd LO output signal. The VCO sends a VCO sample signal to the Reference Mixer (A3A8) and receives tuning correction voltage from the 2nd LO PLL (A3A4). Band select data from the SYN Address/Data Bus organizes VCO tuning into two ranges. When the receiver is tuning the low band frequency range (20-274.9999 MHz), the 2nd LO output frequency tunes from 305.2-305.0001 MHz, corresponding to receiver tuned frequencies of XXX.0000 to XXX.1999 MHz. When the receiver is tuning the high band frequency range (275-500 MHz), the 2nd LO output frequency tuned from 105.2-105.0001 MHz, corresponding to receiver tuned frequencies of XXX.0000 to XXX.1999 MHz.

3.3.4.3 2nd LO PLL (A3A4)

The 2nd LO PLL sends a tuning correction voltage to the 2nd LO VCO (A3A3) to lock the VCO output to the correct frequency. The PLL receives an IF frequency signal from the Reference Mixer (A3A8) and an AUX VCO signal from A3A6. When the receiver is tuned to XXX.0000 (low or high band) the IF signal from A3A8 is 2.6 MHz and the AUX VCO signal from A3A5 is 208 MHz. The tuning voltage sent to A3A3 locks the 2nd LO VCO at 305.2 MHz (low band) or 105.2 MHz (high band). When the receiver is tuned to XXX.1999 (low or high band) the IF signal from A3A8 is 2.50005 MHz and the AUX VCO signal from A3A5 is 200.004 MHz. The tuning voltage sent to A3A3 locks the 2nd LO VCO at 305.0001 MHz (low band) or 105.001 MHz (high band).

3.3.4.4 AUX PLL/Phase Detector (A3A5)

The AUX PLL/Phase Detector works in conjunction with the AUX VCO (A3A6) to produce the AUX VCO signal. It receives a 50 MHz reference signal from Time Base (A3A2), tuning data from the SYN Address/Data Bus and the AUX VCO signal from the AUX PLL/Phase Detector (A3A5). It sends a correction tuning voltage to A3A5 to lock the AUX VCO signal to the correct frequency. The 50 MHz reference signal is also divided down to 5 MHz and is sent to the BFO Assembly (A3A7) and the 1st LO VCO (A3A10).

3.3.4.5 AUX VCO (A3A6)

The AUX VCO produces the AUX VCO signal. The VCO sends a VCO sample signal to the AUX PLL/Phase Detector (A3A5) and receives tuning correction voltage from A3A5. When the receiver is tuned to XXX.0000 MHz (low or high band), the AUX VCO output frequency is 208 MHz. When the receiver is tuned to XXX.1999 MHz (low or high band), the AUX VCO output frequency is 200 MHz.

3.3.4.6 BFO Assembly (A3A7)

The BFO generates the 21.4 MHz BFO signal. The BFO receives the 5 MHz reference signal from the AUX PLL/Phase Detector (A3A5) and BFO offset tuning data from the SYN Address/Data Bus. When a BFO offset of -4.0 kHz is requested, the BFO output frequency is 21.3960 MHz. When a BFO offset of 0.0 is requested, the BFO output frequency is 21.4000 MHz. When a BFO offset of +4.0 kHz is requested, the BFO output frequency is 21.4040 MHz.

3.3.4.7 Reference Mixer (A3A8)

The Reference Mixer receives the 50 MHz reference signal from the Time Base (A3A2) and the LO sample signal from the 2nd LO VCO (A3A3) and produces the IF signal to drive 2nd LO PLL (A3A4). When the receiver is tuned to XXX.0000 MHz (low or high band), the LO signal from A3A3 is 305.2 MHz (low band) or 105.2 MHz (high band) and the IF signal is 2.6 MHz (low or high band). When the receiver is tuned to XXX.1999 MHz (low or high band), the LO signal from A3A3 is 305.0001 MHz (low band) or 105.0001 MHz (high band) and the IF signal is 2.50005 MHz (low or high band).

3.3.4.8 1st LO Phase Detector/Divider (A3A9)

The 1st LO Phase Detector/Divider works in conjunction with the 1st LO to produce the 1st LO signal. It receives 1st LO tuning data from the SYN Address/Data Bus and a 1st LO VCO sample signal from 1st LO VCO (A3A10). It sends a correction tuning voltage to A3A10 to lock the 1st LO VCO to the correct frequency.

3.3.4.9 1st LO (A3A10)

The 1st LO produces the final 1st LO output signal. The VCO sends a sample signal to 1st LO Phase Detector/Divider (A3A9) and receives tuning correction voltage from A3A9. Band select data from the SYN Address/Data Bus organizes VCO tuning into two ranges. When the receiver is tuning the low band frequency range (20-274.9999 MHz), the 1st LO output frequency tunes from 346.6 MHz to 601.4 MHz corresponding to receiver tuned frequencies of 20 MHz to 274.9999 MHz. When the receiver is tuning the high band frequency range (275-512 MHz) the 1st LO output frequency tunes from 401.6 MHz to 638.6 MHz corresponding to receiver tuned frequencies of 275.XXXX MHz to 512.XXXX MHz.

3.3.5 DIGITAL CONTROL (A4)

Figure 3-8 is a block diagram of the Digital Control. As shown in **Figure 3-8**, the Digital Control consists of four major modules:

- Optional I/O (A4A2)
- Extended CPU (A4A3)
- Receiver/EF Interface (A4A5)
- Front Panel Interface (A4A6)

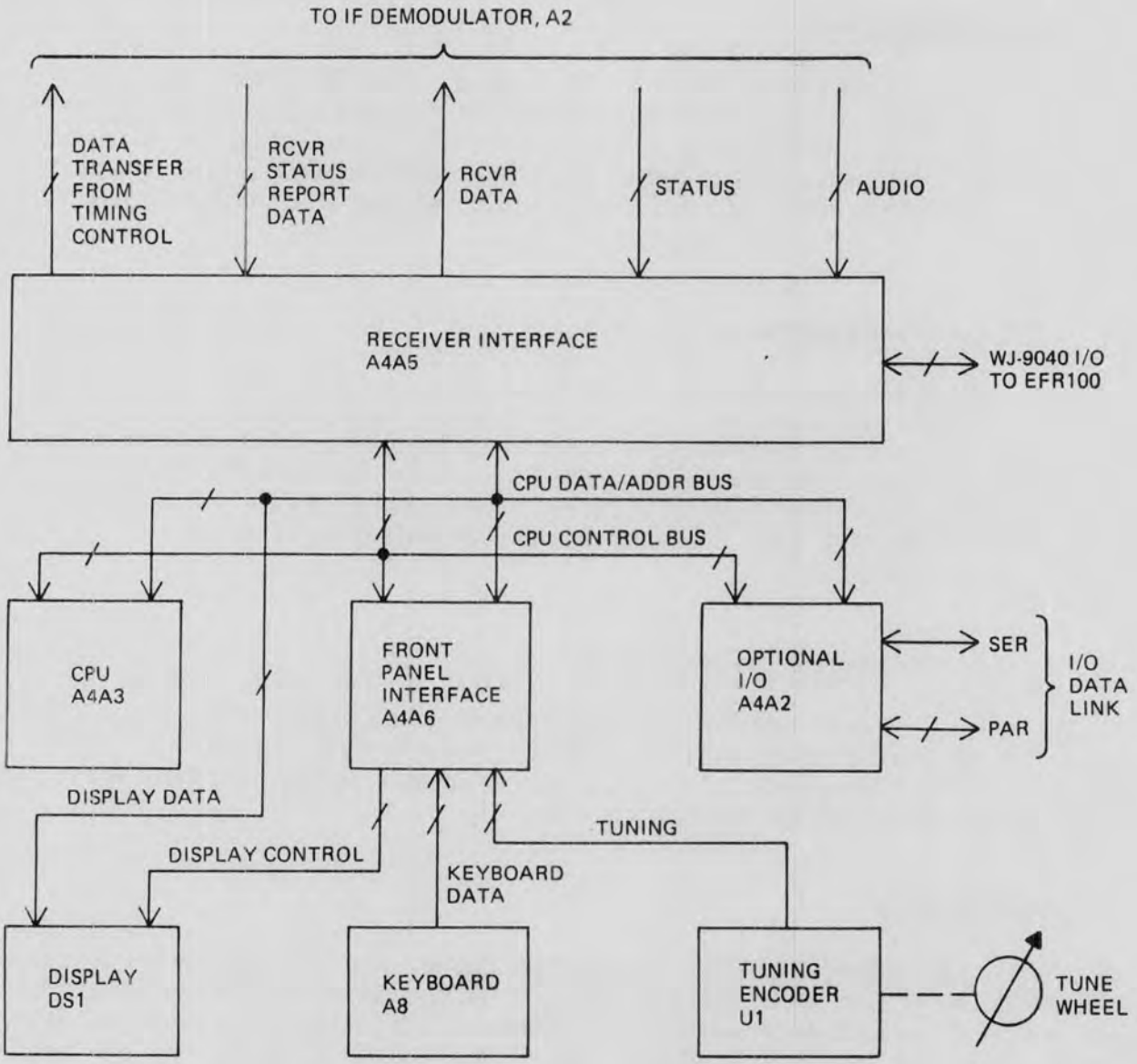


Figure 3-8. Digital Control Block Diagram

3.3.5.1 **Optional I/O (A4A2)**

The Digital I/O module provides serial (RS-232) data communication between an external computer terminal device and the IOM108 Data/Address Bus. The module consists of a UART to provide serial-parallel and parallel-serial conversion and timing logic to coordinate data transfer. The digital I/O interrupts the Extended CPU (A4A3) when the computer terminal transmits data and also transmits data to the terminal when directed to do so by the Extended CPU (A4A3).

3.3.5.2 Extended CPU (A4A3)

The Extended CPU is the main controlling element in the Digital Control section. It consists of a microprocessor controller, RAM for temporary storage of data and commands, and ROM which contains system operating software and I/O timing to coordinate data movement. The Extended CPU is tied to the Receiver/EF Interface (A4A5), Front Panel Interface (A4A6) and Optional I/O (A4A2) via an 8-bit data bus and a control/timing bus.

In the local mode, operator input parameters are transferred from the Front Panel Interface (A4A6) to the Extended CPU. The Extended CPU processes these inputs and generates the 80-bit receiver parameter data word which is sent to the Receiver/EF Interface (A4A5) and then to the Digital Interface.

In the External Control mode, the receiver parameter data from the External Controller is transferred from the Receiver/EF Interface (A4A5) to the Extended CPU (A4A3). The Extended CPU (A4A3) processes this data and generates the 80-bit receiver parameter data which is sent to the Receiver/EF Interface and then to the Digital Interface. Additionally, the Extended CPU system software is designed to recognize and process special commands sent from the External Controller.

3.3.5.3 Receiver/EF Interface (A4A5)

The Receiver/EF Interface consists of a serial to parallel converter, a parallel to serial converter, status reporting logic and timing/control circuitry. It is tied directly to a common 8-bit CPU Data/Address Bus which coordinates A4A2, A4A3, A4A5 and A4A6. The Receiver/EF Interface functions as the major interface point between the Front Panel, External Controller (if connected) and the Digital Interface.

The Receiver/EF Interface communicates directly with the Digital Interface via two serial data streams: Receiver Data and Receiver Report. On power up, the Report provides the controller section with IF BW codes. During operation it is used to inform the Controller of certain status changes in the receiver, including synthesizer UNLOCK and SCAN hit reporting. When a change in receiver status is required, operator selected parameters are inputted to the Receiver/EF Interface via the CPU Data/Address Bus. This is an 8-bit bus (AD0-AD7). Receiver parameter data is transmitted from the Receiver/EF Interface (A4A5) as an 80-bit serial data stream. This 80-bit word completely defines all receiver operating parameters. **Table 3-2** shows the configuration of this word. As shown, the 80-bit stream is organized into ten 8-bit words. The transfer of the serial data stream into the Digital Interface is coordinated by data transfer timing/control signals. These signals consist of three lines: data, clock, and enable. Each 8-bit word is run into a serial to parallel converter and is received by the Extended CPU (A4A3) on the Digital Interface. When all ten words have been transferred, the enable goes low indicating the end of the message. The Extended CPU on the Digital Interface now decodes and converts the data, which is presented to the receiver analog section as tuning and select data.

When operated by an External Controller (typically an IOM108) the Receiver Interface connects to the External Controller using the same serial-to-parallel and parallel-to-serial techniques. As shown in **Figure 3-9**, these lines consist of EF CMD/CONT DATA IN, EF REPORT DATA OUT and timing/control lines (CLOCK, ENABLE).

Table 3-2. 72-Bit Receiver Parameter Data Word

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BYTE 1: COMMAND	(1	1	1	1)	(0	0	0	0)
BYTE 2: SIGN	(10 HZ BFO OPTION)				((SIGN)	*	*	*)
BYTE 3: OFFSET	(1 kHz BFO DIGIT)				(100 Hz BFO DIGIT)			
BYTE 4: FREQ 1	(1 kHz FREQ DIGIT)				(100 Hz FREQ DIGIT)			
BYTE 5: FREQ 2	(100 kHz FREQ DIGIT)				(10 kHz FREQ DIGIT)			
BYTE 6: FREQ 3	(10 MHz FREQ DIGIT)				(1 MHz FREQ DIGIT)			
BYTE 7: FREQ 4	(100 MHz FREQ DIGIT)				(100 MHz FREQ DIGIT)			
BYTE 8: COS	(AFC) (DUMP) (COS THRESHOLD LEVEL)							
BYTE 9: GAIN	(AGC) (MANUAL GAIN CONTROL LEVEL)							
BYTE 10: BW/DET	(IF BW CODE)				*	*	(DET MODE CODE)	

*Indicates bits not used.

The CMD/CONT DATA IN line is a serial data line. The External Controller uses this line to transfer receiver parameter data and communication commands to the Receiver Interface. Data on this line is routed through a serial to parallel converter and then is transferred to the Extended CPU (A4A3) via the Extended CPU Data/Address Bus. If the data is parameter data, the Extended CPU uses the data to generate ten 8-bit parameter commands. These are routed back through the Receiver/EF Interface parallel to serial converter and to the Digital Interface as a 80-bit serial data stream, RCVR DATA. If the data is a communication command, the Extended CPU processes it accordingly and reports back to the External Controller through the Receiver Interface parallel to serial converter via the REPORT DATA OUT LINE.

The REPORT DATA OUT LINE is also used to report a unique serial data word called the configurator. This is a word generated by software that defines the receiver type, tuning range, bandwidth and options present.

The TIMING/CONTROL lines are generated by the external controller and are used to coordinate the transfer of CMD/CONT and REPORT DATA between the Receiver/EF Interface and the External Controller.

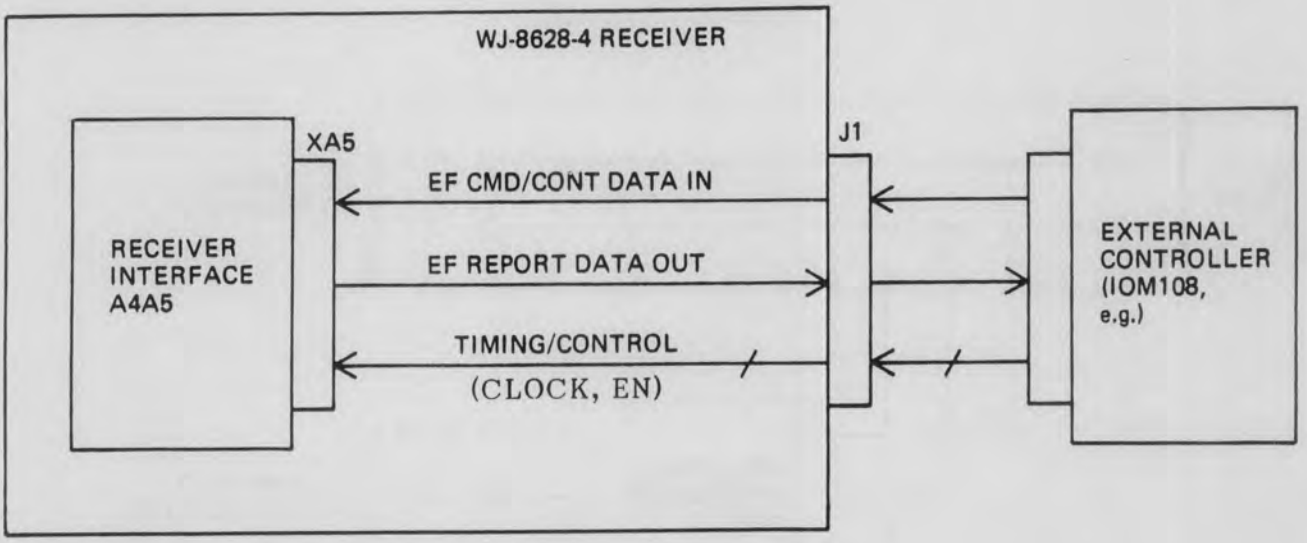


Figure 3-9. External Controller Interface

3.3.5.4 **Front Panel Interface (A4A6)**

The Front Panel Interface is the main interconnection between the front panel switches and indicators and the Extended CPU (A4A3). In normal operation, the Front Panel Interface routine scans the status of the keyboard and tuning encoder and also updates the Front Panel Display.

The front panel keyboard is organized as a row/column matrix. Four row and eight column lines are sent to the keyboard encoder on the Front Panel Interface. The row and column data is encoded into an 8-bit word and sent to the Extended CPU. This informs the Extended CPU of the specific keypad switches that have been depressed.

The tuning encoder outputs two lines which represent direction and speed of turning of the tune wheel. These two lines are selectively strobed through data buffers on the Front Panel Interface and placed on the Extended CPU Data Bus. This informs the Extended CPU of changes in the tune wheel.

The Extended CPU contains a record of current front panel status. This status is periodically read to the LCD for display purposes. The display data is transferred directly to the LCD from the Extended CPU Data/Address Bus. The transfer of display data is coordinated by the display control bus from the Front Panel Interface.

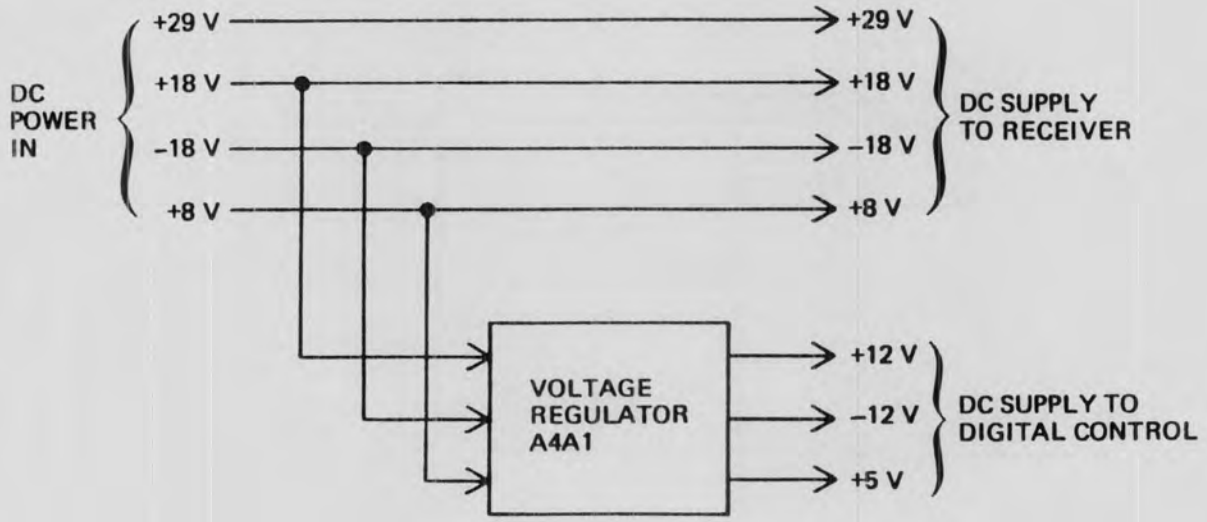


Figure 3-10. Power Supply Block Diagram

3.3.6 **POWER SUPPLY**

Figure 3-10 is a block diagram of the Power Supply. As shown in **Figure 3-10**, the power supply consists of one module, the Voltage Regulator (A4A1).

3.3.6.1 **Voltage Regulator (A4A1)**

The Voltage Regulator is part of the Controller Motherboard (A4) and provides separately regulated power for the digital control circuits. The module consists of three fixed voltage regulator modules. The +18 V input to A4A1 is dropped to a fixed regulated output of +12 V. The -18 V input to A4A1 is dropped to a fixed regulated output of -12 V. The +8 V input to A4A1 is dropped to a fixed regulated output of +5 V.

3.4 DETAILED CIRCUIT DESCRIPTION

3.4.1 RF TUNER (A1)

The following paragraphs describe the circuit operation of the RF Tuner Modules.

3.4.1.1 Input Preselector (A1A1)

Refer to **Figure 3-11**, Input Preselector (A1A1) Block Diagram, and **(Figure 6-2)**, Preselector Schematic Diagram, as aids in understanding the following description. As shown in **(Figure 3-11)**, the Input Preselector consists of the following major circuit areas:

- Pre-Select Band Decoder (U1)
- Input Switch
- Bandpass Filters (FL1-FL4)
- Output Switch

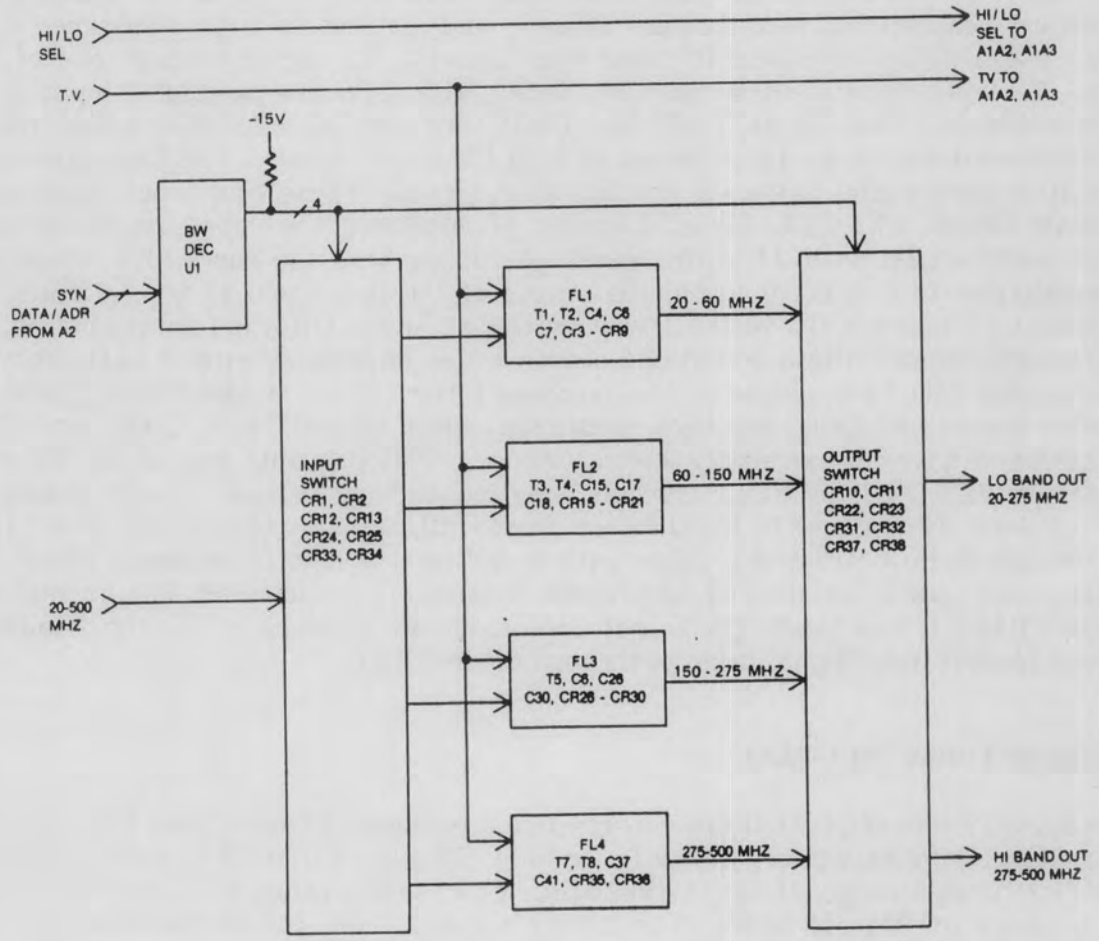


Figure 3-11. Input Preselector (A1A1) Block Diagram

3.4.1.1.1 Pre-Select Band Decoder (U1)

The Bandwidth Decoder (U1) is a 2-bit binary to 4-line decimal decoder. The binary input drives U1 input pins 9 and 10. There are 2 separate 4-line decimal outputs, X0-X3 and Y0-Y3. These 2 sets of outputs are in parallel. Output X0 is paralleled with Y0, X1 is paralleled with Y1, and so on. Each of the 4 outputs of U1 are connected to a -15 volt DC supply through a 4.7 K pull-up resistor. Each output, when selected, is at +7.5 volts DC. Each output, when not selected, is at -15 volts DC. The 2-bit binary input to U1 is driven by the Pre-Select from the IF Demodulator (A2). When the input to U1, pins 9 and 10 is equal to 00, U1 pins 1 and 12 are at +7.5 volts DC. The remaining output pins are at -15 volts DC. When the input to U1, pins 10 and 9, is equal to 10, then U1, pins 5 and 14 are at +7.5 volts DC. When the inputs at pins 9 and 10 is equal to 01, pins 2 and 15 are at +7.5 volts DC. When the inputs at pins 10 and 9 are equal to 11, pins 4 and 11 are at +7.5 volts DC. The decimal outputs from pre-select band decoder U1 provide forward bias to diodes CR1, CR12, CR24, and CR33 in the input switch, and to diodes CR11, CR23, CR33, and CR38 in the output switch.

3.4.1.1.2 Input Switch

The Input Switch consists of 4 separate diode-controlled RF switches. These diodes exhibit low forward resistance when forward biased, and extremely high resistance when reverse biased. These diodes are used to route the incoming RF signal through one of four bandpass filters. RF input signals in the range of 20-500 MHz drive the paralleled input of the four input diode switches. Two diodes, CR39 and CR40, are parallel connected across the RF input to provide overload protection in the event of high RF input signals. The four input diode switches define four input signal paths for the RF input signal. These four input signal paths drive four bandpass filters, FL1-FL4. As an example of analyzing the operation of the input switching diodes, input signal path #1 is discussed. Assuming that the bandwidth select code from the IF Demodulator (A2) is equal to 00, the output of U1 pins 1 and 12 is +7.5 volts, and the remaining output pins equals -15 volts. Diode switch #1, diode CR1, is forward biased, and diode CR2 is reversed biased. These conditions create a low impedance circuit path from the RF input through diode CR1 to the input of the Bandpass Filter (FL1). Diodes CR12, CR24, and CR33 are reversed biased and thus have high resistance, while diodes CR13, CR25, and CR34 are forward biased and have an extremely low resistance. This prevents any of the RF input signal from reaching FL2, FL3, or FL4. Overall isolation exceeds 70 dB. If the bandwidth select code from FROM A2 is equal to 10, then the Bandwidth Decoder (U1) would select input signal path #2 through diode CR12 and a signal path would be provided to bandpass filter FL2. If the bandwidth select code is equal to 01, bandwidth decoder U1 would select input signal path #3 through diode CR24. If the bandwidth select code from A2 is equal to 11, the Bandwidth Decoder (U1) would select input signal path #4 through diode CR33.

3.4.1.1.3 Bandpass Filters (FL1-FL4)

Bandpass Filters (FL1-FL4) are voltage-tuned bandpass filters. Each filter is tuned by means of varactor tuning capacitors in the filter tune circuits. Filter FL1 tunes a range of 20-59.999 MHz FL2 tunes a range of 60-149.999 MHz, FL3 tunes a range of 150-274.999 MHz, and FL4 tunes a range of 275-512 MHz. The tuning voltage from the IF Demodulator (A2) drives all 4 of the bandpass filters simultaneously. Therefore, all filters are tuned at the same time. However, because of the action of the input switch and the bandwidth decoder, the RF signal is only routed through 1 of the 4 bandpass filters at any one time. Filter FL1 consists of 2 tuned circuits comprised of transformer T1, diodes CR4 and CR5, and transformer T2, with diodes CR8 and CR9. The resonant frequency of these tuned circuits is varied by the tuning

voltage. Diodes CR3, CR6, and CR7 are coupling capacitors between the 2 tuned circuits, which provide for the proper bandpass characteristic. The actual capacitance of diode CR6 is adjusted by the tuning voltage to provide the same percentage of bandwidth over the tuning range of the filter. Filter FL2 consists of 2 tuned circuits, T3, and diodes CR14, CR15, and T4, with diodes CR20, CR21. Diodes CR16, CR17, CR18, and CR19 are coupling capacitors which operate in the same manner as the coupling capacitors in filter #1. Filter FL3 consists of 2 tuned circuits, T5, and diode CR26, T6, and diode CR30. CR26, CR28, and CR29 are coupling capacitors. Filter FL4 consists of 2 tuned circuits, T7, CR35, and T8, CR36. L21 is provided as a coupling element between the 2 tuned circuits. L21 is fixed and is, therefore, not adjusted or varied by the tuning voltage over the tuning range of the filter. Filters FL1-FL4 drive the input terminals of the output switch.

3.4.1.1.4 Output Switch

The Output Switch consists of 4 separate PIN diode swithces. These diodes exhibit low forward resistance when forward biased and extremely high resistance when reverse biased. The diodes are used to route the RF signals from the Bandpass Filters (FL1-FL4) to either the low band output or the high band output. Output diode switches 1, 2, and 3 are connected in parallel to provide the low band RF output. Diode switch #4 goes directly to the high band RF output. As an example in analyzing the operation of the diodes, signal path #1 is discussed. Assuming that the bandwidth select code from A2 is equal to 00, the output of U1, pins 1 and 12, is +7.5 volts; and the remaining output pins is -15 volts. Diode switch #1, diode CR11 is forward biased, and CR10 is reverse biased. These conditions create a low impedance circuit path from filter FL1 through diode CR11, to the low band output terminal. Diodes CR23, CR32, and CR38 are reverse biased, while diodes CR22, CR31, and CR37 are forward biased. This prevents the FL2, FL3, or FL4 filter outputs from reaching either the low band or the high band output terminals. If the bandwidth select code from A2 is equal to 01, CR23 is forward biased, CR22 is reverse biased, and a low impedance path is provided from filter FL2 to the low band RF output. If the bandwidth code from A2 is equal to 10, diode CR32 is forward biased, CR31 is reverse biased, and a low impedance signal path is provided from filter FL3 to the low band RF output. If the bandwidth select code from A2 is qual to 11, diode CR38 is forward biased, CR37 is reverse biased, and a low impedance signal path is provided from filter FL4 to the high band RF output terminal.

3.4.1.2 Dual RF Amplifier (A1A2)

Refer to **Figure 3-12**, Dual RF Amplifier (A1A2) Block Diagram, and **Figure 6-3**, Dual RF Amplifier Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-12**, the Dual RF Amplifier consisists of the following major circuit areas:

- Low Band Buffer Filter
- High Band Buffer Filter
- High/Low Select Switches (U3 and U4)
- Output Switch

3.4.1.2.1 Low Band Buffer Filter

Low band RF signals in the frequency range of 20-274.999 MHz from the RF Tuner (A1) drive the input to the Buffer Amplifier (U1). If the receiver is tuning a frequency between 20

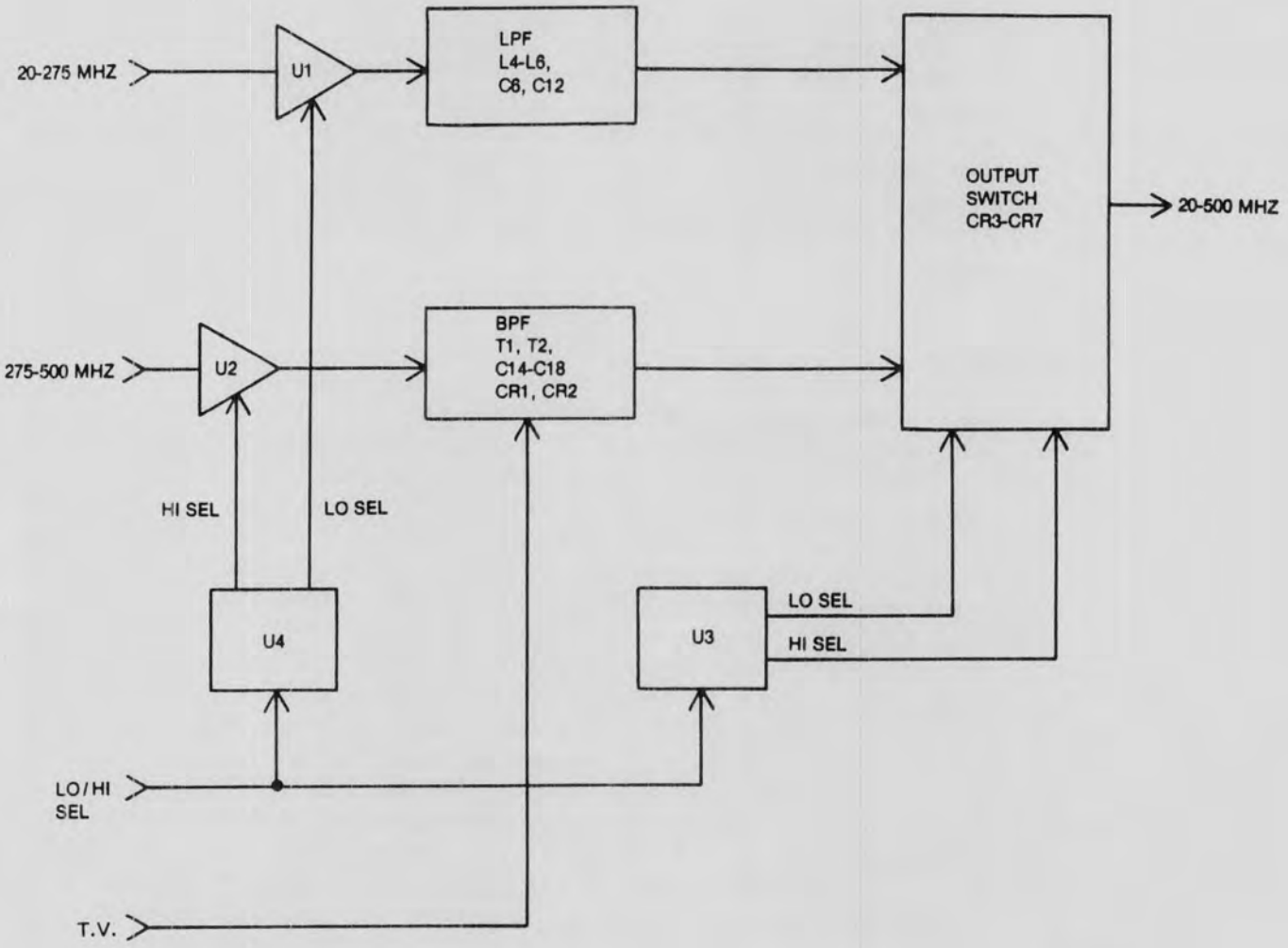


Figure 3-12. Dual RF Amplifier (A1A2) Block Diagram

and 275 MHz, U1 is energized by switch U4. The low band RF signals are amplified by U1 at a voltage gain of approximately 20 dB. These signals are then filtered by elliptical lowpass filters L4, L5, L6, and C6-C12. The signals then are passed to the output switch.

3.4.1.2.2 High Band Buffer Filter

High band RF signals in the frequency range of 275-512 MHz drive the input of the Buffer Amplifier (U2). If the receiver is tuning in the 275-512 MHz range, buffer U2 is energized by switch U4. The high band RF signals are amplified by U2 with an overall voltage

gain of approximately 20 dB. The amplified high band RF signals then drive the input of the bandpass filter. The bandpass filter is voltage tuned by means of varactor diodes driven by tuning voltage from the IF Demodulator (A2). The bandpass filter consists of 2 tuned circuits; T1 and diodes CR1, and T2 and diodes CR2. Inductor (L9) provides coupling between the 2 tuned circuits. The output of the bandpass filter drives the output switch.

3.4.1.2.3 High/Low Select Switches (U3 and U4)

CMOS switches U3 and U4, are wired to function as double-pole, double-throw switches. The position of each switch is determined by the high/low band select signal from the Input Preselector (A1). When the high/low band select signal is at 0 volts DC, U4 pin 2 is connected to pin 3 and U4 pin 12 is connected to pin 13. This sends +15 volts DC to the buffer Amplifier (U1). At the same time, U3 pin 2 is connected to pin 3, and U3 pin 13 is connected to pin 12. This sends -15 volts DC to the low band section of the output switch, and +15 volts DC to the high band section of the output switch. When the high/low band select signal is at +5 volts DC, U4 pin 4 is connected to pin 5, and U4 pin 11 is connected to pin 10. This sends +15 volts DC to U2. At the same time, U3 pin 5 is connected to pin 4, and U3 pin 10 is connected to pin 11. This action sends +15 volts to the low band output switch section and -15 volts DC to the high band section of the output switch.

3.4.1.2.4. Output Switch

The Output Switch consists of two separate diode switches. The #1 diode switches; CR3, CR4, and CR5 connect to the low band RF signal path from buffer U1. The high band output switches; CR6, CR7, and CR8 connect to the high band signal path from buffer U2. When the high/low band select signal is at 0 volts DC, U3 sends -15 volts DC to the low band section of the output switch, diodes CR3 and CR4 are forward biased, and diode CR5 is reverse biased. This creates a low impedance circuit path from U1 through the lowpass filter to the 20-500 MHz RF output terminal. When the high/low band select signal is +5 volts DC, U3 sends -15 volts DC to the high band section of the output switch. Diodes CR6 and CR7 are forward biased and diode CR8 is reverse biased. This creates a low impedance circuit path from buffer U2 through the bandpass filter to the 20-500 MHz RF ouput terminal.

3.4.1.3 1st IF Converter (A1A3)

Refer to **Figure 3-13** 1st IF Converter (A1A3) Block Diagram, and **Figure 6-4**, 1st IF Converter Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-13**, the 1st IF Converter consists of the following major circuit areas:

- Input Amplification
- Mixer (J3)
- High/Low Select Switch (U7)
- Output Switch

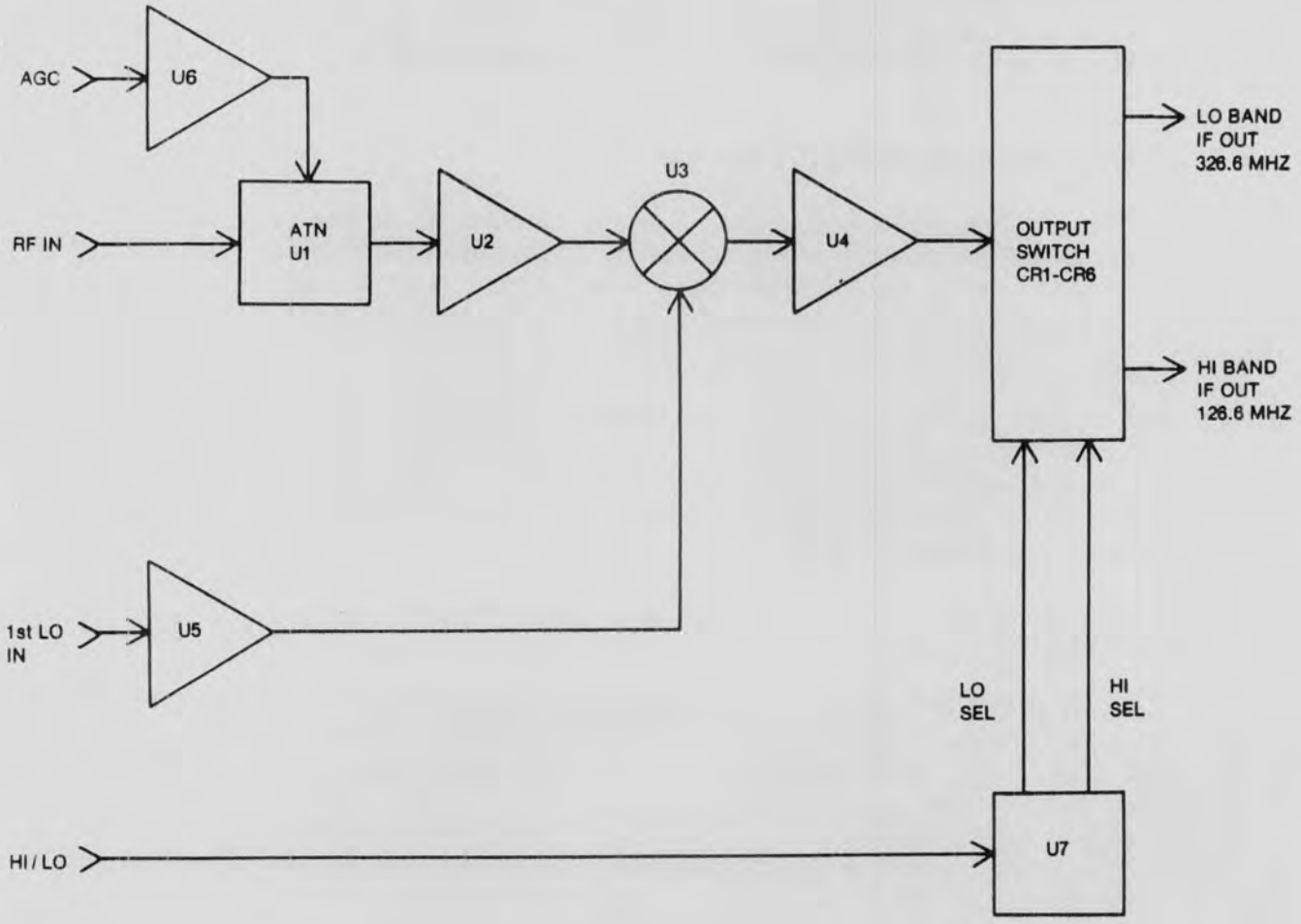


Figure 3-13. 1st IF Converter (A1A3) Block Diagram

3.4.1.3.1 Input Amplification

RF input signals in the range of 20-512 MHz from the dual RF amplifier (A2) are applied to pin 4 of U1, a voltage-controlled attenuator. The attenuation of U1 is controlled by the AGC voltage from the IF Demodulator (A2). The AGC voltage is processed by AGC amplifiers U6B and U6A. The output of U6A, pin 1, drives the U1 control input pin 5. U1 attenuation ranges from -2 dB for a +13 volt input to pin 5 to -32 dB for a +3 volt DC input to pin 5. The output of U1, pin 2, drives the input of U2, pin 2. U2 is a broadband, thin film, hybrid amplifier providing an overall voltage gain of approximately 12 dB. The output of U2, pin 4, drives the Mixer (U3).

3.4.1.3.2 Mixer (U3)

The Mixer (U3) is a double-balanced mixer with an overall conversion loss of approximately 6 dB. U3 combines the RF input signals of 20-512 MHz with the 1st LO signal from the Synthesizer (A3). The output of U3 is the 1st IF signal. The 1st LO signal from the Synthesizer (A3) covers two separate ranges. If the receiver is tuning in the low band 20-275 MHz, the 1st LO signal covers a range of 346.6-601.6 MHz. If the receiver is tuning the high band range 275-512 MHz, the 1st LO from the Synthesizer (A3) covers the frequency range from 366.6-638.8 MHz. The 1st LO signal is amplified by broadband Buffer Amplifier (U5) with an overall voltage gain of 12 dB and drives the local oscillator input of Mixer (U3). The first IF output of U3 is in two distinct ranges. If the receiver is tuning in the low band range of 20-275 MHz, the first IF output from U3 is 326.6 MHz. If the receiver is tuning the high band range of 275-500 MHz, the first IF output of U3 is 126.6 MHz. The IF output of U3 is amplified by Braodband Buffer (U4) with an overall voltage gain of 12 dB and is applied to the input of the output switch.

3.4.1.3.3 High/Low Select Switch (U7)

The High/Low Select Switch (U7) is a CMOS switch wired to function as a double-pull, double-throw switch. The position of U7 is controlled by the high/low band select signal from the Input Preselector (A1). When the high/low band select signal is at 0 volts DC, U7 pins 2 and 3 are connected, and U7 pins 13 and 12 are connected. This action sends +15 volts DC to the high band section of the output switch and sends -15 volts DC to the low band section of the output switch. When the high/low band select signal is at +5 volts DC, U7 pins 5 and 4 are connected, and U7 pins 10 and 11 are connected. This action sends -15 volts DC to the high band section of the output switch and sends +15 volts DC to the low band section of the output switch.

3.4.1.3.4 Output Switch

The Output Switch consists of two separate diode switches, #1 and #2. Diode switch #1 is the low band section of the output switch, consisting of diodes CR1, CR2, and CR3. Diodes switch #2 is the high band section of the output switch, consisting of diodes CR4, CR5, and CR6. The output of buffer Amplifier (U4) drives the input of the two switch sections in parallel. The output of switch #1 is the low band output terminal, and the output of switch section #2 is the high band output terminal. When the high/low band select signal is at 0 volts DC, U7 sends -15 volts to the low band section of the output switch. This forward biases diodes CR1 and CR3, and reverse biases diode CR2, creating a low impedance circuit path from buffer amplifier U4 to the low band output terminal. When the high/low band select signal is at +5 volts DC, U7 sends -15 volts to the high band section of the output switch. This forward biases diodes CR4 and CR6, and reverse biases diode CR5, creating a low impedance circuit path from Buffer Amplifier (U4) to the high band output terminal.

3.4.1.4 Dual IF Amplifier (A6)

Refer to **Figure 3-14,** Dual IF Amplifier (A1A6) Block Diagram, and **Figure 6-7,** Dual IF Amplifier Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-14,** the Dual IF Amplifier consists of the following major circuit areas:

- Input Filtering
- Output Switch

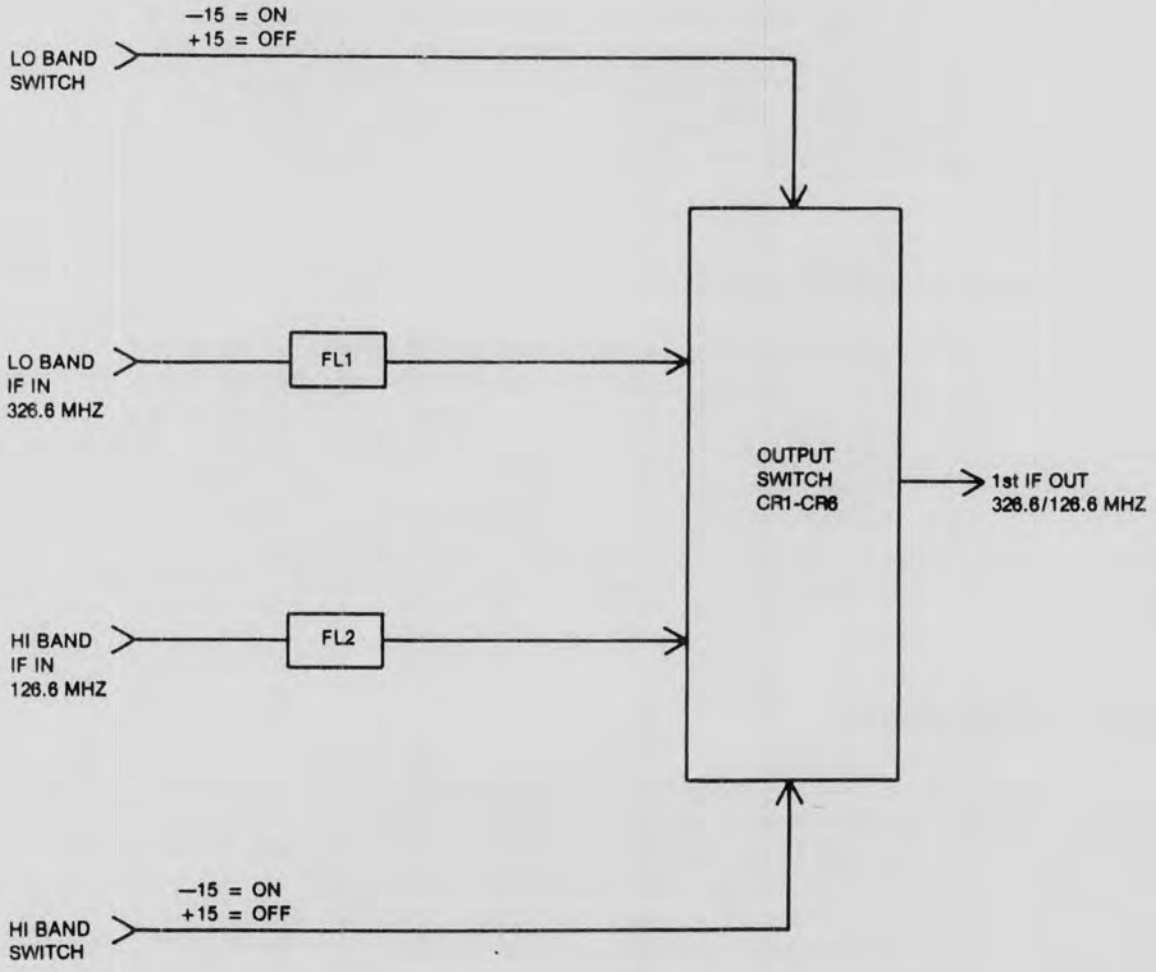


Figure 3-14. Dual IF Amplifier (A1A6) Block Diagram

3.4.1.4.1 Input Filtering

The Input Filtering consists of two bandpass filters, FL1 and FL2. The low band IF input signal 326.6 MHz from the 1st IF Converter (A3) passes through FL1, a bandpass filter with a center frequency of 326.6 MHz. The output of FL1 drives the low band input section of the output switch. The high band IF input signal 126.6 MHz passes through FL2, a bandpass filter with a center frequency of 126.6 MHz. The output of FL2 drives the high band section of the output switch.

3.4.1.4.2 **Output Switch**

The Output Switch consists of two separate diode switches, #1 and #2. Diode switch #1 consists of diodes CR1, CR2, and CR3. Diode switch #2 consists of diodes CR4, CR5, and CR6. The outputs of the two switches are connected in parallel to the first IF output terminal. When the receiver is tuning the low band range of 20-275 MHz, the low band IF signal 326.6 MHz passes through FL1 to the low band section of the output switch. The low band switch signal from the 1st IF Converter (A3) is -15 volts DC. This forward bias diodes CR1 and CR3, and reverse bias diode CR2. This creates a low impedance circuit path from the filter FL1 to the first IF output terminal. When the receiver is tuning in the high band frequency range of 275-512 MHz, the high band IF input signal 126.6 MHz passes through bandpass filter FL2 to the high band section of the output switch. The high band switch signal from the 1st IF Converter (A3) is -15 volts DC, forward biasing diodes CR4 and CR6, and reverse biasing diode CR5. This creates a low impedance circuit path from filter FL2 to the first IF output terminal.

3.4.1.5 **2nd IF Converter (A1A4)**

Refer to **Figure 3-15,** 2nd IF Converter (A1A4) Block Diagram, and **Figure 6-5,** 2nd IF converter Schematic Diagram, as aids in understanding the following description.

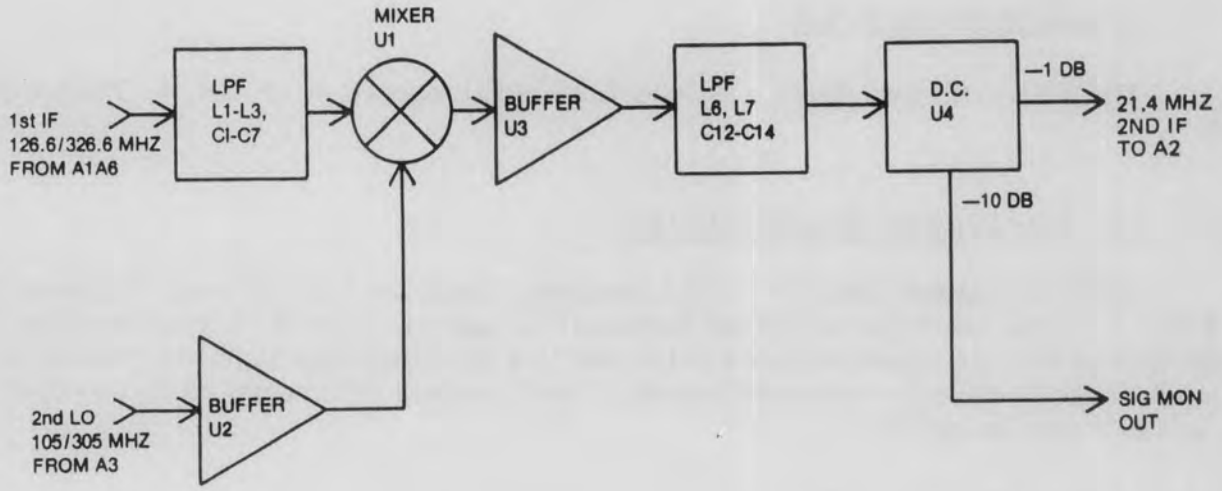


Figure 3-15. 2nd IF Converter (A1A4) Block Diagram

The first IF input signal from the Dual IF Amplifier (A1A6) drives the input of the lowpass filter. If the receiver is tuning a low band frequency range of 20-275 MHz, the first IF input signal is 326.6 MHz. If the receiver is tuning the high band frequency range of 275-512 MHz, the first IF input signal is 126.6 MHz. The lowpass filter consists of inductors L1, L2, L3 and capacitors C1-C7. This filter is an 8-pole elliptic filter with a cutoff frequency of 280 MHz, and exhibits extremely high attenuation for frequencies above its cutoff. The first IF input signal passes through the lowpass filter, through an impedance matching network, directly to the Mixer (U1). The Mixer (U1) is a double-balance mixer with an overall conversion loss of approximately 6 dB. The Mixer (U1) combines the first IF input signal with the 2nd LO signal. The 2nd LO input signal from the Synthesizer (A3) is 305 MHz if the receiver is tuning in the low band frequency of 20-275 MHz or is 105 MHz if the receiver is tuning in the high band frequency of 275-512 MHz. The 2nd LO input signal is amplified by the Buffer Amplifier (U2) which is a broadband integrated amplifier with an overall gain of X dB. The output of U2 drives the local oscillator input to the Mixer (U1). If the receiver is tuning in the low band frequency range, U1 combines the 326.6 MHz first IF signal with a 305 MHz second IF signal to produce a 21.4 MHz IF output signal. If the receiver is tuning the high band frequency range, the Mixer (U1) combines the 126.6 MHz first IF signal with the 105 MHz 2nd LO signal to produce a 21.4 MHz second IF signal. The second IF output from U1 is amplified by the Broadband Buffer Amplifier (U3) with an overall gain of X dB. The output of U3 goes through a 3-pole lowpass filter consisting of inductors L6, L7 and capacitors C12, C13, and C14. The second IF signal passes through the lowpass filter and goes through directional coupler U4 which has two outputs. One output is attenuated by approximately 1 dB, and goes to the 21.4 MHz IF output terminal. The second output is attenuated by approximately 10 dB and goes to the signal monitor output terminal.

3.4.2 IF DEMODULATOR (A2)

The following paragraphs describe the circuit operation of the IF Demodulator modules.

3.4.2.1 21.4 MHz Bandpass Amplifier (A2A1)

Refer to **Figure 3-16**, 21.4 MHz Bandpass Amplifier (A2A1) Block Diagram, and **Figure 6-9**, 21.4 MHz Bandpass Amplifier Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-16**, the 21.4 MHz bandpass amplifier consists of an input amplification section, a bandwidth decoder, four bandpass filters, pin diode switches #1 and #2, and an output amplifier.

3.4.2.1.1 Input Amplification Section

If signals of 21.4 MHz are applied to pin 3 of U1, a voltage controlled attenuator. The attenuation of U1 is controlled by a DC voltage from A2A1 applied to U1, pin 1. The U1 attenuation ranges are from -2 dB for +13 Vdc input to -32 dB for +3 Vdc input. The output of U1, pin 5, drives the input of Q1, pin 2. Broadband Common gate JFET Amplifier (Q2) has a gain of +10 dB. The output of Q1, pin 1, drives impedance matching network L3, L2, and L3, and then the input to the #1 diode switch.

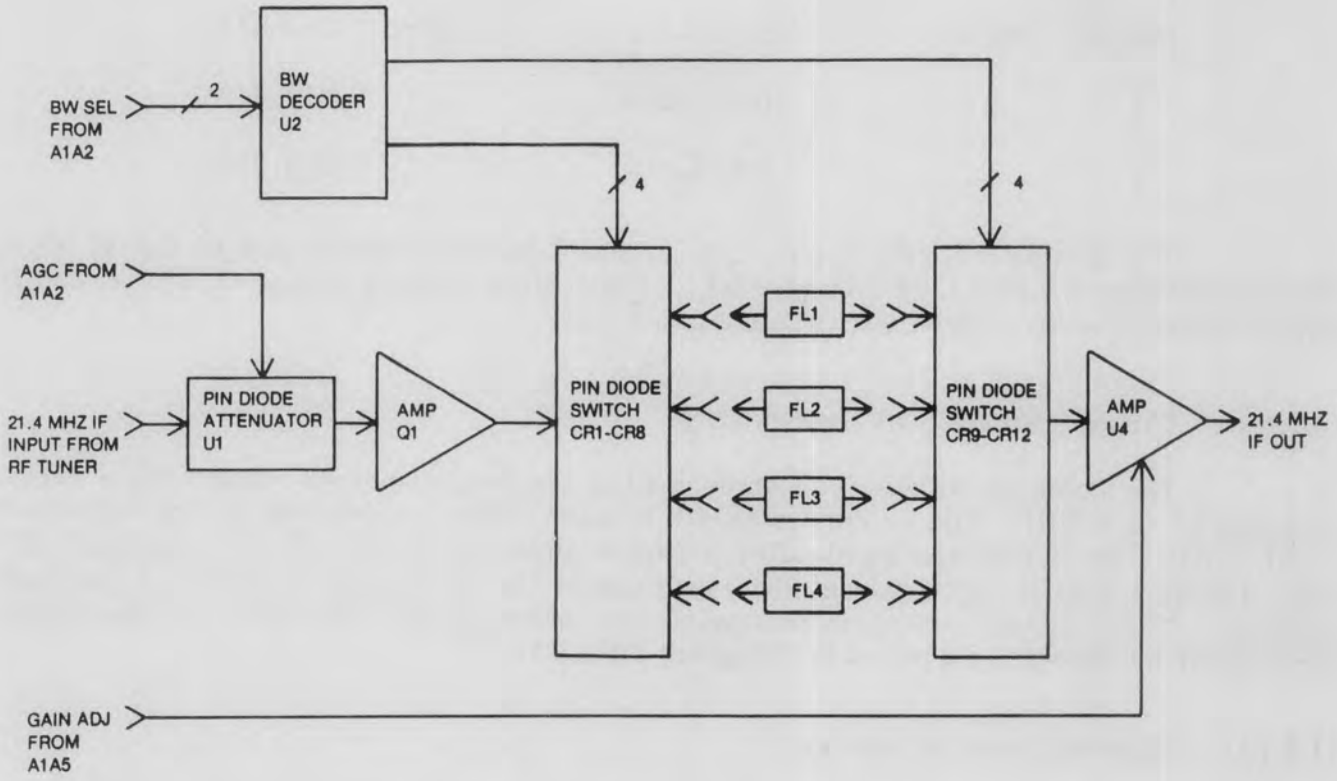


Figure 3-16. 21.4 MHz Bandpass Amplifier (A2A1) Block Diagram

3.4.2.1.2 **Bandwidth Decoder (U2)**

The Bandwidth Decoder (U2), is a 2-bit binary to 4-line decimal decoder. The binary input drives U2 inputs, pins 9 and 10. There are two separate 4-line decimal outputs: output 1 is sent through pins 1, 5, 2, and 4; and ouput 2 is sent through pins 11, 15, 14, and 12.

The 2-bit binary input to U2 is driven by the bandwidth select code from module A2A2. When the input to U2, pins 10 and 9 is equal to 00, U2, pins 1 and 12, are at +15 Vdc. The remaining output pins are open. When the input to U6, pins 10 and 9, is equal to 10 then U6, pins 5 and 14, are at +15 V. When the inputs at pins 10 and 9 are equal to 11, pins 4 and 11 are at +15 V.

Inputs		Outputs	
Pin 10	Pin 9	Pins 1,5,2,4	Pins 11,15,14,12
0	0	+15,0,0,0	0,0,0,+15
0	1	0,+15,0,0	0,0,+15,0

Inputs		Outputs	
Pin 10	Pin 9	Pins 1,5,2,4	Pins 11,15,14,12
1	0	0,0,+15,0	0,+15,0,0
1	1	0,0,0,+15	+15,0,0,0

The decimal outputs at pins 1, 5, 2, and 4 provide forward bias to the #2 diode switch consisting of diodes CR9 through CR12. The decimal outputs at pins 11, 15, 14, and 12 provide forward bias to diodes CR1, CR3, CR5, and CR7.

3.4.2.1.3 Bandpass Filters (FL1 through FL4)

The Bandpass Filters (FL1 through FL4) are fixed bandpass filters with a center frequency of 21.4 MHz. The actual bandwidth of each filter is selectable at the customer's option. The range of available bandwidths is from a minimum of 2.85 kHz to a maximum of 4 MHz. The 21.4 MHz IF signal is routed through one of the four bandpass filters by the diode switches. These filters are field-changeable to accommodate different IF bandwidths. Operation of the diodes is explained in **Paragraph 3.4.2.1.4.**

3.4.2.1.4 Diode Switches (#1 and #2)

Diode Switch #1 consists of diodes CR1 through CR8. Diode switch #2 consists of diodes CR9 through CR12. These diodes exhibit low forward resistance when forward biased and extremely high resistance when reverse biased. The diodes are used to route the IF signal through one of four bandpass filters.

As an example in analyzing the operation of the diodes, the signal path through CR7, FL4, and CR12 is discussed.

Assuming the the BW select code from A1A2 is equal to 00, the output of U6, pins 1 and 12, equals +15 V, and the remaining output pins will be open. Diode switch #1, diode CR7, is forward biased, CR8 is reverse biased, and diode CR12 is forward biased. These conditions create a low impedance circuit path through CR1, FL1, and CR9 to the input of U9, the output amplifier.

Diodes CR3, CR5, and CR1 are reverse biased by -15V through R17, R21, and R9 and thus have a high resistance, while CR4, CR6, and CR2 are forward biased and have an extremely low resistance. This prevents any of the 21.4 MHz IF signal (from T1) from reaching FL2, FL3, FL4. Overall isolation exceeds 70 dB.

3.4.2.1.5 Output Amplifier (U4)

The Output Amplifier (U4) is a broadband, high-gain amplifier. The actual gain of U9 is controlled by a DC current applied to pins 2 and 3. This current is derived from the gain adjust voltage from A2A5. The amplified 21.4 MHz IF signal from U4, pin 7, is sent to A2A2. This amplifier provides proper gain-bandwidth compensation. The maximum gain of U4 is approximately 38 dB.

3.4.2.2 AM/SSB/CW Demodulator (A2A2)

Refer to **Figure 3-17**, the AM/SSB/CW Demodulator (A2A2) Block Diagram and **Figure 6-10**, the AM/SSB/CW Demodulator Schematic Diagram as aids in understanding the following description. As shown in **Figure 3-17**, the AM/SSB/CW Demodulator consists of the following components: an input IF amplifier, a log signal strength detector, a wideband/narrowband filter, an AM detector, a product detector, a video switch, a peak detector, an AGC switch, and a gain control amplifier.

3.4.2.2.1 Input IF Amplifier (Q1, AT1, U2)

The 21.4 MHz IF signal input from A1A1 is coupled through transformer T2 to match the input impedance of IF amplifier Q1, a high-gain, dual-gate FET amplifier. The gain of Q1 is varied over a 10 dB range by the DC voltage on gate number 2, pin 2. This DC voltage is derived from the AGC control seciton and is discussed in a later paragraph. The amplified 21.4 MHz IF signal at Q1, pin 1, is coupled through tuned matching network C8, C9, C10, and L4 and drives a broadband amplifier, U2 through AT1.

The Adjustable Attenuator (AT1) is inserted in the signal path between Q1 and U2. It maintains a constant 50 ohms impedance as its attenuation is varied and, is used to adjust the overall gain of the demodulator during IF gain alignment. The amplified 21.4 MHz IF signal output of U2, pin 2, drives the input of the wideband/narrowband filter.

3.4.2.2.2 Logarithmic Signal Strength Detector (U1)

The Logarithmic Signal Strength Detector (U1) is an integrated circuit whose input at pin 15 is driven from the 21.4 MHz IF signal coming from A1A1. The output of U1, pin 13, is a DC voltage whose level varies from 0 to +2 Vdc and is proportional to the logarithm of the actual IF signal level. The output of U1, pin 13, goes to A1A3 as the LOG SS signal.

3.4.2.2.3 Wideband/Narrowband Filter

The Wideband/Narrowband Filter consists of two circuit paths. One is a broadband low-loss circuit and the other is a narrowband double-tuned IF filter circuit. The actual circuit path is selected by the narrowband select signal from A2A4. The narrowband circuit is selected for all bandwidths less than or equal to 200 kHz. The wideband circuit path consists of diodes CR2 and CR4. The narrowband consists of diodes CR3, CR5-CR7, and the double-tuned circuit comprised of C23 through C28, and L6 and L7.

When the narrowband select signal is low, U3, pin 3, is equal to -15 Vdc and U3, pin 4, is open. This forward biases diodes CR2, CR4, CR5, CR7, and reverse biases CR3 and CR6. In turn, a low impedance circuit path is provided from U2, pin 2, through CR2, R17, and CR4, and to the input of Q2. The narrowband circuit path is cut off since diodes CR3 and CR6 are reverse biased and have extremely high resistance and diodes CR5 and CR7 shunting the signal path to ground.

When the narrowband select signal from A1A4 is high, the U3, pin 3, output is open and the U3, pin 4, output is equal to -15 Vdc. This forward biases CR3 and CR6 and reverse biases CR2, CR4, CR5, and CR7. Therefore, a low impedance circuit path exists from U2, pin 2, through CR3, through the narrowband tuned filter and through CR6 to the input of Q2. The wideband circuit path through CR2 and CR4 is cut off because CR2 and CR4 are reverse biased and, therefore, have high resistance.

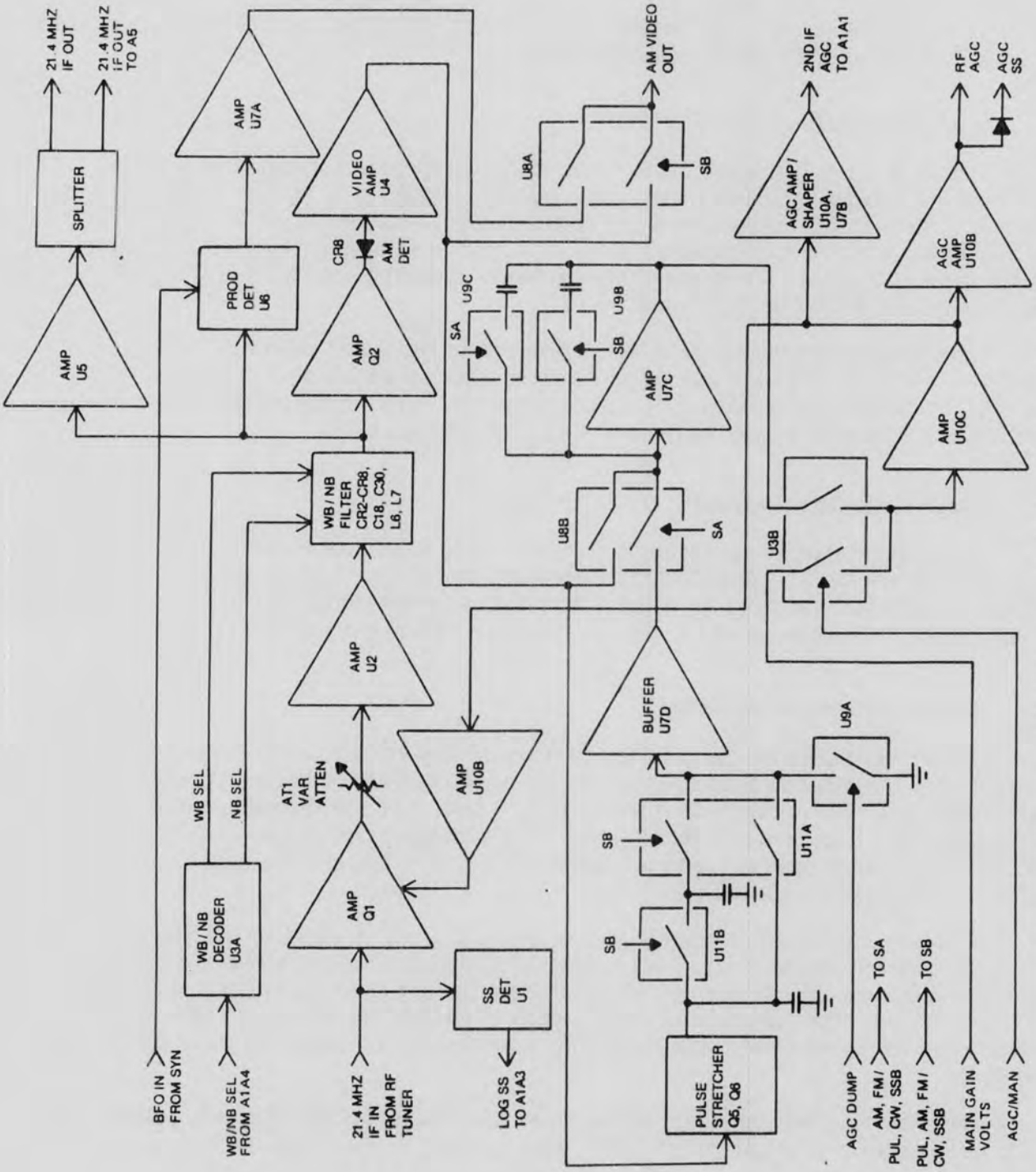


Figure 3-17. AM/SSB/CW Demodulator (A2A2) Block Diagram

3.4.2.2.4 AM Detector (Q2, CR8, U4)

The 21.4 MHz IF signal from the wideband/narrowband filter Broadband is amplified by Q2, IF buffer amplifier. The output of Q2's collector is coupled through Broadband Transformer (T1). The signal is demodulated by CR8, the AM detector. The detected AM signals are filtered and amplified by Video Buffer Amplifier (U4) which is operating at unity gain. CR8 is slightly forward biased by -15V through R29. R32 is used to set the DC offset of U4 and therefore compensate for bias voltage on CR8.

3.4.2.2.5 Product Detector (U6, U7)

The Product Detector (U6) is a balanced demodulator. The 21.4 MHz IF signal from the wideband/narrowband filter is applied to one of the inputs of U6 at pin 4. The BFO signal from the Synthesizer (A3) is applied to the other input of U6 at pin 10. Product Detector (U6) mixes the BFO signal with the 21.4 MHz IF signal.

The resultant output signal at U6, pin 12, is an audio signal representing the difference between the two input frequencies. The audio signal is applied to pin 3 of U7, an audio buffer amplifier. The video output at U7, pin 1, goes to the Video Switch (U8).

3.4.2.2.6 Video Switch (U8)

The Video Switch (U8) has 2 inputs, pins 2 and 5. Pin 5 is the AM video input from the AM detector whose output is U4, pin 6. U8, pin 2, is the CW/SSB audio input from the Audio Buffer Amplifier (U7) pin 1. The U8 switch is controlled by the CW select signal at A2A4. When the CW select signal is high, U8, pin 5, is connected directly to U8, pin 4. The AM video output signal travels from the AM detector through U4, pin 6, to the AM video output. When the CW select signal is low, pin 2 is connected to pin 3 and the AM/CW/SSB video output travels from the product detector through U7, pin 1, to the AM video output.

3.4.2.2.7 Peak Detector (Q5, Q6)

The input for the pulse stretching circuit is taken from the AM Video Amplifier (U4). Q5 and Q6 form a positive peak detector used for pulse, CW, and SSB signals. Capacitor C17 is supplied charging current by Q6 and holds the peak when video signal level drops. The Amplifier (U7) acts as a high impedance input buffer amplifier. The output of U7 is a DC voltage proportional to the peak amplitude of the video signal. Switch U11 adds capacitor C69 across C17 in the Pulse/CW/SSB modes to increase the time constant of the detector.

The AGC Switch (U8B) is controlled by the AM, FM/PUL, CW, SSB select signal which comes from A2A4. In the AM or FM mode, this signal is high and U8, pin 10, is connected to U8, pin 11. This arrangement connects the video signal from U4, pin 6, to the inverting input of the Gain Control Amplifier (U7C). In the CW or Pulse mode, this control line is low and pin 13 is connected to pin 12 of U8. This latter arrangement connects the video signal from U4, pin 6, through the peak detector and then to the input of the gain control amplifier, U7C. The use of the peak detector is necessary in the CW and Pulse modes because the signals may have a very low duty cycle (signals are present only briefly and then absent for a long period of time).

The normal AGC control amplifier is not able to adequately process the signals in the SSB/CW or the Pulse mode. The peak detector captures the short pulse width signals in the SSB/CW and Pulse modes and holds the IF gain constant.

3.4.2.2.8 Gain Control Amplifier (U7, U9, U3, U10)

The gain control voltage from either U4, pin 6, or the peak detector through U7, pin 14, is applied to the input of the Gain Control Amplifier U7. U7 is a high-gain, DC-coupled low pass filter and has a biased threshold point. The output at U7, pin 8, starts moving negative (below 0 Vdc) if the output from the AGC switch U8 exceeds 0.5 Vdc. (At this 0.5 VDC level, the AM Detector Buffer Amplifier (U4) is at 0.5 Vdc and the Receiver input level is approximately equal to the rated sensitivity level for the selected IF Bandwidth.

The output of U7 travels through the AGC/Manual Select Switch (U3B). This switch is controlled from the MAN SEL line coming from A2A4. If AGC has been selected as a function, the MAN SEL line is low and the output from U7, pin 8, goes through U8, pin 13, to U8, pin 12, and directly to U10C, pin 9. If manual mode has been selected, the MAN SEL line is high and pins 12 and 13 open and disconnect the output from U7. U8 pins 10 and 11 are connected, joining the amplifier U10C, pin 9, to the manual gain voltage which comes from A2A4. This manual gain voltage replaces the automatic gain voltage from U7, pin 8, and permits the operator to manually adjust the gain of the demodulator. The voltage from A2A4 is approximately 0 to -10 Vdc.

The unity gain buffer Amplifier (U10C) output drives the gain control amplifier U10A and the gain controlled IF Amplifier (Q1) pin 2, through U10D. The output of U10D is clamped at -3.7 V by Q5. In normal operation, U10C, U10D, and Q5 cause a voltage variation of 0 to -3.7 across CR1. This yields a 30 dB gain reduction through the IF Amplifier (Q1).

3.4.2.2.9 AGC Circuit

The output of U10C draws three separate AGC amplifers, U10D, U10A, and U10B which provide three different AGC voltages. U10D provides the first IF AGC to dual gate MOSFET Q1. The voltage at the output of U10D moves from 0 to approximately -5 Vdc where it is clamped by transistor Q4. This provides the first 40 dB of AGC in the receiver. As the output of U10D is being clamped, the RF AGC voltage at pin 7 of U10B is starting to move from 0 Vdc to a +5 Vdc level for 30 dB of RF AGC before being clamped by Q3. As pin 12 of J2 is clamped at +5 Vdc the output of pin 7 U7B starts to move from +13 Vdc toward approximately 2 Vdc for the last 30 dB of AGC in the unit. The voltage is shaped by diode network (CR12 and CR15) and biasing resistor (RG4, RG5, RG1, and RG2) which provide 2 break points in the output voltage.

3.4.2.2.10 IF Output Amplifier U5 and U15

The 21.4 MHz signal from Wideband/Narrowband filter is stepped down in impedance through T3 and fed to U5 through R45 and R46. U5 output signal is then power split by L11, L12 network. E3 provides 21.4 MHz IF Output to rear panel of unit. C74 couples the signal to U15 which amplifes the signal before it is routed to the FM Demodulator Motherboard (A2A5). R45 is used to adjust the level of 21.4 MHz signal.

3.4.2.3 Video/Audio/COS (A2A3)

Refer to **Figure 3-18**, the Video/Audio/COS (A2A3) Block Diagram and **Figure 6-11**, the Video/Audio/COS Schematic Diagram as aids in understanding the following description. As shown in **Figure 3-18**, the Video/Audio/COS module consists of the following components: an AM video amplifier, a video output amplifier, 2 audio amplifier/lowpass filters, a LOG SS peak detector, an SS combiner/amplifier, a COS comparator, and a COR amplifier.

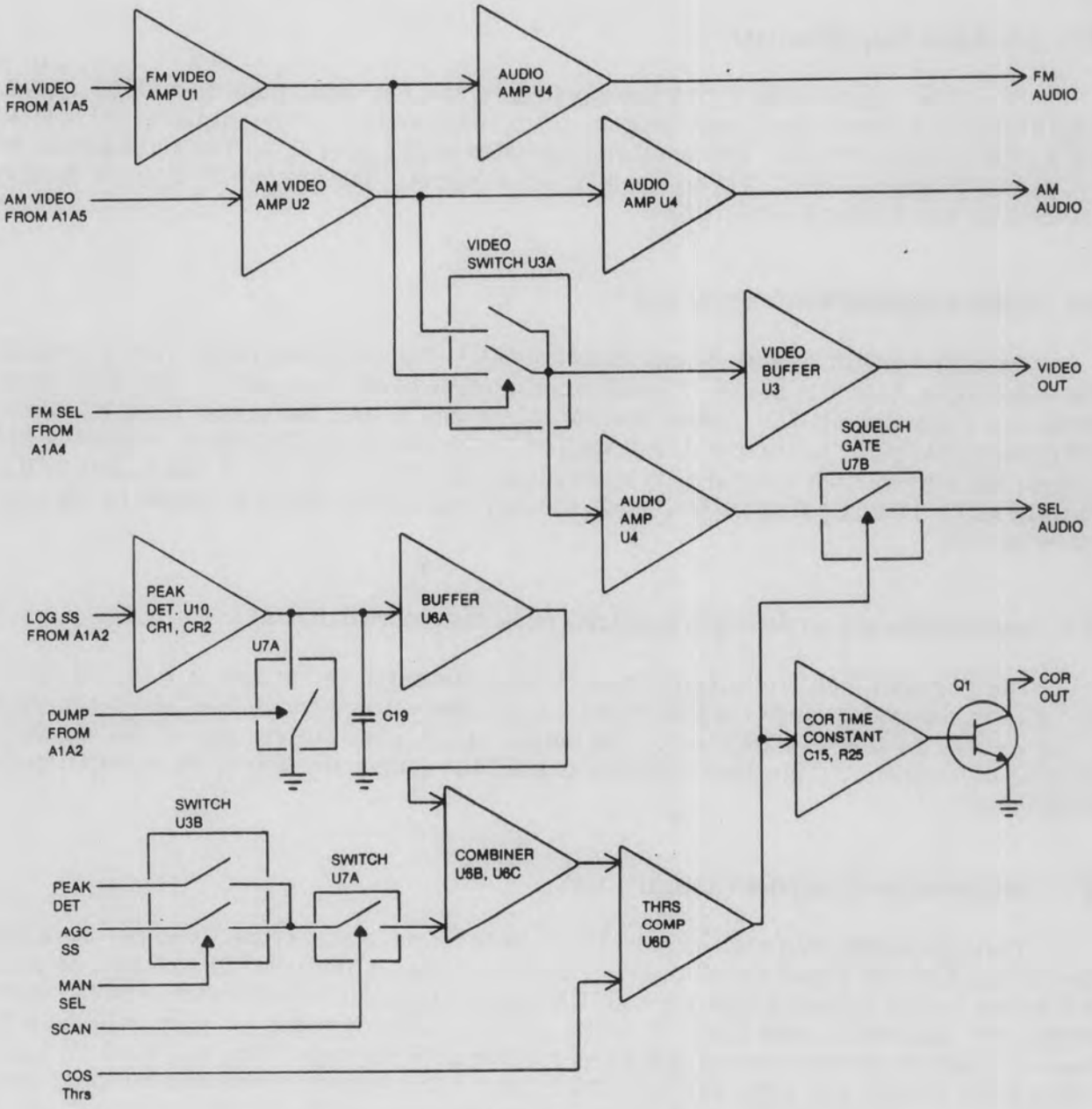


Figure 3-18. Video/Audio/COS (A2A3) Block Diagram

3.4.2.3.1 AM Video Amplifier (U2)

AM/CW or SSB video signals from A2A5 are applied to the AM video amplifier at U2, pin 2. Adjustable Gain Buffer Amplifier (U2) provides an overall voltage gain of approximately 4. The output at U2, pin 6, drives the Audio Amplifier (U4D). This amplifier operates with a gain of 3. The audio output at U4, pin 14, passes through LPF L3, C14 to the AM audio output. The output from U2, pin 6, is also sent to the input of the Analog Switch (U3A).

3.4.2.3.2 FM Video Amplifier (U1)

FM video signals from A2A5 are applied to the FM video amplifier at U1, pin 2. Audio Amplifier (U1) has an overall voltage gain of approximately 6. The output at U1, pin 6, drives the Audio Amplifier (U4A). This amplifier operates with a gain of 3. The audio output at U4, pin 7, passes through LPF L1, C3 to the FM audio output. The output of U1, pin 6, also drives the input to the Analog Switch (U3A).

3.4.2.3.3 Video Amplifier/Switch (U3, U5)

The video amplifier selects one of two inputs: the AM video input from U2, pin 6; or the FM video input from U1, pin 6. The selection is controlled from A2A4. The FM select line controls the Video Switch (U3). When the FM select line is low, the output from U2, pin 6, is coupled through U3, pin 2, to U3, pin 3, and applied to U5, pin 3 and U4, Pin 2. When the FM select is high, the output from U1, pin 6, is coupled through U3, pin 5, to U3, pin 4, and to U5, pin 3 and U4, Pin 2. The output from U5, pin 8, is the video output which is routed to the rear panel connector, J8.

3.4.2.3.4 Logarithmic Signal Strength (LOG SS) Peak Detector (U10, U6)

The Log SS signal from A1A2 drives a peak detector comprised of U10, U6, CR1, and CR2. C19 is charged through CR2 by U10 to a positive voltage which is equal to the peak value of the voltage applied to U10, pin 3. The output at U6, pin 8, drives one of the inputs to the SS Combiner/Amplifier. This peak detector is used to remove any amplified modulation on the LOG SS signal.

3.4.2.3.5 SS Combiner/Amplifier (U3B, U7, U6)

The SS Combiner/Amplifier has two inputs. One input, from U6A, pin 8, is the peak value of the LOG SS signal from A2A2. The other input is the AGC SS voltage, or peak detector voltage in the manual mode through U3D, from the AGC circuitry on A2A2. These two voltages are summed at the input of U6B, pin 13. U6B operates at a voltage gain of approximately unity for the AGC input and at -2 for the LOG SS input. The output of U6B, pin 14, represents the sum of the AGC and LOG SS inputs. This signal is inverted by unity gain inverter U6C. The output at U6C, pin 7, then drives the input of the COS Comparator and is also routed to rear panel connector, J9, for the signal strength output of 0 to 10 Vdc, and to A4 Digital Interface for reporting of signal strength to the front panel display.

3.4.2.3.6 COS Comparator (U6D)

The COS Comparator (U6D) is a voltage comparator. The input at pin 2 is biased from 0 to +10 V by the COS threshold signal. The input at U3 monitors the voltage level from U6C, pin 7. The output at U6D pin drives the SEL AUDIO Switch (U7B) and the COR amplifier U4C. If the output at U6C, pin 7, exceeds the COS threshold, U6D, pin 1, is high. This closes pins 14 and 15 of U7B, passing the video signal from U3A, pin 3 and 4, through U4B, U7B, and LPF L4/C11 to the SEL AUDIO output. At the same time, U4C, pin 8, is high, saturating Q1 and clamping the COR OUT line to ground. If the output at U6C, pin 7, drops below the COS threshold, U6D, pin 1, goes low, opening switch U7B and also turning off Q1 after a delay of approximately 3 seconds.

3.4.2.4 FM Demodulator Motherboard (A2A5)

Refer to **Figure 3-19**, the FM Demodulator Motherboard (A2A5) Block Diagram, and **Figure 6-13**, the FM Demodulator Motherboard Schematic Diagram as aids in understanding the following description. As shown in **Figure 3-19**, the FM demodulator motherboard consists of four FM demodulator modules, an AM video multiplexer, an FM video multiplexer, and a demod select/gain adjust multiplexer. The FM demodulators provide FM demodulation and low pass filtering of the 21.4 MHz IF signal and routing of the AM video signals through the AM video low pass filters.

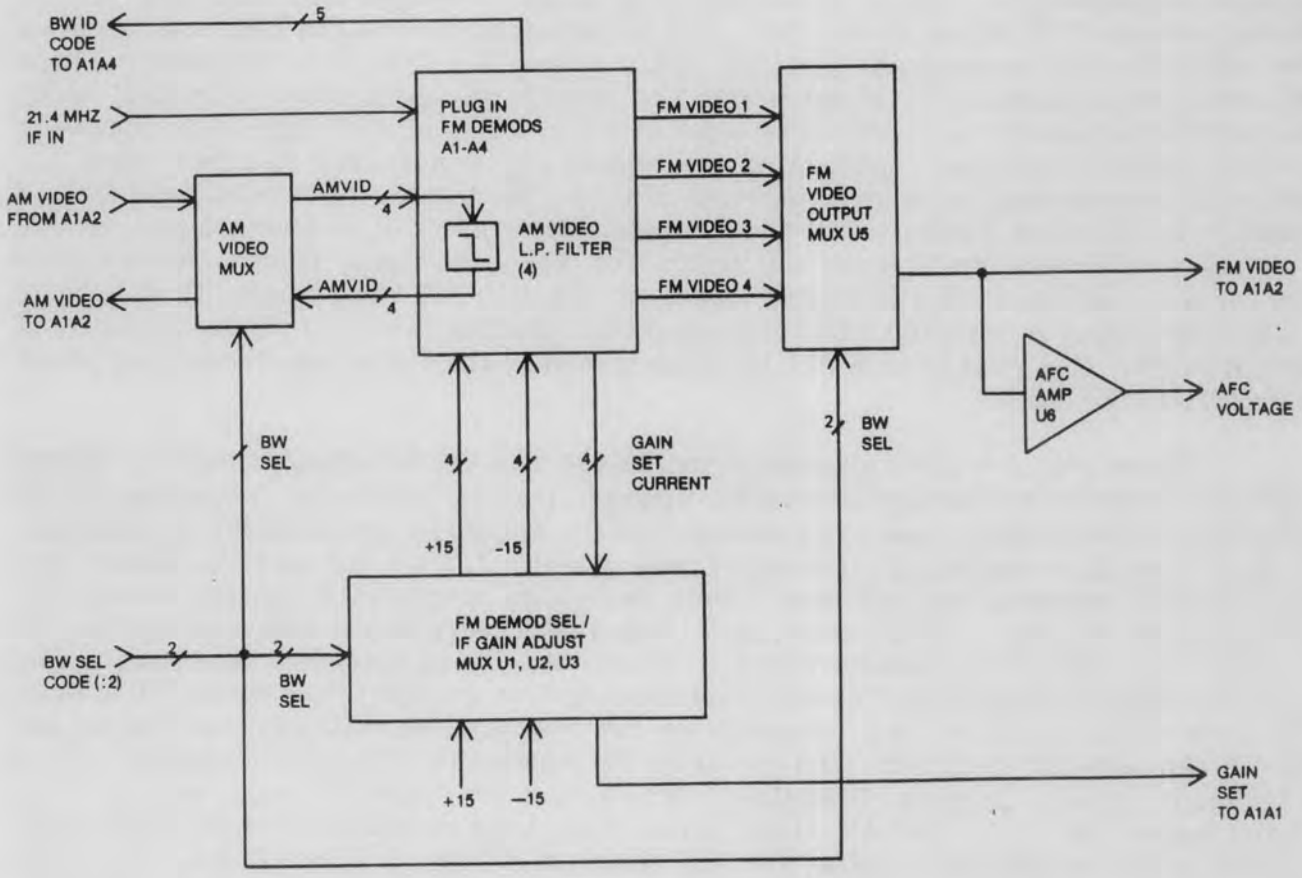


Figure 3-19. FM Demodulator Motherboard (A2A5) Block Diagram

3.4.2.4.1 FM Demodulator Modules (A2A5A1 through A2A5A4)

The FM Demodulator Modules (A2A5A1 through A2A5A4) have four different bandwidths, each corresponding to the bandwidth of a matching bandpass filter in A1A1. The 21.4 MHz IF input signal from A1A2 drives the common input to all four of the demodulator units on P3-1. These modules are field-changeable to accommodate different IF bandwidths.

When selected, each demodulator module is energized by +15 Vdc on P1-11 and -15 Vdc on P2-1. This energizing voltage is provided by the Demod Select/Gain Adjust Multiplexer which decodes the BW Select Word from A1A4. Each demodulator module is assigned a 5-bit bandwidth ID code. During power up, the software initializing routine successively energizes the BW ID network on each demodulator module. The BW ID codes are then read back into the Connector Interface (A1A5) which keeps a record of the actual bandwidth of each module as installed.

There are three types of FM demodulator modules used in the receiver: 10-25 kHz, 30-200 kHz, and 300 kHz - 4 MHz.

Figure 3-20 is a block diagram of the 10-25 kHz BW FM demodulator module. **Figure 6-13**, FM Demodulator Motherboard Schematic Diagram, may be referred to for greater detail. The 21.4 MHz IF input signal from A2A2 is amplified and limited by the Wideband Amp/Limiter (U1). The U1 output is coupled to differential peak detector L1, C7, C10, C11, and C6. Crystal Y1 increases the Q of the tuned network, giving the demodulator the required narrowband characteristic. Below 21.4 MHz, C11 series resonates with the tank circuit, developing maximum IF voltage across C11. The IF voltage is detected by CR2 which sends a positive voltage to the noninverting input of U2A. Above 21.4 MHz, C11 bypasses the tank circuit, developing maximum IF voltage across L1. The IF voltage is detected by CR1 which sends a positive voltage to the noninverting input of U2B. The output at U2A-1 is a composite of the two negative voltages, representing the typical FM demodulator "S-curve" since the output of U2B is connected to the inverting input of U2A. The low level FM video from U2A, B is amplified by the Video Buffer (U2C) and Lowpass Filter (L4-C20) to give a high level FM video output to the video multiplexer via P1-2. The AM video signal from A1A2 is routed through the lowpass filter. This filter establishes an effective AM video bandwidth of 0.7 x IF BW. The filter output is routed to A2A3 through A2A2. The bandwidth ID network consists of R3 and CR3-CR7. This gives a bandwidth ID which is read by the digital interface during power up, as explained previously.

Figure 3-21 is a block diagram of the 30-200 kHz FM demodulator module. **Figure 6-13**, FM Demodulator Motherboard Schematic Diagram, may be referred to for greater detail. The 21.4 MHz IF input signal from A1A2 is amplified and limited by the Wideband Amp/Limiter (U1). The U1 output is coupled to differential peak detector L1, C7, C8, and C6. Below 21.4 MHz, C11 series resonates with the tank circuit, developing maximum IF voltage across C11. The IF voltage is detected by CR2 which sends a negative voltage to the noninverting input of U2A. Above 21.4 MHz, C11 bypasses the tank circuit, developing maximum IF voltage across L1. The IF voltage is detected by CR1 which sends a negative voltage to the noninverting input of U2B. The output at U2A-1 is a composite of the two negative voltages, representing the typical FM demodulator "S-curve". The low level FM video from U2A B is amplified by the Video Buffer (U2C) and Lowpass Filter (L4-C20) to give a high level FM video output to the video multiplexer via P1-2. The AM video signal from A1A2 is routed through the lowpass filter. This filter establishes an effective AM video bandwidth of 0.7 x IF BW. The filter output is routed to A2A3 through A2A2. The bandwidth ID network consists of R3 and CR5-CR7. This gives a bandwidth ID which is read by the digital interface during power up, as explained previously.

Figure 3-22 is a block diagram of the 300 kHz - 4 MHz BW FM demodulator module. **Figure 6-13**, FM Demodulator Motherboard Schematic Diagram, may be referred to for greater detail. The 21.4 MHz IF input signal from A1A2 is amplified and limited by the Wideband Amp/Limiter (U1). The IF output from U1 is applied to the Discriminator. The Discriminator is center-tuned to 21.4 MHz and establishes the necessary phase shifts to convert wideband FM to amplitude variations. These variations are detected by CR1 and CR2 and amplified by the Video Buffer (U2). They are lowpass-filtered at 1/2 the IF bandwidth by L2 and C14 to give a high level FM video output to the video multiplexer via P1-2. The AM video signal from A1A2 is lowpass-filtered by L3 and C5 to approximately 0.7 times the selected IF bandwidth. The filter output is routed back through A1A2 to A1A3 for video and audio outputs. The bandwidth ID network consists of R11, R12, and combinations of diodes CR3 through CR7.

The video outputs from the four FM demodulators are routed through the video multiplexer and are explained in **paragraph 3.4.2.4.3.** The AM video outputs from the four FM demodulators are routed through the AM video multiplexer and are explained in **paragraph 3.4.2.4.2.**

Each FM demodulator module also provides a fixed gain set current output to A2A1U4. The current is derived from the +15 Vdc supply through a dropping resistor (R16-narrowband, R13-wideband.) The gain set current appears at P1-3 of the active FM demodulator module and is routed through the Demod Select/Gain Adjust Multiplexer. It is then sent through A5P5 to A1P1 where it provides gain bandwidth compensation by adjusting the gain of A2A1U4 for the installed IF bandwidth.

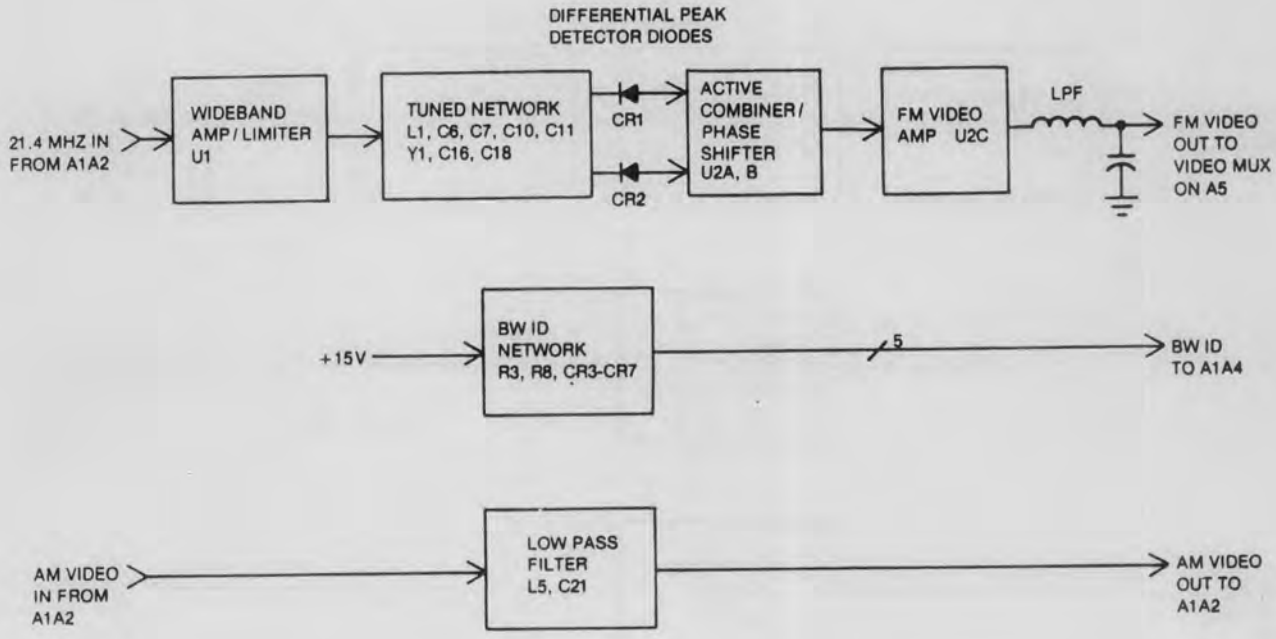


Figure 3-20. FM Demodulator (10-25 kHz BW)

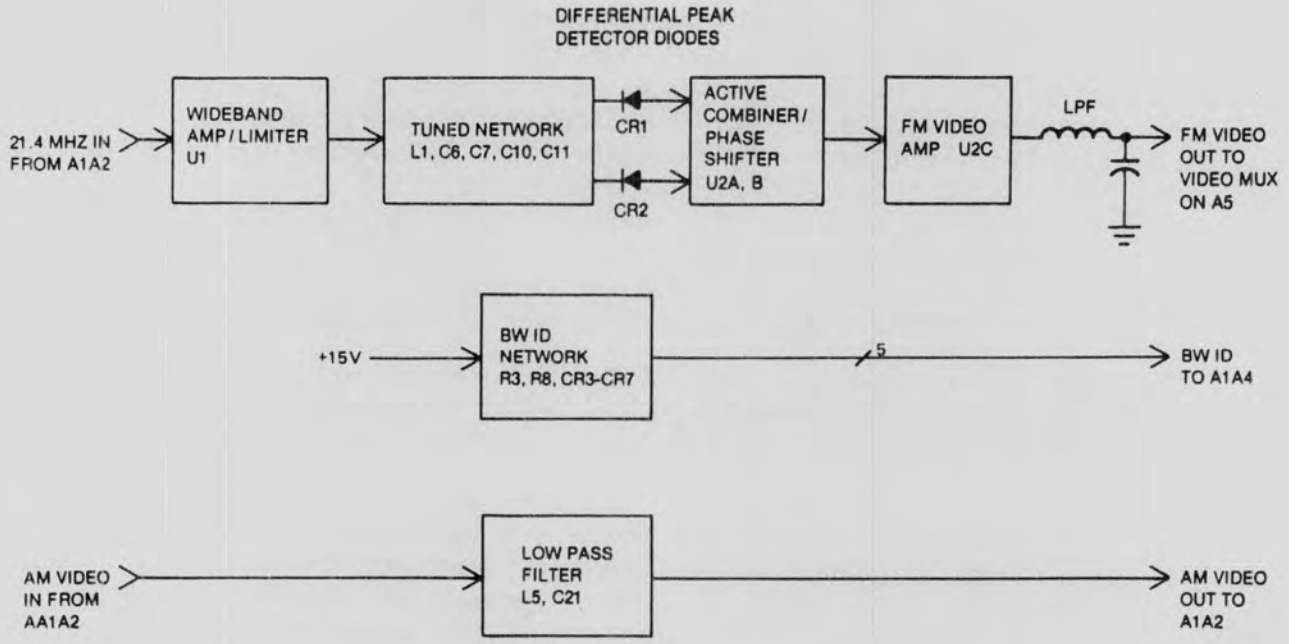


Figure 3-21. FM Demodulator (25-300 kHz BW)

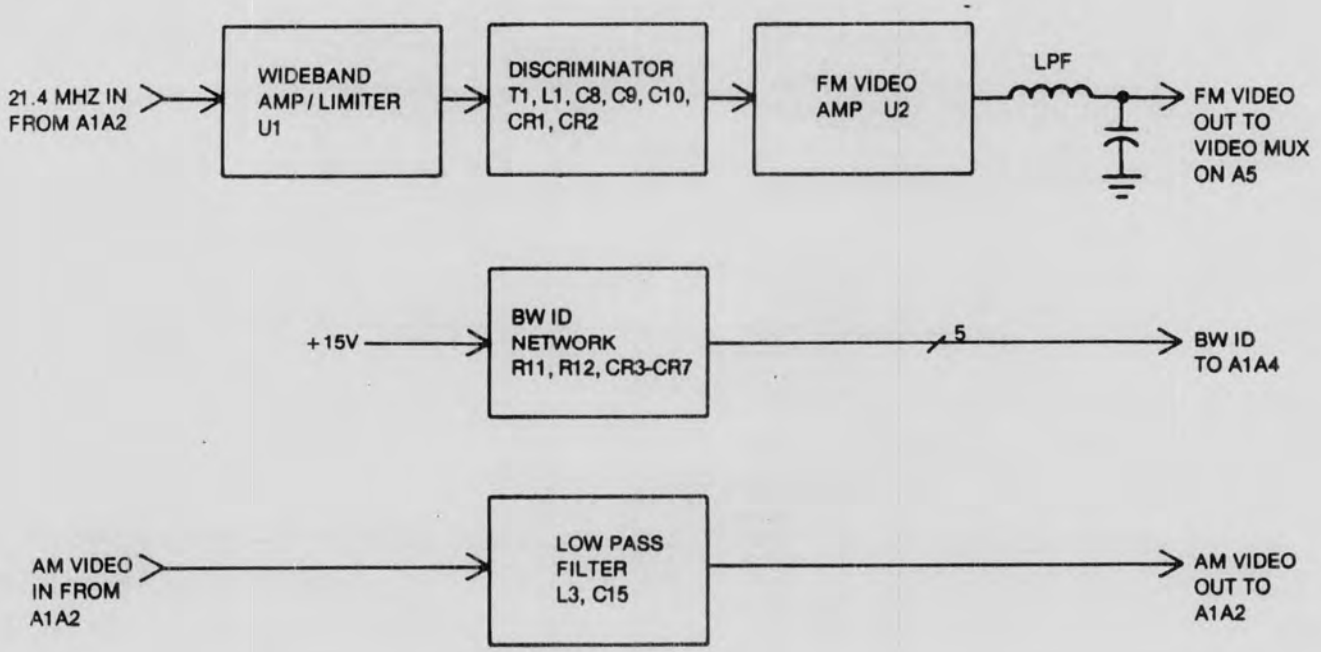


Figure 3-22. FM Demodulator (300 kHz - 4 MHz BW) Block Diagram

3.4.2.4.2 AM Video Multiplexer (U4)

The AM Video Multiplexer (U4) is a two-section addressable analog multiplexer. The address inputs enter on pins 9 and 10 and are driven by the bandwidth code from A2A4. This two-bit code enters U4, which has two separate sections. Each section has one analog input and four analog outputs. The two address inputs, therefore, select one of the four outputs. The multiplexer routes the AM video input to the selected FM demodulator for AM video filtering and then routes the output of the lowpass filter to AM video output P2.

If a code of 00 exists at the inputs, output number one is selected (U4, pins 1 and 12). If a code of 01 is received at the input pins, output number two is selected (U4, pin 5 and 14). If a 10 is received, output number three is selected (U4, pin 2 and 15). If an 11 is received at the input pins, output number four is selected (U4, pin 4 and 7). U4, pin 3, is the AM video input from A2A2; the signal goes through that half of U4 and the AM video signal appears at pins 1, 5, 2, or 4 as selected by pins 9 and 10 (address inputs).

Assuming an address code of 00 is received at input pins 9 and 10, the AM video through pin 3 appears at U14, pin 1, and goes to P1, pin 9, on demodulator module A1. Internally, it is lowpass-filtered in A1 and appears on P1, pin 10, to U4, pin 12. Pin 12 is connected to pin 13 (since the input was 00), and the output is sent through A2A2 to Video/Audio/COS as (A2A3) the filtered AM video signal.

3.4.2.4.3 FM Video Output Multiplexer (U5 and U6)

The FM Video Output Multiplexer is composed of the Analog Switch (U5) and Buffer Amplifier (U6). U5 is an analog multiplexer with two address inputs at pins 10 and 9, driven from the bandwidth select code from A1A4. U5 has four FM video inputs (pins 1, 5, 2, 4) and single output at pin 3. A code of 00 on pins 10 and 9 connects pin 1 to 3. A code of 01 connects pin 2 to pin 3, a code of 10 connects pin 5 to pin 3, and a code of 11 connects pin 4 to pin 3.

Multiplexer (U5) video signals from the four FM demodulator units with one active at a time. An input of 00 to pins 10 and 9 of U5 means that the FM video output of module A1 (P1, pin 2) goes to U5, pin 1, through U5, pin 3. The signal is then routed through A5P1 and A2A2 to A2A3 Video/Audio/COS. The signal also goes to Buffer Amplifier (U6) a high-gain DC-coupled buffer amplifier (operating as a lowpass filter). The output of U6, pin 6, is used as an AFC voltage to generate an error correction voltage to the host unit (external) driving the demodulator.

3.4.2.4.4 Demod Select/Gain Adjust Multiplexer (U1, U2, U3)

The Demod Select/Gain Adjustment Multiplexer performs two functions: to select one of four demodulators to be active and to route the selected demodulator's gain adjust output current through the gain adjust line to A1A1.

Dual Analog Multiplexer (U2) is similar in operation to U4 with two separate sections each having four inputs and one output. Multiplexer U2 is addressed at pins 10 and 9 from the bandwidth select code coming from A1A4.

One-half of U2 sends +15 Vdc to the correct demodulator to be energized; the other half is used to process the gain adjust current for the desired demodulator. Example: 00 is input to pins 10 and 9. U2, pin 12, is connected to U2, pin 13, effectively placing +15 Vdc on the control pin U1, pin 6. These conditions cause U1, pin 2 to be connected to U1, pin 3, and U1, pin 5, to be connected to U1, pin 4. This sends +15 Vdc to demodulator unit A1, P1, pin 11, and also a -15 Vdc to demodulator unit A1, P2, pin 1. Therefore, the 00 sent to U2 energizes the FM Demodulator (A1). A code of 00 sent to U2 also connects pin 1 to pin 3 which connects the gain adjust current from demodulator unit A1 to P5, the gain set output to A2A1U4. The same principles apply to codes 01, 10, and 11 being applied to input pins 9 and 10. Pin 3 is connected to pin 1, 5, 2, or 4 of U2 which are the gain adjustment current outputs of FM demodulators A1, A2, A3, and A4.

3.4.2.5 Digital Interface (A2A4)

Refer to **Figure 3-23** Digital Interface (A2A4) Block Diagram, and **Figure 6-12** Digital Interface Schematic Diagram, as aids in understanding the following description. The digital interface is a single printed circuit card consisting of a CPU, address latch, EPROM, address decoder, serial I/O, interrupt circuit, D to A converter, BW/mode latch, BW ID buffer, RF tune address latch, and a polled I/O analog switch.

3.4.2.5.1 CPU (U1)

The CPU (U1) is an 8031 CMOS microcontroller (CPU) containing 128 bytes of internal RAM. It requires an external ROM for proper operation. It operates at a 10 MHz rate, determined by crystal Y1, and has a 1.2 microsecond instruction cycle. The CPU is a self-contained device with the exception of an external EPROM which contains the system operating software.

The RC circuit U20, R5, R6, C11, C12, connected to the CPU Reset Input, pin 9, pulses high when power is applied to the digital interface. This resets all the internal hardware registers and starts the CPU at addresses 00. The program then performs an initialization rutine which sends data to and initializes the CPU. The CPU has four 8-bit I/O ports, P0 through P3. The initialization routine determines the functions of each of these ports.

A total of 11 bits of data (P1.0 through P1.7 and P3.0, P3.4 and P3.5) are configured for the synthesizer tuning data I/O port. This port sends the synthesizer data from the CPU to the Synthesizer (A3) via the SYN Data/Address Bus.

The INT 0 (P3.2) and INT 1 (P3.3) signals are used when the WJ-9040 I/O Bus is in the remote control.

The PO port (a bidirectional address/data bus) allows the CPU to communicate with the circuitry on or off the card using the WJ-9040 I/O bus. The PO port contains 8 address lines, AD0 through AD7, but 13 address lines are necessary for addressing within the demodulator. The remaining 5 address lines (A8-A11 and A15) defined as P2 complete the necessary address lines for the CPU. A12, P2.4 through A14, P2.6 are not used.

The REM/SEL output, P3.1, is used (local when high, remote when low) to control COS and IF gain analog switches.

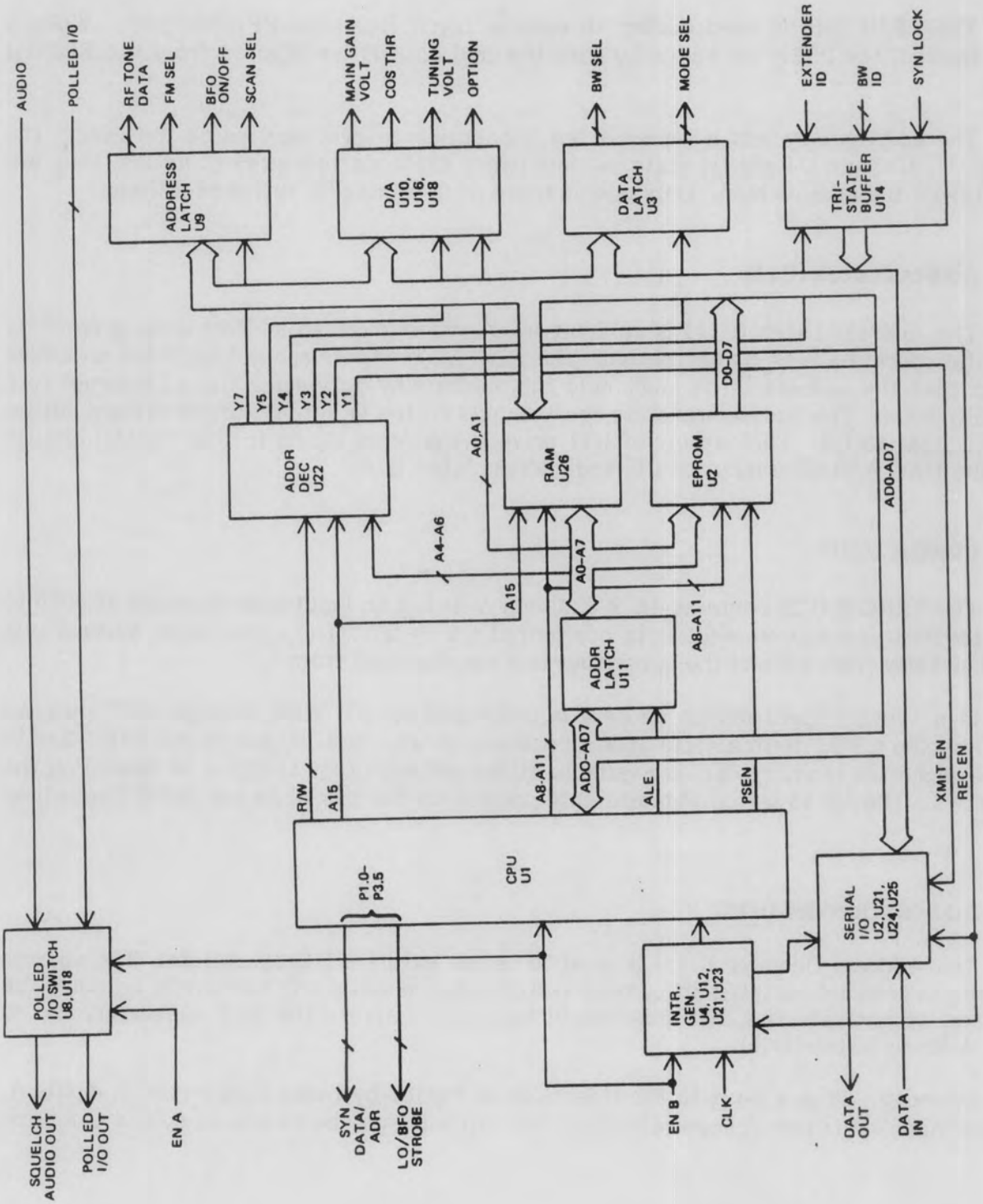


Figure 3-23. Digital Interface (A2A4) Block Diagram

The RD (P3.7), and WR (P3.6), lines are used only for internal data transfers within A2A4.

The ALE (Address Latch Enable) output is toggled from a high to a low to clock valid address data out on the AD0-AD7 lines. Address latch U2 holds the valid address for one complete cycle.

The PSEN line is used during an opcode fetch from the EPROM (U3). When a transfer is required, the PSEN momentarily goes low and data is transferred from the EPROM to the CPU.

The address data bus is an 8-bit bus connecting several devices on the card. The outputs from U1, U2, and U4 are tri-state outputs (when these devices are not active, they are disconnected from the address bus). Only one of these devices may be active at a time.

3.4.2.5.2 Address Latch (U11)

The Address Latch (U11) is an 8-bit latch which holds an address coming from U1 while a specific operation is being performed. The AD0-AD7 outputs are not valid for an entire bus cycle, so that the address latch must hold this address by activating the ALE signal to a high then a low level. This action transfers the D inputs to the Q outputs which remain until a new address is sent to U2. The outputs of U11 drive the address inputs to U22 (A,B,C) and U2 (A0 to A7), the DAC A/DAC B input to U6, and address latch U26.

3.4.2.5.3 EPROM (U2)

The EPROM (U2) contains 4K x 8 memory. It has an input address range of 0000 to FFFF. The EPROM also has an 8-bit data bus output Q0 to Q7. The eight lower address bits are received directly from U2 and the upper four bits are received from U1.

In a typical operation an address is presented to U2 (AD0 through AD7 plus A8 through A11) by the CPU. With a valid address present at U3, the CPU pulses the PSEN line to a low and the addressed memory data is available at the outputs of Q0 to Q7 to be placed on the address data bus. The Q0 to Q7 outputs are only present on the bus while the PSEN line is held low.

3.4.2.5.4 Address Decoder (U22)

The Address Decoder (U22) is used to define external I/O operations. The address decoder is used to select data transmit or receive through the serial I/O circuit, to activate the BW I.D. buffer, to activate the BW mode select latch, to activate the D/A converter, and to activate the Address Latch (U26).

Decoder U22 is a 3-bit to 8-bit decoder addressed by three binary bits on inputs A, B, and C. The input value has a range of 000 to 111. With 000 placed on the A, B, and C inputs,

the Y0 output would go low. With 001 on the input lines, Y1 would be active and so on. Refer to the following example:

Inputs A B C	Output Activate
0 0 0	Y0
0 0 1	Y1
0 1 0	Y2
0 1 1	Y3
1 0 0	Y4
1 0 1	Y5
1 1 0	Y6
1 1 1	Y7

The G2A enable input is driven by the RD and WR lines from U1 and is used to enable U22.

The A, B, and C address inputs are driven by bits A4, A5, and A6 from the address outputs of U11. While U11 has 16 address bits, the least significant eight are used for external device addressing.

To utilize U22, U1 sends an address over the AD0 to AD7 lines, latch it through U11, and on to U22. Two outputs on U22 are not being used: Y0 and Y6. The first valid output on U22 is, therefore, Y1. Y1 is the transmit enable line to the serial I/O circuitry. To activate Y1, 0000 (Q0-A3) and 1000 (Q4-Q7), which equals 10 in hexadecimal is sent from U11 to U22. Simply stated, a hexadecimal address of 10 is sent from the CPU, through U11 to U22, activating the Y1 output. The Y2 output (serial I/O receive enable line) is activated when a hex address of 20 is received from U11. The Y3 output to the tri-state buffer is activated when a hexadecimal address of 30 is received from U11. The Y4 output to the BW mode select latch is selected when a hex address of 40 is received. The Y5 output selects the A portion of the D/A converter (U6) when a hex address of 70 is received from U11. With a hex address of 50 (Y7 from U22 and Q2 from U11) the B portion of the D/A converter will be selected. The Y0 through Y7 outputs are active low signals. The Y7 output selects U26 when a hex address of 74 is received from U11.

HEX Address	U8 Outputs
10	Write Data/Transmit Enable to Serial I/O Circuit
20	Receive Enable/Read Data to Serial I/O Circuit
30	Enable B/W ID Buffer (U4)
40	Enable Mode BW Latch (U5)
50	Enable Address Latch (U26)
70	Enable D/A Converter Section A
74	Enable D/A Converter Section B

3.4.2.5.5 Interrupt (INT0 and INT1)

Data transfers between the demodulator and an external controller are serial synchronous and are made up of three signals: CLK, Enable B, and Data (Input or Output). The CLK and Enable signals are used to interrupt the CPU so that a data transfer function may be performed.

The eight clocks interrupt circuit consists of AND Gate U21B, counter U4, and an inverter U23. Data is clocked in or out eight bits at a time. Counter U4's output is inverted and on the following edge of the eight count interrupts the CPU to read or write the data byte. When a data read is performed the U4 counter is reset to 0 and is ready for another byte of data.

The enable B Input INT1 is high to low edge triggered interrupt. When the Enable B signal goes high to enable the data transfer and then returns low at the end of the data message, the CPU stops what it is currently doing and performs the function according to the message received.

3.4.2.5.6 Serial I/O (U2, U21, U24, U25)

The serial I/O is a bidirectional parallel-to-serial, serial-to-parallel transmitter/receiver circuit consisting of U25, a serial-to-parallel converter, and U24, a parallel-to-serial converter. Both U24 and U25 are driven by a gated CLK U21B with U24 enabled by the transmit enable line Y1 from U22 and U25 enabled by the receive enable line Y2 from U22.

When the data is received from the Digital Control (A4) enable B goes high and eight clocks are received causing the data to be clocked into the device U25. The input INTO goes low, interrupting the CPU to read a byte of data from serial to parallel device U25 by the Y2 output of U22. After the last byte of data has been received, the enable B signal INT1 is reset and notifies the CPU to process the data received.

A data transfer to the Digital Control (A4) is a similar function. A data byte is loaded into the parallel-to-serial device, U24, by the Y1 output of U22. Enable B goes high and eight clocks are received shifting the serial data out. This interrupts the CPU to load up another byte of data for the Digital Control (A4) to read or an Enable B interrupt occurs to finish the cycle.

3.4.2.5.7 D/A Converter (U10)

The D/A Converter (U10) and analog switches U21A and U21B are used to control IF gain, set COS threshold voltage, and generate tuning voltage for the RF tuner.

The D/A Converter has 8 data bits at its input lines D0 through D7 and voltage outputs at VA, VB, VC, and VD. If all of the data inputs are low, the output is equal to 0 Vdc. If the data inputs are all high, the output is 2.5 Vdc. Each one-bit increment or change at the input causes the voltage to change by approximately 10 millivolts. The outputs at VA, VB, VC, and VD are amplified BY U16 and U18 to produce a voltage range at each output of 0 to +10 Vdc. The VA, VB, VC, and VD outputs are selected by the A0 and A1 inputs and are enabled by WR.

3.4.2.5.8 Bandwidth/Mode Latch (U3)

The Bandwidth/Mode Latch (U3) is an 8-bit octal latch similar to the Address Latch (U11). Inputs to U3 consist of eight bits from the data bus (AD0 through AD7). The Q1 through Q4, Q6, and Q7 outputs of U3 are used to define the mode and bandwidth selection for the IF processing section and exit the digital interface card via J3. The Q0 output is a Read Request bit to let the controller know when a demodulator needs service. It is sent to the polled I/O Switch (U8). The Q5 output exists the card to produce the DUMP signal.

In a typical operation, the CPU (U1) examines the front panel data from the Digital Interface every 3 milliseconds. If there is a change in the front panel inputs, the CPU puts the BW/mode select data word on the data bus to the D inputs of U3. The new BW/mode data is latched to the Q outputs and connected to the IF demodulator when the address decoder U22, Y4 output goes from a low to a high.

3.4.2.5.9 Bandwidth I.D. Buffer (U14)

The bandwidth I.D. is the unique code assigned to each of the four demodulator modules as explained in **paragraph 3.4.2.4.1.**

During the power-up initialization routine, the CPU examines each of the four FM demodulator modules and reads the BW I.D. present on each card. The BW I.D. is brought in through U14 and placed on the data bus to the CPU memory. This way, the CPU knows which FM demodulator to energize when it receives the request from one of the four bandwidths.

Five inputs (U4 pins 2, 4, 6, and 11) comprise the BW I.D. information. During the initialization routine, the CPU selects the FM demodulator #1. The BW I.D. code enters U14 which is selected by the Y3 output of U8 (hexadecimal address of 30). The BW I.D. information is then placed on the data bus (AD0 through AD4). The BW I.D. of FM demodulator #1 is then transferred into the memory of the CPU. BW I.D's #2, #3, and #4 are similarly processed.

Inputs 13 and 15 are used to read the Frequency Extender ID and Synthesizer Lock bits into the CPU. These are read via bits AD5 and AD6 respectively.

The BW I.D. code is also used to define a configurator, a 16-bit data word that defines this unit, i.e., operating frequency range, bandwidths available, etc. It is used by the WJ-9040 system controller so that the controller can identify what this unit is, what it contains, and its purpose in the system, i.e., which demodulator and what its bandwidths are.

3.4.2.5.10 Polled I/O Switch (U8)

The Polled I/O Switch (U8) is used by the WJ-9040 System controller to extract information from the demodulator using the Enable A and Enable B inputs. The Enable B input transfers the READ REQ, SIG STR, and COS STATUS (J1, pin 20, 18, 25) to the polled I/O bus to the IOM108. The COS STATUS is not used in this unit.

The SIG STR entering from J2, pin 7, would be passed thorugh U8, pin 6, to J1, pin 29, to the IOM108 when energized by the Enable B input. The COS STATUS output from J2,

pin 5, is connected to U8, pin 1. When the Enable B signal enables U11, the COS STATUS is then connected to the bus through U8, pin 11, to J1, pin 26.

The SEL AUDIO entering from J2, pin 6 is passed through U18 and U8, pin 3, to the IOM108 via J1, pin 32, when U8 is energized by the Enable A input. The Enable A signal is only active for the demodulator that has been selected by the IOM108. AFC from J4, pin 10, is passed through U8, pin 14, to J1, pin 30 when U8 is energized by the EN B signal.

3.4.2.5.11 Tune Data/Mode Latch (U9)

The Tune Data/Mode Latch (U9) is an 8-bit octal latch similar to the Address Latch (U11). Inputs to U9 consist of eight bits from the data bus (AD0-AD7) and the Y7 output of U22. The Q0 and Q1 outputs of U9 are the FM and SCAN SEL signals. QZ selects the BFO. Q3 selects HI or LO BAND tuning. Q4-Q7 are the RF and LO band switch signals. Data on the data bus is latched through U9 to the Q0-Q7 outputs when the address decoder U22 Y7 output goes from low to high.

3.4.3 SYNTHESIZER MODULES (A3)

The following paragraphs describe the circuit operation of the Synthesizer Modules.

3.4.3.1 Time Base (A3A2)

Refer to **Figure 3-24**, Time Base (A3A2) Block Diagram, and **Figure 6-15**, Time Base Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-24**, the Time Base consists of the following major circuit areas:

- Splitter
- Buffer Amplifiers (U2 and U3)

3.4.3.1.1 Splitter

The 50 MHz reference signal from the SRM105 Site Reference Module passes into the time base and drives a two-way Splitter. The Splitter is composed of L3, L4, C10, and C9. The Splitter divides the 50 MHz reference signal into two ouputs with an overall nominal loss of approximately 3dB. The two outputs from the Splitter drive the time-base Buffer Amplifiers (U2 and U3).

3.4.3.1.2 Buffer Amplifiers (U2 and U3)

Buffer Amplifiers (U2 and U3) amplify the 50 MHz reference outputs from the splitter. Each Buffer Amplifier is a hybrid broadband solid state amplifier with an overall gain of approximately 14 dB. The outputs of U2 and U3 form the two reference output signals from the Time Base (A3A2).

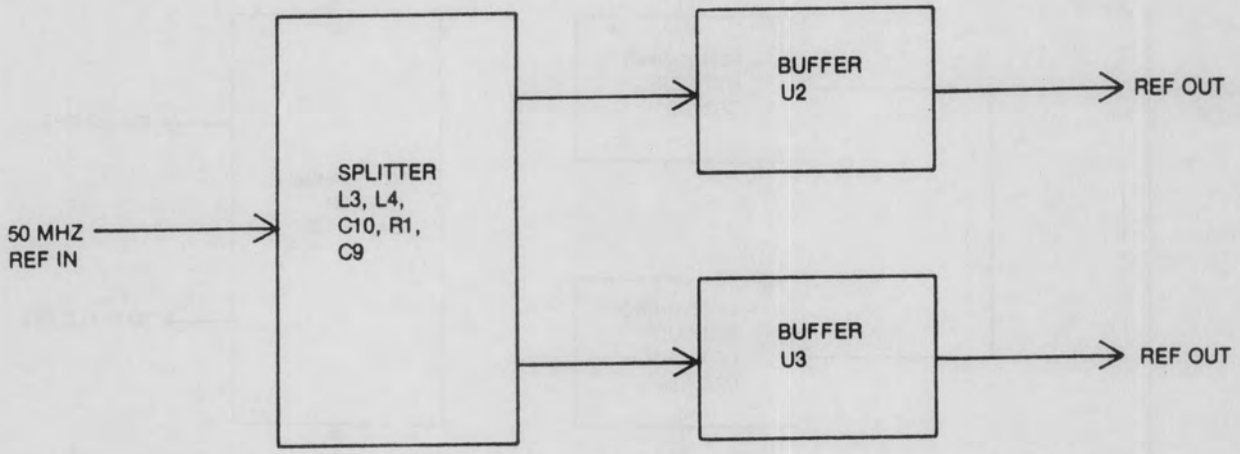


Figure 3-24. Time Base (A3A2) Block Diagram

3.4.3.2 **2nd LO VCO (A3A3)**

Refer to **Figure 3-25,** 2nd LO VCO (A3A3) Block Diagram, and **Figure 6-16,** 2nd LO VCO Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-25,** the 2nd LO VCO consists of the following major circuit areas:

- Low Band VCO
- High Band VCO
- Combiner Buffer

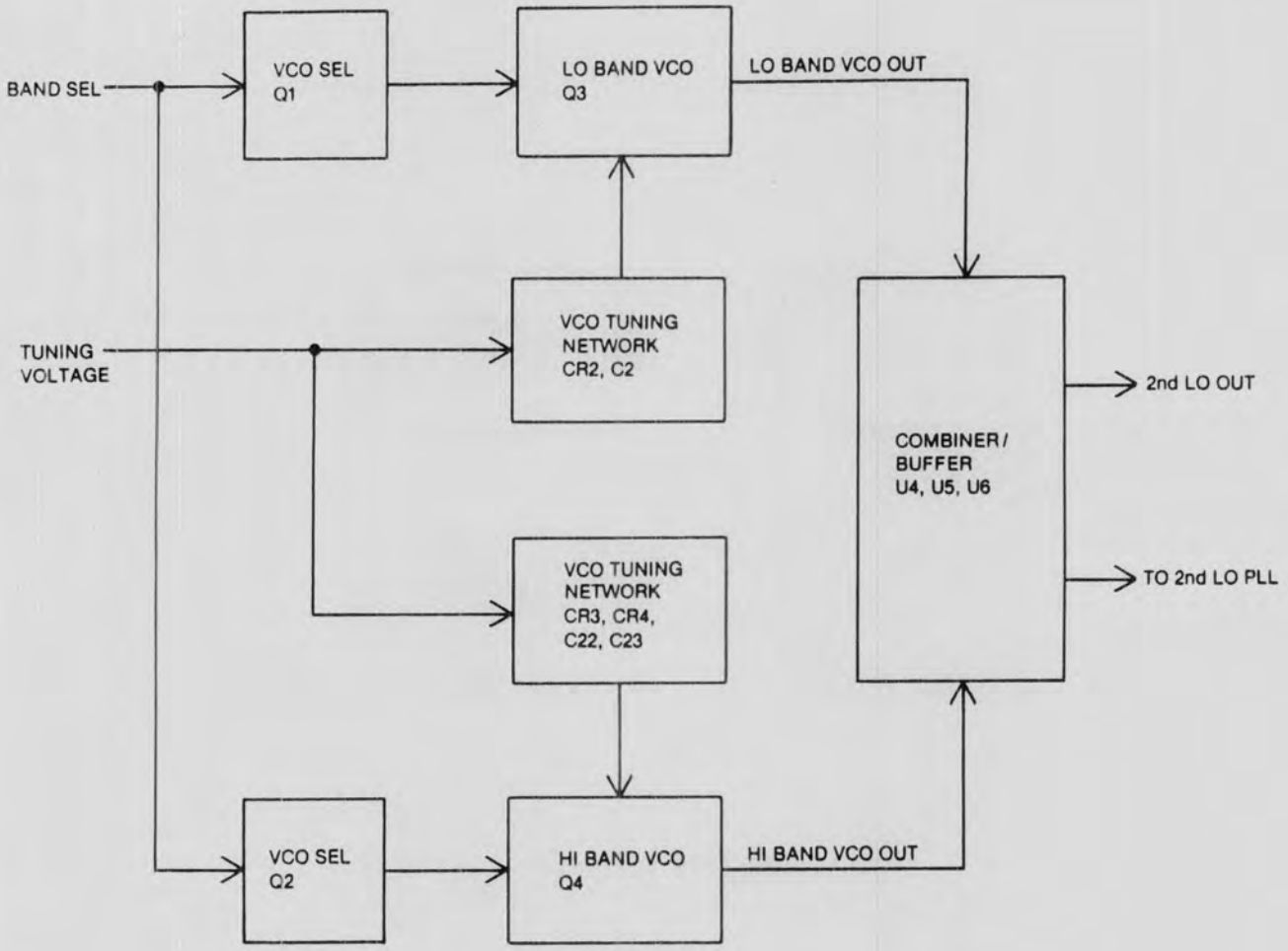


Figure 3-25. 2nd LO VCO (A3A3) Block Diagram

3.4.3.2.1 **Low Band VCO**

The Oscillator Gain Element in the low band VCO (Q3) is tuned by resonant circuit L1, C4, C2, and varactor diode CR2. The low band VCO, is energized by VCO select transistor Q1 when it is enabled by a high +5 volt band select signal. Tuning voltage from the 2nd LO/PLL (A4) is applied to CR2 the low band VCO tuning diode. As the tuning voltage changes, the oscillation frequency of Q3 changes. This allows the 2nd LO/PLL (A4) to force the Low Band VCO to oscillate at the correct frequency.

3.4.3.2.2 High Band VCO

The Oscillator gain element in the high band VCO (Q4) is tuned by resonant circuit C21, DL1, C22, C23, and varactor tuning diodes CR3 and CR4. The High Band VCO is energized by VCO select transistor Q2 which is enabled by a low 0 volt DC band select signal. Tuning voltage from the 2nd LO/PLL (A4) is applied to the junction of the tuning diodes CR3 and CR4. As the tuning voltage changes the oscillation frequency of U4 changes. This permits the 2nd LO/PLL (A4) to force the high band VCO to oscillate at the correct frequency.

3.4.3.2.3 Combiner Buffer

The outputs of the low and high band VCOs are connected to the input ports of a two-way hybrid combiner. Either the low band VCO or the high band VCO is active at any given time as selected by the band select signal. Therefore, the output of the hybrid combiner is either the low band VCO signal or the high band VCO signal. The output from hybrid combiner, U4, passes through an impedance matching pad and is amplified by broadband buffer amplifier U5 with an overall gain of approximately 14 dB. The output of U5 is aplit into two separate outputs by hybrid splitter U6. One output goes directly to the 2nd LO output jack. The other output goes through an impedance matching pad and is sent to the 2nd local oscillator PLL.

3.4.3.3 2nd LO/PLL (A3A4)

Refer to **Figure 3-26**, 2nd LO/PLL (A3A4) Block Diagram, and **Figure 6-17**, 2nd LO/PLL Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-26**, the 2nd LO/PLL consists of the following major circuit areas:

- Prescaler (U4)
- Dual Divider (U3)
- Phase Detector (U2)
- Loop Filter

3.4.3.3.1 Prescaler (U4)

The VCO signal from the Auxiliary VCO (A6) drives the input of the prescaler (U4). The Prescaler is a fixed divide-by-80 counter, which divides the Auxiliary VCO input signal by 80. The output of U4 drives one of the two inputs of the Dual Divider (U3).

3.4.3.3.2 Dual Divider (U3)

The Dual Divider (U3) is a two-section divide-by-5 counter. Each section operates independently. The first section is driven by the output of the Prescaler (U4). The second section of U3 is driven by the IF input signal which comes from the Reference Mixer (A8). The output of the first section of U3 drives one of the two inputs of the Phase Detector (U2). The output of the second section of U3 drives the second input to the Phase Detector (U2).

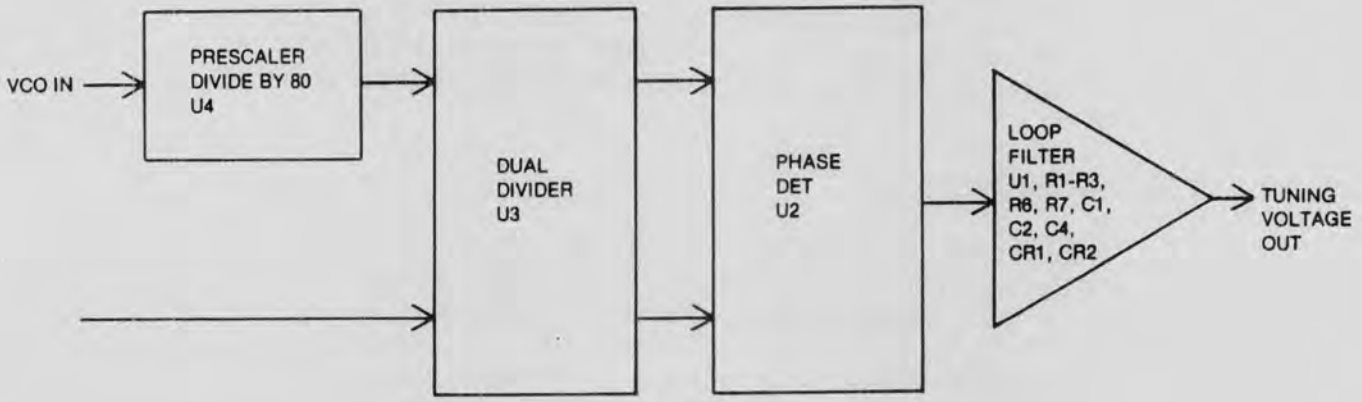


Figure 3-26. 2nd LO/PLL (A3A4) Block Diagram

3.4.3.3.3 Phase Detector (U2)

The Phase Detector (U2) is an integrated single package phase detector with two inputs; one input comes from section one and the other input comes from section two of the Phase Divider (U3). The Phase Detector (U2) compares the frequencies of the signals on its two inputs. In normal operation, the frequency at the #1 input is exactly 520 KHz, and the frequency at the second input is close to 520 KHz. Internally the Phase Detector compares these two frequencies and generates a small DC voltage proportional to the difference in the frequency of the two signals. This voltage is output from U2 as a string of extremely short pulses. These pulses drive the input of the loop filter.

3.4.3.3.4 Loop Filter

The Loop Filter consists of integrated circuits U1, R6, R7, C4, R3, C2, R2, R1, C1 and diodes CR1 and CR2. The lop filter receives the short pulses from the Phase Detector (U2) and averages or integrates these pulses to form an average DC voltage which represents the difference in frequency between the two signals driving the input of U2. This average DC voltage is the tuning voltage which drives the input of 2nd LO VCO (A3). Diodes CR1 and CR2 form a speed-up circuit which increase the lock speed when a large change in frequency is requested. The diodes momentarily conduct and bypass R2 to produce a large step increase in the tuning voltage which quickly forces the 2nd LO VCO to change frequency. As the 2nd LO

VCO frequency moves closer to the correct frequency, diodes CR1 and CR2 no longer conduct and the tuning voltage passes through R2 which, combined with R1 and C1 forms a lead lag low pass filter to smooth the tuning voltage.

3.4.3.4 Auxiliary PLL/Phase Detector (A3A5)

Refer to **Figure 3-27**, Auxiliary PLL/Phase Detector (A3A5) Block Diagram, and **Figure 6-18**, Auxiliary PLL/Phase Detector Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-27**, the Auxiliary PLL/Phase Detector consists of the following major circuit areas:

- Divider (U1)
- Prescaler (U3)
- Frequency Synthesizer (U2)
- Loop Filter

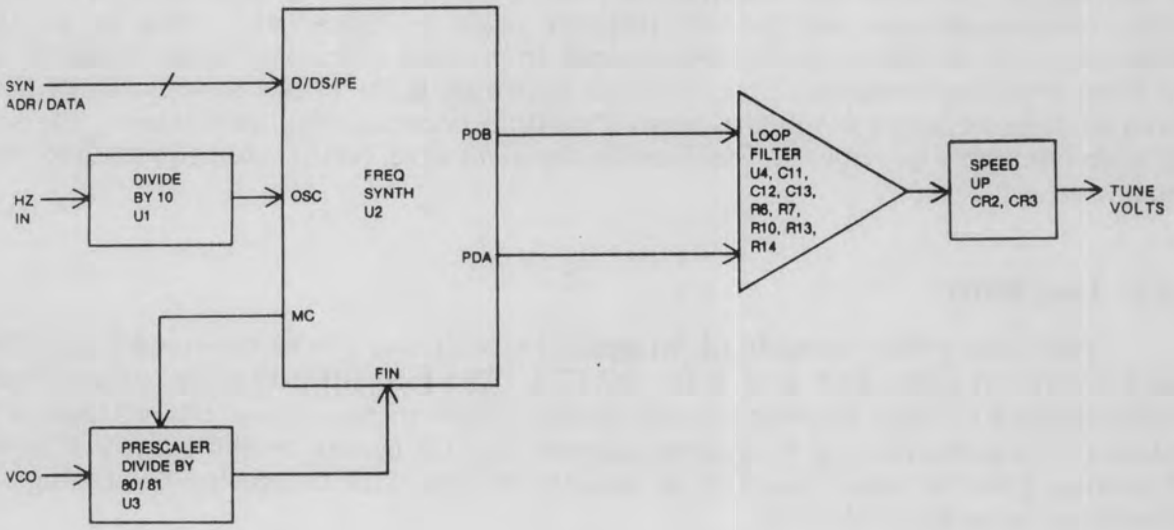


Figure 3-27. Auxiliary PLL/Phase Detector (A3A5) Block Diagram

3.4.3.4.1 Divider (U1)

The 50 MHz reference signal from the Time Base (A2) drives the input to the Divider (U1). The Divider (U1) is a fixed divide-by-10 counter which divides the 50 MHz reference signal by a factor of 10. The output of U1, 5 MHz, drives the oscillator input to the Frequency Synthesizer (U2).

3.4.3.4.2 **Prescaler (U3)**

Prescaler (U3) is driven by the Auxiliary VCO signal from the Auxiliary VCO (A6). The Prescaler (U3) is a two modulus prescaler with divide ratios of 80 or 81. The actual divide ratio is selected by the Frequency Synthesizer (U2). The output of U3 drives the F IN pin of the Frequency Synthesizer (U2).

3.4.3.4.3 **Frequency Synthesizer (U2)**

The Frequency Synthesizer (U2) is an integrated single package frequency synthesizer. Internally, U2 consists of a phase detector, a swallow counter, and a programmable divide-by-N, A, R counters. The overall divide ratio of U2 is determined by frequency tuning data words which are sent to U2 via the synthesizer address data bus. Internally, U2 compares the frequency at its oscillator input with the frequency at its F IN input. Any differences in these two frequencies produces a small DC voltage output at the DA and PDB outputs. At the start of a count cycle, U2 sets prescaler U3 for divide-by-81. Depending on the actual divide ratio requested by the SYN Address Data Bus U2, which continues to the end of the count cycle. In normal operation, the frequency at the oscillator input to U2 is exactly 5 MHz and the frequency at the FIN IN input is between 2.5 and 2.6 MHz. Internally, the 5 MHz Oscillator input is internal phase comparators. The FIN input is fed to the internal programmable divider which is set to produce a frequency very close to 4 kHz. The two 4 kHz frequencies are fed to the internal phase comparators. PDB is a standard phase/frequency detector driving a tristate output to produce a "coarse" error signal to enable fast switching between channels. This output is active until the phase error is within the PDA sample and hold phase detector window, when it's output becomes high impedance. The sample-and-hold phase detector provides a "fine" error signal to give further adjustment and hold the loop in lock.

3.4.3.4.4 **Loop Filter**

The Loop Filter consists of integrated circuit U4, diodes CR4 and CR5, CR2 and CR3, and R6, R10, C11, R7, R13, R14, C12, and C13. The loop filter receives pulses from PDB and samples from PDA and averages or integrates these to produce a DC voltage which is proportional to the difference in frequency between the U2 oscillator and the U2 F IN inputs. This DC voltage goes through the speed-up circuit CR3 and CR2 to become the tuning voltage which drives the Auxiliary VCO (A6).

3.4.3.5 **Auxiliary VCO (A3A6)**

Refer to **Figure 3-28**, Auxiliary VCO (A3A6) Block Diagram, and **Figure 6-19**, Auxiliary VCO Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-28**, the Auxiliary VCO consists of the following major circuit areas:

- VCO (Q1)
- Splitter/Buffer

3.4.3.5.1 **VCO (Q1)**

The VCO (Q1) is the oscillator gain element in the Auxiliary VCO and is tuned by resonant circuit DL1, C3, C5, C7, and varacter diodes CR1-CR4. Tuning voltage from the

Auxiliary PLL Phase Detector (A5) is applied to the junction of diodes CR1, CR2, and CR3, CR4. As the tuning voltage changes, the oscillation frequency of Q1 changes. This permits the Auxiliary PLL Phase Detector to force the VCO (Q1) to oscillate at the correct frequency. The output of Q1 drives the input of the Splitter Buffer.

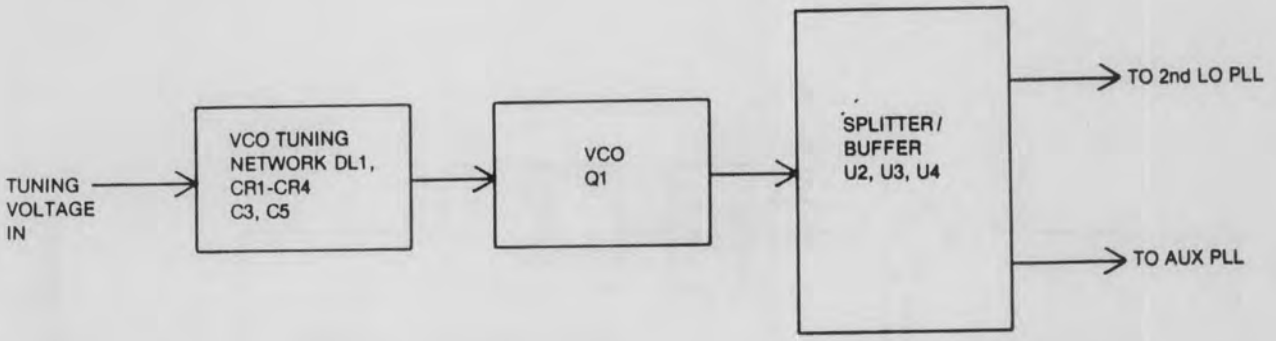


Figure 3-28. Auxiliary VCO (A3A6) Block Diagram

3.4.3.5.2 **Splitter Buffer**

The auxiliary VCO signal from Q1 is split into two outputs by the Hybrid Splitter (U2). Each output of U2 is amplified by a buffer amplifier. The Hybrid wideband integrated buffer amplifiers, U3 and U4, each have an overall gain of approximately 14 dB. The output from U3 goes through a matching pad to the 2nd LO/PLL (A4). The output from U4 goes through a matching pad to the Auxiliary PLL Phase Detector (A5).

3.4.3.6 **BFO Assembly (A3A7)**

Refer to **Figure 3-29**, BFO Assembly (A3A7) Block Diagram, and **Figure 6-20**, BFO Assembly Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-29**, the BFO consists of the following major circuit areas:

- Frequency Synthesizer (U9)
- Prescaler (U8)
- Loop Filter
- VCXO (Q2)
- Divider (U1A)
- Phase Detector Divider (U2)
- VCO (Q1)
- Mixer (U5)

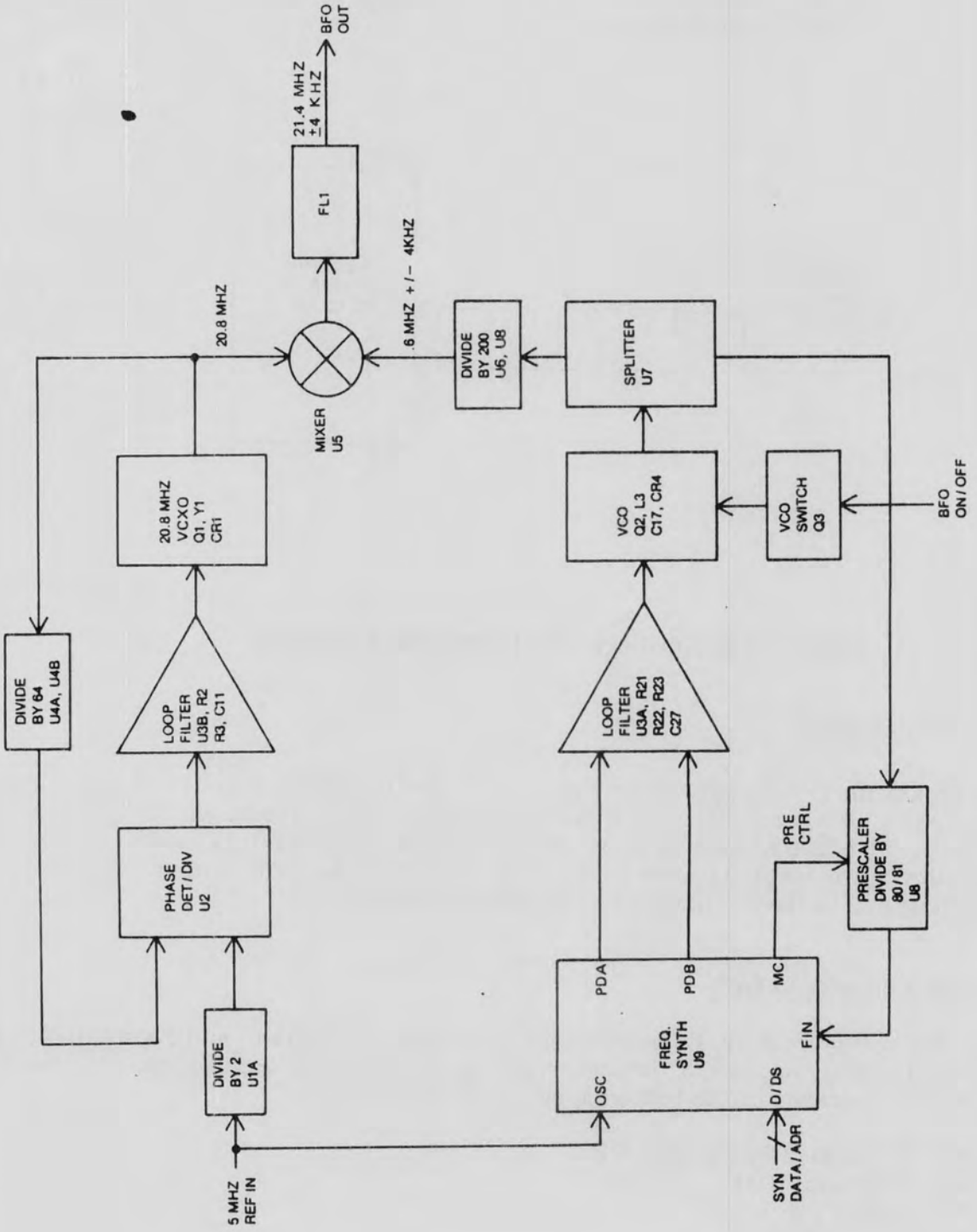


Figure 3-29. BFO Assembly (A3A7) Block Diagram

3.4.3.6.1 Frequency Synthesizer (U9)

Integrated single package Frequency Synthesizer internally, (U9) consists of a phase detector, a swallow counter, and a programmable divide-by-N, A, and R counter. The overall divide ratio of U9 is set by frequency data words which are sent to U9 via the SYN Data Address Bus. Synthesizer U9 compares the frequencies present at its oscillator input and F IN inputs. The frequency of the signal at the U9 oscillator input is 5 MHz, which is sent from the Auxiliary PLL Phase Detector (A5). The frequency at the U9 F IN input is the output of the Prescaler (U8) and is close to 5 MHz. The Frequency Synthesizer (U9) controls the actual divide ratio of the Prescaler (U8) via the MC output. The Synthesizer compares the oscillator/R and F IN/N frequencies and generates a DC voltage proportional to the difference of the two frequencies. In typical operation, the output at the U9 PDA is a series of very short pulses. If a large increase or decrease in frequency is requested via the SYN Data Address Bus, the U9 PDB output momentarily becomes large. This is done to force the VCO (Q2) to rapidly change frequency. The PDA and PDB outputs of U9 both drive the input of loop filter U3A.

3.4.3.6.2 Prescaler (U8)

The Prescaler (U8) is a two modulus prescaler with overall divide ratios of 80 or 81. The actual divide ratio is controlled by the MC output of the Frequency Synthesizer (U9). The input to the Prescaler drives the F IN input to U9.

3.4.3.6.3 Loop Filter

The Loop Filter consists of integrated circuits U3A, R22, R23, C27, and R21. The Loop Filter receives a series of short pulses from U9 and averages or integrates these pulses to produce an average DC voltage proportional to the difference in frequency between the U9 OSC input and the U9 F IN input. The output of loop filter U3A drives the varactor tuning diode in the VCO.

3.4.3.6.4 VCO (Q2)

The oscillator gain element in the VCO (Q2) is tuned by resonant circuits L3, C17, and tuning diode CR4. The VCO (Q2) is energized by switch Q3 which is enabled by a high +5 volt BFO "On" signal. The tuning voltage from the loop filter is applied to tuning diode CR4. As the tuning voltage from the loop filter changes, the oscillation frequency of Q2 changes. This permits the Frequency Synthesizer (U9) to force the VCO to oscillate at the correct frequency. The output of the VCO is split into two outputs by the Splitter (U7). One output is fed back to the input of the Prescaler (U8). The other output goes through a fixed divide-by-200 counter which consists of U6 and U1B. The U1B divided output drives the input to the Mixer (U5).

3.4.3.6.5 Divider (U1A)

The 5 MHz reference signal from the Auxiliary PLL Phase Detector (A5) drives the input to U1A, a divide-by-2 counter. The output of U1A 2.5 MHz drives the input to the Phase Detector Divider (U2).

3.4.3.6.6 Phase Detector Divider (U2)

The 2.5 MHz C1 input is divided by 100 by U2 to produce 25 kHz which is fed to the U2 phase comparator. The C2 input is near 325 kHz and is divided by 13 is U2 to produce a signal near 25 kHz which feeds the other input to the internal phase comparator. The output of Q2 at PC0 is typically a series of short pulses representing a very small DC voltage level. The PC0 output of U2 drives the input to the Loop Filter (U3B).

3.4.3.6.7 Loop Filter

The Loop Filter consists of integrated circuit U3B, R2, R3, and C11. U3B receives the short pulses from the Phase Detector Divider (U2) and averages or integrates these pulses to produce a small average DC voltage proportional to the differences in frequency between the U2 Phase Detector. The tuning voltage outputs from U3B drives tuning diode CR1.

3.4.3.6.8 VCXO (Q1)

The Oscillator gain element in the VCXO (Q1) is tuned by resonant circuits Y1, L1, CR1, and C5. The tuning voltage from Loop Filter (U3B) is applied to the Tuning Diode (CR1). In typical operation Q1 oscillates very close to 20.8 MHz as determined by crystal (Y1). As the tuning voltage from U3B changes, the actual oscillation frequency of Q1 changes slightly. This permits the Phase Detector Divider (U2) to force VCO Q1 to oscillate at exactly 20.8 MHz. The VCO output of Q1 consists of two outputs. The first output goes through a fixed divide-by-4 counter U4A and U4B. The divided output of this counter drives the C2 input of the Phase Detector Divider (U2). The second VCO output from Q1 drives the Mixer (U5).

3.4.3.6.9 Mixer (U5)

The Mixer (U5) is a double-balanced mixer with an overall conversion loss of approximately 6 dB. The Mixer (U5) mixes the 20.8 MHz signal from the VCO (Q1) with a 0.6 MHz $\pm$4 KHz signal from the Divider (U1B). The output of the Mixer (U5) is 21.4 MHz, $\pm$4 KHz. This output is filtered by the Bandpass Filter (FL1) and becomes the BFO output signal.

3.4.3.7 Reference Mixer (A3A8)

Refer to **Figure 3-30**, Reference Mixer (A3A8) Block Diagram, and **Figure 6-21**, Reference Mixer Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-30**, the Reference Mixer consists of the following major circuit areas:

- Doubler (T1 and U6)
- Mixer (U3 and U5)
- Divider and Buffer

3.4.3.7.1 Doubler (T1, U6)

The 50 MHz reference signal from the Time Base (A2) drives the input of the Doubler. The reference signal passes through the Transformer (T1) to the Broadband Integrated

Amplifier (U6), which is configured to function as a frequency doubler. The output of U6, 100 MHz, drives the input to the Mixer (U5).

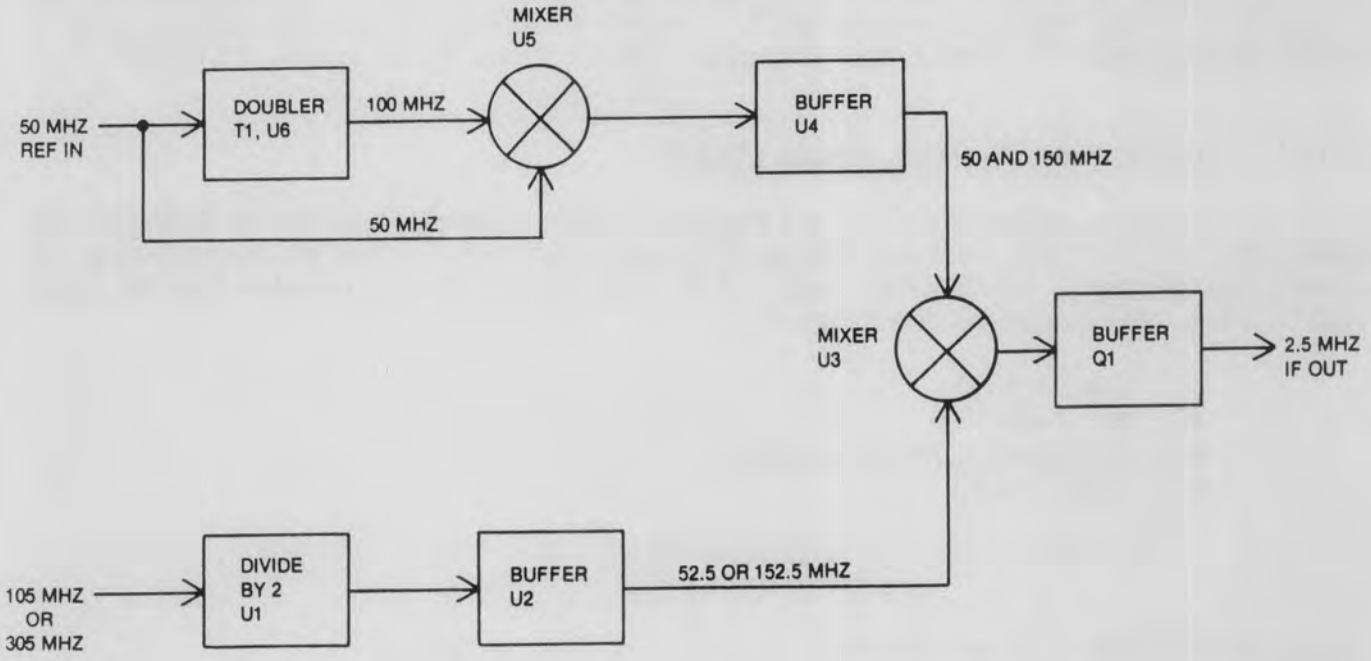


Figure 3-30. Reference Mixer (A3A8) Block Diagram

3.4.3.7.2 Mixer (U5)

The Mixer (U5) is a balanced mixer with an overall conversion loss of approximately 6 dB. Input #1 to the mixer comes directly from the 50 MHz reference signal from the Time Base (A2). Input #2 of the mixer is 100 MHz from the Doubler (U6). The output of the mixer (U5) is 50 MHz and 150 MHz with both signals present simultaneously. These two signals are amplified by the Buffer (U4), a wide band integrated amplifier with an overall gain of approximately 14 dB. The amplified 50 MHz and 150 MHz signals are then applied to the Mixer (U3).

3.4.3.7.3 Divider and Buffer

A 105-105.2 MHz or a 305-305.2 MHz VCO signal from the 2nd LO VCO (A3) is applied to the input of the Divider (U1) a fixed divide-by-2 counter. The output of U1, 52.6 MHz or 152.5-152.6 MHz is amplified by the Buffer (U2) a broadband integrated amplifier with an overall voltage gain of approximately 15 dB. The 52.6 or 152.5-152.6 MHz output from U2 drives the Mixer (U3).

3.4.3.7.4 Mixer (U3)

The Mixer (U3) is a balanced mixer with an overall conversion loss of approxiamtely 6 dB. The Mixer combines the 52.5-52.6 MHz signal from U2 with a 50 MHz signal from U4, or it combines the 152.5-152.6 MHz signal from U2 with the 150 MHz signal from U4. In either case, the result is a 2.5 MHz IF signal which appears at the output of U3 and is amplified by the Buffer Amplifier (Q1). Amplifier Q1 has an overall voltage gain of approximately 30 dB. The 2.5-2.6 MHz IF output from Q1 is sent to the 2nd LO/PLL (A4).

3.4.3.8 1st LO Phase Detector Divider (A3A9)

Refer to **Figure 3-31,** 1st LO Phase Detector Divider (A3A9) Block Diagram, and **Figure 6-22,** 1st LO Phase Detector Divider Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-31,** the 1st LO Phase Detector Divider Mixer consists of the following major circuit areas:

- Divider (U5)
- Prescaler (U2)
- Frequency Synthesizer (U1)
- Loop Filter

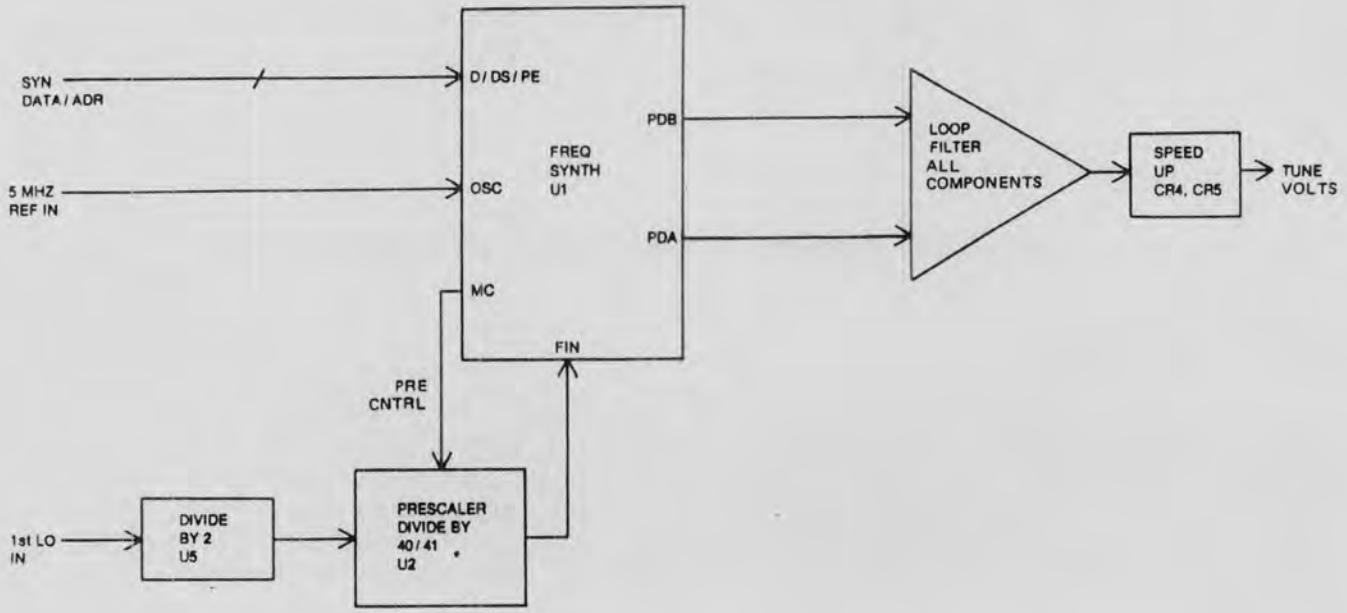


Figure 3-31. 1st LO Phase Detector Divider (A3A9) Block Diagram

3.4.3.8.1 Divider (U5)

The 1st LO signal from the 1st LO (A10) drives the input to the Divider (U5) a fixed divide-by-2 counter which divides the 1st LO input signal by a factor of 2. The Divider (U5) output drives Prescaler (U2).

3.4.3.8.2 **Prescaler (U2)**

The Prescaler (U2) is a two-modulus prescaler operating with divide ratios of 40 or 41. The actual divide ratio is controlled by the Frequency Synthesizer (U1). The divided output of U2 drives the F IN input to the Frequency Synthesizer (U1).

3.4.3.8.3 **Frequency Synthesizer (U1)**

The Frequency Synthesizer (U1) is an integrated single-package frequency synthesizer. Internally, U1 consists of a phase detector, a swallow counter, and a programmable divide-by-N counter. The overall divide ratio of U1 is set by frequency data words which are input to U1 via the SYN Data Address Bus. In normal operation, the 5 MHz reference signal is divided in U1 to produce 100 kHz which feeds the internal phase/frequency detectors. The prescaler U2 output is divided by U1 to produce a signal very close to 100 kHz which feeds the other phase/frequency detector input. The output of U1 at PDA is a series of short pulses representing a very low DC average voltage. If a large increase or decrease in frequency is requested via the SYN Data Address Bus, the output of U1 at PDB momentarily becomes very large. This large voltage forces the 1st LO VCO to change frequency rapidly. The PDA and PDB outputs of U1 both drive the input to the loop filter.

3.4.3.8.4 **Loop Filter**

The Loop Filter consists of integrated circuits U3, R7, C22, C6, R12, C7, R4, R11, and the speed-up circuits CR4 and CR5. The loop filter receives the short pulses from the Frequency Synthesizer (U1) and averages or integrates these pulses to produce an average DC voltage level proportional to the frequency difference between the phase detected inputs. This DC voltage from the loop filter is the 1st LO tuning voltage which is sent to the 1st LO (A10).

3.4.3.9 **1st LO Assembly (A3A10)**

Refer to **Figure 3-32**, 1st LO Assembly (A3A10) Block Diagram, and **Figure 6-23**, 1st LO Assembly Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-32**, the 1st LO Assembly consists of the following major circuit areas:

- Low VCO (Q4)
- High VCO (Q5)
- Combine Buffer

3.4.3.9.1 **Low VCO (Q4)**

The Low VCO (Q4) is tuned by resonant circuits DL1, C10, C11, tuning diodes CR1, CR3, and low/high band select circuits C12 and CR6. The Low VCO (Q4) oscillates in two separate frequency bands. The 1st frequency band is a low band, selected by the low band input signal, from U1, which turns on diode CR6 and shunts the resonant circuit with capacitor C12. The high band tuning range is selected when the low band signal is "Off", resulting in U1 reverse biasing CR6 and removing capacitor C12 from the circuit. The VCO is energized by the VCO select switches Q1 and Q3 when the low VCO signal is at 0 volts DC. The output of the Low VCO drives the input of the Combiner (U5).

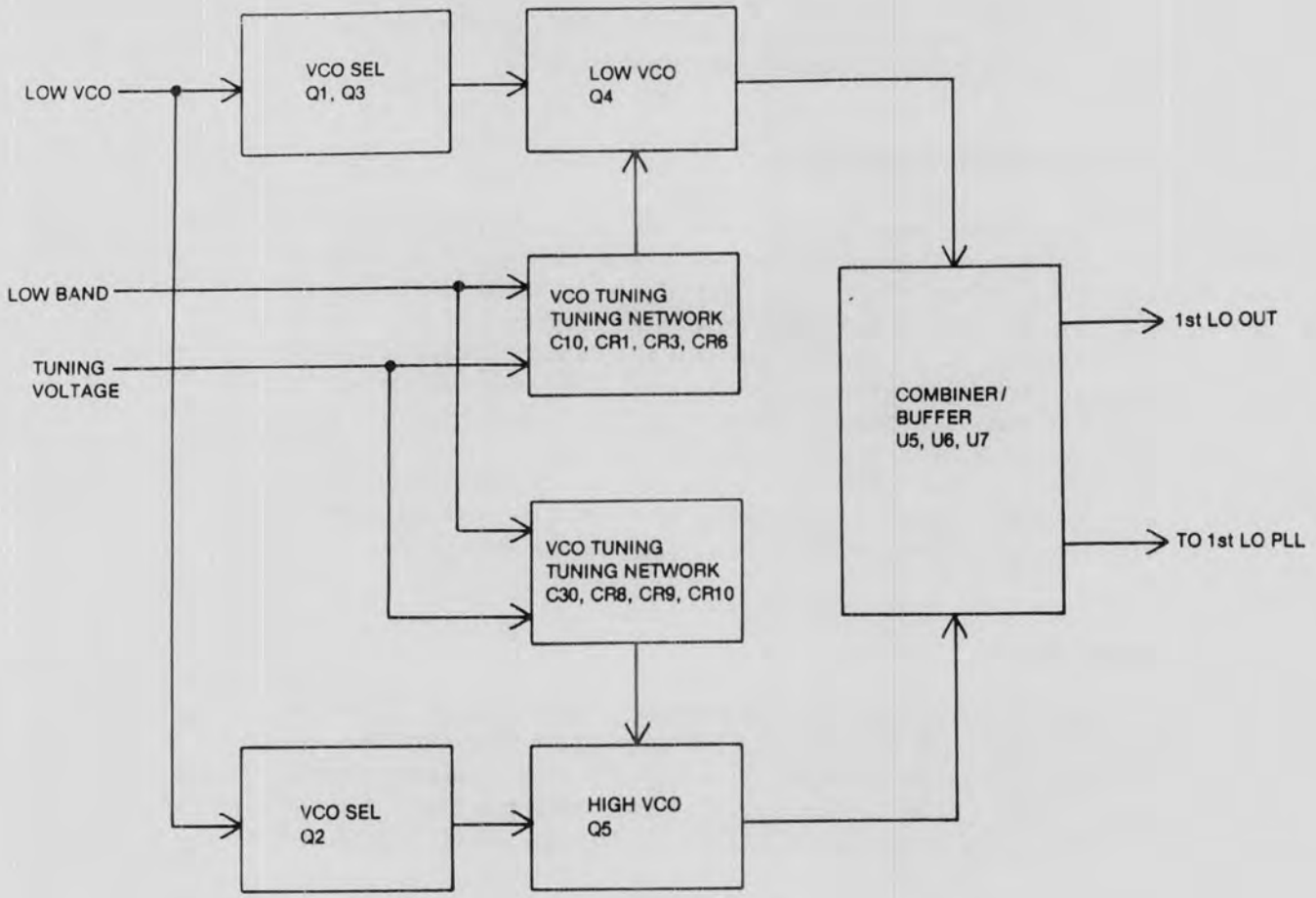


Figure 3-32. 1st LO Assembly (A3A10) Block Diagram

3.4.3.9.2 High VCO (Q5)

The oscillator gain element in the high VCO (Q5) is tuned by resonant circuits DL2, C31, C30, tuning diodes CR8, CR9, and low/high select network C32 and CR10. The High VCO oscillates in two separate frequency ranges. The 1st frequency range is selected by the low band select signal, from U1, which energizes CR10 and shunts the resonant circuit with capacitor C32. The high tuning range is selected when the loband signal is at 0 volts, causing U1 to turn off CR10 and remove C32 from the resonant circuit. The High VCO (Q5) is energized by VCO select transistor Q2, which is enabled when the lo VCO signal is at +5 volts DC. The high VCO output drives the input to the Hybrid Combiner (U5).

3.4.3.9.3 Combiner Buffer

The outputs of the low and high VCOs are both combined with the Hybrid Combiner (U5). Since only one of the two oscillators is active at any given time, the output of U5 is either the low VCO output or the high VCO input. The U5 output drives the Buffer Amplifier (U6), a broadband integrated amplifier with an overall voltage gain of approximately 14 dB. The output of U6 is split into two separate outputs by the Hybrid Splitter (U7). The first output goes directly out as the 1st LO output signal. The second output is fed back to the 1st LO phase detector divider as the VCO signal.

3.4.4 DIGITAL CONTROL (A4)

The following paragraphs describe the circuit operation of the Digital Control Modules.

3.4.4.1 Extended CPU

Refer to **Figure 3-33**, Extended CPU (A4A3) Block Diagram, and **Figure 6-27**, Extended CPU Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-33**, the Extended CPU consists of the following major circuit areas:

- CPU Chip
- Bidirectional Data Latch
- Address Latch
- Address Decoders
- ROM
- RAM

3.4.4.1.1 CPU Chip

The NSC-800 CPU Chip controls a 16-bit address bus and an 8-bit data bus. The lower eight bits of address are in common with the data bus (AD0-AD7). A 4.9152 MHz crystal and oscillator circuit (U1) set the clock rate for the Extended CPU. The CPU Chip also outputs the RD, WR, IO/M, ALE and other control signals necessary for I/O control. It performs instructions which are obtained from the control program contained in the program memory (ROM). These instructions are routed to the instructions register of the Extended CPU and then carried out during instruction cycles. Each instruction cycle specifies the functions to be performed by the Digital Control.

The Extended CPU addresses memory through the address latch (AD0-AD7) for the lower eight bits of address and directly from the address bus for the upper eight bits of the address (A8-A15). Data is transferred between the CPU chip and either a memory or the Digital Control Data Bus via the data latch.

3.4.4.1.2 Bidirectional Data Buffer

The Data Buffer is a bidirectional transceiver. The direction of data flow is controlled by the RD line from the Extended CPU. When the RD line is high, the data buffer

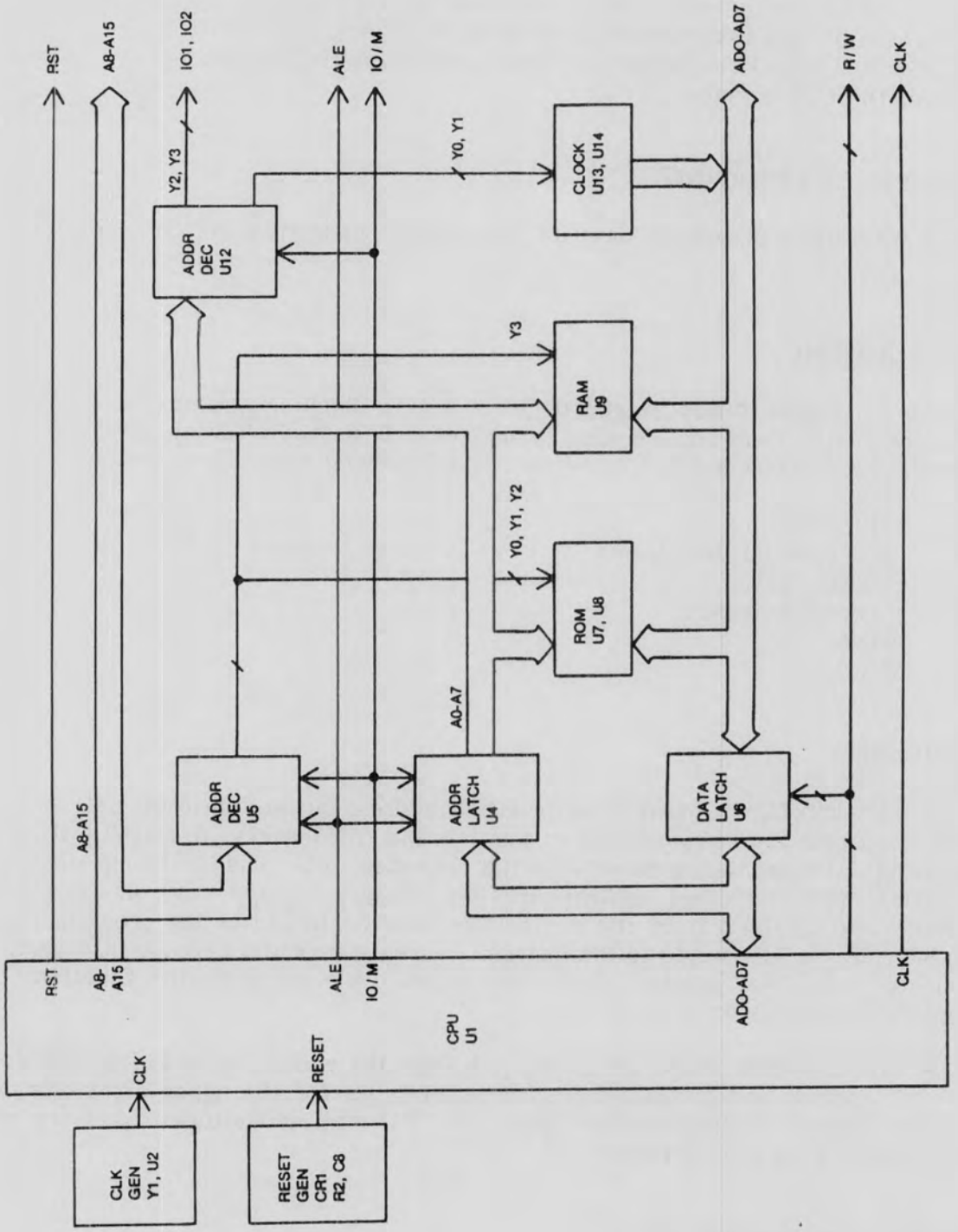


Figure 3-33. Extended CPU (A4A3) Block Diagram

transfers data from the Extended CPU to the Address/Data Bus (AD0-AD7). When the RD line is low, the data buffer transfers data from the Address/Data Bus to the CPU.

3.4.4.1.3 Address Latch

The Address Latch is an 8-bit latch which captures and holds an address from the Extended CPU while a specific operation is being performed. The latch outputs are used to address the lower eight bits of ROM and RAM. The Extended CPU outputs an address on the AD0-AD7 bus and follows by bringing the ALE line momentarily low. This transfers the data on the D inputs of the latch to the Q outputs, to form the address bus A0-A7. The latched address output drives the address inputs of the ROM and RAM.

3.4.4.1.4 Address Decoder #1

The Address Decoder (#1) is used by the Extended CPU to select either ROM or RAM. The Address Decoder consists of a 3 to 8-line decoder (U5) which is addressed by bits A13, A14, and A15 of the CPU Address Bus. U5 is enabled by the ALE and the IO/M control lines from the Extended CPU. The range of hex addresses used by the decoder are from 0000 (U5-Y0) to E000 (U5-Y4). The following list shows the decoder outputs and their functions:

U5-Y0, Y1	—	Select ROM U7
U5-Y2	—	Select ROM U8
U5-Y3	—	Select RAM U9

3.4.4.1.5 Address Decoder (#2)

The Address Decoder (#2) is used by the Extended CPU to select the optional Time/Calendar Clock (U14) and to define two external operations via I/O 1 and I/O 2. The address decoder consists of a 3 to 8-line decoder (U12) which is addressed by bits A0 to A7 of the CPU Address Bus. The Time/Calendar Clock (U14) is enabled by the IO/M control line from the Extended CPU. The range of hex addresses used by the decoder are from 00D4 (U14-Y0) to 00D7 (U14-Y3). The following list shows the decoder outputs and their functions:

U14-Y0, Y1	—	Select Clock/Calendar (U14)
U14-Y2	—	I/O 1 Output
U14-Y3	—	I/O 2 Output

3.4.4.1.6 ROM

The ROM consists of two type 27C256 EPROMs. Each contains 32K 8-bit words for a total of 64K X 8 of program memory. The operating control program is stored in ROM. The ROM is addressed by A0-A7 from the address latch and A8-A14 from the Extended CPU for a total input address range of 0000 to 7FFF for each ROM. The ROM output, D0-D7, is placed on the receiver data bus. In typical operation, a 14-bit address is presented to the ROM from the Extended CPU. When a valid address is present, the CPU momentarily brings the RD line low and the addressed memory data is available at the ROM output to be placed on the data bus. The ROM outputs are present on the bus only while the RD line is low.

3.4.4.1.7 **RAM**

The RAM consists of one 6264 memory chip containing 8K 8-bit words. The RAM is addressed by A0-A7 from the address latch and A8-A12 from the Extended CPU for a total input address range of 0000 to 1FFFF. The RAM is selected by the Y3 output of the Decoder (U5). In typical operation, the RAM inputs data when the WR line is low and outputs data when the WR line is high. RAM data input/output, D0-D7, is interfaced across the Digital Control Data Bus (AD0-AD7).

3.4.4.2 **Front Panel Interface (A4A6)**

Refer to **Figure 3-34**, Front Panel Interface (A4A6) Block Diagram, and **Figure 6-29**, Front Panel Interface Schematic Diagram as aids in understanding the following description. As shown in **Figure 3-34**, the Front Panel Interface consists of the following major circuit areas:

- Address Latch (U5)
- Address Latch (U6)
- Address Decoder (U8)
- Data Latch (U9)
- Keyboard Encoder (U10, 11)
- Tuning Encoder (U12, 13)
- Analog Multiplexer (U2)
- A/D Converter (U4)

3.4.4.2.1 **Address Latch**

Address Latch (U6) is an 8-bit latch which holds an address coming from the Extended CPU via the CPU Address Data Bus while a specific operation is being performed. The AD0-AD7 outputs from the CPU are not valid for an entire bus cycle, so the address latch must capture and hold this address while it is on the bus. In a typical operation, the CPU outputs an address data bus which is presented to the input of U6. The CPU then brings the ALE line momentarily low which transfers the address from the D inputs of U6 to the Q outputs. The Q1, Q2, and Q3 outputs from U6, representing the first three bits of address A0, A1, and A2, drive the A, B, and C address inputs of the Address Decoder (U8). U6 outputs Q4 and Q5 go to the LCD display DS1 as display control data. The Q7 and Q8 outputs of U6, representing address bits 6 and 7, are used to enable the G2 A and B inputs of the Address Decoder (U8).

3.4.4.2.2 **Address Latch (U5)**

The Address Latch (U5) is an 8-bit flip-flop which functions as an address latch. This latch is used to capture and hold an address coming from the CPU via the address data bus while a specific operation is being performed. The AD0-AD7 outputs from the CPU are not valid for an entire bus cycle, so the Address Latch (U5) must capture and hold this address while it is valid on the address bus. In a typical operation, the Extended CPU outputs an address to the address data bus which is then presented to the D inputs of the Address Latch (U5). The Extended CPU then brings the U8Y1 output **(see paragraph 3.4.4.2.3 below)** momentarily low which clocks the D inputs of U5 directly to the Q outputs. Only three of the Q outputs are used, Q6, Q7, and Q8. Q6 and Q7 are used to select the input to the Analog Multiplexer (U2). Q8 is used to initiate the operation of the Analog-to-Digital Converter (U4).

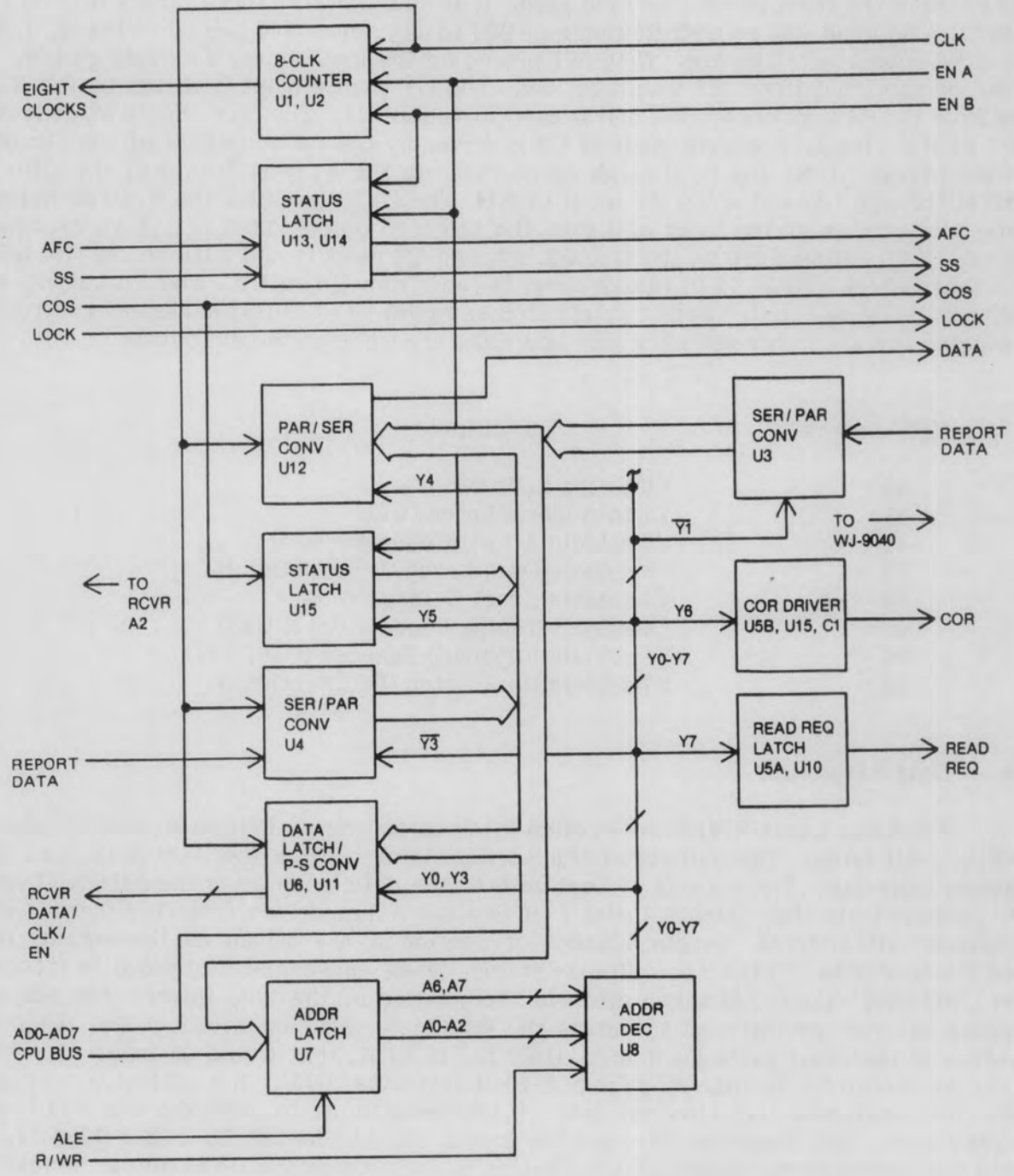


Figure 3-34. Front Panel Interface (A4A6) Block Diagram

3.4.4.2.3 Address Decoder (U8)

The Address Decoder (U8), a 3-bit to 8-bit decoder, is used to define internal operations within the front panel interface card. It is addressed by three binary bits on inputs A, B, and C. The input has an address range of 000 to 111. With 000 placed on the A, B, and C inputs, the Y0 output would go low. With 001 placed on the input lines, Y1 would go low. With 111 placed on the input lines, Y7 would go low. The G1 enable input is driven by the RD and WR lines from the CPU through U7D, and is used to enable U8. The G2B enable input is driven by bit Q7 of U6. The G2A enable input of U8 is driven by the Q8 output bit of U6. To utilize the Address Decoder (U8), the CPU sends an address via the AD0-AD7 lines of the CPU data bus, latch it through U6, and on to the input of U8. The CPU then uses the Read or Write line to transfer the address at the input of U8 to the selected output Y0-Y7. As an example, to activate the U8Y0 output 0000 on the Q1, Q2, Q3, and Q4 outputs and 0010 on the Q5, Q6, Q7, and Q8 outputs which equals 40 in hexadecimal is sent from U6 to U8. The Y0 output, which goes low upon being selected, passes through U7B and goes to LCD DS1 as display control data. The U8 outputs and their corresponding Hex addresses are summarized as follows:

HEX Address	U8 Outputs
40	Y0 to the LCD DS1
41	Y1 to Address Latch (U5)
42	Y2 selects A to D Converter (U4)
43	Y3 selects Data Latch (U9), section B
44	Y4 selects Reset C Timer (U14)
45	Y5 selects Tuning Encoder (U12, U13)
46	Y6 selects Keyboard Encoder (U10, U11)
47	Y7 selects Data Latch (U9), section A

3.4.4.2.4 Data Latch (U9)

The Data Latch (U9) is a 2-section latch consisting of Section A, a 4-bit latch, and Section B, a 4-bit latch. The outputs of the Section A latch drive the AD0-AD3 lines of the CPU Address Data Bus. The outputs of Section B of the data latch drive the AD4-AD7 lines of the CPU Address Data Bus. Inputs 1 and 2 of Section A are driven from the outputs of the Tuning Encoder (U12, U13). Inputs 3 and 4 of Section A are driven by the outputs of the Keyboard Encoder (U10, U11). The outputs of the tuning encoder are intended to inform the Extended CPU that change has taken place in the position of the tune wheel. The outputs of the keyboard encoder are intended to inform the Extended CPU that a change has taken place in the status of the front panel keyboard. Only the B input, that would be input #1, of U9 is used. It is connected to the Busy line from A-to-D Converter (U4). In a typical operation, the Extended CPU examines the 4 output bits of U9, Section A, by bringing the U8Y7 output momentarily low. This transfers the data on inputs A1-A4 directly to bits AD0-AD3. The Extended CPU examines the output of U9, Section B, by bringing the U8Y3 output momentarily low. This transfers input B1 directly to bit AD4 of the CPU Address Data Bus.

3.4.4.2.5 Keyboard Encoder (U10, U11)

The Keyboard Encoder is comprised of two keyboard matrix decoders, U10 and U11. Decoder U10 is used to define 4 of the 8 column signals that come from the front panel

keyboard. Decoder (U11) is used to define the remaining 4 column signals that come from the keyboard and also to define the 4 row signals which are sent to the keyboard. Decoders U10 and U11 are both internally clocked by 3 running oscillators and in normal operation, scan the front panel keyboard for a momentary contact closure. This contact closure would result in a closure between one column signal and one row signal. Decoders U10 and U11 would then process this unique contact closure and would assign a unique 8-bit word to represent the switch that was closed. The CPU signal that a contact closure has taken place by outputting a signal to the Data Latch (U9) which would then, in turn, transfer that data to the Extended CPU, informing the Extended CPU that a keyboard contact closure has taken place. The Extended CPU would then bring the U8Y6 output momentarily low, which would force U10 and U11 to transmit the 8-bit data word, representing the unique switch that was closed, to the CPU address Data Bus. This would transfer the data word back to the Extended CPU.

3.4.4.2.6 Tuning Encoder

The Tuning Encoder consists of a dual flip-flop (U12) and a buffer (U13). U12, Section A, is driven from one section of the tuning wheel; flip-flop U12B is driven from the second part of the tuning wheel. These two inputs from the tuning wheel consist of square wave pulses, phase shifted by 90 degrees. The phase shift is necessary to inform the Extended CPU of the direction of rotation of the tuning wheel. The tuning wheel inputs drive the clock inputs to U12A and U12B. The output of U12A drives the A2 input of U9. The output of U12B drives the A1 input of U9. In normal operation, rotation of the tuning wheel results in a series of square wave pulses at the output of U12A and a steady High or a Low output from U12B, depending on direction of rotation of the tuning wheel. The outputs of U12, A and B, are examined by the Extended CPU through data latch U9 using the U8Y7 output. In typical operation, the Extended CPU brings the U8Y7 output momentarily low, which transfers the U12 outputs through U9 to the CPU Address Data Bus. If the data has not changed from the previous reading, the Extended CPU takes no further action on the tuning encoder. If the Extended CPU senses that a change in the tuning encoder data has taken place, the Extended CPU processes the changed data and then brings the U8Y5 output low, which clears and resets the outputs of U12, A and B.

3.4.4.2.7 Analog Multiplexer (U2)

The Analog Multiplexer (U2) is a 4-input by 1-output analog multiplexer. The 4 inputs to U2 are selected by address inputs A and B. Inputs A and B are driven by the Q6 and Q7 outputs of the Address Latch (U5). Input 0 of U2 is driven by the signal strength voltage from the IF Demodulator (A2). Input 2 is driven by the select AFC voltage from the IF Demodulator (A2). Input 3 of U2 is driven by the squelch audio input voltage from IF Demodulator (A2). When the address input at A and B is 00, input 0 is connected to the output. When the address input is 10, input 1 is connected to the output. When the address input is 01, input 2 is connected to the output. When the address input is 11, input 3 is connected to the output. The U2 output goes through buffer U1 and drives the analog input of the A/D Converter (U4).

3.4.4.2.8 A/D Converter (U4)

The A/D Converter (U4) accepts an analog input voltage from U2 and converts it to an equivalent 8-bit data word with a range of 0 to 255. The A/D Converter (U4) is selected by the U8Y2 output and its conversion cycle is initiated by the U5Q8 output. In a typical

operation, the Extended CPU selects 1 of the 4 analog inputs of U2 via U5Q6 and Q7 outputs. This analog output passes through U2 to the input of U4. The Extended CPU then uses the U5Q8 output to perform an analog-to-digital conversion within A4. At the conclusion of the conversion cycle, the Extended CPU brings the U8Y2 output momentarily low, which transfers converted 8-bit data word from U4 directly to the CPU Address Data Bus.

3.4.4.3 Receiver/EF Interface (A4A5)

Refer to **Figure 3-35**, Receiver/EF Interface (A4A5) Block Diagram, and **Figure 6-28**, Receiver/EF Interface Schematic Diagram, as aids in understanding the following description. As shown in **Figure 3-35**, the Receiver/EF Interface consists of the following major circuit areas:

- Address Latch (U7)
- Address Decoder (U8)
- Data Latch (U6)
- Serial-to-Parallel Converters (U3, U4)
- Parallel-to-Serial Converters (U11, 12)
- Eight Clocks Counter, (U1, U2)
- Status Latches, (U13, 14)

3.4.4.3.1 Address Latch (U7)

Address Latch (U7) is an 8-bit latch which holds an address coming from the CPU Address/Data Bus while a specific operation is being performed. The AD0-AD7 outputs from the Extended CPU are not valid for an entire bus cycle, so the address latch must capture the address from the Extended CPU while it is present on the bus. In a typical operation, the Extended CPU outputs an address to the AD0-AD7 bus and follows this by bringing the ALE line momentarily low. This action transfers the address from the D inputs of U7 to the Q outputs. The address, which is latched at the Q outputs, remains until a new address is sent to U7 from the Extended CPU. The A0, A1, and A2 outputs from U7 drive the address inputs to U8. The A6 and A7 outputs of U7 drive the enable inputs to U8.

3.4.4.3.2. Address Decoder (U8)

The Address Decoder (U8) is used to select specific internal operations within the receiver interface card. Address Decoder (U8) is a 3-bit to 8-bit decoder addressed by 3 binary bits on inputs A, B, and C. The input address has a range of 000 to 111. The outputs of the Address Decoder (U8) are Y0-Y7, normally high with the selected output being low. With 000 placed on the A, B, and C inputs, the Y0 output would go low. With 001 on the A, B, and C inputs, Y1 would go low. With 111 on the A, B, and C inputs, the Y7 output wold go low. The G2B enable input is driven by the RD and WR lines from the CPU Control Bus and it is used to enable U8. The G1 and G2A enable inputs of U8 are driven by the A6 and A7 address outputs from U7. To utilize U8, the CPU sends an address over the AD0-AD7 lines on the CPU Address Data Bus, latch it through address latch U7, and on to the Address Decoder (U8). When a valid address is input to U8, the CPU brings either the Read or the Write line momentarily low, which selects Y0-Y7 on the U8 outputs. All 8 outputs of U8 are used to define internal operations in the receiver interface card. As an example, to activate the U8Y0 output, 0000 on the A0-A3 outputs of U7 and 0001 on the A4-A7 outputs of U7 are sent to U8 from U2. This address from

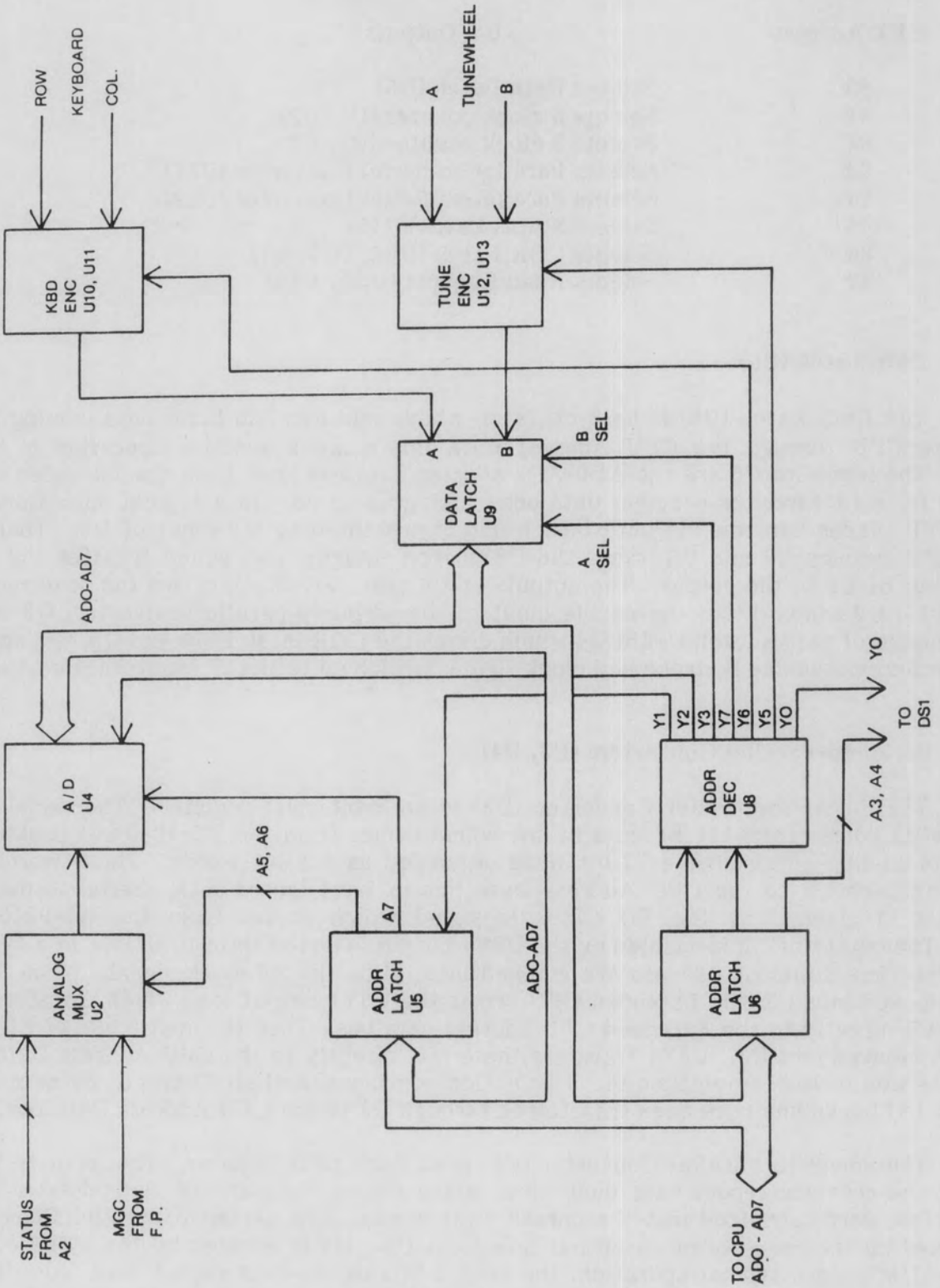


Figure 3-35. Receiver/EF Interface (A4A5) Block Diagram

U2 to U8 equals a hexadecimal address of 80. The hex addresses corresponding to U8 outputs and the destination of each U8 output is summarized as follows:

HEX Address	U8 Outputs
80	Selects Data Latch (U6)
81	Selects 8 clock counter (U1, U2)
82	Selects 8 clock counter (U1, U2)
83	Selects Parallel-to-Serial Converter (U11)
84	Selects Parallel-to-Serial Converter (U12)
85	Selects Status Latch (U15)
86	Selects COR Latch (U5B, U15, Q1)
87	Selects Read Request (U5A, U10)

3.4.4.3.3 Data Latch (U6)

The Data Latch (U6) is an 8-bit latch which captures and holds data coming from the Extended CPU through the CPU Address Data Bus while a specific operation is being performed. The inputs to U6 are the AD0-AD7 address data bus lines from the Extended CPU. The outputs from U6 form the receiver data bus which goes to A2. In a typical operation, the Extended CPU places data on the data bus, which is presented to the input of U6. Then the Extended CPU through U7 and U8 brings the U8Y0 momentarily low, which transfer the data from the input of U6 to the output. The outputs of U6 are: Q1, which drives the read request latch, U5AU10; Q2 which drives the enable input to the serial-to-parallel converter; Q3 which drives the enable of status latch U13B; Q4 which drives the COR latch U5B; and Q5, Q6, and Q7 (the receiver address enable B strobe and clock signals) which go to the IF Demodulator (A2).

3.4.4.3.4 Serial-to-Parallel Converters (U3, U4)

The Serial-to-Parallel Converter (U3) is an 8-bit shift register. The serial data input line to U3 comes from the EF data in line which comes from the WJ-9040 I/O backplane. The EF Data In line consists of a 72-bit word organized as 9 8-bit words. These words are transferred through U3 to the CPU Address Data Bus in 8-bit increments. Serial-to-parallel converter U3 is clocked by the ED Clock In signal which comes from the WJ-9040 I/O backplane. The output of U3 is enabled by the U8Y1 output inverted through U10B. In a typical operation, the first 8 bits of EF data are clocked into U3 by the EF clock signal. When 8 bits have been clocked into U3, the Extended CPU brings the U8Y1 output low, which transfers the 8 bits from U3 directly to the Extended CPU address data bus. Then the next 8 bits of EF data are similarly clocked into U3. U8Y1 transfers these bits directly to the CPU Address Data Bus after 8 of the bits have been clocked in. This action continues until all 72 bits of EF data from the WJ-9040 I/O backplane have been transferred through U3 to the CPU Address Data Bus.

The Serial-to-Parallel Converter (U4) is an 8-bit shift register. The input to U4 is driven from the receiver report data input line, which comes from the IF Demodulator (A2). This is a 72-bit word organized into 9 separate 8-bit words. The Serial-to-Parallel Converter (U4) is clocked by the receiver clock output line from U6. U4 is enabled by the U8Y3 output inverted by U10C. In a typical operation, the first 8 bits of receiver report data from the IF Demodulator (A2) are clocked into U4 by the receiver clock out signal from U6. When 8 of the receiver report data bits have been clocked into U4, the Extended CPU brings the U8Y3 output

low, which transfers the 8 bits in U4 directly to the CPU Address Data Bus. This action continues in 8-bit increments until all 72 bits of receiver report data have been transferred from the IF Demodulator (A2) to the CPU Address Data Bus.

3.4.4.3.5 Parallel-to-Serial Converters (U11, U12)

The Parallel-to-Serial Converter (U11) is an 8-bit shift register driven by 8 bits from the CPU Address Data Bus and its serial output forms the receiver data output line which goes to the IF Demodulator (A2). The receiver data output line is a 72-bit serial data word which completely defines all operating parameters required by the IF Demodulator (A2) to operate the receiver. The Parallel-to-Serial Converter (U11) is clocked by the receiver clock output line from U6 and is enabled by the Y3 output of U8. In a typical operation, the Extended CPU places an 8-bit data word on the CPU Address Data Bus which is presented to the input of U11. These 8 bits are clocked through U11 by the receiver clock output of U6 and these 8 bits appear in serial format at the output of U11 and are transferred to the IF Demodulator (A2) via the receiver data out line. When all 8 of the bits from the Extended CPU have been clocked through U11, the Extended CPU then places the second 8-bit data word on the address data bus and these bits are similarly clocked through U11 by the receiver clock output line. This action continues until all 9 of the data words from the Extended CPU have been clocked through U11 and transferred to the IF Demodulator (A2).

The Parallel-to-Serial Converter (U12) is an 8-bit shift register. The inputs to U12 are driven from the CPU Address Data Bus. The output of U12 is the EF report data out line, which goes to the WJ-9040 I/O backplane. This line reports the status of the various circuits within the receiver to the IOM108 on the EFR100. U12 is clocked by the EF clock input line from the WJ-9040 I/O backplane. U12 is enabled by the U8Y4 output. In a typical operation, the Extended CPU places an 8-bit data word on the address data bus which is presented to input of U12. These 8 bits are then clocked through U12 by the EF clock input line. When all 8 of these bits have been clocked through U12, and transferred to the WJ-9040 I/O backplane, the Extended CPU places the second 8-bit word on the address data bus which is then similarly clocked through U12 by the EF clock in signal. This continues until all 9 of the 8-bit words from the Extended CPU have been clocked through U12.

3.4.4.3.6 Eight Clocks Counter (U1, U2)

The Eight Clocks Counter (U1, U2) is used to signal the Extended CPU when 8 successive clock signals have been received via the EF clock in line from the WJ-9040 I/O backplane. The inputs to the eight clocks counter are the EF clock in, the enable A, and the enable B lines of the WJ-9040 I/O backplane. The output of the eight clocks counter is the eight clocks line, normally high, which goes to the Extended CPU. In typical operation, the IOM108 on the EFR100 brings the EF address enable B line high. This clears the status of the eight clocks counter. The IOM108 then sends clock signals via the EF clock in line. When 8 successive clock signals have been received, the eight clocks counter responds by bringing the eight clocks output low. This signals the Extended CPU that 8 EF clock signals have been received. The Extended CPU then clears the eight clocks counter by bringing the U8Y1 output momentarily low. This sets the eight clocks counter to start a new 8 clock count cycle. Every 8 clock pulses from the EF clock in line causes the eight clocks output to go low. The Extended CPU uses this eight clocks output as an interrupt signal to coordinate the transfer of serial and parallel data through U3 and U12.

3.4.4.3.7 Status Latches (U13, U14)

The Status Latch (U13) consists of two sections, U13A and U13B. Each section is a double-pole, single-throw CMOS switch. The switch is open when the enable input is low and the switch is closed when the enable input is high. U13A is enabled by the EF address enable B line from the WJ-9040 I/O backplane. U13B is enabled by the Q3 output of the Data Latch (U6). U13B is wired to select either AFC or FSK tuning input from the IF Demodulator (A2). This selected signal passes through U13B, is buffered by U14B, and goes into Switch (U13A). Switch U13A also passes the signal strength voltage from the IF Demodulator (A2). This voltage is buffered by U14A and passed to the input of U13A. In a typical operation the IOM108 reads the output of U13A by bringing the EF address enable B line momentarily high. This closes both sections of the switch transferring the voltage at the inputs of the switch to the addressed AFC out and addressed signal strength out, both of which go to the IOM108 via the WJ-9040 I/O backplane.

3.4.4.3.8 COR Latch (U5B, U15, Q1)

The COR Latch consists of flip-flop U5B and buffer U15 and Q1. The input to U5B is driven from the U6Q4 output. U5B is clocked by the U8Y6 output. When COR is not activated, the U5B output is low and transistor Q1 is not energized. When the COR threshold is exceeded to activate COR, the Extended CPU brings the U6Q4 output high and then clocks U5B via the U8Y6 output. This brings the U5B output high, which energizes transistor Q1, clamping the COR output line to ground.

3.4.4.3.9 Read Request (U5A, U10)

Flip-flop U5A's input is driven from the U6Q1 output and is clocked by the U8Y7 output. The output of U5A is inverted through U10H to become the addressed read request output. This is a command which goes to the IF Demodulator (A2) whenever the Extended CPU wants A2 to report back its current status. In a typical operation, when the Extended CPU desires to generate a read request, it brings the U6Q1 output high. It then clocks U5A via the U8Y7 output. This brings the U5 output high, is inverted by U10H to become low, and is sent to IF Demodulator (A2) as a read request.

3.4.4.4 Remote I/O Interface (A4A2) Option

Refer to **Figure 3-36** Remote I/O Interface (A4A2) Block Diagram, and **Figure 6-26**, Remote I/O Interface Schematic Diagram as aids in understanding the following description. As shown in **Figure 3-36**, the Remote I/O Interface consists of the following major circuit areas:

- UART
- Data Buffer
- J/O Data Latch
- Address Latch
- Address Decoder

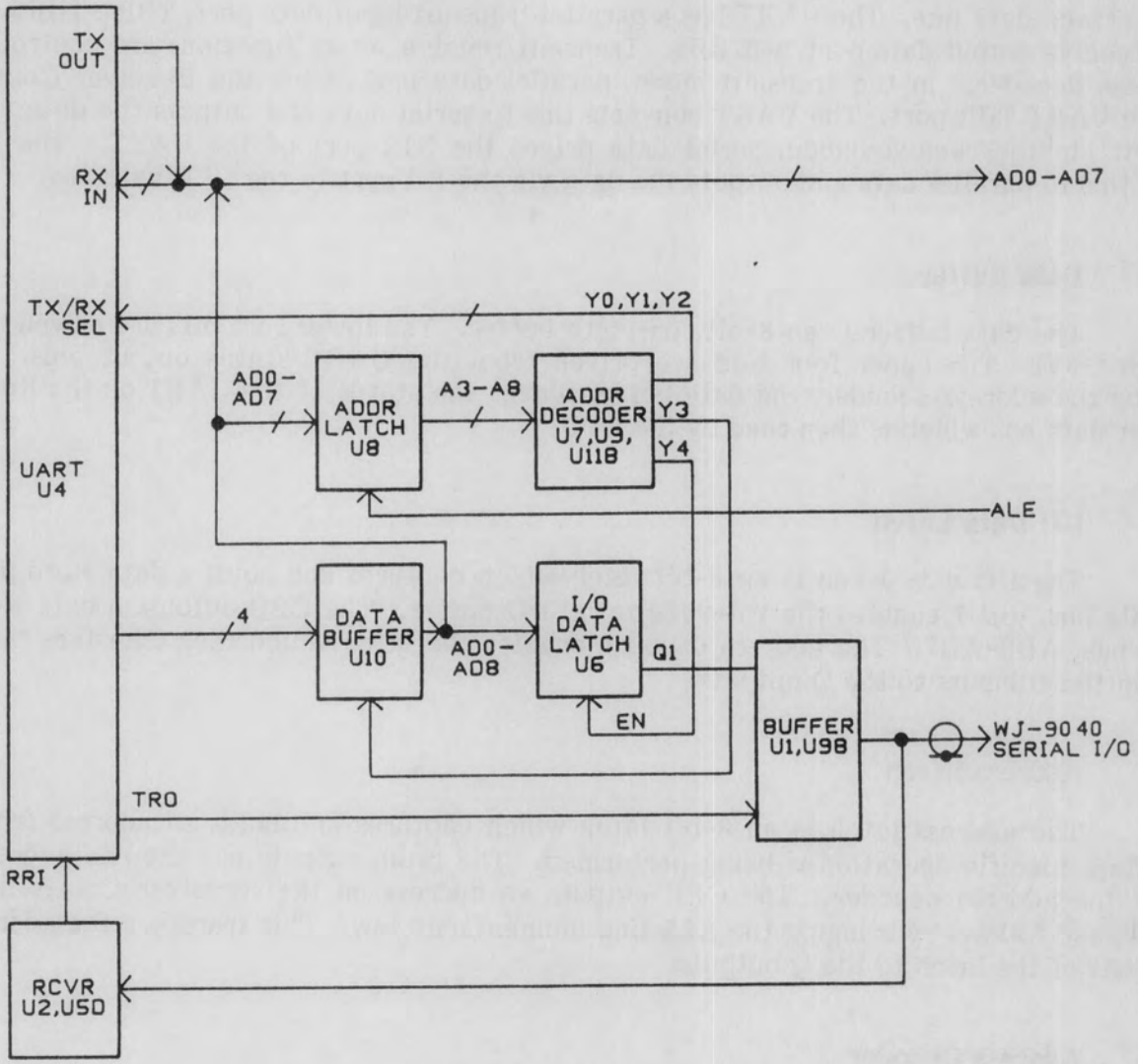


Figure 3-36. Remote I/O (A4A2), Block Diagram

3.4.4.4.1 UART

The UART (Universal Asynchronous Receiver Transmitter) is a bidirectional transmitter/receiver interfacing between the Receiver Controller data bus and the WJ-9040 serial interface data line. The UART has a parallel transmit input data port, TBR1-TBR8, and a parallel receive output data port, RB/RB8. Transmit/receive select functions are controlled by the address decoder. In the transmit mode, parallel data input from the Receiver Controller drives the UART TBR port. The UART converts this to serial data and outputs the data via the TRO port. In the receive mode, serial data drives the RRI port of the UART. The UART converts this to parallel data and outputs the data via the RB port to the CPU data bus.

3.4.4.4.2 Data Buffer

The data buffer is an 8-bit, tri-state buffer. The lower four bits are driven from a logic high (+5V). The upper four bits are driven from the UART status output pins. When enabled by the address decoder, the data buffer places the status of the UART on the Receiver Controller data bus which is then read by the CPU.

3.4.4.4.3 I/O Data Latch

The I/O data latch is an 8-bit latch which captures and holds a data word present on the data bus. Bit 1 enables the WJ-9040 serial I/O buffer. The CPU outputs a data word on the data bus, AD0-AD7. The address decoder enables the latch which then transfers the data word from the D inputs to the Q outputs.

3.4.4.4.4 Address Latch

The address latch is an 8-bit latch which captures and holds an address from the CPU while a specific operation is being performed. The latch outputs are used to address the inputs of the address decoder. The CPU outputs an address on the Receiver Controller bus, AD0-AD7, and follows by bringing the ALE line momentarily low. This transfers the address on the D inputs of the latch to the Q outputs.

3.4.4.4.5 Address Decoder

The address decoder is used by the CPU to select the particular I/O operation to be performed. The address decoder consists of a 3-to-8 line decoder. The decoder input is addressed by the address latch. When a valid address is present at the decoder input, the IOM line is brought high, activating the addressed decoder output. The range of hex addresses used by the decoder are from 80 (U7-Y0) to 88 (U7-Y7). The following list shows the decoder outputs and their functions.

Y0 — UART receive enable
Y1 — UART transmit enable
Y2 — UART control register
Y3 — UART Status Enable
Y4 — I/O Data Latch Enable
Y5 — N.U.
Y6 — N.U.
Y7 — N.U.

SECTION IV

MAINTENANCE

4.1 GENERAL

This section contains maintenance procedures for the WJ-8628-4 VHF/UHF Receiver. Included are preventive maintenance procedures, performance verification tests and troubleshooting.

4.2 MODULE ACCESS

The receiver is a highly compact unit consisting of four major assemblies attached to the front panel and an interconnecting cable. Internal access to each of the assemblies may be gained by removing the interconnecting cable on the receiver rear panel, removing the eight (8) screws holding the rear panel bracket in place and then detaching each assembly from the front panel. The cover plate(s) on each module may then be removed to provide internal access to the circuitry.

4.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of visual inspection and cleaning. The procedures described in this paragraph are designed to improve the receiver's reliability by preventing breakdowns and uncovering potential malfunctions before they impair operation of the unit. **Table 4-1** is a recommended schedule for performing preventive maintenance procedures.

Table 4-1. Preventive Maintenance Schedule

Procedure	Interval	Comments
Cleaning	60 days	Interval variable depending on operating environment.
Inspection for damage	60 days	Interval variable depending on operating environment and equipment use.
Performance tests	180 days	Interval variable depending on operating environment and equipment use.
Adjustment/Alignment	---	Adjustment/Alignment keyed to results of Performance Tests.

4.3.1 VISUAL INSPECTION

Many potential or existing faults can be detected by making a visual inspection of the unit. For this reason, a complete visual inspection should be made on a routine basis and whenever the receiver is inoperative. At a minimum, the unit should be inspected for the following items:

1. Inspect the cover, enclosure and front panel for condition of finish and panel markings.
2. Inspect for dents, punctures, or warped areas.
3. Inspect for loose or missing screws or washers.
4. Inspect the receptacles for condition of pins, contacts, and mountings.
5. Inspect the internal components for signs of deterioration, discoloration or charring. Check for melted insulation and damaged, cracked, or broken components.
6. Inspect the printed circuit boards for damaged tracks, loose connections, corrosion, or other signs of deterioration.
7. Inspect the PC connectors, interface connectors, and chassis wiring for excessive wear, looseness, misalignment, corrosion, or other signs of deterioration.

4.3.2 CLEANING

Perform cleaning to remove accumulated dust and other contamination, and to ensure trouble-free operation.

CAUTION

Avoid the use of chemical cleaning agents containing benzene, toluene, zylene, acetone or similar solvents. These chemicals may damage the plastics used in the receiver.

1. Exterior - Dust the cabinet with a soft cloth or a small soft-bristled paint brush. Dirt clinging to the cabinet may be removed with a clean lint-free cloth dampened with a mild detergent and water solution. Avoid using abrasive cleaners. They will scratch the finish.

2. Interior - Dust in the interior of the unit should be removed before it builds up enough to cause arcing and short circuits during periods of high humidity. Dust is best removed by dry, low-pressure air. Dirt on surfaces may be removed with a soft-bristled paint brush or a clean, lint-free cloth dampened with a mild detergent and water solution. Use a cotton tipped applicator for cleaning in narrow spaces and on the circuit boards.

4.4 RECEIVER PERFORMANCE TESTS

4.4.1 GENERAL

The Performance Tests outlined in this paragraph define the minimum performance standards which ensure adequate receiver functioning in all detection modes, gain modes and IF bandwidths. The tests should be used for initial inspection, preventive maintenance checks, troubleshooting and post-repair performance verification.

4.4.2 MINIMUM PERFORMANCE STANDARDS

Table 4-2 summarizes the parameters tested by the Performance Tests. To be acceptable for use, the receiver should meet or exceed all minimum performance standards listed.

4.4.3 TEST EQUIPMENT REQUIRED

Table 4-3 lists the test equipment required for performance testing of the unit. Equivalent types may be used.

4.4.4 PROCEDURE GUIDELINES

1. Read each test procedure thoroughly before attempting to perform the test.
2. Configure test equipment as shown in the test setup figures for each test.
3. Set the test equipment and receiver controls as directed for each test.
4. Allow a minimum of 30 minutes warm-up time for test equipment prior to performing any of the tests.
5. Unless otherwise directed, acceptable tolerances are ±3 dB for signal levels and ±20% for AC and DC supply voltages.
6. The tests should be performed in the sequence given. If a malfunction is noted, refer to **paragraph 4.4.5** for troubleshooting.

Table 4-2. Minimum Performance Standards

Parameter to be Tested	Performance Standard
Front Panel Control Status	All local mode functions are operational (**paragraph 2.4.3.2**)
RF/IF Gain, RF IN to IF OUT	IF BW / GAIN 10 kHz +83 dB 20 kHz +80 dB 50 kHz +76 dB 100 kHz +73 dB 200 kHz +70 dB 500 kHz +66 dB 1 MHz +63 dB 2 MHz +60 dB 4 MHz +57 dB
Video Output in AM Mode	350 mVrms minimum into 75 ohms with rated sensitivity input and 50% AM at 400 Hz.
Video Output in FM Mode	350 mVrms minimum into 75 ohms with rated sensitivity input and 30% IF BW FM deviation at 400 Hz.
Video Output in CW Mode	350 mVrms minimum into 75 ohms with rated sensitivity input.
AGC Control Range	Rated input to -7 dBm with less than 6 dB output change.
Manual Gain Control Range	100 dB, minimum
Frequency Tuning Accuracy	±510 Hz at 510.0000 MHz

Table 4-3. Test Equipment Required

Instrument Type	Recommended Instrument
Signal Generator	HP-8640B
RF Voltmeter	Boonton 92B
Frequency Counter	HP-5303A
Digital Voltmeter	Fluke 8100A
Oscilloscope	HP-180C
EFR100 frame extender cable (2)	WJ part # 271408

4.4.5 KEYBOARD/DISPLAY FUNCTION TEST

1. Connect the receiver to a DC power source such as the EPS100 Power Supply in the EFR100 Equipment Frame.
2. Energize the DC power source.
3. Rotate the front panel DISPLAY ADJUST control from maximum counterclockwise to maximum clockwise. The LCD display should change from totally invisible to almost completely dark (total illumination).
4. Set the DISPLAY ADJUST Control for a comfortable viewing intensity with all display characters clearly illuminated.
5. Turn the BACKLIGHT Switch to the ON position. Verify the illumination of the LCD module.
6. Deenergize and then reenergize the DC power source.
7. Verify that the initialization routine is correctly executed as explained in **paragraph 2.4.3.1.**
8. Repeatedly press the upper/lower case arrow keypad and observe the shift arrow on the LCD display toggle between upper and lower case. Set the arrow for lower case functions.
9. Press the 0 and the EXEC keypads. The display should indicate 0 in the CHAN/ADDR window and EXEC in the CONTROL STATUS window.
10. Verify the local mode entry procedures in **paragraphs 2.4.3.2.1** through **2.4.3.2.6.**
11. Deenergize the DC power source.

4.4.6 RECEIVER IF GAIN TEST

1. Connect the receiver as shown in **Figure 4-1.**
2. Energize the DC power source.
3. Using the receiver front panel controls and keypad, set the receiver to the following parameters:
   a. Detection Mode - AM
   b. Bandwidth - BW #1
   c. Gain Mode - Manual

d. RF Gain - Maximum clockwise

e. Tuned Frequency - 40.1000 MHz

4. Set the signal generator output frequency to 40.1000 MHz. Refer to **Table 4-4** and set the signal generator output level as shown for BW #1.

5. Set the RF voltmeter to the -20 dBm range. The meter should indicate -20 dBm ±2 dBm.

6. Repeat steps 3, 4 and 5 for tuned frequencies of 105.1000 MHz, 210.1000 MHz and 390.1000 MHz. The output level for each frequency should be -20 dBm ±2 dBm.

7. Use the IF BW keypad to step the receiver through all available bandwidths. For each bandwidth, refer to **Table 4-4** and set the signal generator output level as shown for that bandwidth. The output level for each bandwidth should be -20 dBm ±2 dBm.

8. Deenergize the DC power source.

Table 4-4. Receiver Gain Test Input Level

	kHz						MHz		
Bandwidth	10	20	50	100	200	500	1.0	2.0	4.0
Input Level (dBm)	-105	-102	-98	-95	-92	-88	-85	-82	-79

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

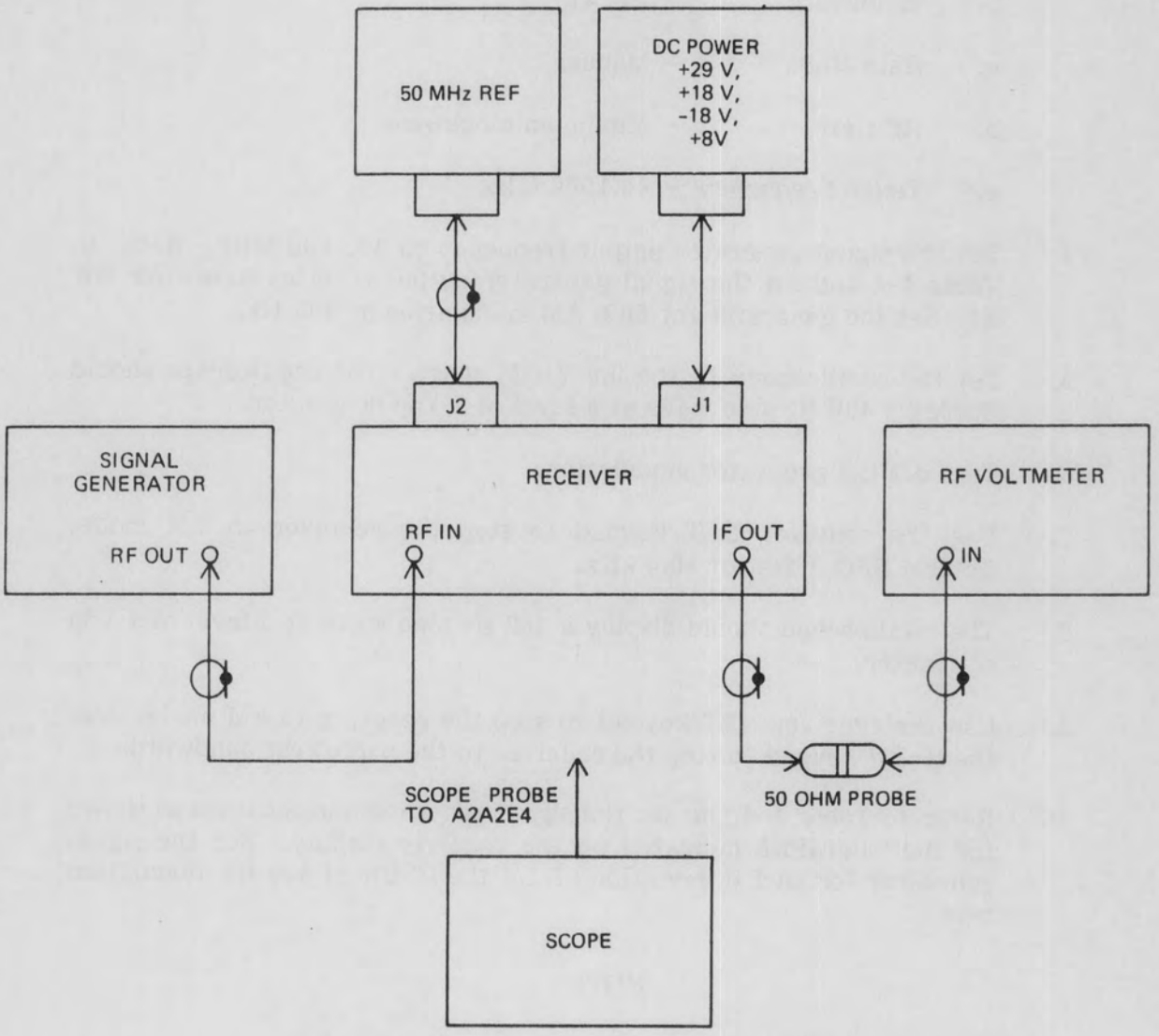


Figure 4-1. IF Gain Test Equipment Setup

4.4.7 DETECTION MODE TEST (AM, FM AND CW)

1. Connect the receiver as shown in **Figure 4-2.**
2. Energize the DC power source.
3. Using the receiver front panel controls and keypad, set the receiver to the following parameters:
   a. Detection Mode - AM
   b. Bandwidth - BW #1
   c. Gain Mode - Manual
   d. RF Gain - Maximum clockwise
   e. Tuned Frequency - 40.1000 MHz
4. Set the signal generator output frequency to 40.1000 MHz. Refer to **Table 4-4** and set the signal generator output level as shown for BW #1. Set the generator for 50% AM modulation at 400 Hz.
5. Set the oscilloscope to the 0.5 V/CM range. The oscilloscope should display a 400 Hz sine wave at a level of 1 Vpp or greater.
6. Turn off the generator modulation.
7. Use the receiver DET keypad to step the receiver to CW mode. Enter a BFO offset of -0.4 kHz.
8. The oscilloscope should display a 400 Hz sine wave at a level of 1 Vpp or greater.
9. Use the receiver DET keypad to step the receiver to FM mode. Use the IF BW keypad to step the receiver to the narrowest bandwidth.
10. Refer to **Table 4-4** and set the signal generator output level as shown for the bandwidth indicated on the receiver display. Set the signal generator for an FM deviation of 1/3 the IF BW at 400 Hz modulation rate.

NOTE

If the signal generator cannot deviate far enough (no modulation) tune to a frequency equal to ±1/3 the IF BW slected. The DC video output should move ±0.5 VDC.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

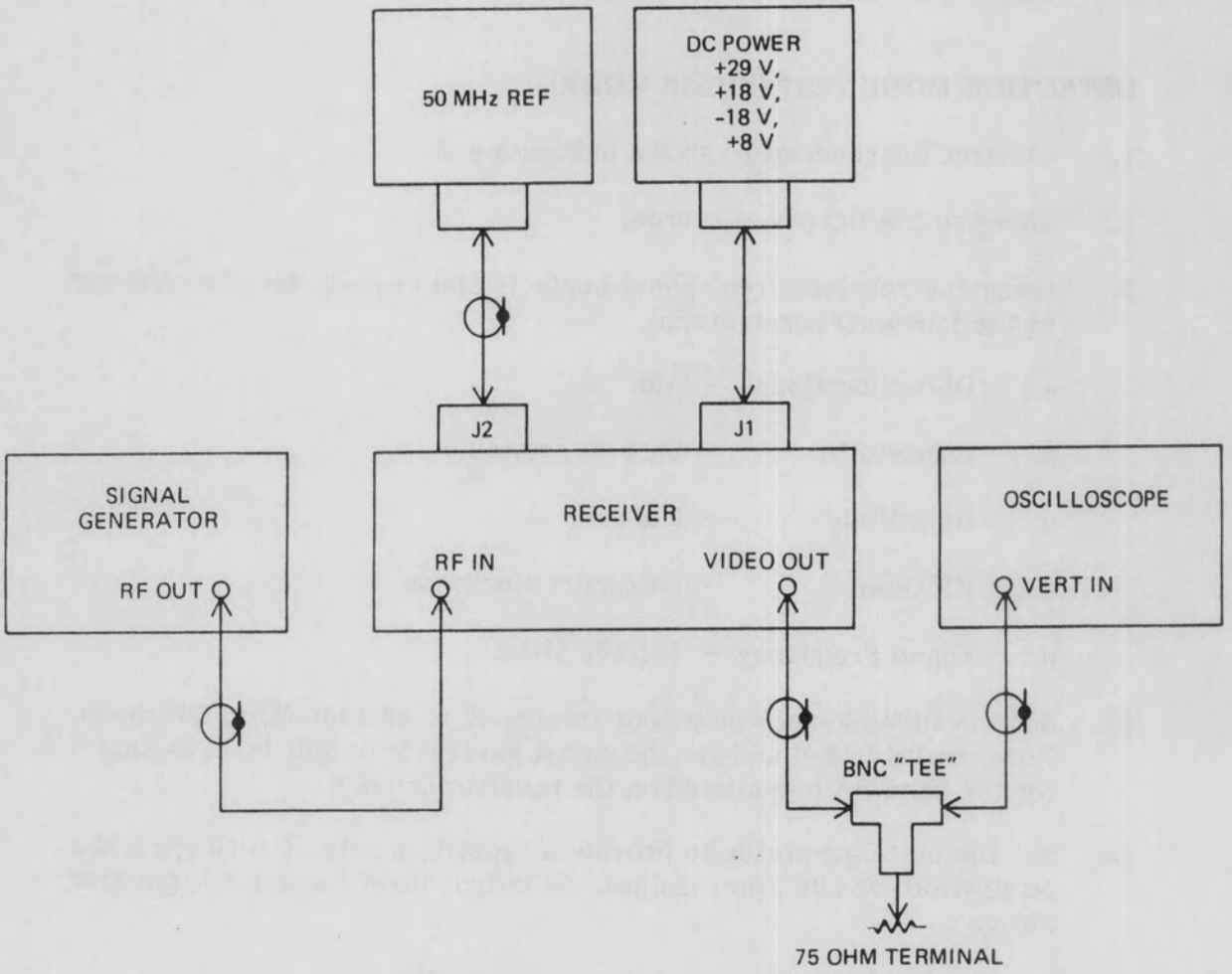


Figure 4-2. AM, CW, FM Detection Mode Test Equipment Setup

11. The oscilloscope should display a 400 Hz sine wave at a level of 1 Vpp or greater.

12. Use the receiver IF BW keypad to step the receiver through the remaining IF bandwidths. For each bandwidth, refer to **Table 4-4** and set the signal generator output level as shown for the bandwidth indicated on the receiver display. Set the signal generator FM deviation to 1/3 the IF bandwidth indicated on the receiver display.

13. The oscilloscope should display a 400 Hz sine wave at a level of 1 Vpp or greater for each bandwidth position.

14. Deenergize the DC power source.

4.4.8 DETECTION MODE TEST (PULSE MODE)

1. Connect the receiver as shown in **Figure 4-3.**

2. Energize the DC power source.

3. Using the receiver front panel controls and keypad, set the receiver to the following parameters:

   a. Detection Mode - AM

   b. Bandwidth - Largest available

   c. Gain Mode - Manual

   d. RF Gain - Maximum clockwise

   e. Tuned Frequency - 40.1000 MHz

4. Set the signal generator output frequency to 40.1000 MHz, CW mode. Refer to **Table 4-4** and set the signal generator output level as shown for the bandwidth indicated on the receiver display.

5. Set the pulse generator to provide a repetition rate of 1000 pps and a pulse width of 100 µsec. Adjust the output level for a 1.0 V positive pulse.

6. Set the signal generator to AM pulse external.

7. The oscilloscope should display a square wave pulse with a level of 1 V peak minimum.

8. Deenergize the DC power source.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

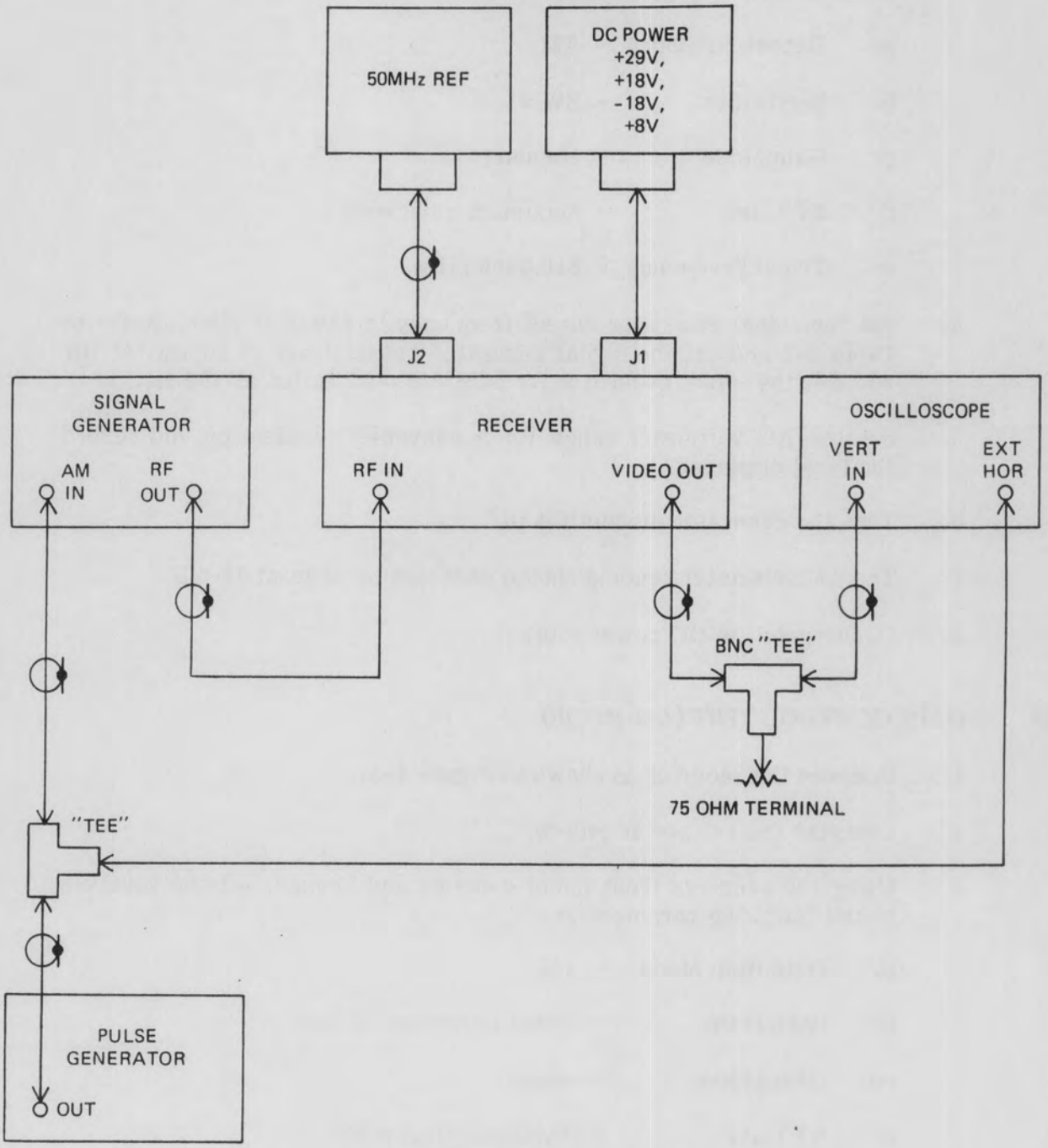


Figure 4-3. Pulse Mode Detection Test Setup

4.4.9 SIGNAL-TO-NOISE RATIO TEST

1. Connect the receiver as shown in **Figure 4-4.**
2. Energize the DC power source.
3. Using the receiver front panel controls and keypad, set the receiver to the following parameters:
   a. Detection Mode - AM
   b. Bandwidth - BW #1
   c. Gain Mode - Manual
   d. RF Gain - Maximum clockwise
   e. Tuned Frequency - 510.0000 MHz
4. Set the signal generator output frequency to 510.0000 MHz. Refer to **Table 4-4** and set the signal generator output level as shown for BW #1. Set the signal generator for 50% AM modulation at 400 Hz.
5. Set the AC voltmeter range for a convenient indication and record the level displayed.
6. Turn the generator modulation off.
7. The AC voltmeter reading should decrease by at least 10 dB.
8. Deenergize the DC power source.

4.4.10 GAIN CONTROL TEST (AM MODE)

1. Connect the receiver as shown in **Figure 4-5.**
2. Energize the DC power source.
3. Using the receiver front panel controls and keypad, set the receiver to the following parameters:
   a. Detection Mode - AM
   b. Bandwidth - Select narrowest IF BW
   c. Gain Mode - Manual
   d. RF Gain - Maximum clockwise
   e. Tuned Frequency - 40.1000 MHz

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

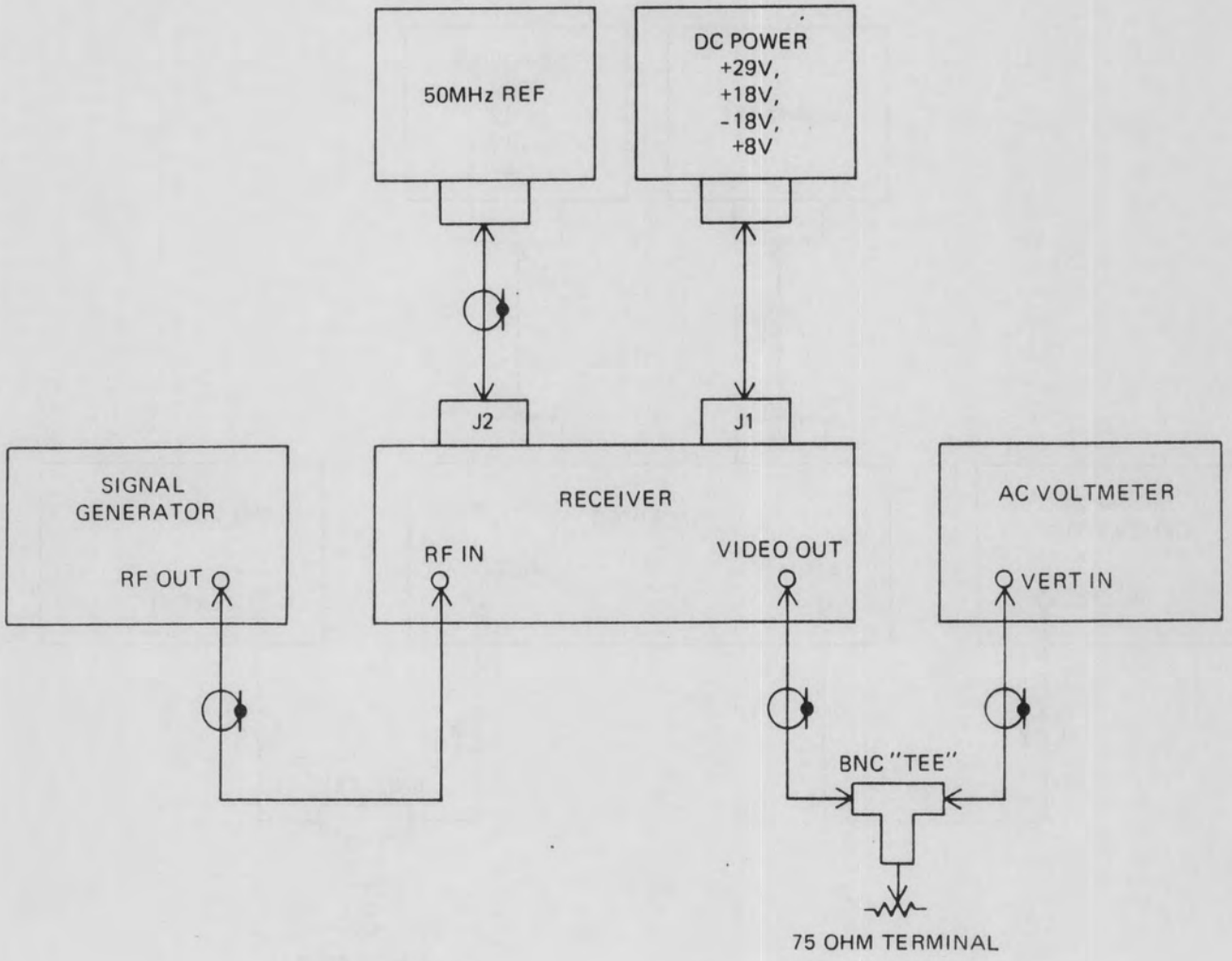


Figure 4-4. SNR Test Equipment Setup

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

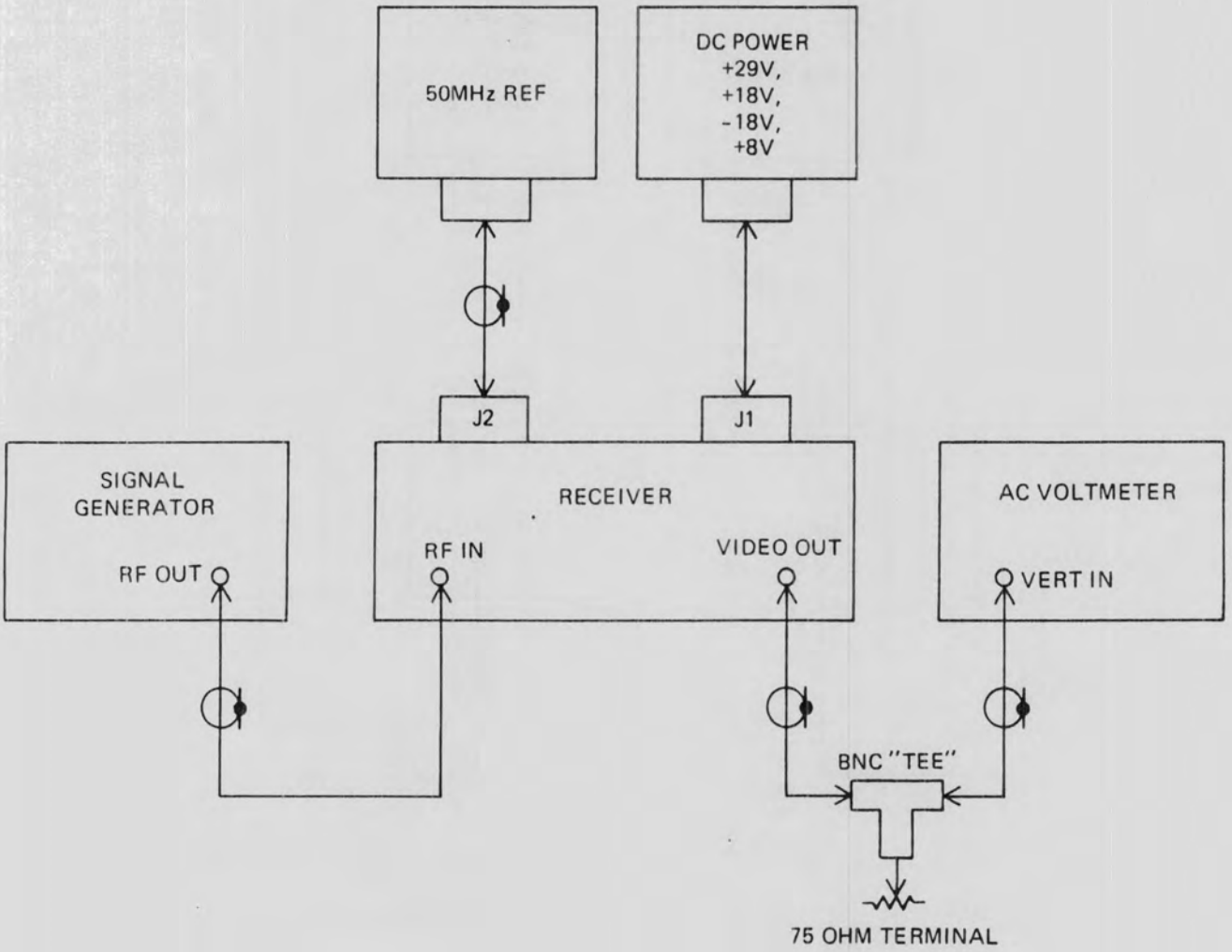


Figure 4-5. Gain Control (AM Mode) Test Equipment Setup

4. Set the signal generator output frequency to 40.1000 MHz. Refer to **Table 4-4** and set the signal generator output level as shown for the bandwidth indicated on the receiver. Set the signal generator for 50% AM modulation at 400 Hz.

5. Set the AC voltmeter range for a convenient indication and record the level displayed.

6. Increase the signal generator level in 10 dBm increments until -10 dBm is reached. For each 10 dBm increase, rotate the RF GAIN control counterclockwise until the AC voltmeter indicates the level recorded in step 5 above.

7. Decrease the signal generator output level back to the level set in step 4 above.

8. Use the receiver GAIN keypad to step the receiver to the AGC gain mode. Record the level displayed on the AC voltmeter.

9. Increase the signal generator output level to -10 dBm. The AC voltmeter reading should increase no more than 6 dB above the level recorded in step 8 above.

10. Deenergize the DC power source.

4.4.11 GAIN CONTROL TEST (PULSE MODE)

1. Connect the receiver as shown in **Figure 4-6.**

2. Energize the DC power source.

3. Using the receiver front panel controls and keypad, set the receiver to the following parameters:

   a. Detection Mode - Pulse

   b. Bandwidth - Largest available

   c. Gain Mode - AGC

   d. Tuned Frequency - 40.1000 MHz

4. Set the signal generator output frequency to 40.1000 MHz, CW mode. Refer to **Table 4-4** and set the signal generator output level as shown for the bandwidth indicated on the receiver display.

5. Set the pulse generator to provide a repetition rate of 1000 pps and a pulse width of 100 µsec. Adjust the output level for a 1.0 V positive pulse.

6. Set the signal generator to AM pulse external.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

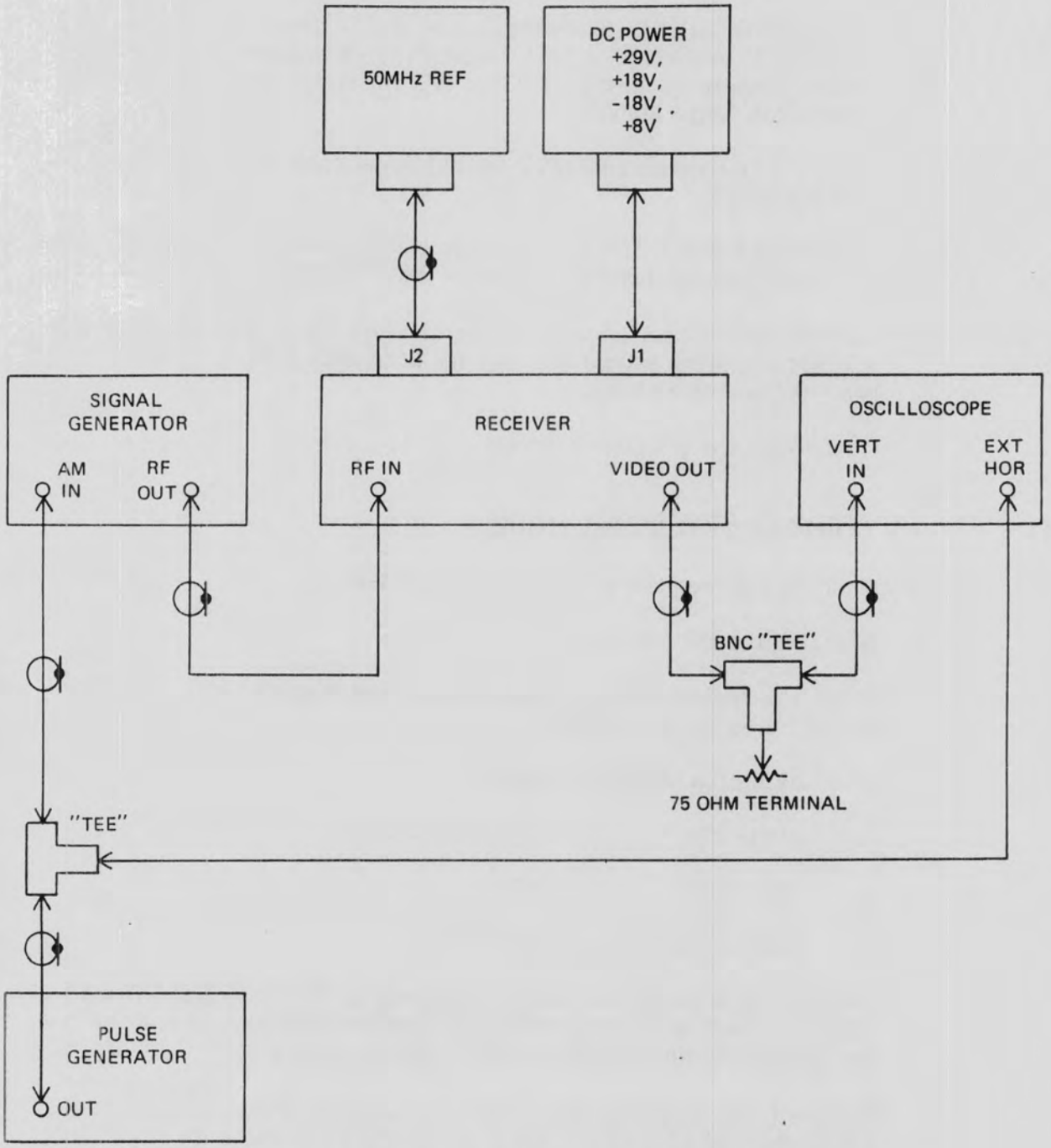


Figure 4-6. Gain Control (Pulse Mode) Test Equipment Setup

7. Observe the pulse level on the oscilloscope.

8. Increase the signal generator output level to -10 dBm. The signal on the oscilloscope should change a maximum of 6 dB.

9. Deenergize the DC power source.

4.4.12 FREQUENCY TUNING ACCURACY TEST

1. Connect the receiver as shown in **Figure 4-7.**

2. Energize the DC power source.

3. Using the receiver front panel controls and keypad, set the receiver to the following parameters:

   a. Detection Mode - AM

   b. Bandwidth - Narrowest available

   c. Gain Mode - AGC

   d. Tuned Frequency - 510.0000 MHz

4. Set the signal generator output frequency to 510.0000 MHz, unmodulated and output level to -60 dBm.

5. Set the frequency to provide 10 Hz resolution at a 1 second sample rate.

6. The frequency counter should indicate 21.40000 MHz ±750 Hz.

7. Deenergize the DC power source.

4.5 RECEIVER TROUBLESHOOTING PROCEDURES

4.5.1 GENERAL

Information is provided in this paragraph to troubleshoot the receiver to a defective replaceable assembly or PC board. The receiver normally requires troubleshooting as a result of failure to pass any of the performance tests outlined in **paragraph 4.4,** or as a result of operator-observed malfunctions during normal receiver operation.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

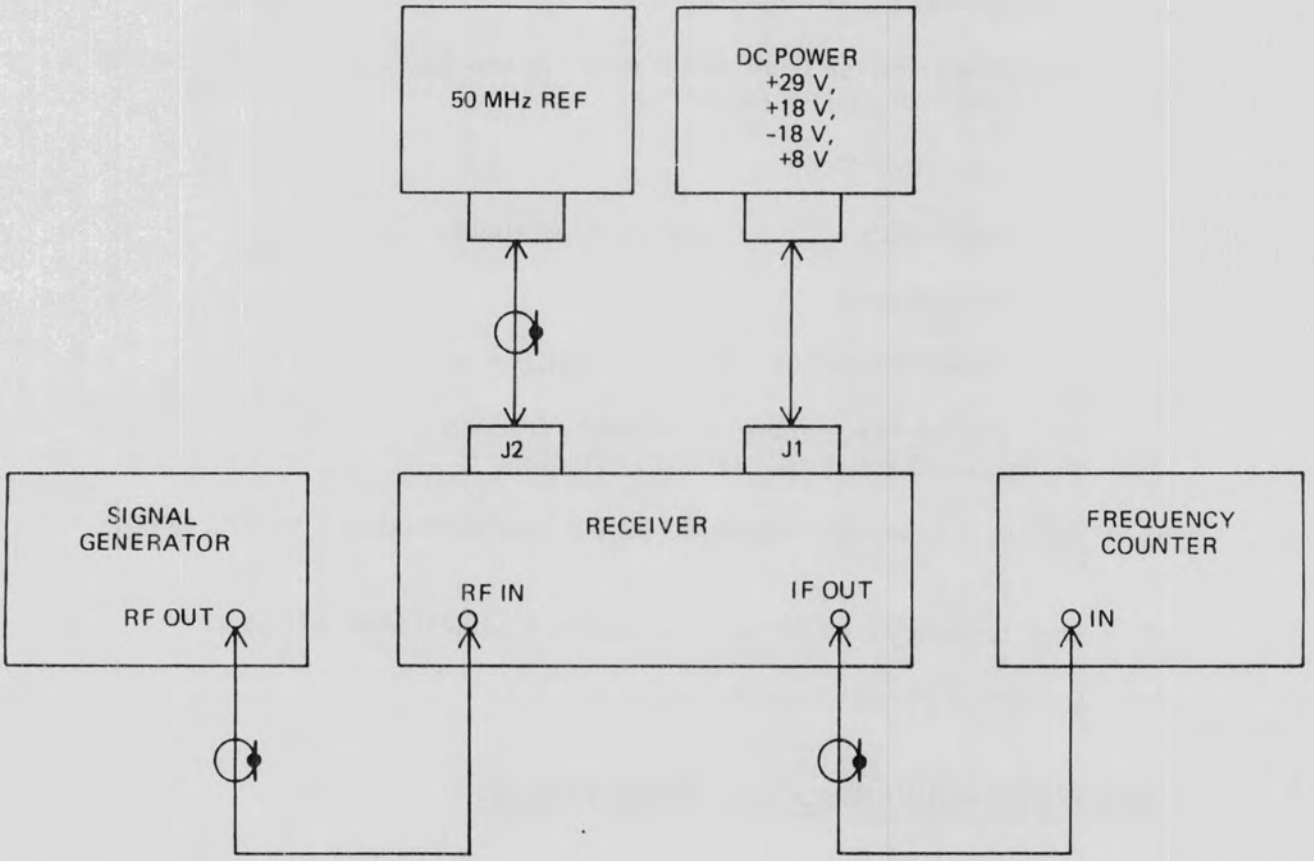


Figure 4-7. Frequency Tuning Accuracy Test Equipment Setup

4.5.2 TROUBLESHOOTING GUIDELINES

Table 4-5, WJ-8628-4 VHF/UHF Receiver Troubleshooting Chart, is provided as an aid in locating defective assemblies and PC boards within the receiver. The chart is designed to be used in conjunction with the receiver performance tests outlined in **paragraph 4.4.** The troubleshooting procedures provide a listing of specific fault symptoms that could occur for each of the performance tests outlined in **paragraph 4.4.** Probable causes of the fault and suggested corrective actions are also listed. The following guidelines should be applied when using **Table 4-5.**

1. Perform each of the performance tests in **paragraph 4.4.** Note any failures to achieve the expected test result or results.
2. Refer to **Table 4-5.** Locate the performance test and fault symptom noted in step 1.
3. Perform the corrective action associated with the fault symptom. If a module is replaced requiring alignment, refer to **paragraph 4.6** and perform the indicated alignment.
4. Repeat the performance test in **paragraph 4.4** that resulted in the fault symptom to confirm the corrective action.
5. The receiver may be returned to service if it successfully passes all the performance tests in **paragraph 4.4.**
6. **Table 4-5** is intended as a general troubleshooting guide and is not a substitute for standard signal tracing/fault isolation techniques performed by skilled technicians familiar with the receiver circuitry.

Table 4-5. WJ-8628-4 VHF/UHF Receiver Troubleshooting Chart

Performance Test	Fault Symptom	Probable Cause	Corrective Action
KEYBOARD/ DISPLAY FUNCTION	No display brightness	No display exciting voltage	Check A4J5-17 for 90 Vac. If bad replace A4U1.
		Power supply voltage low	Check regulator outputs: A4A1-1: +5 V A4A1-4: +12 V A4A1-5: -12 V If bad, replace A4A1. If OK, replace A4A6.

Table 4-5. WJ-8628-4 VHF/UHF Receiver Troubleshooting Chart (Continued)

Performance Test	Fault Symptom	Probable Cause	Corrective Action
KEYBOARD/ DISPLAY FUNCTION (continued)	Display/Adjust control does not work	Defective control	Voltage at A4J5-9 should vary from -2 to +1 V. If OK, replace A4A1. If bad replace R3.
	Initialization does not execute	Digital control is dead	Replace A4A3. If still dead, check CPU Addr/Data/Contr Bus for activity, selectively remove digital modules until lines become active. If still bad, replace A4A5, then A4A6 and reinitialize.
	Keypad is inoperative	Defective keyboard lines on interface	Check R1-R4 and C1-C7 lines on A4J3. If OK replace A4A6. If bad replace A8.
RF/IF GAIN TEST	IF output dead on all test frequencies & all BWs.	Defective Frequency Extender (FE)	Inject test signal directly into A1J1. If OK, replace FE.
		Incorrect Preselector tuning voltage	Check tuning voltage at A5J1-39. Should be 1.5 to 23 Vdc. If bad, replace A2A4.
		Incorrect 1st LO signal.	Check 1st LO at A3J4. Frequency should be 326.6 (lo band) + rcvr tuned freq. or 126.6 (hi band) + rcvr tuned freq. If bad, replace A3A9, then A3A10.

Table 4-5. WJ-8628-4 VHF/UHF Receiver Troubleshooting Chart (Continued)

Performance Test	Fault Symptom	Probable Cause	Corrective Action
RF/IF GAIN TEST (continued)	IF output dead on all test freqs and BWs (continued)	Incorrect 2nd LO signal.	Check 2nd LO at A3J3. Frequency should be 305.1 (lo band) or 105.1 (hi band) for all test freqs. If bad, check A3A6-E4. Should be 204 MHz. If bad, replace A3A6, then A3A5. If good, replace A3A3, then A3A4, then A3A8.
		Defective 1st IF Converter	Check output at A1A3-326.6/126.6. Signal should be 17 dB above RF input. If bad, replace A1A3.
		Defective 2nd IF Converter	Check output at A1A4-J3. Should be 15 dB above RF input. If bad, replace A1A4.
		Defective A2A1	Check signal at A2A1-E2. Should be 40 dB above IF input at A2J3. If bad, check A2A1J2-4 for +13 V, and A2A1-P1 for 100 mV. If all readings are good replace A2A1.
		Defective A2A2	Check A2A2J2-9 for +5 V and A2A2J2-11 for 0 V. If both are good, replace A2A2.
		Incorrect RF AGC Voltage	Check RF AGC voltage at A5J1-10. Should be 0 V. If bad, replace A2A4.

Table 4-5. WJ-8628-4 VHF/UHF Receiver Troubleshooting Chart (Continued)

Performance Test	Fault Symptom	Probable Cause	Corrective Action
RF/IF GAIN TEST (continued)	IF output dead on 1 or more test freqs.	Incorrect hi/lo select voltage	Check hi/lo select voltage A5J1-8. Should be 0 V in lo band, +5 in hi band. If bad, replace A2A4. Also check hi band/ lo band sw signals at A1A6-E1,E2. If bad, replace A1A3.
		Defective Input Preselector	Check hi/lo band RF outputs at A1A1-E14, E15. If either is bad, replace A1A1.
		Defective Dual RF Amplifier	Check RF out at A1A2-E3. If output is bad in either hi or lo band, replace A1A2.
		Defective Dual IF Filter	Check IF out at A1A6-E3. If output is bad in either hi or lo band, replace A1A2.
	IF output dead on 1 or more BWs	Defective A2A1	Check IF output at A2A1-E2 for all BWs. If not good, replace A2A1. If good, replace A2A2.
	IF Filter switching does not occur	Defective BW select code	Check BW select code at A2A2J2-4,5. If not good, replace A2A4.
DETECTION MODE TEST	No video output in any mode	Defective A2A3	Check AM,FM Video inputs to A2A3 at A2A3J2-1,4. If bad replace A2A2. If good replace A2A3.

Table 4-5. WJ-8628-4 VHF/UHF Receiver Troubleshooting Chart (Continued)

Performance Test	Fault Symptom	Probable Cause	Corrective Action
DETECTION MODE TEST (continued)	No video output in AM mode.	Defective A2A2	Check AM Video at A2A2J1-1. If bad, check AM SEL at A2A2J2-8 for high. If bad, replace A2A4. If good, replace A2A2. If AM Video at A2J1-1 is good, check FM SEL at A2A3J1-3 for low. If bad, replace A2A4. If good replace A2A3.
	No video output in FM mode	Defective A2A5	Check FM Video at A2A5-P1. If not good check IF IN at A2A5-J4. If not good, replace A2A2. If good, replace A2A5 or A2A5A1-A2A5A4.
		Defective A2A2	Check FM Video at A2A2J1-4. If bad, replace A2A2. If good, check FM SEL at A2A3J1-3 for high. If bad, replace A2A4. If good replace A2A3.
	No video output in CW mode.	Defective A2A2	Check A2A2J2-7 for low and A2A2J2-8 for low. If not good, replace A2A4. If good replace A2A2.
	No video output	Defective A2A4	Check A2A2J2-7 for low and A2A2J2-8 for low. If not good, replace A2A4. If good replace A2A2.

Table 4-5. WJ-8628-4 VHF/UHF Receiver Troubleshooting Chart (Continued)

Performance Test	Fault Symptom	Probable Cause	Corrective Action
SNR TEST	Signal to noise ratio less than 10 dB	RF Tuner out of alignment	Perform alignment on Input Preselector, Dual RF Amplifier and overall gain (see **paragraph 4.6**)
		Excessive loss in front end of receiver.	Replace A1A1 and/or A1A2.
GAIN CONTROL TEST	Inadequate control range (AGC mode)	Defective A2A1	Check IF output at A2A1E2. Should be 40 dB above IF input. If bad, check A2A1J2-4 for +2 V. If good, replace A2A1. If bad check A2A2J2-9 for 0 V. If good, replace A2A2. If bad, replace A2A4.
		Defective A2A2	Check IF output level at A2J4 (rear panel) Should be -20 dBm min. If bad, replace A2A2.
		Defective A1A3	Check IF output at A1A4E5. Should be 15 dB above RF input. If bad check RF AGC at A1A3J3-2. If good, replace A1A3. If bad, replace A2A4.
	Inadequate control range (MAN mode)	Defective IF GAIN control	Set IF GAIN control at max CW. Check A4J5-16 for +5 V. If bad replace R2. If good, check A2A4J3-11 for +6 V. If bad, replace A2A4, then A4A6.

Table 4-5. WJ-8628-4 VHF/UHF Receiver Troubleshooting Chart (Continued)

Performance Test	Fault Symptom	Probable Cause	Corrective Action
FREQUENCY TUNING ACCURACY TEST	Tuning error more than 510 Hz at 510.0000 MHz	Time Base	Verify accuracy of 50 MHz reference.
		2nd LO unlocked	Check 2nd LO signal at A3J2. Perform 2nd LO alignment if necessary.
		1st or 2nd LO tuning error	Replace A3A3, A3A5 or A3A9. If still bad, replace A2A4, then A4A5.

4.6 RECEIVER ALIGNMENT PROCEDURES

4.6.1 GENERAL

The following alignment procedures should only be performed when indicated by the results of performance testing (**paragraph 4.4**) or troubleshooting (**paragraph 4.5**). Prior to performing any alignment, allow 30 minutes for test equipment warm-up.

4.6.2 INPUT PRESELECTOR ALIGNMENT

1. Remove the RF Tuner cover and connect the receiver as shown in **Figure 4-8.**
2. Energize the DC power source.
3. Using the receiver front panel controls and keypad, set the receiver to the following parameters:
   a. Detection Mode - AM
   b. Bandwidth - BW #1
   c. Gain Mode - Manual
   d. RF Gain - Maximum clockwise
   e. Tuned Frequency - 500.0000 MHz
4. Set the signal generator output frequency to 500.0000 MHz unmodulated and output level to -10 dBm.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

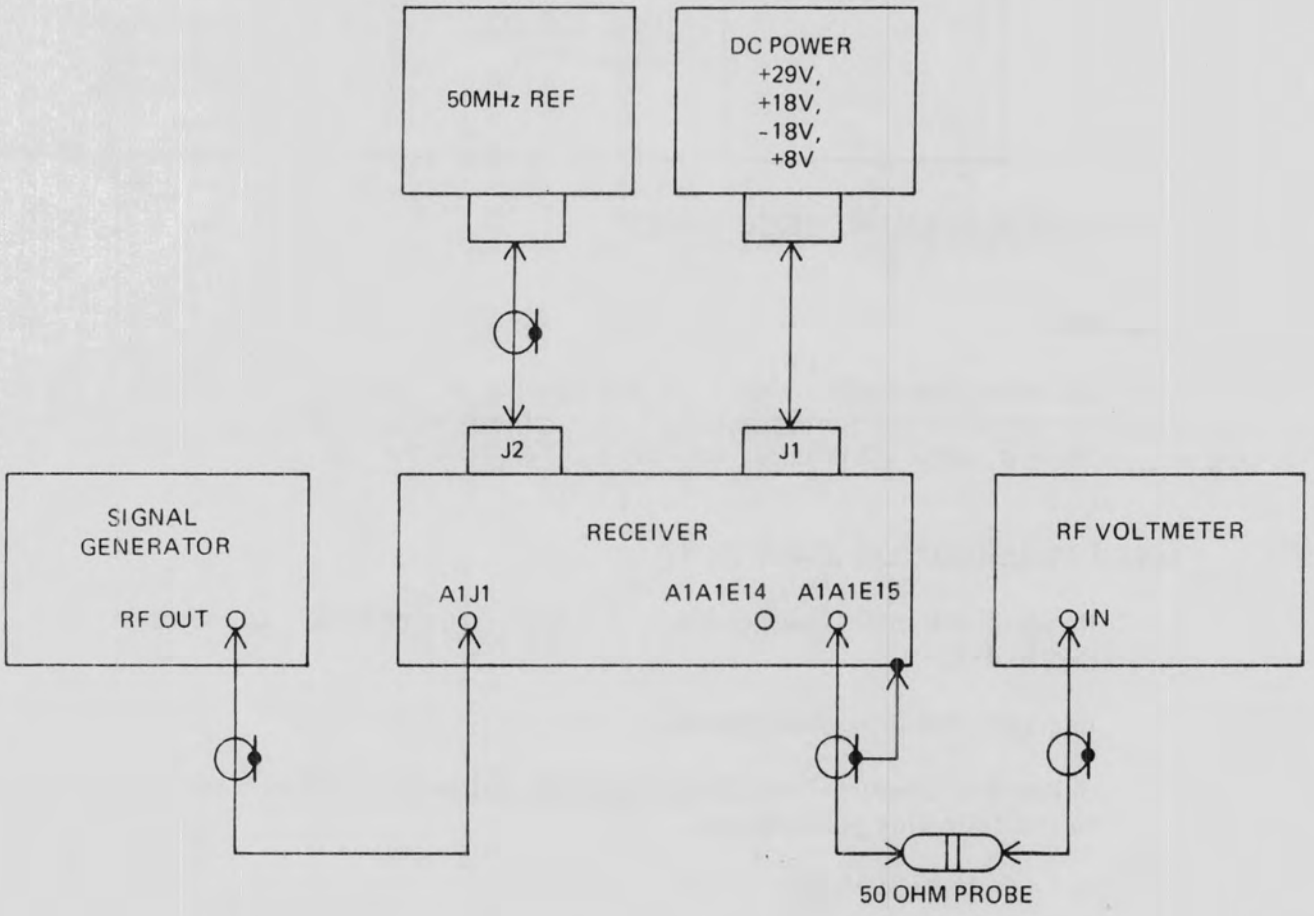


Figure 4-8. Input Preselector Alignment Equipment Setup

5. Tune C37 and C41 for maximum RF voltmeter indication.

6. Set the signal generator output frequency to 275.0000 MHz. Use the receiver front panel keypad to change the receiver tuned frequency to 275.0000 MHz.

7. Tune L19 and L22 for best VSWR indication.

8. Steps 5 and 7 interact with each other. Repeat steps 4 through 7 until maximum output is achieved at 500.0000 and 275.0000 MHz simultaneously.

9. Connect the RF voltmeter clip lead to terminal A1A1E14. Use the receiver front panel keypad to change the receiver tuned frequency to 275.0000 MHz.

10. Set the signal generator output frequency to 274.0000.

11. Tune C26 and C30 for maximum RF voltmeter indication.

12. Set the signal generator output frequency to 150.0000 MHz. Use the receiver front panel keypad to change the receiver tuned frequency to 150.0000 MHz.

13. Tune L14 and L16 for best VSWR indication.

14. Steps 11 and 13 interact with each other. Repeat steps 10 through 13 until maximum output is achieved at 274.0000 and 150.0000 MHz simultaneously.

15. Use the receiver front panel keypad to change the receiver tuned frequency to 150.0000 MHz.

16. Set the signal generator output frequency to 149.5000 MHz.

17. Tune C15 and C18 for maximum RF voltmeter indication.

18. Set the signal generator output frequency to 60.0000 MHz. Use the receiver front panel keypad to change the receiver tuned frequency to 60.0000 MHz.

19. Tune L9, T3, T4 and L11 for maximum RF voltmeter indication.

20. Steps 17 and 19 interact with each other. Repeat steps 16 through 19 until maximum output is achieved at 149.5000 and 60.0000 MHz simultaneously.

21. Use the receiver front panel keypad to change the receiver tuned frequency to 60.0000 MHz.

22. Set the signal generator output frequency to 59.5000 MHz.

23. Tune C4 and C7 for maximum RF voltmeter indication.

24. Set the signal generator output frequency to 20.0000 MHz. Use the receiver front panel keypad to change the receiver tuned frequency to 20.0000 MHz.

25. Tune L3, T1, T2 and L5 for maximum RF voltmeter indication.

26. Steps 23 and 25 interact with each other. Repeat steps 22 through 25 until maximum output is achieved at 59.5000 and 20.0000 MHz simultaneously.

27. Deenergize the DC power source.

28. Replace the cover on the RF Tuner.

4.6.3 DUAL RF AMPLIFIER ALIGNMENT

1. Remove the RF Tuner cover and connect the receiver as shown in **Figure 4-9.**

2. Energize the DC power source.

3. Using the receiver front panel controls and keypads, set the receiver to the following parameters:

   a. Detection Mode - AM

   b. Bandwidth - BW #1

   c. Gain Mode - Manual

   d. RF Gain - Maximum clockwise

   e. Tuned Frequency - 105.0000 MHz

4. Set the signal generator output frequency to 330.0000 MHz unmodulated and output level to -10 dBm.

5. Tune capacitor C5 all the way out.

6. Tune L5 for a minimum RF voltmeter indication.

7. Set the signal generator output frequency to 372.0000 MHz.

8. Tune L6 for a minimum RF voltmeter indication.

9. Set the signal generator output frequency to 581.0000 MHz.

10. Tune L4 for a minimum RF voltmeter indication.

11. Set the signal generator output frequency to 326.6000 MHz.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

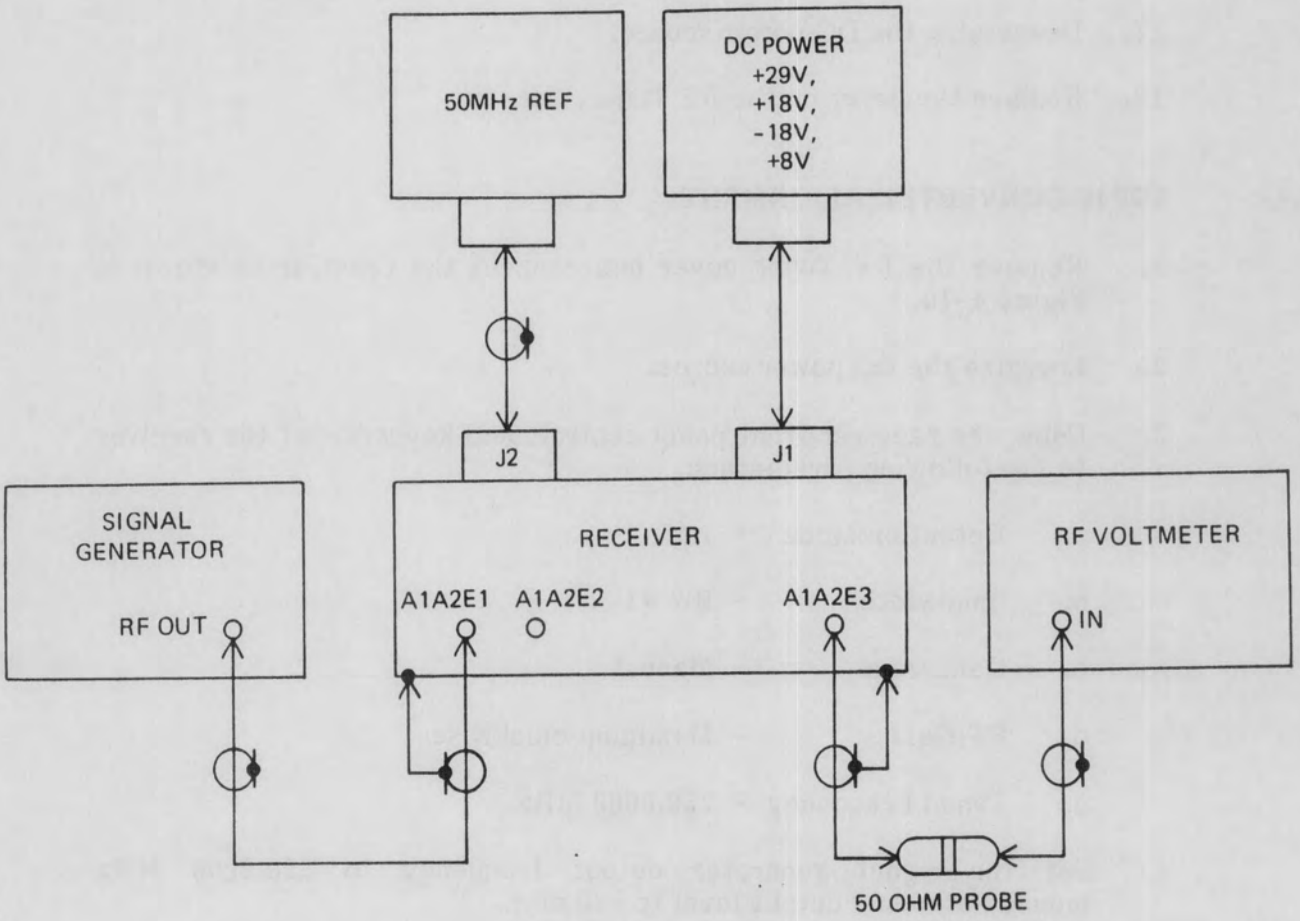


Figure 4-9. Dual RF Amplifier Alignment Equipment Setup

12. Tune C5 for a minimum RF voltmeter indication.

13. Connect the signal generator clip lead to terminal A1A2E2. Set the signal generator output frequency to 500.0000 MHz. Use the receiver front panel keypad to change the receiver tuned frequency to 500.0000 MHz.

14. Tune C14 and C18 for maximum RF voltmeter indication.

15. Set the signal generator output frequency to 126.6 MHz.

16. Tune C13 for a minimum RF voltmeter indication.

17. Deenergize the DC power source.

18. Replace the cover on the RF Tuner.

4.6.4 1ST IF CONVERTER ALIGNMENT

1. Remove the RF Tuner cover and connect the receiver as shown in **Figure 4-10.**

2. Energize the DC power source.

3. Using the receiver front panel controls and keypads, set the receiver to the following parameters:

   a. Detection Mode - AM

   b. Bandwidth - BW #1

   c. Gain Mode - Manual

   d. RF Gain - Maximum clockwise

   e. Tuned Frequency - 250.0000 MHz

4. Set the signal generator output frequency to 250.0000 MHz unmodulated and output level to -30 dBm.

5. Note the indication on the RF voltmeter.

6. Rotate the RF GAIN control fully counterclockwise.

7. Adjust R18 until the RF voltmeter indication is 30 dB below the level noted in step 5 above.

8. Deenergize the DC power source.

9. Replace the cover on the RF Tuner.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

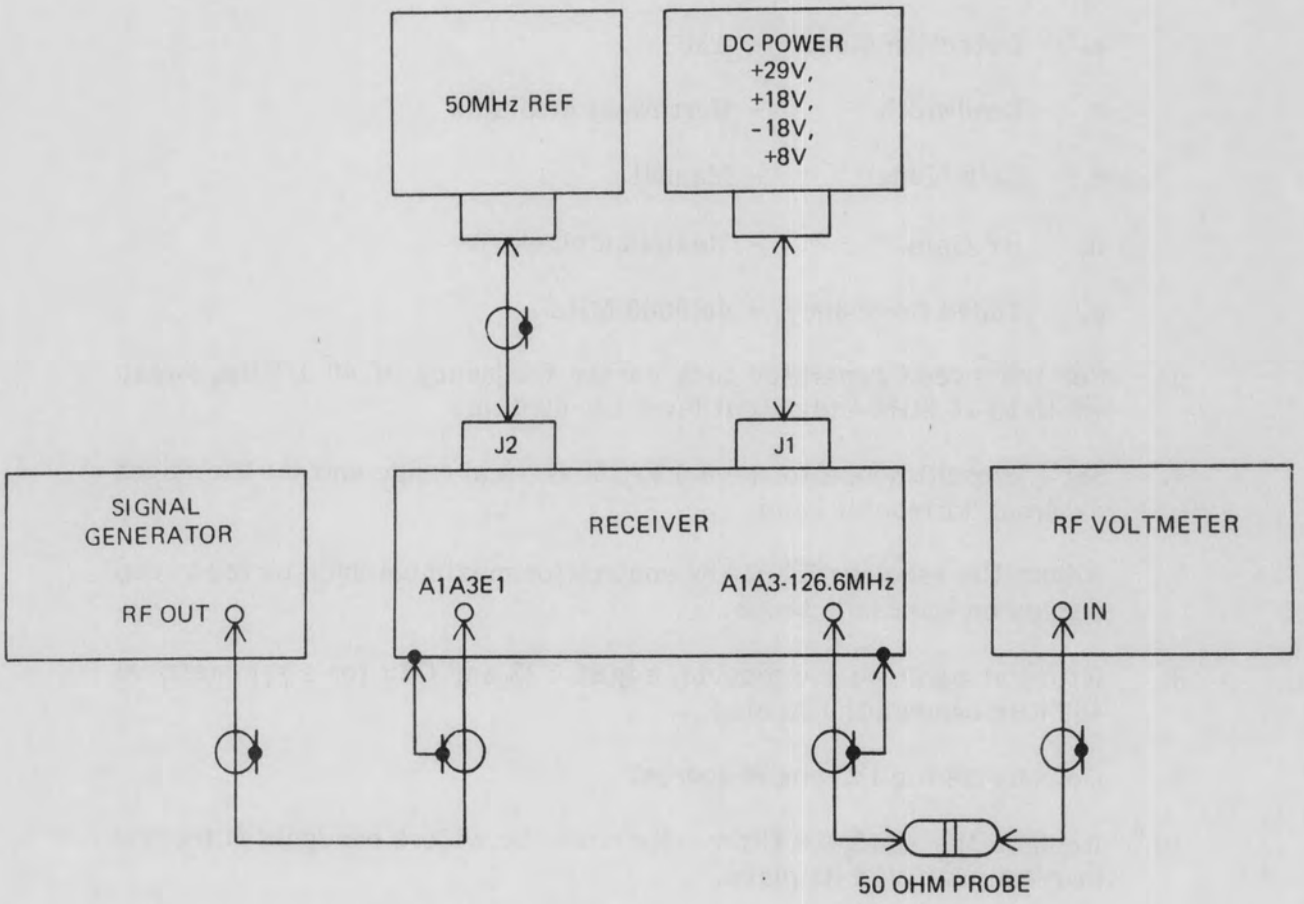


Figure 4-10. 1st IF Converter Alignment Equipment Setup

4.6.5 WIDE/NARROW FILTER ALIGNMENT

1. Remove the IF Demodulator cover and connect the receiver as shown in **Figure 4-11.**
2. Remove the narrowest filter from module A1A1 and insert a jumper in its place.
3. Energize the DC power source.
4. Using the receiver front panel controls and keypads, set the receiver to the following parameters:
   a. Detection Mode - AM
   b. Bandwidth - Narrowest available
   c. Gain Mode - Manual
   d. RF Gain - Maximum clockwise
   e. Tuned Frequency - 40.0000 MHz
5. Set the sweep generator to a center frequency of 40.0 MHz, sweep width to 10 MHz and output level to -60 dBm.
6. Set the oscilloscope to the 0.5 V/CM vertical range and set the select external horizontal input.
7. Adjust the receiver RF GAIN control for maximum undistorted sweep display on the oscilloscope.
8. With the cover on the module, adjust C22 and C25 for a symmetrical 400 kHz bandwidth response.
9. Deenergize the DC power source.
10. Replace the bandpass filter. Remove the widest bandpass filter and insert a jumper in its place.
11. Energize the DC power source. Use the receiver front panel controls and keypad to set the receiver to the parameters listed in step 4. Select the widest IF bandwidth available.
12. Adjust C1, C8 and C10 for a symmetrical broadband response.
13. Deenergize the DC power source.
14. Replace the bandpass filter.
15. Replace the cover on the IF Demodulator.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

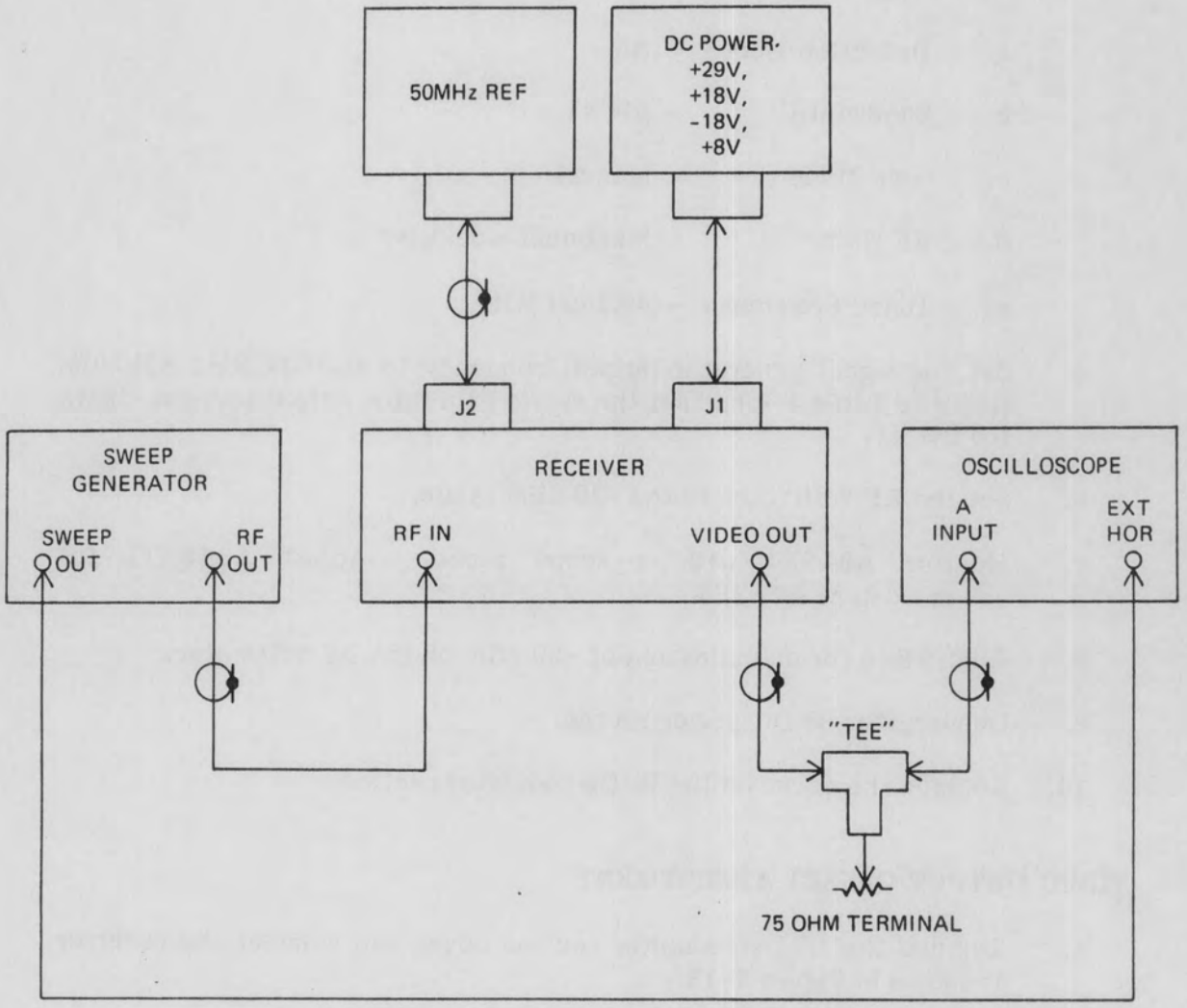


Figure 4-11. Wide/Narrow Filter Alignment Equipment Setup

4.6.6 RECEIVER OVERALL GAIN ADJUSTMENT

1. Connect the receiver as shown in **Figure 4-12.**
2. Remove the cover from the IF Demodulator section.
3. Energize the DC power source.
4. Using the receiver front panel controls and keypads, set the receiver to the following parameters:
   a. Detection Mode - AM
   b. Bandwidth - BW #1
   c. Gain Mode - Manual
   d. RF Gain - Maximum clockwise
   e. Tuned Frequency - 40.1000 MHz.
5. Set the signal generator output frequency to 40.1000 MHz AM 50%. Refer to **Table 4-4** and set the signal generator output level as shown for BW #1.
6. Set the RF voltmeter to the -20 dBm range.
7. Monitor A2A2E4 with a scope probe. Adjust A2A2AT1 for 500 mV p-p at A2A2E4.
8. Adjust R45 for an indication of -20 dBm on the RF voltmeter.
9. Deenergize the DC power source.
10. Replace the cover on the IF Demodulator section.

4.6.7 VIDEO OUTPUT OFFSET ADJUSTMENT

1. Remove the IF Demodulator section cover and connect the receiver as shown in **Figure 4-13.**
2. Energize the DC power source.
3. Using the receiver front panel controls and keypads, set the receiver to the following parameters:
   a. Detection Mode - AM
   b. Bandwidth - BW #1

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

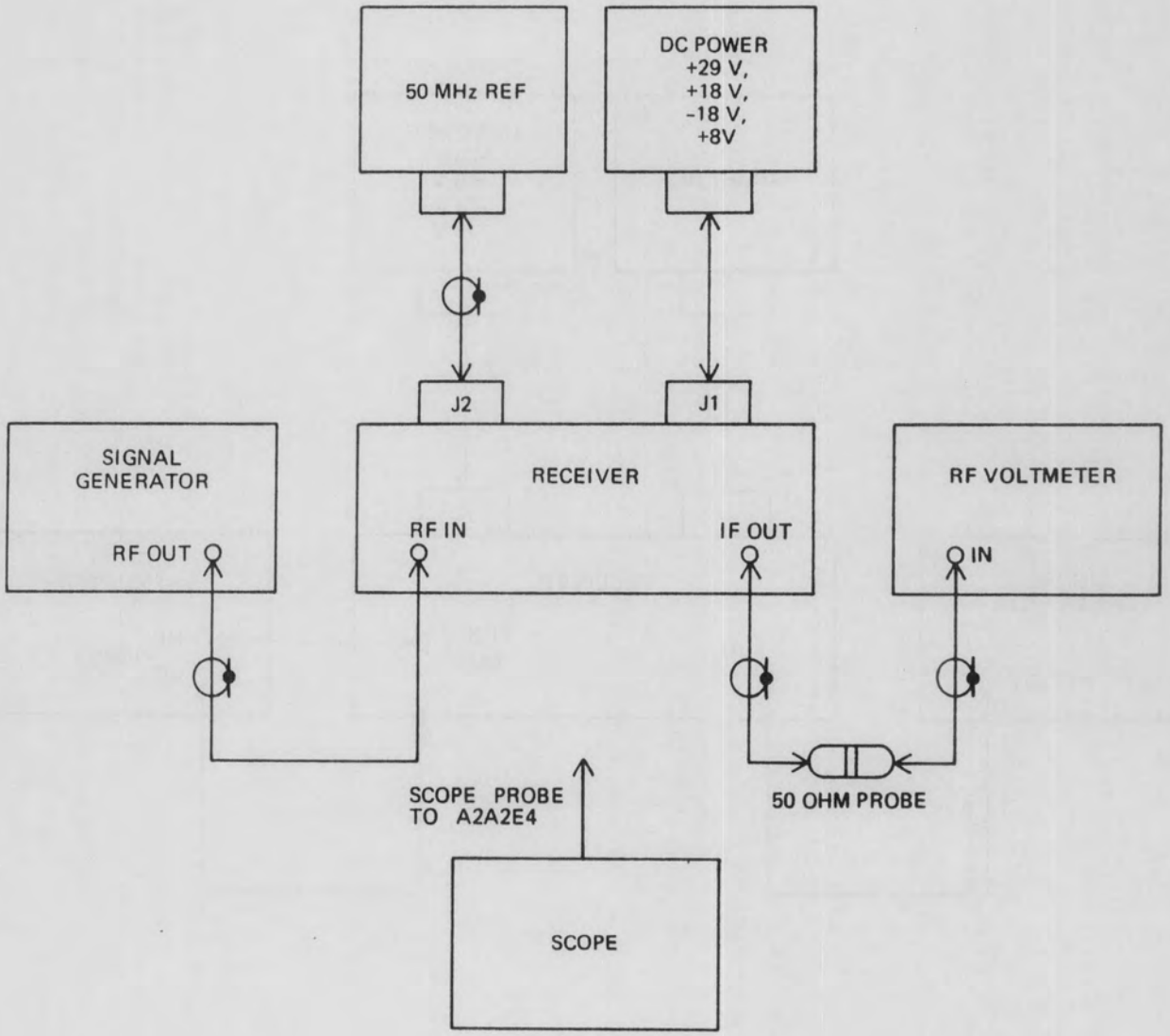


Figure 4-12. Receiver IF Gain Adjustment Equipment Setup

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

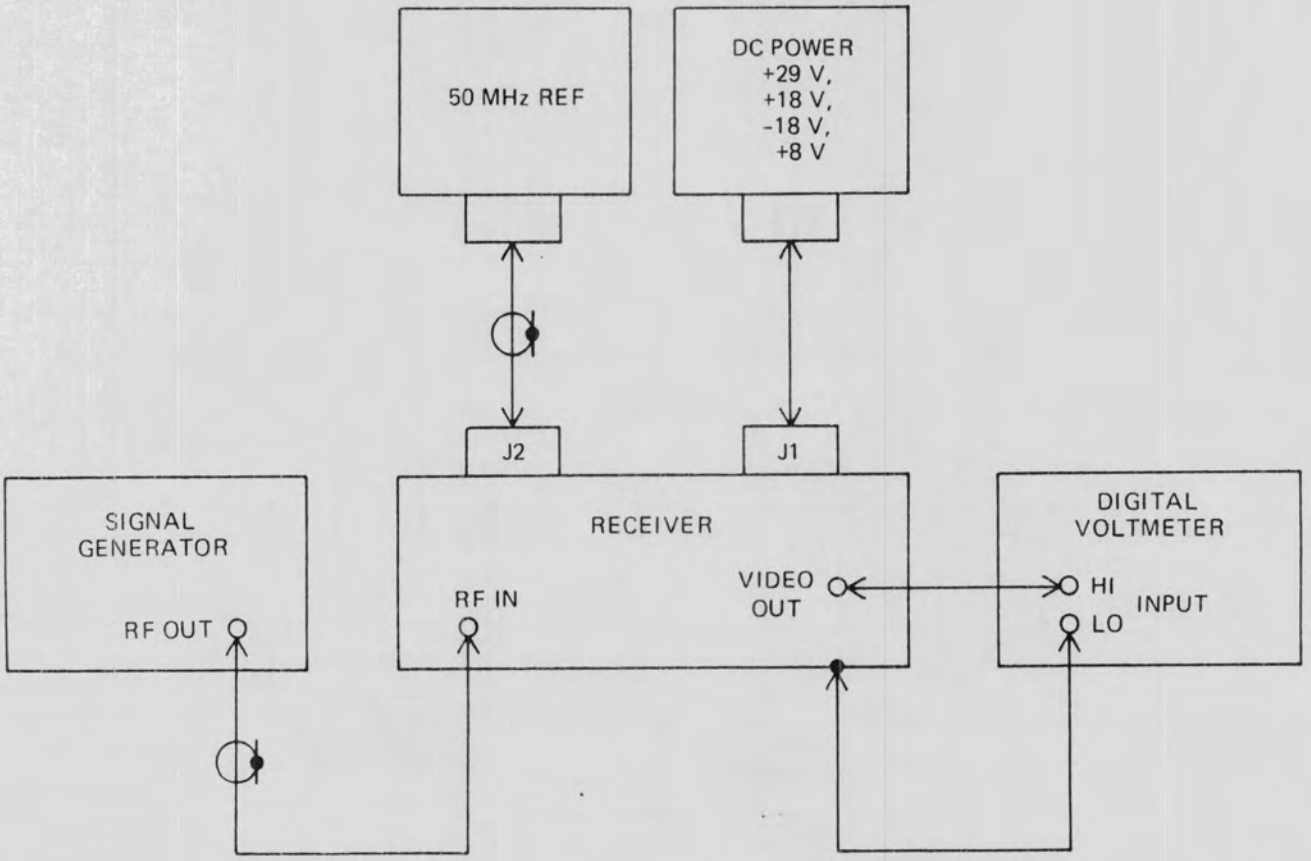


Figure 4-13. Video Output Offset Adjustment Equipment Setup

c. Gain Mode - Manual

d. RF Gain - Maximum clockwise

e. Tuned Frequency - 40.1000 MHz.

4. Set the signal generator RF output off.

5. Set the digital voltmeter to the 2 Vdc range.

6. Adjust A2A2R34 for an indication of 0 Vdc, ±0.05 Vdc on the digital voltmeter.

7. Deenergize the DC power source.

8. Replace the cover on the IF Demodulator section.

4.6.8 AM VIDEO LEVEL ADJUSTMENT

1. Remove the IF Demodulator cover and connect the receiver as shown in **Figure 4-14.**

2. Energize the DC power source.

3. Using the receiver front panel controls and keypads, set the receiver to the following parameters:

   a. Detection Mode - AM

   b. Bandwidth - BW #1

   c. Gain Mode - FST

   d. Tuned Frequency - 40.1000 MHz

4. Set the signal generator output frequency to 40.1000 MHz and set the output level to -60 dBm. Set the generator for 50% AM modulation at 400 Hz.

5. Set the oscilloscope to the 0.5 V/CM range.

6. Adjust A2A3R11 for an indication of 1 Vpp on the oscilloscope.

7. Deenergize the DC power source.

8. Replace the IF Demodulator cover.

4.6.9 FM DETECTOR ALIGNMENT

1. Remove the IF Demodulator cover and connect the receiver as shown in **Figure 4-15.**

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

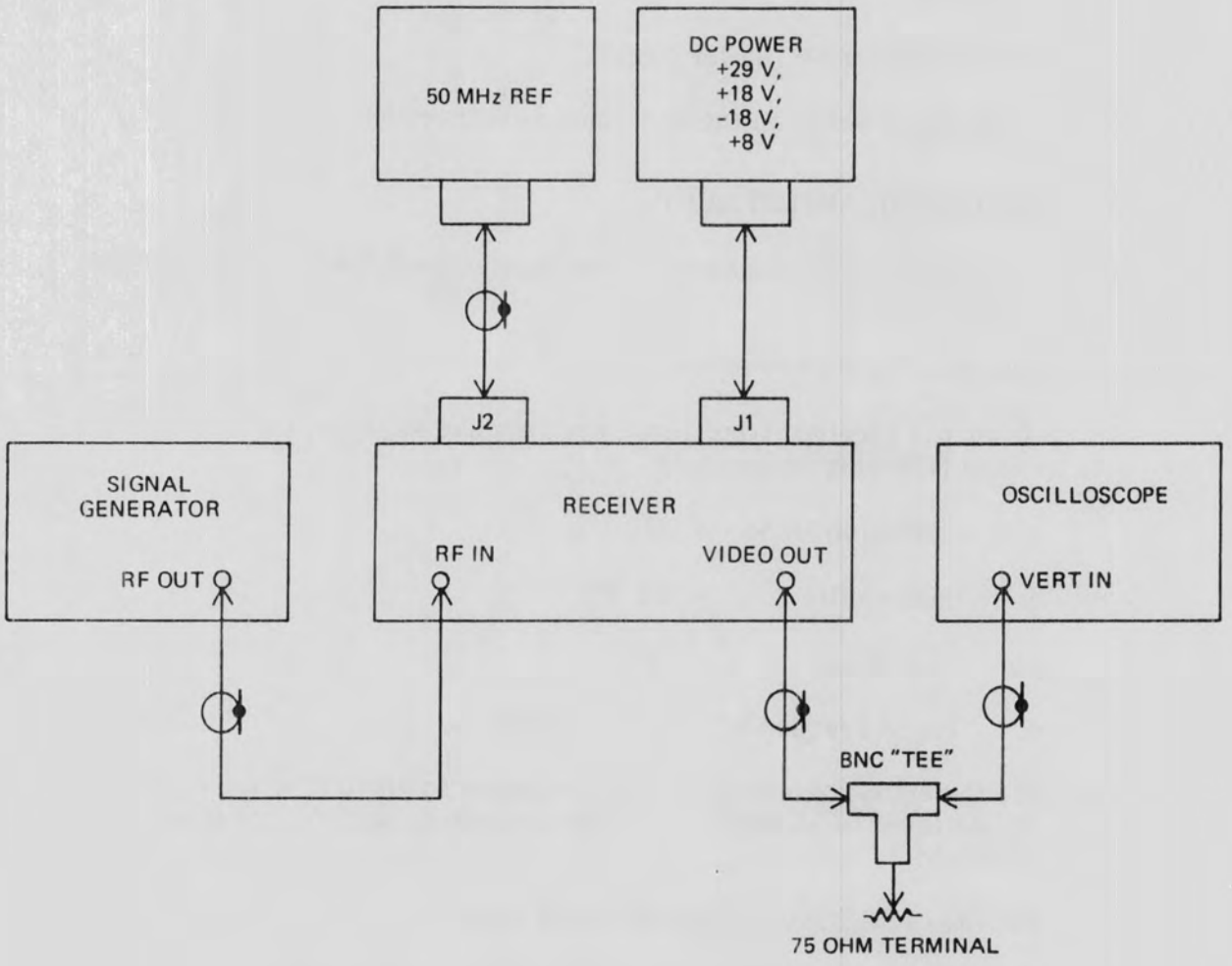


Figure 4-14. AM Video Level Adjustment Equipment Setup

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

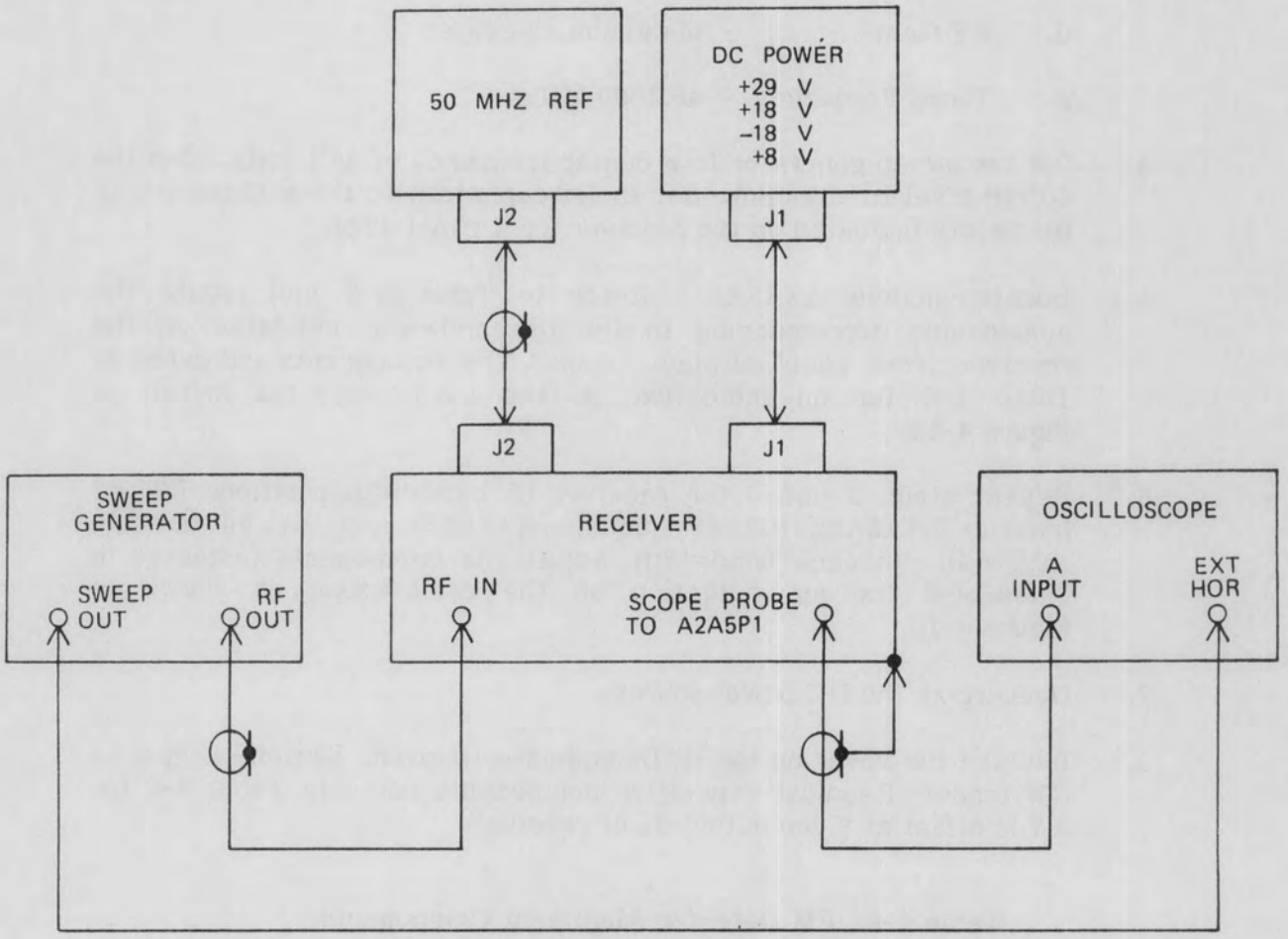


Figure 4-15. FM Detector Alignment Equipment Setup

2. Energize the DC power source.

3. Using the receiver front panel controls and keypads, set the receiver to the following parameters:

   a. Detection Mode - FM

   b. Bandwidth - BW #1

   c. Gain Mode - Manual

   d. RF Gain - Maximum clockwise

   e. Tuned Frequency - 40.1000 MHz

4. Set the sweep generator to a center frequency of 40.1 MHz. Set the output level to -60 dBm. Set the sweep width to three times the IF bandwidth indicated on the receiver front panel display.

5. Locate module A2A5A1. Refer to **Table 4-6** and locate the components corresponding to the IF bandwidth indicated on the receiver front panel display. Adjust the components indicated in **Table 4-6** for an indication on the oscilloscope as shown in **Figure 4-16.**

6. Repeat steps 5 and 6 for receiver IF bandwidth positions BW #2 (module A2A5A2), BW #3 (module A2A5A3) and BW #4 (module A2A5A4). In each bandwidth, adjust the components indicated in **Table 4-6** for an indication on the oscilloscope as shown in **Figure 4-16.**

7. Deenergize the DC power source.

8. Replace the cover on the IF Demodulator section. Switch sweeper to CW mode. Readjust capacitive components listed in **Table 4-6** for 0 Vdc offset at video output J1 of receiver.

Table 4-6. FM Detector Alignment Components

Bandwidth	Alignment Components
10 - 25 kHz	C6, C16, R13
30 - 200 kHz	C6, R13
300 kHz - 4 MHz	C6, C9, R7, R8

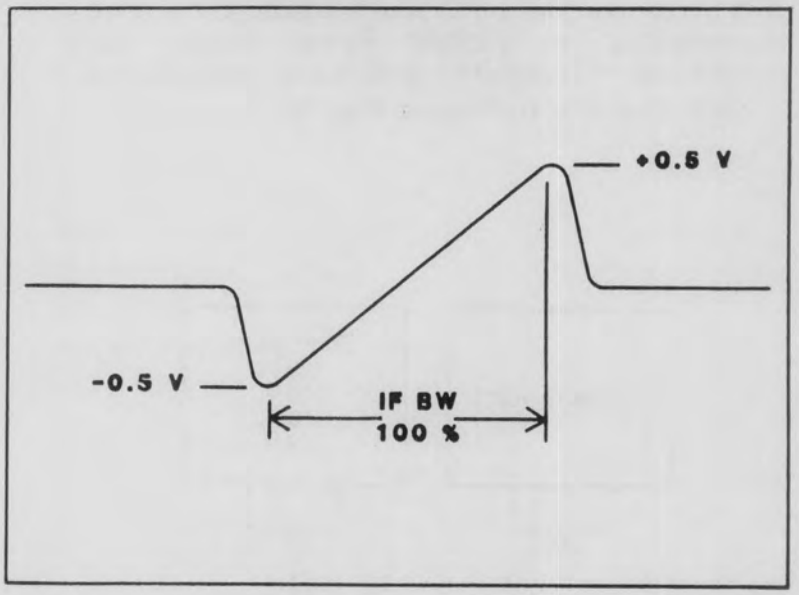


Figure 4-16. FM Detector S-Curve

4.6.10 **FM VIDEO LEVEL ADJUSTMENT**

1. Remove the IF Demodulator cover and connect the receiver as shown in **Figure 4-17.**
2. Energize the DC power source.
3. Using the receiver front panel controls and keypads, set the receiver to the following parameters:
   a. Detection Mode - FM
   b. Bandwidth - BW #1
   c. Gain Mode - AGC FST
   d. Tuned Frequency - 40.1000 MHz
4. Set the signal generator output frequency to 40.1000 MHz and output level to -60 dBm. Set the signal generator for FM deviation equal to 1/3 the receiver IF bandwidth at a 400 Hz rate.
5. Set the oscilloscope to the 0.2 V/CM range.

NOTE

These two sources may be provided by placing the receiver in an EFR100 Equipment Frame containing an EPS100 Power Supply and FRM150 Frequency Reference Module or SRM105A Site Reference Module.

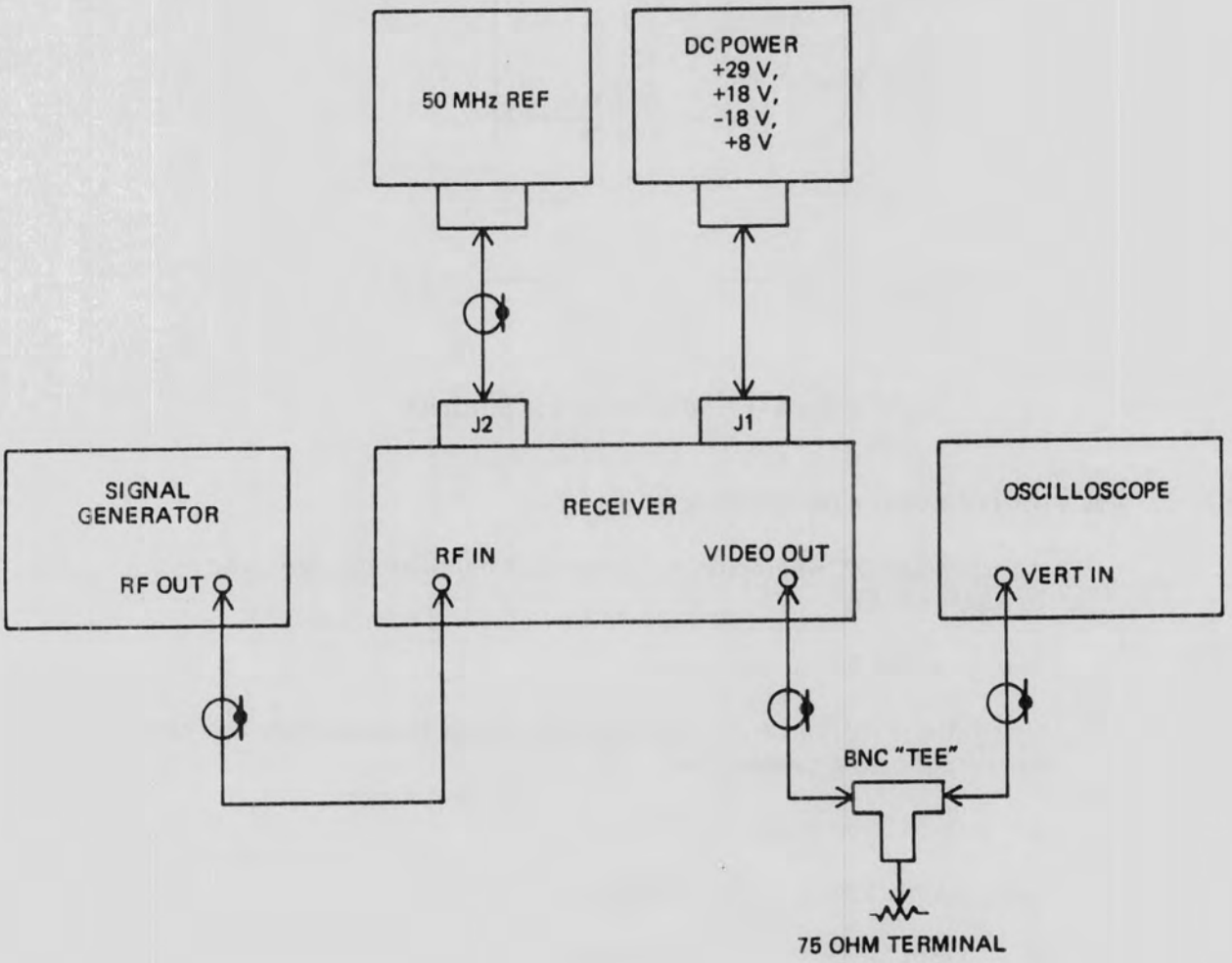


Figure 4-17. FM Video Level Adjustment Equipment Setup

6. Locate module A2A5A1. Refer to **Table 4-6** and locate the component corresponding to the IF bandwidth indicated on the receiver front panel display. Adjust R3 on A2A3 for 0.6 Vpp on the oscilloscope.

7. Repeat steps 4-6 for receiver IF bandwidth positions BW #2 (module A2A5A2), BW #3 (module A2A5A3) and BW #4 (module A2A5A4). In each bandwidth, verify an indication of 0.6 Vpp on the oscilloscope. (R3 should not need to be readjusted.)

8. Deenergize the DC power source.

9. Replace the cover on the IF Demodulator section.

4.6.11 DISPLAY BACKLIGHT ADJUSTMENT

1. Connect the receiver to a power source such as the EPS100 Power Supply mounted in the EFR100 Equipment Frame.

2. Energize the DC power source. Turn the BACKLIGHT switch on.

3. While observing the front panel display, adjust A4A1R3 for the minimum backlight brightness necessary to achieve adequate visibility.

NOTE

The electro-luminescent backlight lamp has a half-life related to use and intensity. The brightness adjustment is intended to compensate for this over the life of the unit, and should be considered when making this adjustment.

4. Deenergize the DC power souce.

4.6.12 A/D CONVERTER REFERENCE ADJUSTMENT

1. Connect the receiver to a power source such as the EPS100 Power Supply mounted in the EFR100 Equipment Frame.

2. Place module A4A6 on an extender card.

3. Set the receiver for MAN mode and RF GAIN at maximum clockwise.

4. Enter the following keystrokes via the front panel keypad:

5. Observe that the display indicates:

   MAINTENANCE TEST 1
   MGC A/D OUTPUT = XXX

6. Adjust A4A6R14 until the display indicates between 250 and 254.

7. Deenergize the DC power source.

8. Replace module A4A6 in the receiver.

4.6.13 1ST LO SYNTHESIZER ALIGNMENT

1. Remove the cover from the Synthesizer Module.

2. Connect the receiver to a power source such as the EPS100 Power Supply mounted in the EFR100 Equipment Frame.

3. Energize the DC power source.

4. Using the receiver front panel keypad, tune the receiver to 158.5000 MHz.

5. Connect a digital voltmeter to terminal A3A10C6.

6. Adjust A3A10C10 for an indication of 20 ±.2 Vdc on the digital voltmeter.

7. Tune the receiver to 258.5000 MHz.

8. Adjust A3A10C30 for an indication of 20 ±.2 Vdc on the digital voltmeter.

9. Deenergize the DC power source.

10. Remove the digital voltmeter connection.

11. Replace the cover on the Synthesizer Module.

4.6.14 2ND LO SYNTHESIZER ALIGNMENT

The 2nd LO Synthesizer alignment consists of an AUX VCO alignment and a 2nd LO VCO alignment. Perform the procedure in the given sequence.

1. Preliminary Setup

   a. Connect the receiver to a DC power source such as the EPS100 Power Supply mounted in the EFR100 Equipment Frame.

b. Remove the cover from the Synthesizer Module.

c. Energize the receiver.

2. AUX VCO Alignment

a. Connect a digital voltmeter to terminal A3A6E5.

b. Using the receiver front panel keypad, tune the receiver to 20.0000 MHz.

c. Adjust A3A5C5 for an indication of 15 ±1 Vdc on the digital voltmeter.

3. 2nd LO VCO Alignment

a. Connect a digital voltmeter to terminal A3A3E7.

b. Using the receiver front panel keypad, tune the receiver to 125.0000 MHz.

c. Adjust A3A3L1 for an indication of 9 ±.5 Vdc on the digital voltmeter.

d. Tune the receiver to 390.0000 MHz.

e. Adjust A3A3C21 for an indication of 9 ±.5 Vdc on the digital voltmeter.

4. Deenergize the DC power source.

5. Disconnect the digital voltmeter.

6. Replace the cover on the Synthesizer Module.

4.6.15 BFO SYNTHESIZER ALIGNMENT

1. Connect the receiver to a DC power source such as the EPS100 Power Supply mounted in the EFR100 Equipment Frame.

2. Remove the cover from the Synthesizer Module.

3. Connect a digital voltmeter to pin A3A7U3-7.

4. Energize the DC power source.

5. Using the receiver front panel keypad, select CW mode and 0.0 kHz BFO offset.

6. Adjust A3A7L1 for an indication of 3 ±.2 Vdc on the digital voltmeter.

7. Connect the digital voltmeter to pin A3A7U3-1.

8. Adjust A3A7L3 for an indication of 2.5 ±.2 Vdc on the digital voltmeter.

9. Deenergize the DC power source.

10. Disconnect the digital voltmeter.

11. Replace the cover on the Synthesizer Module.

4.7 MODULE TESTING AND REPAIR

4.7.1 GENERAL

This paragraph provided the testing, troubleshooting and repair information necessary to restore a malfunctioning module to normal operation. The information provided consists of the following categories:

1. Module test and troubleshooting procedures to assist signal tracing and localize faulty circuit areas.

2. Fault isolation tables to assist isolating defective components in faulty circuit areas.

3. Parts replacement guidelines, **paragraph 4.7.7** are provided to assist in repairing a defective module.

4.7.2 PROCEDURE GUIDELINES

The module testing and troubleshooting procedures are defined using an EFR100 Equipment Frame, an EPS100 Power Supply and a functional WJ-8628-4 VHF/UHF Receiver as a test bed. **Figure 4-18** is a block diagram showing the test bed configuration which is used in each of the module testing and troubleshooting procedures.

When testing and troubleshooting a defective module, observe the following guidelines:

1. Allow the test equipment to warm up for 30 minutes before any test is performed.

2. Refer to the testing and troubleshooting paragraph for the desired module. Configure the receiver and test equipment as indicated in the test procedure for the module.

3. Perform the testing and troubleshooting procedure in the sequence given. If any failure is encountered or any desired result is not obtained, the Fault Isolation Table lists which key components would most likely cause the failure.

4. Refer to **paragraph 4.7.7**, Parts Replacement Guidelines, and replace the key components indicated in step 3 above. Repeat the Testing and Troubleshooting Procedure to confirm the corrective action.

5. If the module still fails, additional troubleshooting and signal tracing is required. Refer to the circuit descriptions in **Section III** and schematic diagrams in **Section IV** as aids in performing additional troubleshooting.

4.7.3 RF TUNER (A1) MODULE TESTING AND TROUBLESHOOTING

4.7.3.1 Input Preselector (A1A1) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the Input Preselector. A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3**) are required to perform the tests outlined below.

4.7.3.1.1 Preliminary Setup Procedure

The following preliminary setup procedures should be performed prior to testing or troubleshooting the Input Preselector:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A1A1.
4. Interconnect J1 on the receiver rear panel with its mating connector on the EFR100 Equipment Frame.
5. Connect the signal generator RF output to receiver rear panel RF input jack (A1J1) using a BNC to SMA adaptor.
6. Set the signal generator as follows:

   a. RF Frequency — 30.000 MHz
   b. Output Level — -20 dBm
   c. Modulation — None

7. Energize the receiver using the power switch on the equipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — Maximum available
   f. TUNED FREQ — 30.000 MHz

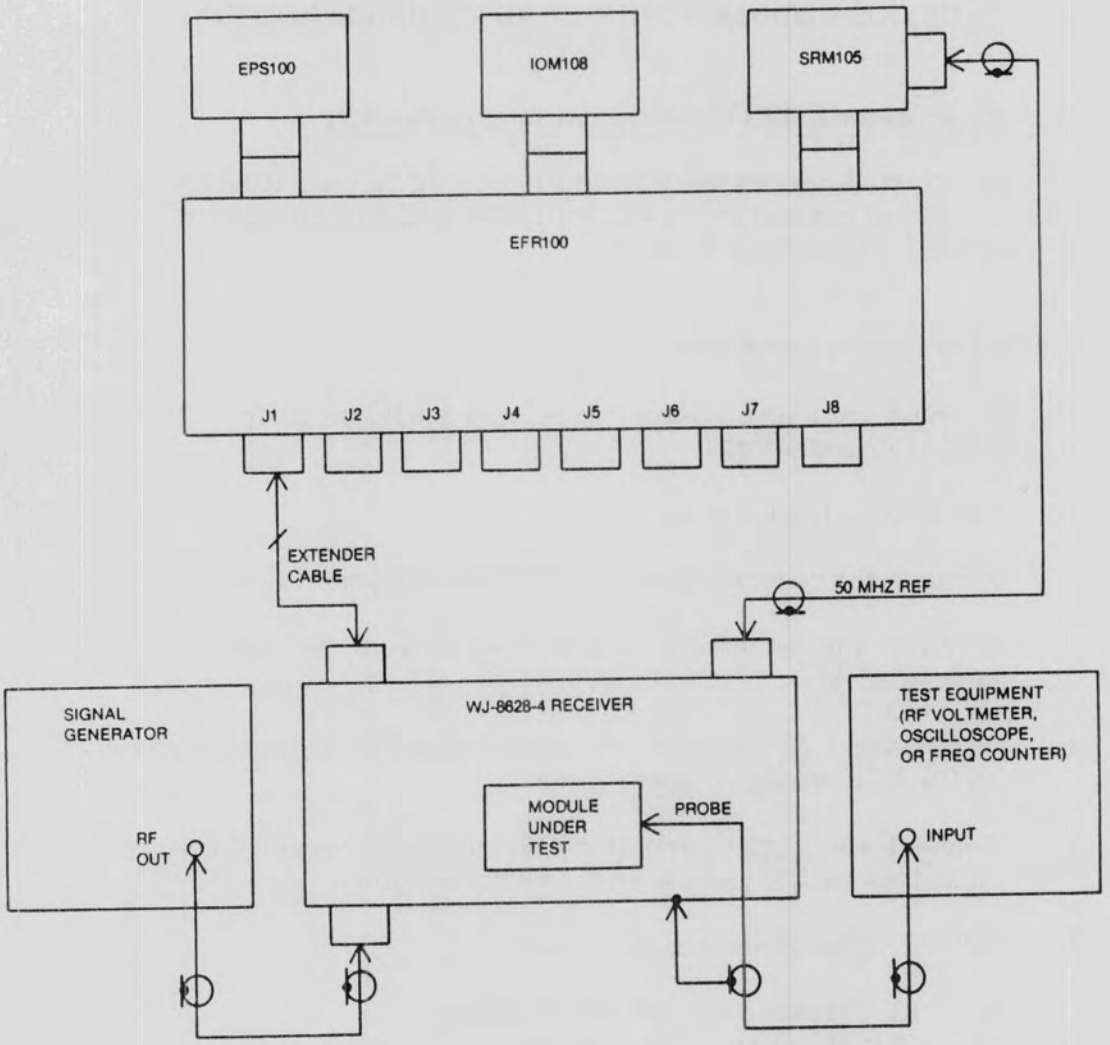


Figure 4-18. Receiver Module Test Bed Configuration

8. Using the RF voltmeter probe tip, verify that a -20 dBm signal is present at A1A1E16. Adjust the signal generator output level slightly as necessary to achieve correct signal level.

4.7.3.1.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-7**, Input Preselector (A1A1) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.3.1.1.**

2. Use an RF voltmeter RF probe tip or oscilloscope to check each test point listed in **Table 4-7.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-7. Paragraph 4.7.7**, Parts Replacement Guideline, should be referred to as a aid in removing and replacing any PCB components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing-fault isolation is necessary. Refer to **paragraph 3.4.1.1**, Input Preselector Circuit Description, and Figure 6-2, Input Preselector Schematic Diagram for additional aid in troubleshooting.

Table 4-7. Input Preselector Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
J1-6	+6 V	A2A4	Tuning Voltage
U1-1	+7.5 V	U1	Band Select Signal
E14	-24 dBm	FL1 Components	
J1-6	+4.2 V	A2A4	Tune Receiver to 80 MHz
U1-5	+7.5 V	U1	
E14	-24 dBm	FL2 Components	
J1-6	+9.2 V	A2A4	Tune Receiver to 190 MHz
U1-2	+7.5 V	U1	

Table 4-7. Input Preselector (A1A1) Fault Isolation Table (Cont'd)

Test Point	Normal Signal	Key Components	Comments
E14	-24 dBm	FL3 Components	
J1-6	+10 V	A2A4	387.5 MHz
U1-4	+7.5 V	U1	
E14	-24 dBm	FL4 COMPONENTS	

4.7.3.2 **Dual RF Amplifier (A1A2) Testing and Troubleshooting**

This paragraph describes the procedures needed to test, troubleshoot and repair the Dual RF Amplifier (A1A2). A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3**) are required to perform the tests outlined below.

4.7.3.2.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Dual RF Amplifier:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A1A2.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Connect the signal generator RF output to receiver rear panel RF input jack, A1J1, using a BNC to SMA adaptor.
6. Set the signal generator as follows:
   a. RF Frequency — 190.000 MHz
   b. Output Level — -20 dBm
   c. Modulation — None
7. Energize the receiver using the power switch on the equipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:
   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM

e. IF BW — Maximum available
f. TUNED FREQ —190.000 MHz

8. Using the RF voltmeter probe tip, verify that a mV rms signal is present at A1A2E1. Adjust the signal generator output level slightly as necessary to achieve correct signal level.

4.7.3.2.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-8**, Dual RF Amplifier Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure in **paragraph 4.7.3.2.1.**

2. Using an RF voltmeter RF probe tip or oscilloscope as indicated, check each test point listed in **Table 4-8.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-8. Paragraph 4.7.7,** Parts Replacement Guide, should be referred to as a aid in removing and replacing any PCB components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing-fault isolation is necessary. Refer to **paragraph 3.4.1.2,** Dual RF Amplifier Circuit Description, and **Figure 6-3,** Dual RF Amplifier Schematic Diagram for additional aid in troubleshooting.

Table 4-8. Dual RF Amplifier Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U4-3	+15 V	U4	Band Select Signal
U3-12	-15 V	U3	Band Select Signal
U1-4	-6.5 dBm	U1	
CR3 Anode	-6.8 dBm	L3-L6, C5-C12	Low Pass Filter Output. Filter loss at 275 MHz 1 dB.
E3	-7 dBm	CR3-CR5	Low Band Switch
U4-4	+15 V	U4	Tune Rcvr to 387.5000 MHz
U3-4	-15 V	U3	

Table 4-8. Dual RF Amplifier Fault Isolation Table (Cont'd)

Test Point	Normal Signal	Key Components	Comments
U2-4	-8 dBm	U2	Tune Sig Gen to 400.000 MHz
CR6 Anode	-6.5 dBm	L8-L10, C13-C19	Band Pass Filter Output
E3	-6.5 dBm	CR6-CR8	High Band Switch

4.7.3.3 **1st IF Converter (A1A3) Testing and Troubleshooting**

This paragraph describes the procedure needed to test, troubleshoot and repair the 1st IF Converter (A1A3). A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3**) are required to perform the tests outlined below.

4.7.3.3.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior to testing or troubleshooting the 1st IF Converter:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A1A3.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Connect the signal generator RF output to receiver rear panel RF input jack, A1J1, using a BNC to SMA adaptor.
6. Set the signal generator as follows:

   a. RF Frequency — 400.000 MHz
   b. Output Level — -20 dBm
   c. Modulation — None

7. Energize the receiver using the power switch on the equipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW

d. DET. MODE — AM
e. IF BW — Maximum available
f. TUNED FREQ — 400.000 MHz

8. Use the RF voltmeter probe tip, to verify that a -6.5 dBm signal is present at. Adjust the signal generator output level slightly as necessary to achieve correct signal level.

4.7.3.3.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-9,** 1st IF Converter (A1A3) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.3.3.1.**

2. Use an RF voltmeter RF probe tip or oscilloscope to check each test point listed in **Table 4-9.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-9. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/ fault isolation is necessary. Refer to **paragraph 3.4.1.3,** 1st IF Converter Circuit Description, and **Figure 6-4,** lst IF Converter Schematic Diagram for additional aid in troubleshooting.

Table 4-9. 1st IF Converter (A1A3) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
J1-2	-2V	Digital Control, A4	
U6-7	+13V	U6	
U6-1	+13V	U6,CR7,CR8	
E2	+2 dBm	Synth., A3	1st LO signal
U3-4	+17 dBm	U5	
U3-2	-8 dBm	U3	1st IF Output (-24 dBm with Signal Generator off)

Table 4-9. 1st IF Converter (A1A3) Fault Isolation Table (Cont'd)

Test Point	Normal Signal	Key Components	Comments
U4-2	+2 dBm	U4	
U7-12	-15 V	U7	Low Band Select
CR3 Anode	+2 dBm	CR1-CR3	Low Band IF Output
U7-4	-15 V	U7	High Band Select Tune Rcvr to 400.000 MHz
CR6 Anode	+2 dBm	CR4-CR6	High Band IF Output. Tune Sig Gen to 400.000 MHz

4.7.3.4 **2nd IF Converter (A1A4) Testing and Troubleshooting**

This paragraph describes the procedures needed to test, troubleshoot and repair the 2nd IF Converter (A1A4). A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3** are required to perform the tests outlined below.

4.7.3.4.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior to testing or troubleshooting the 2nd IF Converter:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A1A4.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Connect the signal generator RF output to receiver rear panel RF input jack (A1J1) using a BNC to SMA adaptor.

6. Set the signal generator as follows:

   a. RF Frequency -- 200.000 MHz
   b. Output Level -- -20 dBm
   c. Modulation -- None

7. Energize the receiver using the power switch on the equipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. RF GAIN -- Max. CW
   d. DET. MODE -- AM
   e. IF BW -- Maximum available
   f. TUNED FREQ -- 200.000 MHz

8. Use the RF voltmeter probe tip to verify that a -10 dBm signal is present at A1A4E1. Adjust the signal generator output level slightly as necessary to achieve correct signal level.

4.7.3.4.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-10,** 2nd IF Converter (A1A6) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.3.4.1.**

2. Use an RF voltmeter RF probe tip or oscilloscope to check each test point listed in **Table 4-10.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-10. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.1.5,** 2nd IF Converter Circuit Description, and **Figure 6-5,** 2nd IF Converter Schematic Diagram for additional aid in troubleshooting.

Table 4-10. 2nd IF Converter (A1A4) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U1-1	-11 dBm	C1-C7,L1-L3,R1-R3	
U1-4	+5 dBm	U2, Synth A3	2nd LO Signal
U3-4	-2 dBm	U3, U1	
E5	-6 dBm	C12-C14,L6,L7,U4	

4.7.3.5 **Dual IF Amplifier (A1A6) Testing and Troubleshooting**

This paragraph describes the procedure needed to test, troubleshoot and repair the Dual IF Amplifier (A1A6). A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3**) are required to perform the tests outlined below.

4.7.3 5.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Dual IF Amplifier:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A1A6.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Connect the signal generator RF output to receiver rear panel RF input jack (A1J1) using a BNC to SMA adaptor.
6. Set the signal generator as follows:

   a. RF Frequency — 400.000 MHz
   b. Output Level — -20 dBm
   c. Modulation — None

7. Energize the receiver using the power switch on theequipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:

a. LOCAL/REMOTE — LOCAL
b. MAN/AGC — MAN
c. RF GAIN — Max. CW

d. DET. MODE -- AM
e. IF BW -- Maximum available
f. TUNED FREQ -- 400.000 MHz

8. Use the RF voltmeter probe tip to verify that a +3 dBm signal is present at A1A6-Lo Band Input. Adjust the signal generator output level slightly as necessary to achieve correct signal level.

4.7.3.5.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-11**, Dual IF Amplifier (A1A6) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.3.5.1.**

2. Use an RF voltmeter RF probe tip or oscilloscope to check each test point listed in **Table 4-11.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-11. Paragraph 4.7.7**, Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.1.4**, Dual IF Amplifier Circuit Description, and **Figure 6-7**, Dual IF Amplifier Schematic Diagram for additional aid in troubleshooting.

Table 4-11. Dual IF Amplifier (A1A6) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
E1	-15 V	A1A3, Digital Control, A4	Low Band Switch
E3	-3 dBm	FL1, CR1-CR3	
E2	-15 V	A1A3, Digital Control, A4	High Band Switch. Tune Rcvr to 387.5000 MHz
E3	-3 dBm	FL2, CR4-CR6	Tune Sig Gen to 387.5 MHz

4.7.4 IF DEMODULATOR (A2) TESTING AND TROUBLESHOOTING

4.7.4.1 21.4 MHz Bandpass Amplifier (A2A1) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the 21.4 MHz Bandpass Amplifier (A2A1). A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3**) are required to perform the tests outlined below.

4.7.4.1.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the 21.4 MHz Bandpass Amplifier:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Separate RF, IF, and Syn modules to provide access to IF module.
4. Remove the necessary subassembly covers to provide access to module A2A1.
5. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
6. Connect the signal generator RF output to IF module IF Input A2J3.
7. Set the signal generator as follows:

   a. RF Frequency -- 21.4 MHz
   b. Output Level — -40 dBm
   c. Modulation — None

8. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display, to set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — Narrowest Bandwidth

9. Use the RF voltmeter probe tip to verify that a 2.25 mV rms signal is present at A2A1E1. Adjust the signal generator output level slightly as necessary to achieve the correct signal level.

4.7.4.1.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-12,** 21.4 MHz Bandpass Amplifier (A2A1) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.4.1.1.**

2. Use an RF voltmeter RF probe tip or oscilloscope to check each test point listed in **Table 4-12.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-12. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.2.1,** 21.4 MHz Bandpass Amplifier Circuit Description, and **Figure 6-9,** 21.4 MHz Bandpass Amplifier Schematic Diagram for additional aid in troubleshooting.

Table 4-12. 21.4 MHz Bandpass Amplifier (A2A1) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U1-3	2.25 mv RMS	U1	Adjust signal generator to obtain correct level
Q1-2	2.0 mv RMS	U1	Also check for Plus 13 V at U1-1
Q1-1	13 mv	Q1, Q2	
Q2-1	0.8 Vdc	Q1, Q2	Q1 sets bias for Q2
CR7 cathode CR7 anode CR12 cathode CR12 anode	6 mv RMS 6 mv RMS 6 mv RMS 6 mv RMS	CR7 CR7 CR12 CR12	Test may be run on any selected BW. Turn signal generator off for DCVM measurements.

Table 4-12. 21.4 MHz Bandpass Amplifier (A2A1) Fault Isolation Table (Cont'd)

Test Point	Normal Signal	Key Components	Comments
E2	-39 dB	SSB	See **Table 4-12a** for input level as a function of BW for this test. Check all BWs for correct gain at E2.
E2	-39 dB	10 kHz	
E2	-31 dB	20 kHz	
E2	-32 dB	50 kHz	
E2	-29 dB	100 kHz	
E2	-26 dB	200 kHz	
E2	-24 dB	300 kHz	
E2	-22 dB	500 kHz	
E2	-19 dB	19 MHz	
E2	-16 dB	2 MHz	
E2	-13 dB	4 MHz	

Table 4-12a. Input Levels

BW	Input Level
SSB	-90 dBm
10 kHz	-90 dBm
20 kHz	-87 dBm
50 kHz	-83 dBm
100 kHz	-80 dBm
200 kHz	-77 dBm
300 kHz	-75 dBm
500 kHz	-73 dBm
1 MHz	-70 dBm
2 MHz	-67 dBm
4 MHz	-64 dBm

4.7.4.2 AM/SSB/CW Demodulator (A2A2) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the AM/SSB/CW Demodulator (A2A2). Testing and troubleshooting of the AM/SSB/CW Demodulator consists of two different procedures: one procedure for the IF section and one procedure for the AGC section. These procedures may be performed independently, although it is advised to verify proper IF section operation before performing the AGC section procedure. A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3**) are required to perform the tests outlined below.

4.7.4.2.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the AM/SSB/CW Demodulator:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Separate RF, IF, and Syn modules to provide access to IF module.
4. Remove the necessary subassembly covers to provide access to module A2A2.
5. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
6. Disconnect W1P3 from IF Input Jack, A2J3. Connect the signal generator RF output to IF Input Jack (A2J3) using a BNC to SMA adaptor.

4.7.4.2.2 IF Section Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-13,** AM/SSB/CW Demodulator (A2A2) Fault Isolation Table (IF Section). This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.4.2.1.**
2. Set the signal generator as follows:

   a. RF Frequency — 21.4 MHz
   b. Output Level — Approx. -50 dBm
   c. Modulation — None

3. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — As desired

4. Use the RF voltmeter probe tip to verify that a 360 mV rms signal is present at A2A2R9. Adjust the signal generator output level slightly as necessary to achieve correct signal level.

5. Use an RF voltmeter RF probe tip or oscilloscope to check each test point listed in **Table 4-13.**

6. When a faulty component is found, replace the key component(s) indicated in **Table 4-13. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as an aid in removing and replacing any PC board components.

7. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.2.2,** AM/SSB/CW Demodulator Circuit Description, and **Figure 6-10,** AM/SSB/CW Demodulator Schematic Diagram for additional aid in troubleshooting.

Table 4-13. AM/SSB/CW Demodulator (A2A2) Fault Isolation Table (IF Section)

Test Point	Normal Signal	Key Components	Comments
Q1-3	90 mv RMS	T1	
Q1-1	100 mv RMS 21.4 MHz (Reduce input to -80 dBm.)	Q1	Check voltage at Q1-2. Should be +4 Vdc. If not, check CR1 and AGC section.
U2-2	65 mv	U2,U14	
CR6 Anode	20 mV (NB) 5 mV (WB)	CR2-CR7, U3	Rotate BW switch through all BW positions. Set input level according to Table 4-12a.
E4	+0.5 Vdc Change as signal is switched on and off.	Q1,CR8	Use Oscilloscope. Adjust generator to achieve 0.5 Vdc change.
U6-10	260 mV		BFO Signal. Set Rcvr to CW mode, -0.4 kHz BFO.

Table 4-13. AM/SSB/CW Demodulator (A2A2) Fault Isolation Table (IF Section) (Cont'd)

Test Point	Normal Signal	Key Components	Comments
E4	0.5 V p-p	U1, CR8, Q1	Set signal generator for 50% AM modulation.
U4-6	0.5 V p-p	U4	Set signal generator for 50% AM modulation.
U6-12	0.6 V p-p 400 Hz	U6	Use Oscilloscope.
U7-1	0.6 V p-p 400 Hz	U7	Use Oscilloscope

4.7.4.2.3 **AGC Section Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-14,** AM/SSB/CW Demodulator (A2A2) Fault Isolation Table (AGC Section). This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.4.2.1,** except leave W1P3 connected to IF input and connect signal generator to RF input A1J1.

2. Set the signal generator as follows:

   a. RF Frequency -- 100.000 MHz
   b. Output Level -- -40 dBm
   c. Modulation -- None

3. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. RF GAIN -- Max. CW
   d. DET. MODE -- AM
   e. IF BW -- Narrowest available
   f. TUNED FREQ -- 100.00 MHz

4. Use an oscilloscope to verify that a 0.5 V p-p signal is present at U4-6. Adjust the signal generator output level slightly as necessary to achieve correct signal level.

5. Use an oscilloscope as indicated, check each test point listed in **Table 4-14.**

6. When a faulty component is found, replace the key component(s) indicated in **Table 4-14.** **Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PCB components.

7. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.2.2,** AM/SSB/CW Demodulator Circuit Description, and **Figure 6-10,** AM/SSB/CW Demodulator Schematic Diagram for additional aid in troubleshooting.

Table 4-14. AM/SSB/CW Demodulator (A2A2) Fault Isolation Table (AGC Section)

Condition	Test Point	Normal Signal	Key Components	Comments
AGC ON	U4-6	0.5 Vdc		Gen. Modulation off.
AGC ON	U7-8	0 Vdc		As U4-6 = 0.5 Vdc U7-8 should be starting negative thru 0 Vdc
AGC ON, Input Signal is 60 dB above level in **Table 4-2.**	U10-8 U10-14 U10-7 U7-7 U7-8	+4.5 Vdc -6 Vdc +5.4 Vdc +11.5 Vdc -4.4 Vdc		
Change gain cont. mode to MAN and set RF Gain control maximum CCW.	U10-8 U10-7 U10-14 U7-7	+5.6 Vdc +8 Vdc -6 Vdc 1.8 Vdc		
AGC ON, DET MODE set to CW, Signal Generator = **Table 4-2.**	U7-14 U7-8	+0.5 Vdc 0 Vdc		As U4-6 = 0.5 Vdc U7-8 should be starting negative thru 0 Vdc
AGC ON, DET MODE set to SSB, Signal Generator = **Table 4-2.**	U7-14 U7-8			As U4-6 = 0.5 Vdc U7-8 should be starting negative thru 0 Vdc
AGC ON, DET MODE set to PULSE, Signal Generator = **Table 4-2.**	U7-14 U7-8	+0.5 Vdc 0 Vdc		As U4-6 = 0.5 Vdc U7-8 should be starting negative thru 0 Vdc

4.7.4.3 Video/Audio/COS (A2A3) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the Video/Audio/COS (A2A3). A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3**) are required to perform the tests outlined below.

4.7.4.3.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Video/Audio/COS:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A2A3.
4. Connect J1 on the receiver rear panel with its mating connector on the EFR100 Equipment Frame.
5. Disconnect W1P3 from IF Input Jack (A2J3). Connect the signal generator RF output to IF Input Jack (A2J3) using a BNC to SMA adaptor.
6. Set the signal generator as follows:

   a. RF Frequency — 21.4 MHz
   b. Output Level — According to **Table 4-12a**
   c. Modulation — None

7. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — Narrowest Available

4.7.4.3.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-15,** Video/Audio/COS (A2A3) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.4.3.1.**

2. Use an oscilloscope to check each test point listed in **Table 4-15.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-15. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.2.3,** Video/Audio/COS Circuit Description, and **Figure 6-11,** Video/Audio/COS Schematic Diagram for additional aid in troubleshooting.

Table 4-15. Video/Audio/COS (A2A3) Fault Isolation Table

Condition	Test Point	Normal Signal	Key Components	Comments
Set signal generator for 50% AM, 1 kHz rate	J2-1	0.25Vpp		Adjust signal generator to obtain level
	U2-6	2Vpp	U2	
	U3-4	2Vpp	U3	
	U5-8	2Vpp		
	E4	7Vpp		
	U4-1	11Vpp		
Using front panel change squelch threshold to verify audio can be turned on and off at U7-15	U7-15		U7	
	U7-16	+5/0 Vdc		
Change DET. MODE to FM, set signal gen. to Freq. = to 21.4 MHz +0.5 x selected IF BW	J2-4	0.5 Vdc		
	U1-6	-1.7 Vdc	U1	
	U3-4	-1.7 Vdc	U3	
	U5-8	-1.7 Vdc	U5	
	U4-7	+6 Vdc	U4	
Set signal gen. for no modulation with level = 30 dB above **Table 4-2.** Set Receiver DET. MODE to AM and Gain Mode to AGC.	U10-3	+1.7 Vdc		
	U6-10	+1.7 Vdc	U10	
	U6-8	+1.7 Vdc	U6	
	U6-14	-3.6 Vdc	U6	
	U6-7	+3.6 Vdc	U6	

4.7.4.4 Digital Interface (A2A4) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the Digital Interface (A2A4). An oscilloscope (see Table 4-3) is required to perform the tests outlined below.

4.7.4.4.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Digital Interface:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A2A4.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Energize the receiver using the power switch on the equipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:

a.	LOCAL/REMOTE	— LOCAL
b.	MAN/AGC	— MAN
c.	RF GAIN	— Max. CW
d.	DET. MODE	— AM
e.	IF BW	— Maximum available

4.7.4.4.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective integrated circuit or functional group of integrated circuits. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.4.4.2.**
2. Use an oscilloscope, verify the external input signals to the Microcontroller (U1) using **Table 4-16.**

Table 4-16. Microcontroller Input Signals

Test Point	Normal Signal	Key Components	Comments
U1-12	Pulse Train 200 ms	U4,U21,U23	INT0
U1-13	Pulse Train 200 ms	U12	INT1
U1-18,19	10 MHz Sine Wave, 5 V	Y1,U1	Clock signal
U1-9	0 Vdc	U20	Reset Signal

3. Use an oscilloscope to verify microcontroller U1 data bus and control signal activity using **Table 4-17.**

Table 4-17. Microcontroller Bus Activity Check

Test Point	Normal Signal	Key Components	Comments
U1 Pin 32-29 (AD0-AD7)	Rapidly changing logic levels on each pin	U1	Observe irregular pulse trains
U1 pin 24-29 (A8-A11)	Rapidly changing logic levels on each pin	U1	
U1-16,17 (WR/RD)	Sharp, negative going pulses, 1 µs	U1	
U1-29 (PSEN)	Square wave, 1 µs	U1	
U1-30 (ALE)	Square wave, 1 µs	U1	

4. Use an oscilloscope to verify I/O signal activity using **Table 4-18.**

Table 4-18. Digital Interface (A2A4) I/O Signal Check

Test Point	Normal Signal	Key Components	Comments
U11 Q0-Q7 outputs	Rapidly changing logic levels	U11	Address Latch
U22 Y0-Y7 outputs	Sharp, negative going pulses	U22	Address Decoder
U3-2	Low	U3	
U3-5	Depends on BW	U3	
U3-6	Depends on BW	U3	
U3-9	Depends on BW	U3	
U3-12	High	U3	
U3-15	Pulse	U3	
U3-16	High	U3	
U3-19	High	U3	
U10-4	+2.5 Vdc	U19	D/A Reference
U10-2	+1 Vdc	U10	MAN Gain Volts
U10-1	0 Vdc	U10	COS THR Volts
U10-20	Depends on Freq.	U10	Tuning Volts
U1 pin 1-7, 14,15	Pulses when tuning	U1	Syn Addr/Data

5. Use the oscilloscope to check the serial data input and output lines of serial interface circuit using **Table 4-19.**

6. When a faulty component is found, replace the key component(s) indicated in the fault isolation tables. **Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as an aid in removing and replacing any PC board components.

Table 4-19. Serial Interface Data Check

Test Point	Normal Signal	Key Components	Comments
U24-9	Sharp negative going pulse	U22,U23	
U12-9	Serial pulse train	U24,U12,U23	Report Data Out
U25-15	Sharp negative going pulse	U22,U23	
U25-2	Serial pulse train	U21	Command Data In

7. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/ tracing/fault isolation is necessary. Refer to **paragraph 3.4.2.5,** Digital Interface Circuit Description, and **Figure 6-12,** Schematic Diagram for additional aid in troubleshooting.

4.7.4.5 FM Demodulator (A2A5) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the FM Demodulator (A2A5), and FM Demodulator modules (A2A5A1 through A2A5A4). A signal generator, an RF voltmeter and an oscilloscope (see **Table 4-3**) are required to perform the tests outlined below.

4.7.4.5.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the FM Demodulator:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A2A5.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.

5. Disconnect W1P3 from IF Input Jack (A2J3). Connect the signal generator RF output to IF input jack (A2J3) using a BNC to SMA adaptor.

6. Set the signal generator as follows:

   a. RF Frequency — 21.4 MHz
   b. Output Level — -60 dBm
   c. Modulation — None

7. Energize the receiver using the power switch on the equipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — AGC
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — Narrowest available

8. Using the RF voltmeter probe tip, verify that a 20 mV rms signal is present at A5P4. Adjust the signal generator output level slightly as necessary to achieve correct signal level.

4.7.4.5.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-20**, FM Demodulator Motherboard (A2A5) Fault Isolation Table, **Table 4-21**, FM Demodulator (10-25 kHz) Fault Isolation Table, **Table 4-22**, FM Demodulator (25-300 kHz) Fault Isolation Table and **Table 4-23**, FM Demodulator (300 kHz-4 MHz) Fault Isolation Table. These tables are used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.4.5.1.**

2. Use an RF voltmeter RF probe tip or oscilloscope to check the FM Motherboard test points listed in **Table 4-20.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-20. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. If **Table 4-20** indicates a faulty FM Demodulator module(s) A2A5A1 through A2A5A4, the module fault may be confirmed by removing it and substituting one of the other three modules in its place. Once the module is confirmed as faulty, refer to either **Table 4-21,**

Table 4-22, or **4-23** as appropriate. Use the RF voltmeter probe tip and an oscilloscope to check each test point listed in the appropriate table. When a faulty signal is found on the FM demodulator module, replace the key components indicated in the fault isolation table. **Paragraph 4.7.7**, Parts Replacement Guidelines, should be referred to as an aid in removing and replacing any PC board components.

5. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.2.4**, FM Demodulator Circuit Description, and **Figure 6-13**, Demodulator Motherboard Schematic Diagram for additional aid in troubleshooting.

Table 4-20. FM Demodulator Motherboard Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
A1 P1-11	+15 V	U1,U2	Select BW #1
A1 P2-1	-15 V	U1,U2	Select BW #1
A2 P1-11	+15 V	U1,U2	Select BW #2
A2 P2-1	-15 V	U1,U2	Select BW #2
A3 P1-11	+15 V	U2,U3	Select BW #3
A3 P2-1	-15 V	U2,U3	Select BW #3
A4 P1-11	+15 V	U2,U3	Select BW #4
A4 P2-1	-15 V	U2,U3	Select BW #4
U5-3	**0.6 Vpp (OR 0.3 Vdc) @ 400 Hz	A1-A4,U5	Select BWs 1 through 4. *FM Deviation = 1/3 IF BW, Frequency modulation = 400 Hz.
U6-6	0 Vdc	U6	No modulation
U6-6	+2.5 Vdc		Set dem = 0, Freq = 21.4 MHz +1/2 + IF BW.

Table 4-20. FM Demodulator Motherboard Fault Isolation Table (Cont'd)

Test Point	Normal Signal	Key Components	Comments
U4-13	250 mVpp @ 400 Hz	U4	Select AM mode. Set generator for 50% AM @ 400 Hz. Select BW1 through BW4.
U2-3	Approx 100 mVdc (Gain Set)	U2,A1-A4	Select BW1-BW4
* If signal generator cannot be deviated by 1/3 the IF Bandwidth, set the signal generator to 21.4 MHz (no modulation) + 1/3 x selected IF Bandwidth. ** DC offset may be observed with the cover removed.			

Table 4-21. FM Demodulator (10-25 kHz) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U1-5	700 mVrms @ 21.4 MHz	U1,VR1,VR2	
U2-14	1.2 Vpp @ 400 Hz	Y1,CR1,CR2,U2	FM Deviation = 1/3 IF BW

Table 4-22. FM Demodulator (25-300 kHz) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U1-5	1000 mVrms @ 21.4 MHz	U1,VR1,VR2	
U2-14	1.2 Vpp @400 Hz	CR1,CR2,U2	FM Deviation = 1/3 IF BW

Table 4-23. FM Demodulator (300 kHz–4 MHz) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U1-5	700 mVrms	U1,VR1	
U2-6	600 mVpp	T1,CR1,CR2,U2	FM Deviation = 1/3 IF BW

4.7.5 SYNTHESIZER (A3) TESTING AND TROUBLESHOOTING

4.7.5.1 Time Base (A3A2) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the Time Base (A3A2). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.1.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Time Base:

1. Deenergize the receiver.

2. Remove the receiver from the EFR100 Equipment Frame.

3. Remove the necessary subassembly covers to provide access to module A3A2.

4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.

5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — Maximum available
   f. TUNED FREQ — 500.000 MHz

8. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.1.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-24,** Time Base (A3A2) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.1.1.**

2. Use an oscilloscope or frequency counter to check each test point listed in **Table 4-24.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-24. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as an aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.1,** Time Base Circuit Description, and **Figure 6-15,** Time Base Schematic Diagram for additional aid in troubleshooting.

Table 4-24. Time Base (A3A2) Fault Isolation Table

Test Point	Normal Signal	Key Components
E1	0 dBm @ 50.000000 MHz	Freq. Reference
U2,U3 Pin 1	-9 dBm	Splitter Components
E2,E3	+5 dBm	U2,U3
U3-1	-13 dBm	Splitter
E3	0 dBm	U3

4.7.5.2 **2nd LO VCO (A3A3) Testing and Troubleshooting**

This paragraph describes the procedures needed to test, troubleshoot and repair the 2nd LO VCO (A3A3). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.2.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior to testing or troubleshooting the 2nd LO VCO:

1. Deenergize the receiver.

2. Remove the receiver from the EFR100 Equipment Frame.

3. Remove the necessary subassembly covers to provide access to module A3A3.

4. Connect J1 on the receiver rear panel with its mating connector on the EFR100 Equipment Frame.

5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — Maximum available
   f. TUNED FREQ — 300.0000 MHz

6. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.2.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-25**, 2nd LO VCO (A3A3) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.2.1.**

2. Use an oscilloscope or frequency counter to check each test point listed in **Table 4-25.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-25. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.2,** 2nd LO VCO Circuit Description, and **Figure 6-16,** 2nd LO VCO Schematic Diagram for additional aid in troubleshooting.

Table 4-25. 2nd LO VCO (A3A3) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U2-1	+5 Vdc	U2	
U3-3	+11 Vdc	U3	
Q1-C	+1 Vdc	Q1 High Band Switch	
E7	+9 Vdc	A3A4	Tuning Voltage
R8	+10 dBm @105.2 MHz	Q3	VCO
U4-1	-3 dBm	U4	
U5-2	+8 dBm	U5	
U6-5,6	+5 dBm	U6	2nd LO output
Q2-E	+1 Vdc	Q2	
E7	+9 Vdc	A3A4	Tuning Voltage
U4-1	-3 dBm @ 305.2 MHz	Q4,U4	

4.7.5.3 **2nd LO PLL (A3A4) Testing and Troubleshooting**

This paragraph describes the procedures needed to test, troubleshoot and repair the 2nd LO PLL (A3A4). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.3.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior to testing or troubleshooting the 2nd LO PLL:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A3A4.

4. Connect J1 on the receiver rear panel with its mating connector on the EFR100 Equipment Frame.

5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. RF GAIN -- Max. CW
   d. DET. MODE -- AM
   e. IF BW -- Maximum available
   f. TUNED FREQ -- 20.0000 MHz

8. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.3.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-26**, 2nd LO PLL (A3A4) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.3.1.**

2. Use an oscilloscope or frequency counter to check each test point listed in **Table 4-26.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-26.** **Paragraph 4.7.7**, Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.3**, 2nd LO PLL Circuit Description, and **Figure 6-17**, 2nd LO PLL Schematic Diagram for additional aid in troubleshooting.

Table 4-26. 2nd LO PLL (A3A4) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U6-1	+5 Vdc	U6	
U5-1	+15 Vdc	U5	

Table 4-26. 2nd LO PLL (A3A4) Fault Isolation Table (Cont'd)

Test Point	Normal Signal	Key Components	Comments
U4-5	-2 mVpp @208 MHz	A3A6	AUX VCO In
U3-12	+9 Vdc	U4	
U3-4	2 Vpp @2.6 MHz	A3A8	IF In
U3-7	+5 Vdc	U3	
U3-9	+5 Vdc		
U2-5	Sharp positive going pulses	U2	PLL Out
E1	+9 Vdc	U1	Tuning Voltage Out

4.7.5.4 **AUX PLL/Phase Detector (A3A5) Testing and Troubleshooting**

This paragraph describes the procedures needed to test, troubleshoot and repair the Aux PLL/Phase Detector (A3A5). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.4.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior totesting or troubleshooting the AUX PLL/Phase Detector A3A5:

1. Deenergize the receiver,
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A3A5.
4. Connect J1 on the receiver rear panel with its mating connector on the EFR100 Equipment Frame.
5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

a. LOCAL/REMOTE -- LOCAL
b. MAN/AGC -- MAN
c. RF GAIN -- Max. CW
d. DET. MODE -- AM
e. IF BW -- Maximum available

6. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.4.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-27**, AUX PLL/Phase Detector (A3A5) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.4.2.**

2. Use an oscilloscope or frequency counter to check each test point listed in **Table 4-27.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-27. Paragraph 4.7.7**, Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.4**, AUX PLL/Phase Detector Circuit Description, and **Figure 6-18**, AUX PLL/Phase Detector Schematic Diagram for additional aid in troubleshooting.

Table 4-27. AUX PLL/Phase Detector (A3A5) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U5-1	+5 Vdc	U5	
U6-1	+24 Vdc	U6	
U1-12	+5 V @5 MHz	U12	Time Base Reference

Table 4-27. AUX PLL/Phase Detector (A3A5) Fault Isolation Table (Continued)

Test Point	Normal Signal	Key Components	Comments
U3-5	-6 dBm	A3A6	AUX VCO In
U3-3	+4 V 2.6 MHz	U3	Prescaler Out
U2 Pin 11-17	Rapidly changing logic levels	IF Demod A2	Syn Addr/Data Bus
U2-1	Sharp positive going pulses	U2	PLL Out
E2	+14 Vdc	U4	

4.7.5.5 **AUX VCO (A3A6) Testing and Troubleshooting**

This paragraph describes the procedures needed to test, troubleshoot and repair the AUX VCO (A3A6). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.5.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior to testing or troubleshooting the AUX VCO (A3A6):

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A3A6.
4. Interconnect J1 on the receiver rear panel with its mating connector on the EFR100 Equipment Frame.
5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. RF GAIN -- Max. CW

d. DET. MODE -- AM
e. IF BW -- Maximum available
f. TUNED FREQ -- 20.0000 MHz

8. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.5.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-28,** AUX VCO (A3A6) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.5.2.**

2. Using an oscilloscope or frequency counter to check each test point listed in **Table 4-28.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-28. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.5,** AUX VCO Circuit Description, and **Figure 6-19,** AUX VCO Schematic Diagram for additional aid in troubleshooting.

Table 4-28. AUX VCO (A3A6) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U1-3	+11.07 Vdc	U1	
U5-1	+5 Vdc	U5	
E5	+14 Vdc	A3A5	Tuning Voltage
Q1-1	-5 dBm @208 MHz	Q1	Use RF Voltmeter
U3,U4 pin 2	-4 dBm @208 MHz	U2,U3,U4	Use RF Voltmeter

4.7.5.6 BFO Assembly (A3A7) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the BFO Assembly (A3A7). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.6.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the BFO Assembly (A3A7):

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A3A7.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

a.	LOCAL/REMOTE	— LOCAL
b.	MAN/AGC	— MAN
c.	RF GAIN	— Max. CW
d.	DET. MODE	— CW
e.	IF BW	-- Maximum available
f.	BFO OFFSET	— 0.0 kHz

8. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.6.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-29**, BFO Assembly (A3A7) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.6.1.**
2. Using an oscilloscope or frequency counter as indicated, check each test point listed in **Table 4-29.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-29.** **Paragraph 4.4.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.6,** BFO Assembly Circuit Description, and **Figure 6-20,** BFO Assembly Schematic Diagram for additional aid in troubleshooting.

Table 4-29. BFO Assembly (A3A7) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U10-1	+5 Vdc	U10	
E1	+5 V @5 MHz	A3A5	Time Base Reference
U7-1	0 dBm @120 MHz	Q2,Q3	VCO Out Use RF Voltmeter
U8-5	-3 dBm	U7	Use RF Voltmeter
U8-3	4 Vpp	U8	Prescaler Out Use RF Voltmeter
U3-1	+3 Vdc	U3	
U5-4	Low level clock @0.6 MHz	U6,U1	
U2-9	+5 V @2.5 MHz	U1	
Q1-C	5 Vpp @ 20.80000 MHz	Q1,Y1	Use RF Voltmeter
U2-1	5 Vpp @25 kHz	U4	
U3-7	+2.5 Vdc	U3	
E3	500 mVpp @21.4 MHz	FL1, T1, U5	BFO Out

4.7.5.7 Reference Mixer (A3A8) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the Reference Mixer (A3A8). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.7.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Reference Mixer (A3A8):

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A3A8.
4. Connect J1 on the receiver rear panel with its mating connector on the EFR100 Equipment Frame.
5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

a.	LOCAL/REMOTE	— LOCAL
b.	MAN/AGC	— MAN
c.	RF GAIN	— Max. CW
d.	DET. MODE	— AM
e.	IF BW	— Maximum available
f.	TUNED FREQ	— 20.0000 MHz

8. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.7.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-30**, Reference Mixer (A3A8) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.7.2.**
2. Use an oscilloscope or frequency counter to check each test point listed in **Table 4-30.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-30.** **Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.7,** Reference Mixer Circuit Description, and **Figure 6-21,** Reference Mixer Schematic Diagram for additional aid in troubleshooting.

Table 4-30. Reference Mixer (A3A8) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U1-1	+2 dBm @ 305.2 MHz	A3A3	2nd LO Signal
U1-7	-13 dBm @ 152.6 MHz	U1	
U3-1	-13 dBm @ 152.6 MHz	U2	
U5-8	+2 dBm @ 50.000000 MHz	Splitter Components	50 MHz Reference
U5-1	0 dBm @ 100.000000 MHz	T1,U6	
U5-4	+3 dBm	U5	50 and 150 MHz signals present simultaneously
U3-8	+8 dBm	U4	50 and 150 MHz signals present simultaneously
E3	2 Vpp 2.6 MHz	U3,Q1	

4.7.5.8 **1st LO Phase Detector/Divider (A3A9) Testing and Troubleshooting**

This paragraph describes the procedures needed to test, troubleshoot and repair the 1st LO Phase Detector/Divider (A3A9). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.8.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the 1st LO Phase Detector/Divider (A3A9):

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module (A3A9).
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Energize the receiver using the power switch on the equipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — Maximum available
   f. TUNED FREQ — 20.0000 MHz

8. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.8.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-31**, 1st LO Phase Detector/Diver (A3A9) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.8.2.**
2. Use an oscilloscope or frequency counter to check each test point listed in **Table 4-31.**
3. When a faulty component is found, replace the key component(s) indicated in **Table 4-31. Paragraph 4.7.7**, Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.
4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.8**, 1st LO Phase Detector/Divider Circuit Description, and **Figure 6-22**, 1st LO Phase Detector/Divider Schematic Diagram for additional aid in troubleshooting.

Table 4-31. 1st LO Phase Detector/Divider (A3A9) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U8-1	+5 Vdc	U8	
U6-3	+24 Vdc	U6	
U5-1	-5 dBm @ 34.6 MHz	A3A10	1st LO Signal Use RF Voltmeter
U2-5	200 mVrms @ 173.3 MHz	U5	Use RF Voltmeter
U1-4	4 Vpp @ 4.3 MHz	U2	Prescaler Out Use RF Voltmeter
U1-7	4 Vpp sinewave @ 5.000000 MHz	A3A5, Y1	Time Base Reference
U1-18	Sharp Negative going pulses	U1	
U1-1	+2.5 V	U1	PLL Out
E2	+4 Vdc	U3	Tuning Voltage

4.7.5.9 1st LO Assembly (A3A10) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the 1st LO Assembly (A3A10). An oscilloscope and a frequency counter (see **Table 4-3**) are required to perform the tests outlined below.

4.7.5.9.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the 1st LO Assembly (A3A10):

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A3A10.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.

5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. RF GAIN -- Max. CW
   d. DET. MODE -- AM
   e. IF BW -- Maximum available
   f. TUNED FREQ -- 360.0000 MHz

6. Verify that a 50.000000 MHz, 0 dBm reference signal is present at A3J2.

4.7.5.9.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-32,** 1st LO Assembly (A3A10) Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.5.9.1.**

2. Using an oscilloscope or frequency counter to check each test point listed in **Table 4-32.**

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-32. Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as a aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.3.9,** 1st LO Assembly Circuit Description, and **Figure 6-23,** 1st LO Assembly Schematic Diagram for additional aid in troubleshooting.

Table 4-32. 1st LO Assembly (A3A10) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
U4-3	+21 Vdc	U4	
U3-1	+15 Vdc	U3	
U2-1	-15 Vdc	U2	

Table 4-32. 1st LO Assembly (A3A10) Fault Isolation Table

Test Point	Normal Signal	Key Components	Comments
E6	+5 Vdc	IF Demod, A2	LO VCO Select
Q2-C	+1 Vdc	Q2	
E9	+4 Vdc	A3A9	Tuning Voltage
E5	+5 Vdc	IF Demod, A2	LO Band Select
U1-6	+5 Vdc	U1	
U5-6	-6 dBm @ 486.6 MHz	Q5,CR8-CR10	Use RF Voltmeter
E5	0 Vdc	IF Demod, A2	Tune Rcvr to 460 MHz
U1-6	0 Vdc	U1	
U5-6	586.6 MHz	CR11	
E6	0 Vdc	IF Demod, A2	Tune Rcvr to 20 MHz
Q1-C	+1 Vdc	Q1,Q3	
E9	+5 Vdc	A3A9	Tuning Voltage
E5	+5 Vdc	IF Demod, A2	
U5-5	-6 dBm @ 346.6 MHz	Q4,CR1,3,6,7	Use RF voltmeter
E5	0 Vdc	IF Demod, A2	Tune Rcvr to 100 MHz
U5-5	426.6 MHz	CR7	
E7,E8	+3 dBm @ 426.6 MHz	U5,U6,U7	Use RF Voltmeter

4.7.6 DIGITAL CONTROL (A4) TESTING AND TROUBLESHOOTING

4.7.6.1 Remote I/O Interface Option (A4A2) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the Remote I/O Interface Option. An oscilloscope (see **Table 4-3**) is required to perform the tests outlined below.

4.7.6.1.1 Preliminary Setup Procedure

The following preliminary setup steps should be performed prior to testing or troubleshooting the Optional Digital I/O, RS-232:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A4A2.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE -- LOCAL
   b. MAN/AGC -- MAN
   c. RF GAIN -- Max. CW
   d. DET. MODE -- AM
   e. IF BW -- Maximum available

6. If a Receiver/Controller is available, use the oscilloscope to verify UART activity using **Table 4-33.** If no Receiver/Controller is available, this step may be ignored.

4.7.6.1.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to several fault isolation tables. These tables are used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.6.1.1.**
2. Use the oscilloscope to verify the UART and I/O signal/data activity using **Tables 4-33** and **4-34.** Activity should be checked in conjunction with sending commands from a remote terminal to the IOM108.

Table 4-33. UART Activity Signal Check

Test Point	Normal Signal	Key Components	Comments
U4-25	Short bursts of 25 µsec prr pulses, each 100 µsec apart	U4	Present when receiver transmits to the IOM108.
U4-20	Short bursts of 25 µsec prr pulses, each 100 µsec apart	U2, U5	Present when IOM108 transmits to the receiver.
U4-13, 14, 15	Sharp negative going pulse, 200 µsec prr	U4	
U1-6	Short bursts of 25 µsec pulses; each burst 100 µsec apart	U1, U3, U9	Present when receiver transmits to IOM108.

Table 4-34. I/O Signal Activity Check

Test Point	Normal Signal	Key Components	Comments
U6-Q1 to Q8 outputs	Pulse train, less than 1 µsec prr	U6	
U8-Q1 to Q8 outputs	Pulse train, less than 1 µsec prr	U8	
U7-Y0, Y1, Y2, Y3, Y4	Pulse train, less les than 1 µsec prr	U11, U8, U7, U3, U9	Present when WJ-9040 serial I/O occurs.
U3-12	Low-going pulse	U3, U11, U9	Present when UART is ready to transmit or receive.

3. When a faulty component is found, replace the key component(s) indicated in the tables. **Paragraph 4.7.7**, Parts Replacement Guidelines, should be referred to as an aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal

tracing/fault isolation is necessary. Refer to **paragraph 3.4.4.4,** Remote I/O Interface Option Circuit Description, and **Figure 6-26,** Remote I/O Interface Option Schematic Diagram for additional aid in troubleshooting.

4.7.6.2 CPU, A4A3, Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the Extended CPU (A4A3). An oscilloscope (see **Table 4-3**) is required to perform the tests outlined below.

4.7.6.2.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Extended CPU:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A4A3.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.
5. Energize the receiver using the power switch on the equipment frame power supply. Using the receiver front panel keypad and display, set the receiver to the following parameters:

a.	LOCAL/REMOTE	-- LOCAL
b.	MAN/AGC	-- MAN
c.	RF GAIN	-- Max. CW
d.	DET. MODE	-- AM
e.	IF BW	-- Maximum available

4.7.6.2.2 Testing and Troubleshooting Procedure

The testing and troubleshooting information contained in this paragraph is keyed to several fault isolation tables. These tables are is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.6.3.1.**
2. Use an oscilloscope to verify the external input signals to the Microcontroller (U1) using **Table 4-35.**

Table 4-35. Microcontroller Input Signal Check

Test Point	Normal Signal	Key Components	Comments
U1-11	Clock signal, 4.9152 MHz	U2,U3,Y1	
U1-33	+5 Vdc	R2,C3	Power Up Reset
U1-36	+5 Vdc	R10	
U1-21	+5 Vdc	U11,CR2,CR3	
U1 pin 22-25	+5 Vdc		

3. Use an oscilloscope to verify Microcontroller (U1) data bus and control signal activity using **Table 4-36.**

Table 4-36. Microcontroller Bus Activity Check

Test Point	Normal Signal	Key Components	Comments
U1 pin 12-19	Pulse train, less than 1 µs prr.	U1,U4,U5,U6,U7, U8,U12	
U1 pin 1-8	Pulse train, less than 1 µs prr.	U1,U4,U5,U6,U7, U8,U12	
U1-31,32	Pulse train, less than 1 µs prr.	U1,U4,U5,U6,U7, U8,U12	
U1-30,34	Pulse train, 0.4 µs prr	U1,U4,U5,U6,U7, U8,U12	
U1-9	Clock Pulse	U1	

4. Use an oscilloscope to verify I/O signal activity using **Table 4-37.**

5. When a faulty component is found, replace the key component(s) indicated in the tables. **Paragraph 4.7.7,** Parts Replacement Guidelines, should be referred to as an aid in removing and replacing any PC board components.

Table 4-37. Extended CPU I/O Signal Check

Test Point	Normal Signal	Key Components	Comments
U6 pin 11-18	Pulse train, less than 1 µs prr.	U6	
U4 Q1 to Q8	Pulse train, less than 1 µs prr.	U4	
U5 pin 12-15	Square wave, 1 ms prr.	U3,U5,U10	
U12 pin 12-15	Square wave, 1 ms prr.	U10,U12	

6. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.4.4.1**, Extended CPU Circuit Description, and **Figure 6-27**, Extended CPU Schematic Diagram for additional aid in troubleshooting.

4.7.6.3 Receiver/EF Interface (A4A5) Testing and Troubleshooting

This paragraph describes the procedures needed to test, troubleshoot and repair the Receiver/EF Interface (A4A5). An oscilloscope (see **Table 4-3**) is required to perform the tests outlined below.

4.7.6.3.1 Preliminary Setup Procedure

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Receiver/EF Interface:

1. Deenergize the receiver.
2. Remove the receiver from the EFR100 Equipment Frame.
3. Remove the necessary subassembly covers to provide access to module A4A5.
4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.

5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

a. LOCAL/REMOTE — LOCAL
b. MAN/AGC — MAN
c. RF GAIN — Max. CW
d. DET. MODE — AM
e. IF BW — Maximum available

4.7.6.3.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-38**, Receiver/EF Interface Control Signal/Data Activity Check. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure in outlined **paragraph 4.7.6.4.1.**

2. Use an oscilloscope to verify control signal/data activity indicated in the following table.

3. When a faulty component is found, replace the key component(s) indicated in **Table 4-38. Paragraph 4.7.7**, Parts Replacement Guidelines, should be referred to as an aid in removing and replacing any PC board components.

Table 4-38. Receiver/EF Interface Control Signal/Data Activity Check

Test Point	Normal Signal	Key Components	Comments
U7 pin 12,15, 16,6,9	Pulse train, less than 1 µs prr.	U7	
U8 Y0-Y7	Square wave, 1 msec PW.	U8,U9	
U6 Q0-Q7	Pulse train, less than 1 µs prr.	U6	
U11-9	Serial data stream	U11,U10	
U12-7	Serial data stream	U12,U9	

Table 4-38. Receiver/EF Interface Control Signal/Data Activity Check (Cont'd)

Test Point	Normal Signal	Key Components	Comments
U4-2	Serial data stream		
U4-3	Clock signal	U6	
U4-15	Pulse train	U9	
U3-2	Serial data stream		
U3-3	Clock signal	U9	
U3-15	Pulse train less than 1 µs prr.	U10	
U13 pin 3,14	Pulse train, less than 1 µmsec prr.	U13,U14	
U1-8	Pulse train, less than 1 msec prr.	U1,U2,U9	

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.3.5.3** Receiver/EF Interface Circuit Description, and **Figure 6-28**, Receiver/EF Interface Schematic Diagram for additional aid in troubleshooting.

4.7.6.4 **Front Panel Interface (A4A6) Testing and Troubleshooting**

This paragraph describes the procedures needed to test, troubleshoot and repair the Front Panel Interface (A4A6). An oscilloscope (see **Table 4-3**) is required to perform the tests outlined below.

4.7.6.4.1 **Preliminary Setup Procedure**

The following preliminary setup procedure should be performed prior to testing or troubleshooting the Front Panel Interface (A4A6):

1. Deenergize the receiver.

2. Remove the receiver from the EFR100 Equipment Frame.

3. Remove the necessary subassembly covers to provide access to module A4A6.

4. Connect J1 on the receiver rear panel to its mating connector on the EFR100 Equipment Frame.

5. Energize the receiver using the power switch on the equipment frame power supply. Use the receiver front panel keypad and display to set the receiver to the following parameters:

   a. LOCAL/REMOTE — LOCAL
   b. MAN/AGC — MAN
   c. RF GAIN — Max. CW
   d. DET. MODE — AM
   e. IF BW — Maximum available

4.7.6.4.2 **Testing and Troubleshooting Procedure**

The testing and troubleshooting information contained in this paragraph is keyed to **Table 4-39**, Front Panel Interface Fault Isolation Table. This table is used to isolate the module fault to a defective stage or circuit. Perform the following procedures in the sequence given.

1. Perform the preliminary setup procedure outlined in **paragraph 4.7.6.5.1.**

2. Use an oscilloscope to verify control signal/data activity as indicated in the following table.

Table 4-39. Front Panel Interface Control Signal/Data Activity Check

Test Point	Normal Signal	Key Components	Comments
U6 Q1-Q8	Pulse train, less than 1 µs prr.	U6	
U8 Y0-Y7	Square wave, 1 msec PW.	U8,U7	
U5 Q6-Q8	Pulse train, less than 1 µs prr.	U5	
U2-3	Audio signal	U1,U2,U3	
U4-2	-1.5 Vdc	U1	A/D Reference

Table 4-39. Front Panel Interface Control Signal/Data Activity Check (Cont'd)

Test Point	Normal Signal	Key Components	Comments
U4-17	Clock signal	U4	
U4-14	Sharp negative going pulse	U4	
U10-12	Serial data stream	U10,U11, Keyboard	Present when keypad is depressed
U11-12	Serial data stream	U10,U11, Keyboard	Present when keypad is depressed
U12-5	Square wave pulses	U12,U13, Tuning Encoder	Present when tunewheel is rotated
U12-9	Square wave pulses	U12,U13 Tuning encoder	High when tunewheel is rotated clockwise, low when counter-clockwise

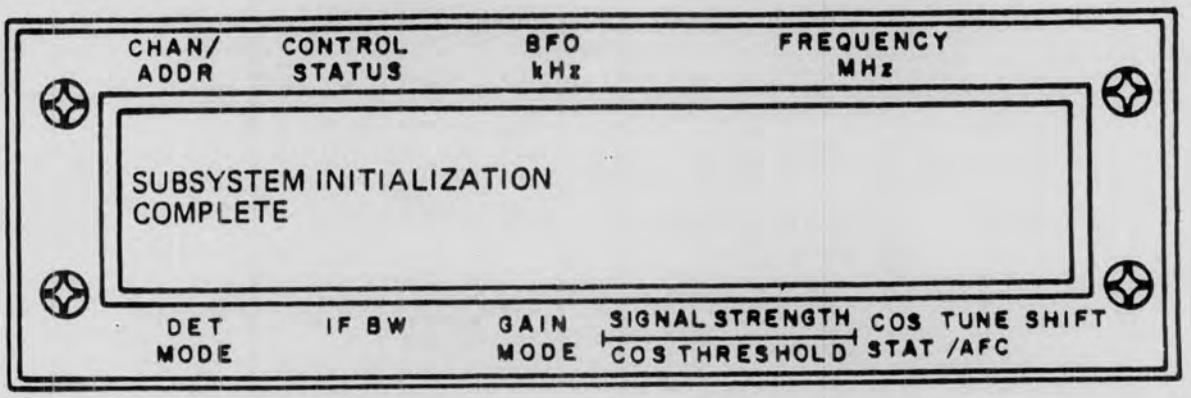
3. When a faulty component is found, replace the key component(s) indicated in **Table 4-39. Paragraph 4.4.7**, Parts Replacement Guidelines, should be referred to as an aid in removing and replacing any PC board components.

4. Replacement of the indicated key component(s) will normally restore the faulty test point signal to a normal level. If a faulty signal is still observed after key component replacement, additional signal tracing/fault isolation is necessary. Refer to **paragraph 3.3.5.4**, Front Panel Interface Circuit Description, and **Figure 6-29**, Front Panel Interface Schematic Diagram for additional aid in troubleshooting.

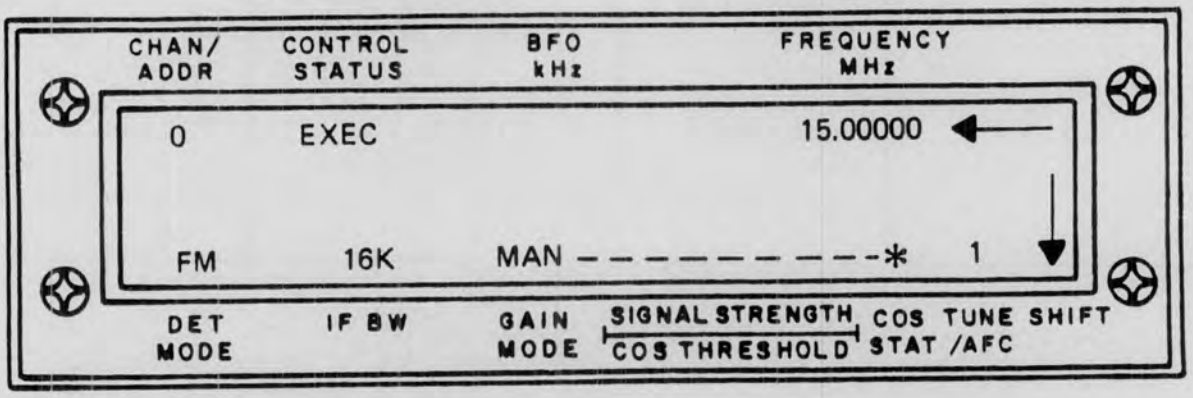
4.7.7 FUNCTIONAL TEST VIA WJ-9040 SERIAL INTERFACE (OPTION)

This paragraph describes the procedure for testing the operation of the WJ-9040 System Common Equipment by communicating through the WJ-9040 High Speed Serial Interface Port. A test bed consisting of an EFR100 Equipment Frame, one HF or VHF receiver/controller (option MHO), and one remotely controllable WJ-9040 receiving module are required to perform this test. This test is based on the front panel operator sequences defined for the WJ receiver/controllers. Perform the following procedures in the sequence given:

1. Energize the EFR100 Equipment Frame. The receiver/controller should display the following message briefly:



This will be replaced by a display of the receiver/controller status, shown typically as follows:



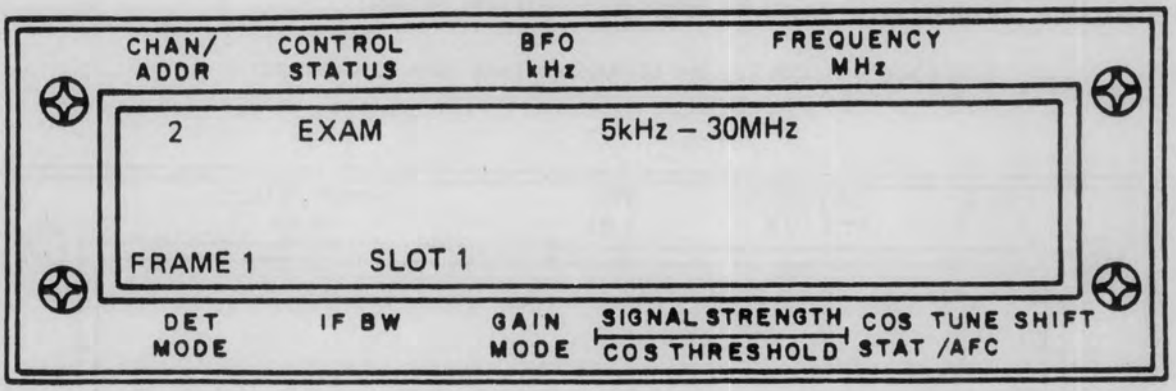
NOTE

A failure of the serial I/O, polled or EFR100 backplane will result in the message:

"I/O ERROR ON POWERUP ENTER (11) (OPR AID)"

2. Enter the following keystrokes on the receiver/controller keypad:
   2 EXAM

   The receiver/controller should display the following:

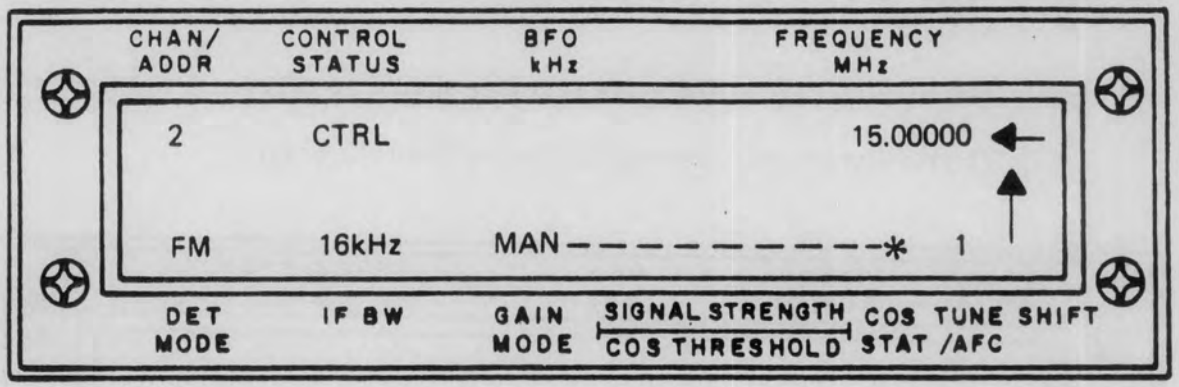


NOTE

The frequency range indication may vary depending upon the type of slave unit used.

3. Enter the following keystrokes on the receiver/controller kaypad:
   2 CTRL

   The receiver/controller should display the following:



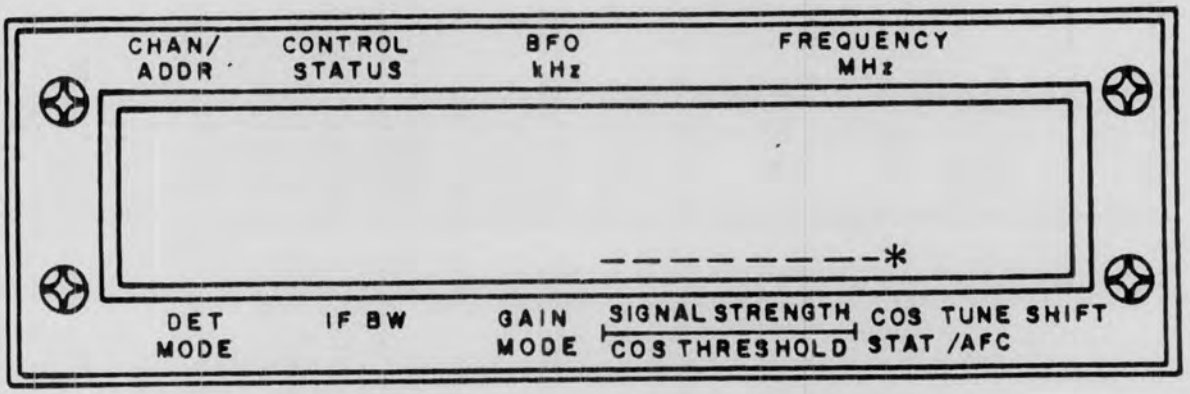
NOTE

The status parameters (i.e., frequency, bandwidth) may be different.

4. Enter the following keystrokes on the receiver/controller keypad: 0 COS

The squelch light on the slave receiver should go on.

The receiver/controller should display the following:



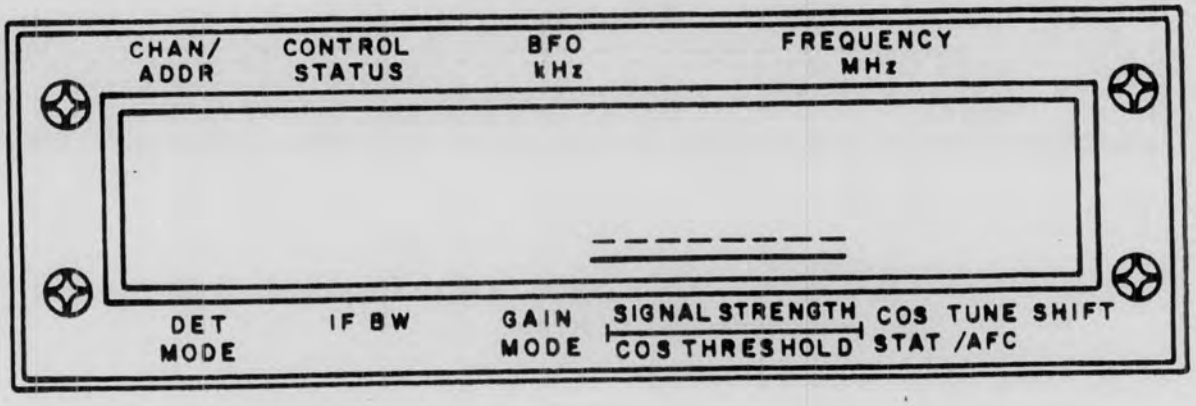
NOTE

Verify that the asterisk above COS STAT is displayed.

5. Enter the following keystrokes on the receiver/controller keypad: 63 COS

The squelch ligh on the slave receiver should go off.

The receiver/controller should display the following:



NOTE

Verify that the asterisk above COS STAT is erased.

6. Leave the receiver/controller in the 2 CTRL mode. Connect a signal generator to the RF input of the slave receiver in the EFR100 frame. Set the generator as follows:

   HF Receiver-Generator frequency: 15.00000 MHz
   Generator level: -50 dBm

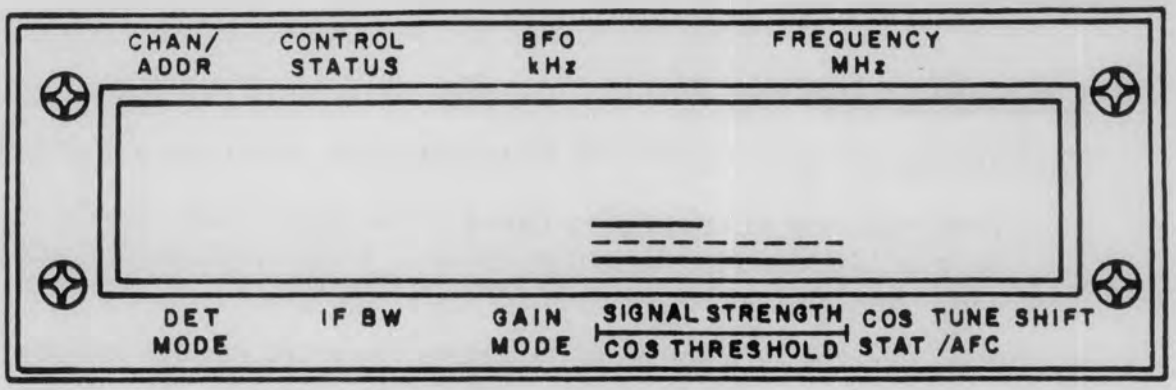
   VHF Receiver-Generator frequency: 100.00000 MHz
   Generator level: -50 dBm

7. Enter the following keystrokes on the receiver/controller keypad:

   HF Receiver - 1 5 Mhz
   VHF Receilver - 1 0 0 MHz

   Use the main keypad to select AGC FST gain mode.

8. The signal strength bar on the receiver/controller display should deflect approximately half scale s shown below:



9. If AFC mode is enabled, indicated by the letter "A" above TUNE/AFC, disable AFC by pressing the AFC keypad.

10. Note the slave receiver IF bandwidth displayed on the receiver/controller. Slowly change the signal generator frequency by an amount equal to one-half the displayed bandwidth. The tune indicator on the display should slowly move left and right as it tracks the signal generator frequency change.

11. Remove the 50 MHz reference input to the slave receiver. The receiver/controller should blink "UNLOCK" over the frequency display area.

12 Each of the above steps should be repeated for slots 2 through 8. Deenergize the frame and move the receiver extension cable to the next frame connector before repeating the procedure.

4.7.8 PARTS REPLACEMENT GUIDELINES

This paragraph provides techniques to assist the technician in replacing components on PC boards.

WARNING

To prevent electrical shock or damage to the unit, always disconnect the receiver from the AC power source before soldering or replacing components.

4.7.8.1 Soldering Techniques

When removing components from a printed circuit board for inspection or replacement, be especially careful not to damage the track. The soldering iron power should be no higher than 40 watts, and a solder sipper or wicking procedure should be employed when removing solder. Noncorrosive solder flux should be used when removing solder by wicking. In returning components to the board, make sure that holes are clear and that leads do not catch the edge of the track and lift it from the board. A good grade of rosin core 60/40 solder should be used. Do not heat longer than is necessary to achieve a good joint. A heat sink should be used where possible.

4.7.8.2 Component Replacement

The following are specific guidelines for replacing the various kinds of components:

1. When soldering or unsoldering diodes or resistors, solder quickly to allow as little heat conduction as possible. When wiring permits, use a heat sink between the soldering iron and the part.

2. When soldering or unsoldering transistors, use a low wattage iron and a heat sink. Solder as quickly as possible. The use of a circular solder tip to heat all three joints simultaneously is recommended.

3. When soldering or unsoldering glass or ceramic capacitors, use a heat sink between the capacitor and the iron. Excessive heat will crack the capacitor body.

4. When any electronic part is removed, note the position of the part and its leads, and replace it the same way.

SECTION V

REPLACEMENT PARTS LIST

5.1 UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations (electrical symbol numbers) has been used to identify assemblies, subassemblies (and modules) and parts. An example of the unit numbering method follows:

Subassembly Designation A1	R1 Class and No. of Item
Identify from right to left as:	First (1) resistor (R) of first (1) subassembly (A)

As shown on the main chassis schematic, components which are an integral part of the main chassis have no subassembly designation.

5.2 REFERENCE DESIGNATION PREFIX

Partial reference designations have been used on the equipment and on the illustrations in this manual. The partial reference designations consist of the class letter(s) and identifying item number. The complete reference designations may be obtained by placing the proper prefix before the partial reference designations. Reference Designation Prefixes are provided on drawings and illustrations in parentheses within the figure titles.

5.3 LIST OF MANUFACTURERS

Mfr. Code	Name and Address
00779	AMP, Incorporated P.O. Box 3608 Harrisburg, PA 17105
01121	Allen-Bradley Company 1201 South 2nd Street Milwaukee, WI 53204
01295	Texas Instruments, Inc. Semiconductor-Components Div. 15300 North Central Expressway Dallas, TX 75231
02735	RCA Corporation Solid State Division Route 202 Somerville, NJ 08876
04013	Taurus Corporation 1 Academy Hill Lambertville, NJ 08530
04213	Caddell-Burns Mfg. Co., Inc. 40 E. Second Street Mineola, NY 11501
04713	Motorola Incorporated Semiconductor Products Div. 5005 East McDowell Road Phoenix, AZ 85008
06776	Robinson-Nugent, Inc. 800 E. 8th Street Albany, IN 47150

Mfr. Code	Name and Address
07263	Fairchild Camera & Instr. Corp. Semiconductor Division 464 Ellis Street Mountain View, CA 94040
09021	Airco Inc. Airco Electronics Bradford, PA 17055
12498	Teledyne Crystalonics Division of Teledyne Industries, Inc. 147 Sherman Street Cambridge, MA 02140
12969	Unitrode Corp. 5 Forbes Road Lexington, MA 02173
14193	CAL-R, Inc. 1601 Olympic Blvd P.O. Box 1397 Santa Monica, CA 90404
14482	Watkins-Johnson Co. 3333 Hillview Avenue Palo Alto, CA 94304
14632	Watkins-Johnson Co. 700 Quince Orchard Road Gaithersburg, MD 20878
15542	Mini-Circuits Laboratories Division of Scientific Components Corp. 2625 E. 14th Street Brooklyn, NY 11235
17856	Siliconix, Inc. 2201 Laurelwood Road Santa Clara, CA 95050
18324	Signetics Corporation 811 East Arques Avenue Sunnyvale, CA 94086
19505	Applied Eng. Products, Co. Division of Samarious, Inc. 300 Seymour Avenue Derby, CT 06418
22526	Du Pont El De Nemours and Co. Inc., Photo Products Dept. Berg Electronics Div., Rt. 83 New Cumberland, PA 17070
24355	Analog Devices, Inc. Route 1 Industrial Park P.O. Box 280 Norwood, MA 02062
24539	Avantek, Inc. 3175 Bowers Avenue Santa Clara, CA 95051
26805	MA-COM Omni Spectra, Inc. 140 Fourth Avenue Walton, MA 02154
27014	National Semi-Conductor Corp. 2950 San Ysidro Way Santa Clara, CA 95051
27956	Relcom 3333 Hillview Avenue Palo Alto, CA 94304
28480	Hewlett-Packard Company Corporate Headquarters 1501 Page Mill Road Palo Alto, CA 94304

Mfr. Code	Name and Address
29990	American Technical Ceramics One Norden Lane Huntington Station, NY 11746
32293	Intersil Inc. 10600 Ridge View Court Cupertino, CA 95014
33095	Spectrum Control, Inc. 152 E. Main Street Fairview, PA 16415
34649	Intel Corp. 3065 Bowers Avenue Santa Clara, CA 95051
51406	Morata Erie North America, Inc. 1148 Franklin Road, SE Marietta, GA 30067
52648	Plessey Trading Corp. Plessey Optoelectronics and Microwave 1641 Kaiser Avenue Irvine, CA 92714
52673	KSW Electronics Corp. Burlington, MA 01803
54473	Matsushita Electric Corp. One Panasonic Way P.O. Box 1501 Secaucus, NJ 07094
55322	Samtec, Inc. 810 Progress Blvd. P.O. Box 1147 New Albany, IN 47150
56289	Sprague Electric Company Marshall Street North Adams, MA 01247
59660	Tusonix, Inc. 2155 N. Forbes Blvd. Tucson, AZ 85745
71279	Cambridge Thermionic Corp. 445 Concord Avenue Cambridge, MA 02138
71468	ITT Canon Electric Div. of ITT Corp. 10550 Talbert Ave. P.O. Box 8040 Fountain Valley, CA 92708
72136	Electro Motive Mfg. Co., Inc. South Park & John Streets Willimantic, CT 06226
72982	Murata Erie North America, Inc. 645 W. 11th Street Erie, PA 16512
73138	Beckman Instruments, Inc. Helipot Division 2500 Harbor Boulevard Fullerton, CA 92634
73899	JFD Electronic Components Division of Murata Erie North America 112 Mott Street Oceanside, NY 11572
80131	Electronic Industries Assoc. 2001 Eye Street, N.W. Washington, DC 20006

Mfr. Code	Name and Address
80294	Bourns Instruments, Inc. 6135 Magnolia Avenue Riverside, CA 92506
81349	Military Specifications
81350	Joint Army-Navy Specifications
82389	Switchcraft, Incorporated 5555 North Elston Avenue Chicago, IL 60630
84048	Vernitron Corp. 2801 72nd Street North P.O. Box 44000 St. Petersburg, FL 33743
91293	Johanson Manufacturing Co. P.O. Box 329 Boonton, NJ 07005
95121	Quality Components, Inc. P.O. Box 113 St. Mary's, PA 15857
95146	Alco Electronic Products, Inc. P.O. Box 1348 North Andover, MA 01842
98291	Sealectro Corp. 40 Lindeman Drive Trumbull, CT 06611
98900	American Precision Industries Delevan Electronics Division 270 Quaker Road East Aurora, NY 14052

5.4 PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear or damage. When ordering replacement parts from Watkins-Johnson Company, specify the type and serial number of the equipment and the reference designation and description of each part ordered. The list of manufacturers provided in **paragraph 5.3** and the manufacturer's part number for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment; however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

NOTE

As improved semi-conductors become available, it is the policy of Watkins-Johnson to incorporate them in proprietary products. For this reason some transistors, diodes, and integrated circuits installed in the equipment may not agree with those specified in the parts list and schematic diagrams of this manual. However, the semi-conductors designated in the manual may be substituted in every case with satisfactory results.

5.5 **TYPE WJ-8628-4 VHF/UHF RECEIVER, MAIN CHASSIS**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	RF Tuner 20-512 MHz	1	794445-2	14632	
A2	21.4 MHz IF Demodulator	1	794446-1	14632	
A3	Synthesizer Module	1	794447-1	14632	
A4	Controller Motherboard	1	794431-2	14632	
A5	Controller/Receiver Interface	1	794457-1	14632	
A6	Not Used				
A7	Not Used				
A8	Keyboard Assembly	1	371037-2	14632	
DS1	Led Display, Modified	1	271504-3	14632	
J1	Connector, Plug	1	DBSPRB25P	71468	
J2 Thru J4	Not Used				
J5	Connector, Phone Jack	1	L12B	82389	
MP1	Handle, Front	1	10221-B-0632-4A	06540	
MP2	Knob, Round	3	50-2WD-1G	94144	
MP3	Same as MP2				
MP4	Same as MP2				
MP5	Control Knob	1	18665-1	14632	
P1	Connector, Plug	2	65043-028	22526	
P2	Connector, Plug	1	65039-034	22526	
P3	Connector, Plug	1	65039-033	22526	
W1P1	Connector Jack, SMB	6	2002-7571-005	19505	
W1P2	Connector, Plug	1	65039-034	22526	
W2P1	Same as W1P1				
W2P2	Same as W1P1				
W3P1	Same as W1P1				
W3P2	Same as W1P1				
W4P1	Connector, Plug	4	66900-040	22526	
W4P2	Same as W4P1				
W4P3	Same as W4P1				
W4P4	Same as W4P1				
W5P1	Same as W1P1				
W5P2	Same as W1P1				
W6P1	Connector, Plug	2	IDD-09-G	55322	
W6P2	Same as W6P1				
W7P1	Connector, Plug	6	66900-014	22526	
W7P2	Same as W7P1				
W8P1	Same as W7P1				
W8P2	Same as W7P1				
W9P1	Same as W7P1				

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Figure 5-1. WJ-8628-4 VHF/UHF Receiver, Front Panel, Location of Components

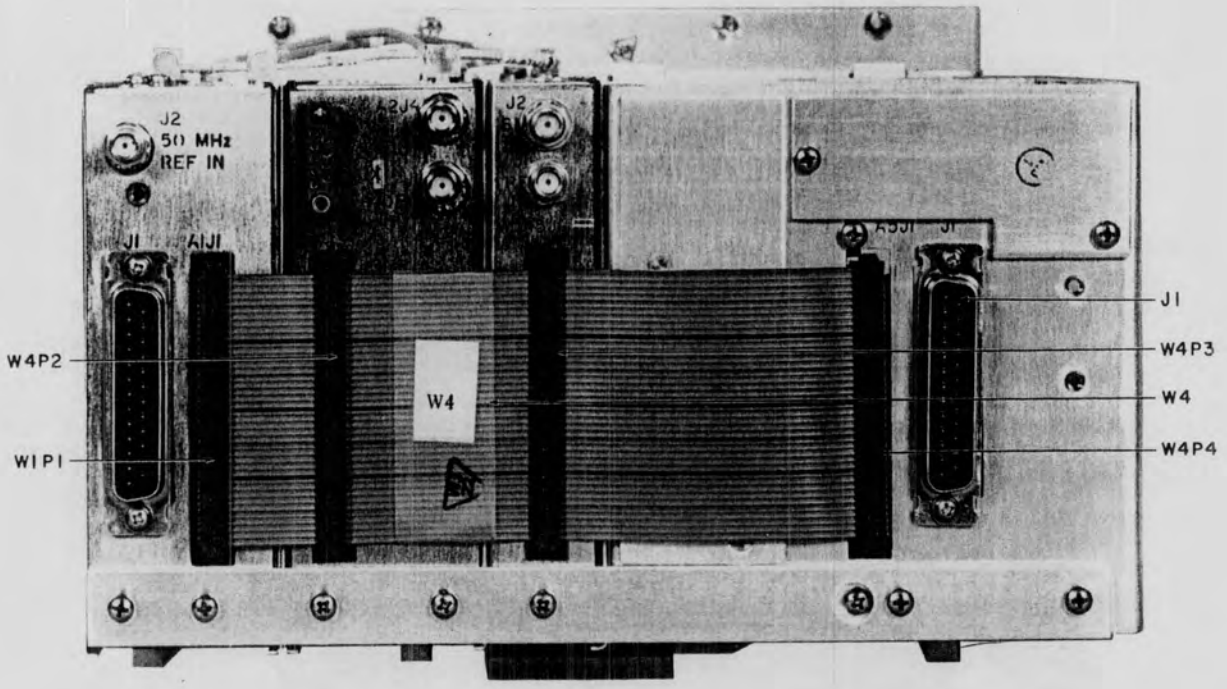

Figure 5-2. WJ-8628-4 VHF/UHF Receiver, Rear Panel, Location of Components

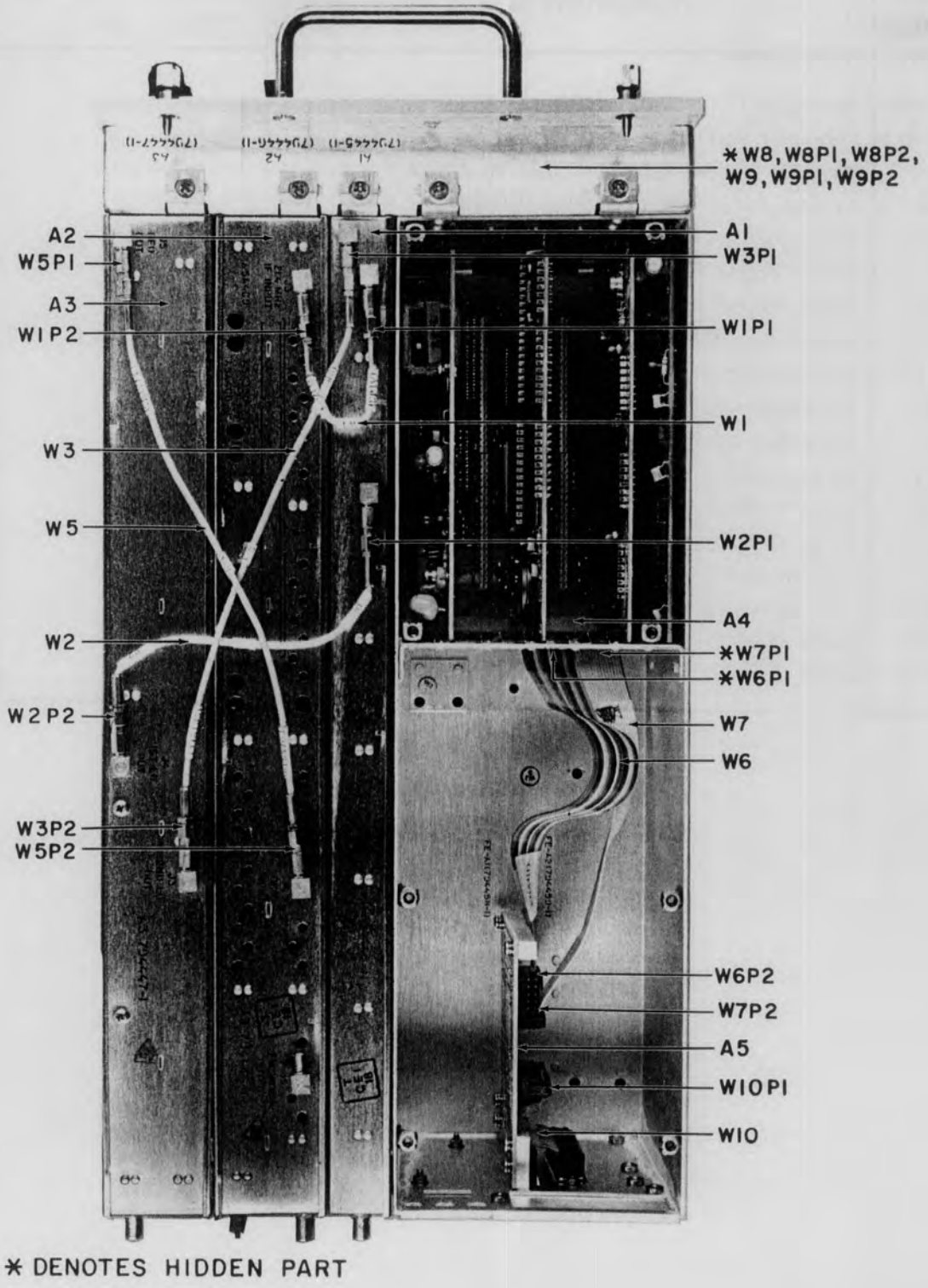

Figure 5-3. WJ-8628-4 VHF/UHF Receiver, Top View, Location of Components

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
W9P2	Same as W7P1				
W10P1	Connector, Multipin, PL	1	66900-026	22526	
R1	Resistor, Variable, Composition: 50 kΩ, 10%, 1 W	1	70A3N056L503A	01121	
R2	Resistor, Variable, Composition: 10 kΩ, 10%, 1 W	2	70A3N056L103U	01121	
R3	Same as R2				
S1	Switch, Toggle	1	MTF-126D	95146	
S2	Switch, Toggle	1	MTF-126G	95146	
U1	Encoder Assembly	1	SP-16 W/Hardware	USDIG	
W1	Cable Assembly	1	17300-348-1	14632	
W2	Cable Assembly	1	17300-348-2	14632	
W3	Cable Assembly	1	17300-348-3	14632	
W4	Cable Assembly	1	271373	14632	
W5	Cable Assembly	1	17300-348-4	14632	
W6	Cable Assembly	1	271409	14632	
W7	Cable Assembly	1	271331-2	14632	
W8	Cable Assembly	1	271332-2	14632	
W9	Cable Assembly	1	271333-2	14632	
W10	Cable Assembly	1	271372-1	14632	

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5.5.1 **TYPE 794445-2 RF TUNER (20-512 MHz)** REF DESIG PREFIX **A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Preselector	1	371140-1	14632	
A2	Dual R.F. Amplifier	1	371139-1	14632	
A3	1st Converter	1	371138-1	14632	
A4	2nd Converter	1	371137-2	14632	
A5	Connector Interface	1	371141-1	14632	
A6	Dual IF Converter	1	371285-2	14632	
C1	Capacitor Ceramic, Feedthru: 0.05 µF, GMV, 300 V	10	54-785-002-503P	33095	
C2	Capacitor, Modified	18	271492-1	14632	
C3	Same as C1				
C4	Same as C1				
C5 Thru C12	Same as C2				
C13	Same as C1				
C14	Same as C2				
C15	Same as C2				
C16	Same as C1				
C17	Same as C2				
C18	Same as C2				
C19	Same as C1				
C20	Same as C1				
C21	Same as C2				
C22	Same as C1				
C23 Thru C25	Same as C2				
C26	Same as C1				
C27	Same as C2				
C28	Same as C1				
J1	Connector, Receptacle: SMA Series	1	2058-0000-00	26805	
J2	Connector, Jack	1	50-610-3702-31	98291	
J3	Connector, Receptacle: SMB Series	3	2012-1511-000	19505	
J4	Same as J3				
J5	Same as J3				
L1	Coil, Fixed, Molded: 1000 µH, 10%	5	1025-92	99800	
L2 Thru L5	Same as L1				
L6	Inductor	1	22292-105	14632	
L7	Coil, Fixed, Molded: 12 µH, 10%	2	1025-46	99800	
L8	Same as L7				

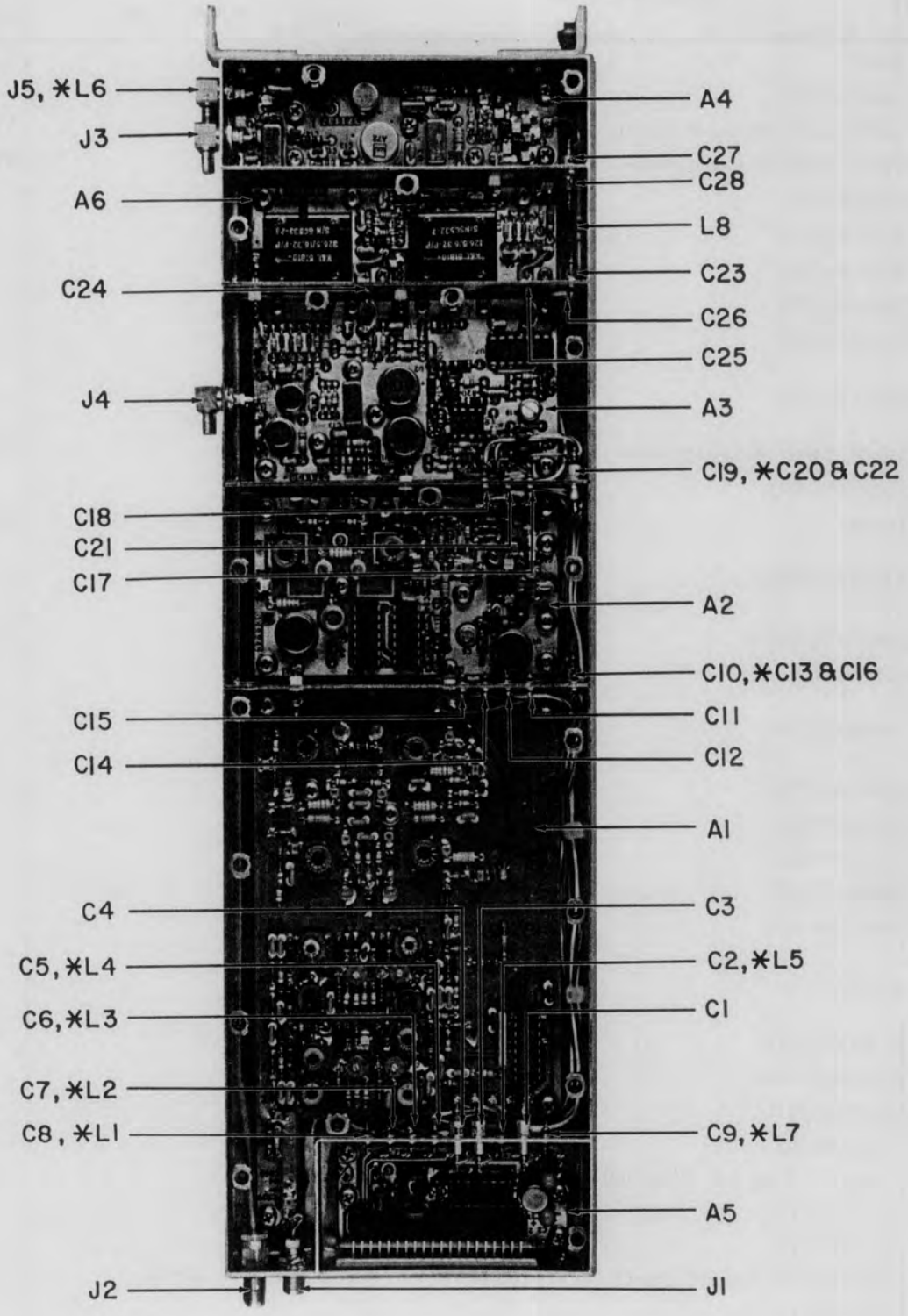

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Figure 5-4. Type 794445-2 RF Tuner (20 - 512 MHz) A1, Location of Components

5.5.1.1 **Type 371140-1 Input Preselector** REF DESIG PREFIX **A1A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	16	KS3542	52673	
CR2	Same as CR1				
CR3	Diode, Variable, Capacitance	5	KV3901	52673	
CR4	Diode, Variable, Capacitance	4	KV2501A	52673	
CR5	Same as CR4				
CR6	Same as CR3				
CR7	Same as CR3				
CR8	Same as CR4				
CR9	Same as CR4				
CR10 Thru CR13	Same as CR1				
CR14	Diode, Variable, Capacitance	4	KV2201A	52673	
CR15	Same as CR14				
CR16	Diode	9	U11-3102	52673	
CR17 Thru CR19	Same as CR16				
CR20	Same as CR14				
CR21	Same as CR14				
CR22 Thru CR25	Same as CR1				
CR26	Same as CR16				
CR27	Same as CR3				
CR28	Same as CR16				
CR29	Same as CR16				
CR30	Same as CR3				
CR31 Thru CR34	Same as CR1				
CR35	Same as CR16				
CR36	Same as CR16				
CR37	Same as CR1				
CR38	Same as CR1				
C1	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 50 V	23	34453-1	14632	
C2	Same as C1				
C3	Same as C1				
C4	Capacitor, Variable, Ceramic: 5-25 pF, 100 V	4	518-000A5-25	59660	
C5	Same as C1				
C6	Capacitor, Ceramic, Chip: 1.5 pF ±0.1 pF, 500 V	1	ATC700B1R5BP500X	29990	
C7	Same as C4				

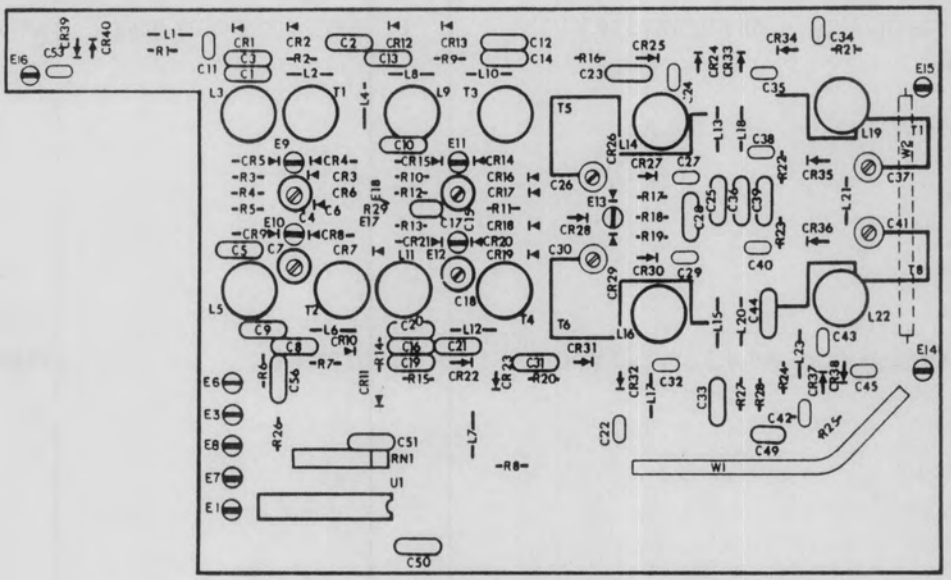

Figure 5-5. Type 371140-1 Input Preselector (A1A1), Location of Components

REF DESIG PREFIX **A1A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C8 Thru C10	Same as C1				
C11	Capacitor, Ceramic, Chip: 1000 pF, 10%, 50 V	9	ATC100B102KP50X	29990	
C12 Thru C14	Same as C1				
C15	Same as C4				
C16	Same as C1				
C17	Capacitor, Ceramic, Disc: 68 pF, 5%, 100 V	1	8121-100-COGO-680J	59660	
C18	Same as C4				
C19 Thru C21	Same as C1				
C22	Same as C11				
C23	Same as C1				
C24	Same as C11				
C25	Same as C1				
C26	Capacitor, Variable, Air: 0.6-4.5 pF, 500 VDC	2	GT-24R	73899	
C27	Same as C11				
C28	Same as C1				
C29	Same as C11				
C30	Same as C26				
C31	Same as C1				
C32	Same as C11				
C33	Same as C1				
C34	Same as C11				
C35	Capacitor, Ceramic, Chip: 510 pF, 10%, 100 V	5	ATC100B511KP100X	29990	
C36	Same as C1				
C37	Capacitor, Variable, Air: 0.4-2.5 pF, 500 V	2	GT12R	73899	
C38	Same as C35				
C39	Same as C1				
C40	Same as C35				
C41	Same as C37				
C42	Same as C11				
C43	Same as C35				
C44	Same as C1				
C45	Same as C35				
C46 Thru C48	Not Used				
C49	Capacitor, Ceramic, Disc: 470 pF, 5%, 50 V	1	8121-050-COGO-471J	59660	
C50	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	2	34452-1	14632	

REF DESIG PREFIX A1A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C51	Same as C50				
C52	Not Used				
C53	Same as C11				
C54	Capacitor, Ceramic, Chip: 0.5 pF ±0.1 pF, 500 V	2	ATC100B0R5BP500X	29990	
C55	Same as C54				
C56	Same as C1				
E1	Terminal, Forked	12	140-1941-02-01	71279	
E2	Not Used				
E3	Same as E1				
E4	Not Used				
E5	Not Used				
E6 Thru E16	Same as E1				
L1	Coil, Fixed	8	1025-32	99800	
L2	Same as L1				
L3	Coil, Mounted	1	271423-6	14632	
L4	Same as L1				
L5	Coil, Mounted	1	271423-10	14632	
L6 Thru L8	Same as L1				
L9	Coil, Mounted	2	271423-7	14632	
L10	Same as L1				
L11	Same as L9				
L12	Same as L1				
L13	Coil, Fixed, Molded: 0.56 µH, 10%	3	1025-14	99800	
L14	Coil, Mounted	2	271423-8	14632	
L15	Same as L13				
L16	Same as L14				
L17	Same as L13				
L18	Coil, Fixed, Molded: 0.22 µH, 10%	3	1025-04	99800	
L19	Coil, Mounted	2	271423-9	14632	
L20	Same as L18				
L21	Coil, Fixed	1	1025-06	99800	
L22	Same as L19				
L23	Same as L18				
RN1	Resistor/Network	1	4306R101-472	80294	
R1	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	3	CF1/8-1.5K/J	09021	
R2	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/8 W	9	CF1/8-4.7K/J	09021	
R3	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	16	CF1/8-47K/J	09021	

REF DESIG PREFIX **A1A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R4 Thru R6	Same as R3				
R7	Same as R2				
R8	Same as R1				
R9	Same as R2				
R10 Thru R14	Same as R3				
R15	Same as R2				
R16	Same as R2				
R17 Thru R19	Same as R3				
R20	Same as R2				
R21	Same as R2				
R22	Same as R3				
R23	Same as R3				
R24	Same as R2				
R25	Same as R1				
R26	Same as R2				
R27	Same as R3				
R28	Same as R3				
T1	Coil, Mounted	1	271423-2	14632	
T2	Coil, Mounted	1	271423-3	14732	
T3	Coil, Mounted	1	271423-4	14632	
T4	Coil, Mounted	1	271423-5	14632	
T5	Integral Part of Printed Wiring Board				
T6	Integral Part of Printed Wiring Board				
T7	Integral Part of Printed Wiring Board				
T8	Integral Part of Printed Wiring Board				
U1	Integrated Circuit	1	CD4052BE	02735	
W1	Cable, RF	1	271424-1	14632	
W2	Cable, RF	1	271425-1	14632	

5.5.1.2 **Type 371139-1 Dual RF Amplifier** REF DESIG PREFIX **A1A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	2	U11-3102	52673	
CR2	Same as CR1				
CR3	Diode	6	KS3542	52673	
CR4 Thru CR8	Same as CR3				
C1	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	4	34452-1	14632	
C2 Thru C4	Same as C1				
C5	Capacitor, Variable, Air: 0.6-4.5 pF, 500 Vdc	1	GT-24R	73899	
C6	Capacitor, Ceramic, Chip: 10 pF, 2%, 500 V	1	ATC700B100GP500X	29990	
C7	Capacitor, Ceramic, Chip: 2.2 pF, 0.1 pF, 500 V	1	ATC700B2RBP500X	29990	
C8	Capacitor, Ceramic, Chip: 15 pF, 5%, 500 V	1	ATC700B150JP500X	29990	
C9	Capacitor, Ceramic, Chip: 12 pF, 5%, 500 V	2	ATC700B120JP500X	29990	
C10	Same as C9				
C11	Capacitor, Ceramic, Chip: 8.2 pF ±0.25 pF, 500 V	2	ATC700B8R2CP500X	29990	
C12	Capacitor, Ceramic, Chip: 9.1 pF ±0.25 pF, 500 V	1	ATC700B9R1CP500X	29990	
C13	Capacitor, Variable, Air: 1.0-10 pF, 250 V	1	8052	91293	
C14	Capacitor, Variable, Air: 0.4-2.5 pF, 500 V	2	GT12R	73899	
C15	Capacitor, Ceramic, Chip: 510 pF, 10%, 100 V	4	ATC700B511KP100X	29990	
C16	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 100 V	3	8121-100-651-103M	59660	
C17	Same as C15				
C18	Same as C14				
C19	Same as C11				
C20	Same as C16				
C21	Capacitor, Ceramic, Chip: 2200 pF, 10%, 50 V	1	ATC700B222KP500X	29990	
C22	Capacitor, Ceramic, Chip: 1000 pF, 10%, 50 V	2	ATC700B102KP500X	29990	
C23	Same as C22				
C24	Same as C16				
C25	Same as C15				
C26	Same as C15				
C27	Capacitor, Ceramic, Chip: 100 pF, 20%, 500 V	2	ATC100B101MP500X	29990	
C28	Same as C27				
E1	Terminal, Forked	7	140-1941-02-01	71279	
E2 Thru E7	Same as E1				
J1	Not Used				
L1	Coil, Fixed, Molded: 10 µH	2	1025-44	99800	
L2	Same as L1				
L3	Coil, Fixed, Molded: 0.1 µH	1	1025-94	99800	
L4	Inductor, Air Core	1	22292-86	14632	

REF DESIG PREFIX **A1A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
L5	Inductor, Air Core	2	22292-157	14632	
L6	Same as L5				
L7	Coil, Fixed, Molded: 0.22 µH, 10%	2	1025-04	99800	
L8	Coil, Mounted	2	271423-9	14632	
L9	Same as L7				
L10	Same as L8				
L11	Coil, Fixed: 2.2 µH, 10%	1	1025-28	99800	
L12	Coil, Fixed, Molded: 1.0 µH, 10%	1	1025-20	99800	
R1	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	7	CF1/8-1.5K/J	09021	
R2 Thru R7	Same as R1				
R8	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	1	CF1/8-10K/J	09021	
R9	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	2	CF1/8-47K/J	09021	
R10	Same as R9				
U1	Amplifier/RF	1	QBH-101	55027	
U2	Amplifier/RF	1	QBH-119	55027	
U3	Integrated Circuit	2	DG303CJ	17856	
U4	Same as U3				

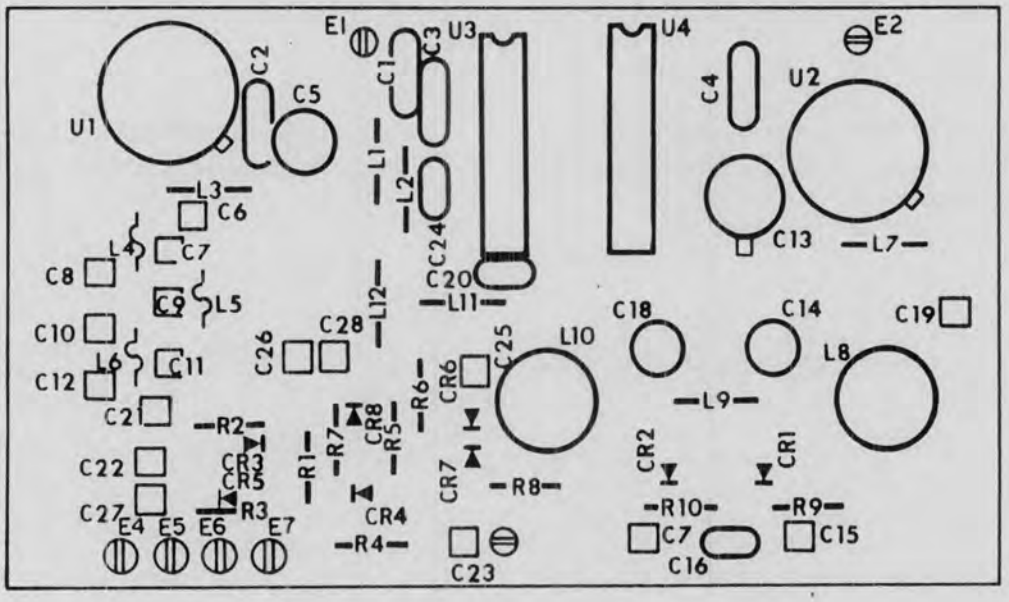

Figure 5-6. Type 371139-1 Dual RF Amplifier (A1A2), Location of Components

5.5.1.3 **Type 371138-1 1st IF Converter** REF DESIG PREFIX A1A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	6	KS3542	52673	
CR2 Thru CR6	Same as CR1				
CR7	Diode	2	1N4148/JAN	81350	
CR8	Same as CR7				
C1	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	6	34452-1	14632	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 1500 pF, 5%, 100 V	5	8121-100-COGO-152J	59660	
C4	Same as C3				
C5	Capacitor, Ceramic, Monolithic: 510 pF ±2%	1	150-100-NPO-511G	51642	
C6	Capacitor, Ceramic, Disc: 1000 pF, 5%, 100 V	6	8121-100-COGO-102J	59660	
C7	Same as C6				
C8	Same as C6				
C9	Same as C3				
C10	Same as C3				
C11	Same as C3				
C12 Thru C14	Same as C6				
C15	Same as C1				
C16	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	8121-050-651-104M	59660	
C17	Same as C1				
C19	Same as C16				
C20	Same as C1				
C21	Same as C1				
E1	Terminal, Forked	9	140-1941-02-01	71279	
E2 Thru E9	Same as E1				
L1	Coil, Fixed, Molded: 10 µH	4	1025-44	99800	
L2	Same as L1				
L3	Coil, Fixed, Molded: 1.8 µH, 10%	4	1025-26	99800	
L4	Coil, Fixed, Molded: 1.0 µH, 10%	1	1025-20	99800	
L5	Same as L3				
L6	Same as L3				
L7	Coil, Fixed: 18 µH, 10%	1	1025-50	99800	
L8	Same as L3				
L9	Same as L1				
L10	Same as L1				
R1	Resistor, Fixed, Film: 430 Ω, 5%, 1/8 W	2	CF1/8-430 OHMS/J	09021	
R2	Resistor, Fixed, Film: 12 Ω, 5%, 1/8 W	1	CF1/8-12 OHMS/J	09021	
R3	Same as R1				

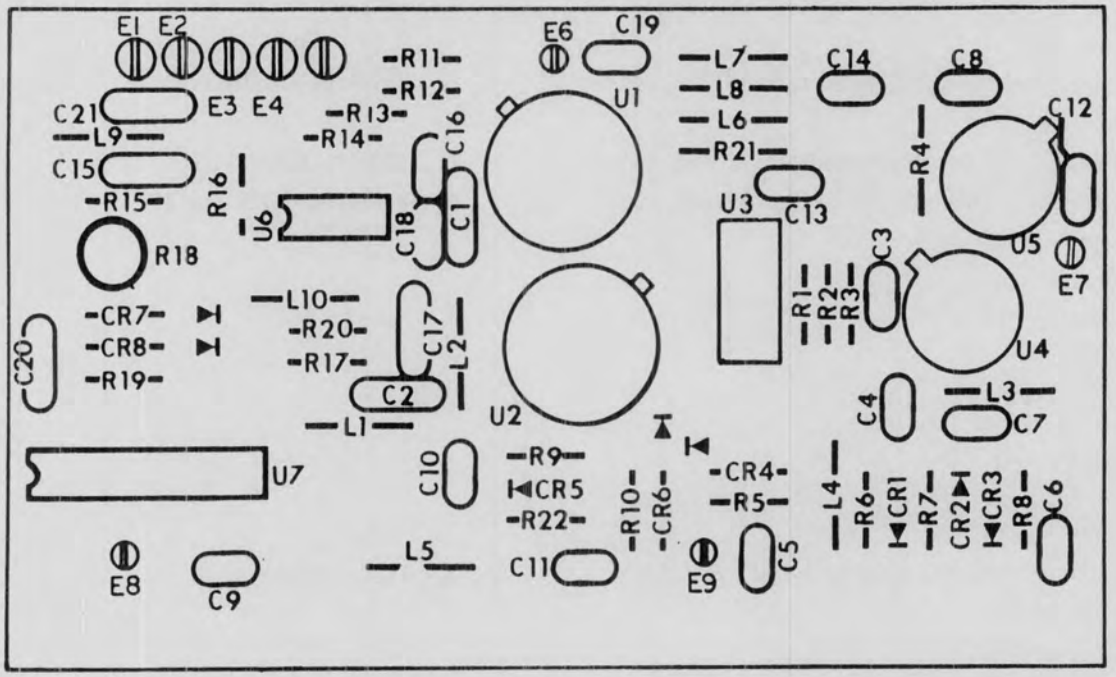

Figure 5-7. Type 371138-1 1st IF Converter (A1A3) Location of Components

REF DESIG PREFIX A1A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R4	Resistor, Fixed, Film: 39 Ω, 5%, 1/4 W	2	CF1/4-39 OHMS/J	09021	
R5	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	6	CF1/8-1.5K/J	09021	
R6	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	2	CF1/8-1.0K/J	09021	
R7 Thru R10	Same as R5				
R11	Resistor, Fixed, Film: 33 kΩ, 5%, 1/8 W	1	CF1/8-33K/J	09021	
R12	Resistor, Fixed, Film: 180 kΩ, 5%, 1/8 W	1	CF1/8-180K/J	09021	
R13	Resistor, Fixed, Film: 18 kΩ, 5%, 1/8 W	1	CF1/8-18K/J	09021	
R14	Resistor, Fixed, Film: 120 kΩ, 5%, 1/8 W	1	CF1/8-120K/J	09021	
R15	Resistor, Fixed, Film: 5.6 kΩ, 5%, 1/8 W	1	CF1/8-5.6K/J	09021	
R16	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	1	CF1/8-22K/J	09021	
R17	Resistor, Fixed, Film: 100 k, 5%, 0.125 W	1	CF1/8-100K/J	09021	
R18	Resistor, Variable, Film: 10 kΩ, 10%, 1/2 W	1	62PR10K	73138	
R19	Same as R5				
R21	Same as R4				
R22	Same as R6				
U1	Attenuator	1	TG9001	60979	
U2	Amplifier/RF	1	QBH-109	55027	
U3	Mixer, Double Balanced	1	TFM-2H	15542	
U4	Integrated Circuit	2	GPD 430	24539	
U5	Same as U4				
U6	Integrated, Circuit	1	MC1458N	18324	
U7	Integrated, Circuit	1	DG303CJ	17856	

5.5.1.4 **Type 371137-2 2nd IF Converter** REF DESIG PREFIX **A1A4**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Chip: 9.1 pF ±0.25 pF, 500 V	1	ATC700B9R1CP500X	29990	
C2	Capacitor, Ceramic, Chip: 0.5 pF ±0.1 pF, 500 V	1	ATC700B0R5BP500X	29990	
C3	Capacitor, Ceramic, Chip: 12 pF, 5%, 500 V	1	ATC700B120JP500X	29990	
C4	Capacitor, Ceramic, Chip: 6.2 pF ±0.25 pF, 500 V	1	ATC700B6R2CP500X	29990	
C5	Capacitor, Ceramic, Chip: 10 pF, 5%, 500 V	1	ATC700B100JP500X	29990	
C6	Capacitor, Ceramic, Chip: 4.3 pF ±0.25 pF, 500 V	1	ATC700B4R3CP500X	29990	
C7	Capacitor, Ceramic, Chip: 2.0 pF ±0.1 pF, 500 V	1	ATC100B2R0BP500X	29990	
C8	Capacitor, Ceramic, Disc: 1500 pF, 5%, 100 V	2	8131-100-COGO-152J	59660	
C9	Same as C8				
C10	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	4	34475-1	14632	
C11	Same as C10				
C12	Capacitor, Ceramic, Disc: 100 pF, 5%, 100 V	2	8121-100-COGO-101J	59660	
C13	Capacitor, Ceramic, Monolithic: 220 pF, 5%, 100 V	1	8121-100-COGO-221J	59660	
C14	Same as C12				
C15	Same as C10				
C16	Same as C10				
C17	Capacitor, Ceramic, Chip: 11.0 pF, 2%, 500 V	1	ATC100B110GP500X	29990	
E1	Terminal, Forked	4	140-1941-02-01	71279	
E2	Not Used				
E3	Same as E1				
E4	Not Used				
E5	Same as E1				
E6	Same as E1				
L1	Coil, Air	1	22292-86	14632	
L2	Coil, Air	2	22292-157	14632	
L3	Same as L2				
L4	Coil, Fixed, Molded: 1.8 µH,. 10%	2	1025-26	99800	
L5	Same as L4				
L6	Coil, Fixed: 0.47 µH	2	1025-12	99800	
L7	Same as L6				
L8	Coil, Fixed, Molded: 8.2 µH	1	1025-42	99800	
R1	Resistor, Fixed, Film: 300 Ω, 5%, 1/8 W	2	CF1/8-300 OHMS/J	09021	
R2	Resistor, Fixed, Film: 18 Ω, 5%, 1/8 W	1	CF1/8-18 OHMS/J	09021	
R3	Same as R1				
R4	Resistor, Fixed, Film: 39 Ω, 5%, 1/4 W	1	CF1/4-39 OHMS/J	09021	
R5	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/8 W	1	CF1/8-4.7K/J	09021	
U1	Mixer	1	TFM-1H	15542	
U2	Integrated Circuit	1	GPD-430	24539	
U3	Amplifier	1	A72	14482	
U4	Integrated Circuit	1	TDC-10-1	15542	

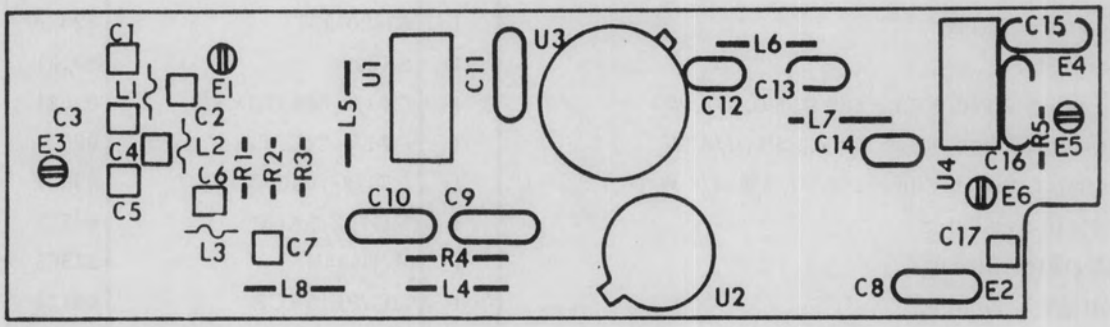

Figure 5-8. Type 371137-2 2nd IF Converter (A1A4) Location of Components

5.5.1.5 **Type 371141-1 Connector Interface** REF DESIG PREFIX **A1A5**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.47 µF, 10%, 50 V	2	8131-050-X7RO-474K	59660	
C2	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35V	2	196D475X0035JE3	56289	
C3	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	8121-050-651-104M	59660	
C4	Same as C2				
C5	Same as C1				
C6	Same as C3				
C7	Capacitor, Ceramic, Disc: 470 pF, 10%, 200 V	1	CK05BX471K	81349	
E1	Terminal, Forked	9	140-1941-02-01	71279	
E2 Thru E9	Same as E1				
J1	Connector, Plug	1	65820-003	22526	
Q1	Transistor	1	2N2904	80131	
R1	Resistor, Fixed, Film: 560 Ω, 5%, 1/8 W	1	CF1/8-560 OHMS/J	09021	
R2	Resistor, Fixed, Film: 24 kΩ, 5%, 1/8 W	1	CF1/8-24K/J	09021	
R3	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	1	CF1/8-100K/J	09021	
U1	Voltage Regulator	1	MC78L15ACP	04713	
U2	Integrated Circuit	1	UC3834N	12969	
U3	Voltage Regulator	1	MC79L15ACP	04713	

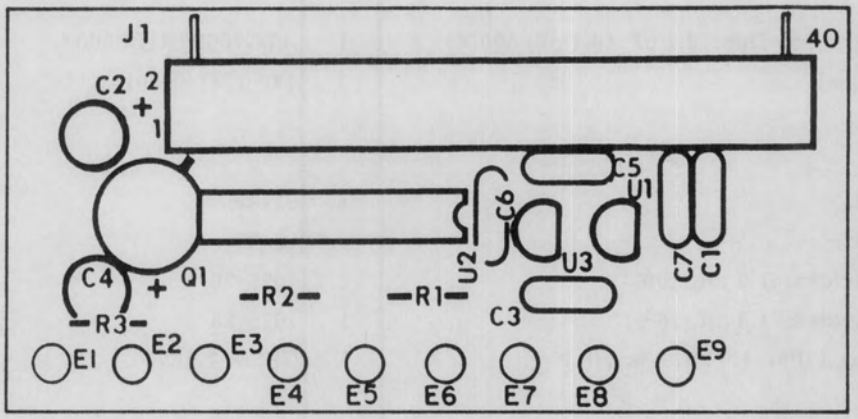

Figure 5-9. Type 371141-1 Connector Interface (A1A5), Location of Components

5.5.1.6 **Type 371285-2 Dual IF Amplifier** REF DESIG PREFIX **A1A6**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	6	KS3542	52673	
CR2 Thru CR6	Same as CR1				
C1	Capacitor, Ceramic, Disc: 1000 pF, 5%, 50 V	3	8121-050-COGO-102J	59660	
C2	Same as C1				
C3	Capacitor, Ceramic, Monolithic: 1500 pF ±2%, 100 V	4	150-100-NPO-152G	51642	
C4	Same as C3				
C5	Same as C1				
C6	Same as C3				
C7	Same as C3				
C8	Capacitor, Ceramic, Chip: 2.1 pF ±0.1 pF, 500 V	1	ATC700B2R1BP500X	29990	
E1	Terminal, Forked	3	140-1941-02-01	71279	
E2	Same as E1				
E3	Same as E1				
FL1	Filter, Bandpass	1	92448	50621	
FL2	Filter, Bandpass	1	92449	50621	
L1	Coil, Fixed, Molded: 1.0 µH, 10%	1	1025-20	99800	
L2	Coil, Fixed, Molded: 1.8 µH, 10%	1	1025-26	99800	
R1	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	5	CF1/8-1.5K/J	09021	
R2	Same as R1				
R3	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	2	CF1/8-1.0K/J	09021	
R4	Same as R1				
R5	Same as R3				
R6	Same as R1				
R7	Same as R1				

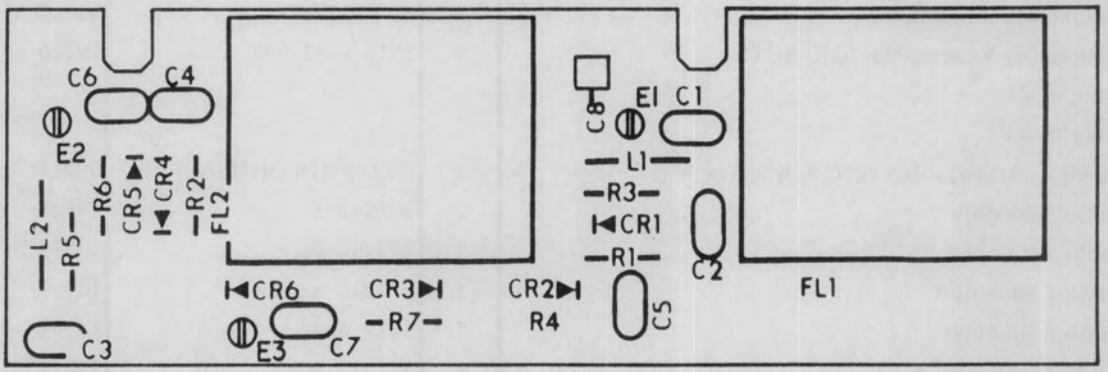

Figure 5-10. Type 371285-2 Dual IF Amplifier (A1A6), Location of Components

5.5.2 **TYPE 794446-1 21.4 MHz IF DEMODULATOR** REF DESIG PREFIX **A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Bandpass, Amplifier: 21.4 MHz	1	371150-1	14632	
A2	AM/SSB/CW Demodulator	1	371151-1	14632	
A3	Video/Audio/COS	1	371152-1	14632	
A4	Digital Interface	1	371153-1	14632	
A5	FM Demodulator Motherboard	1	371154-1	14632	
E1	Term, Feedthru, Insulated	5	SFU16Y	04013	
E2 Thru E5	Same as E1				
J1	Connector, Receptacle: SMA Series	1	9412-7113-000	19505	
J2	Connector, Receptacle	1	SRE9SJ	81312	
J3	Connector, Receptacle: SMB Series	3	2012-1511-000	19505	
J4	Same as J3				
J5	Same as J3				
R1	Resistor, Fixed, Film: 270 Ω, 5%, 1/4 W	1	CF1/4-270 OHMS/J	09021	
W1	Cable Assembly	1	371213-1	14632	
W2	Cable Assembly	1	371213-2	14632	
W3	Cable Assembly	1	371213-3	14632	
W4	Cable Assembly	1	371213-4	14632	
W5	Cable Assembly	1	371213-5	14632	
W1P1	Connector, Plug	2	IDS-9-G	55322	
W1P2	Same as W1P1				
W2P1	Connector, Strip	4	IDS-6-G	55322	
W2P2	Same as W2P1				
W3P1	Connector, Plug	2	IDS-12-G	55322	
W3P2	Same as W3P1				
W4P1	Connector, Plug	2	IDS-14-G	55322	
W4P2	Same as W4P1				
W5P1	Same as W2P1				
W5P2	Same as W2P1				

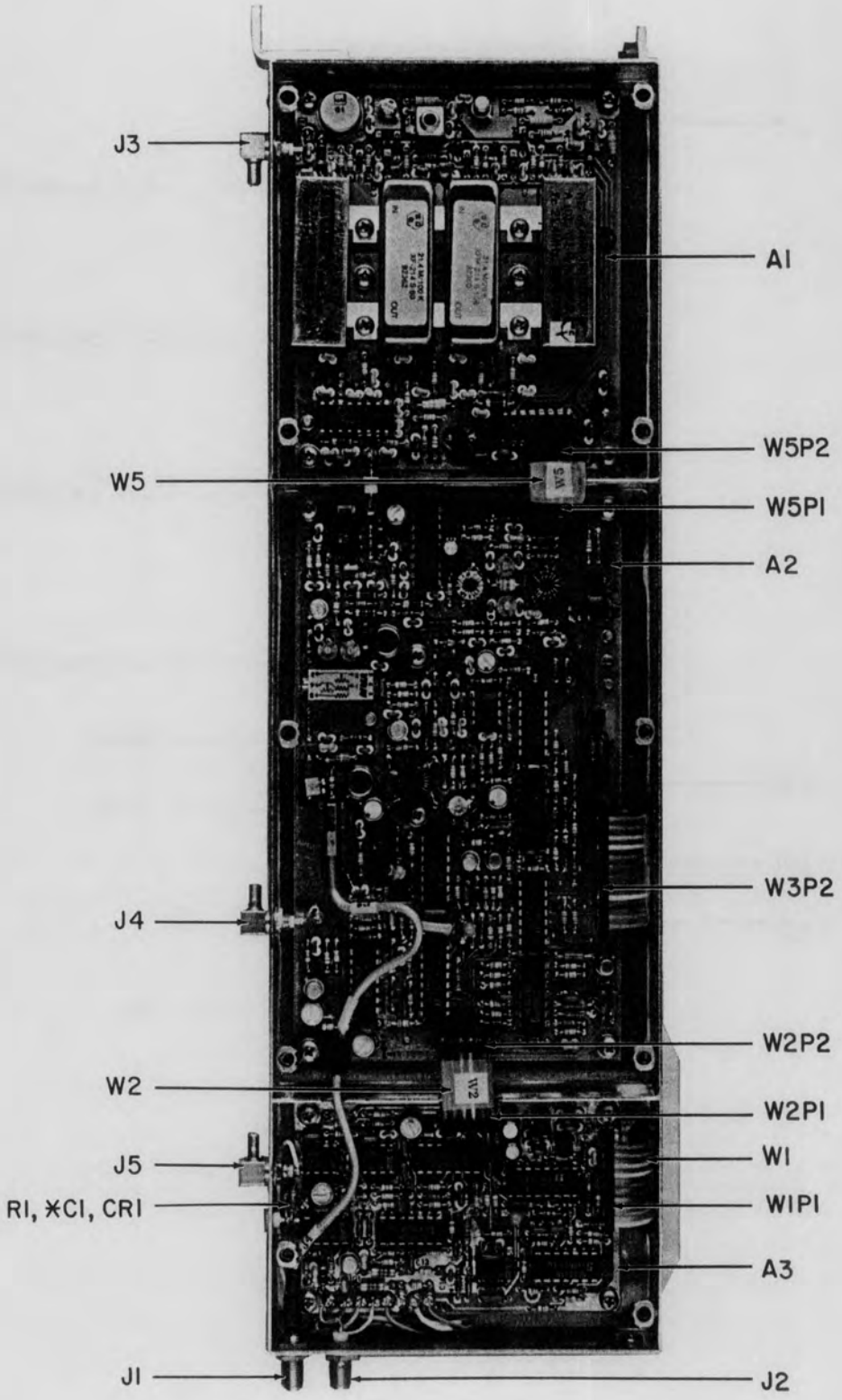

Figure 5-11. Type 794446-1 21.4 MHz IF Demodulator (A2), Top View, Location of Components

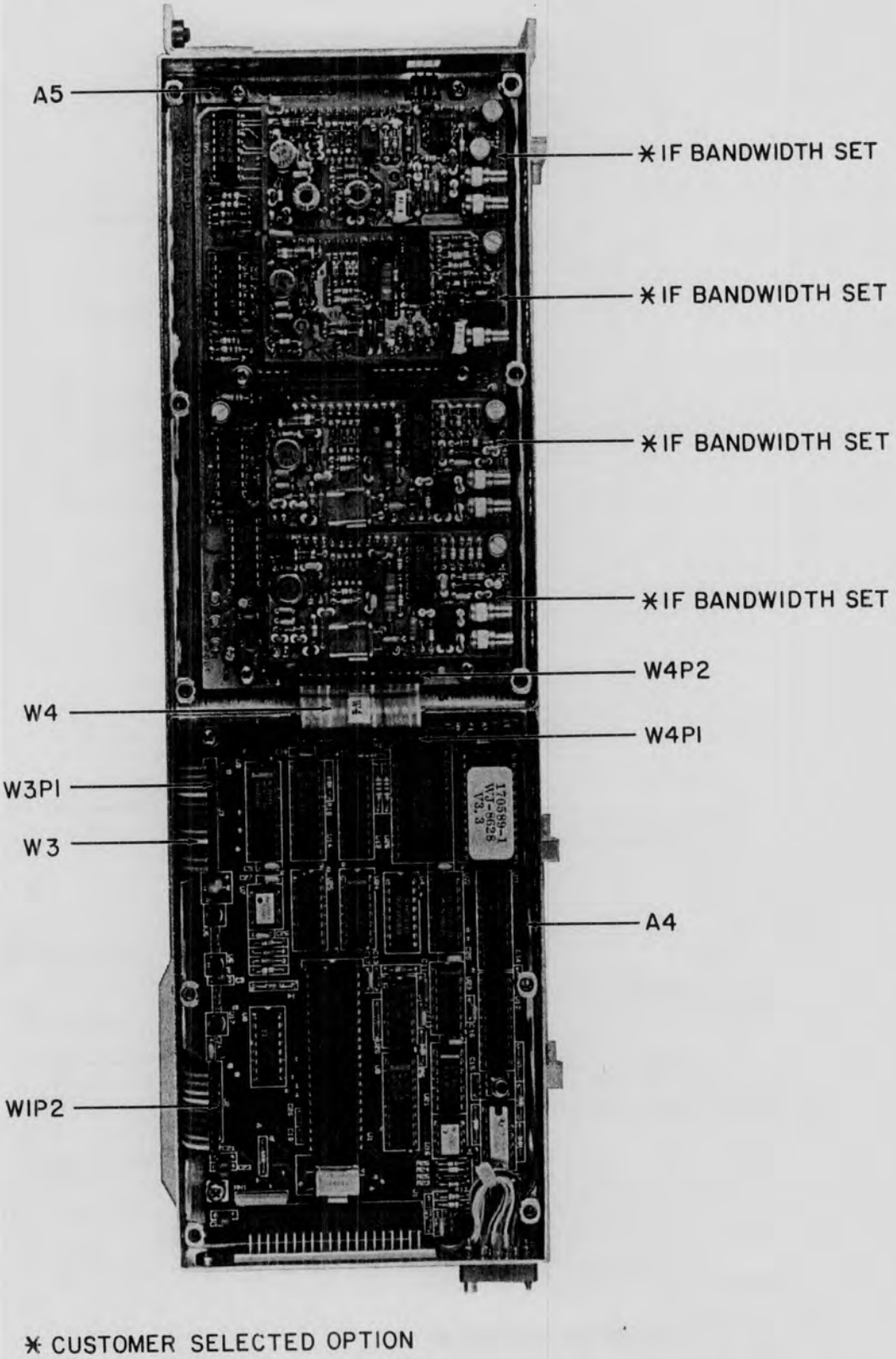

Figure 5-11. Type 794446-1 21.4 MHz IF Demodulator (A2), Bottom View, Location of Components

5.5.2.1 **Type 371150-1 21.4 MHz Bandpass Amplifier** REF DESIG PREFIX A2A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	12	5082-3188	28480	
CR2 Thru CR12	Same as CR1				
CR13	Diode	1	1N4449	80131	
C1	Capacitor, Ceramic, Disc: 4700 pF, 10%, 50 V	35	8111-050-X7RO-472K	59660	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 3.3 pF ±.25 pF, 100 V	1	8101-100-COJO-339C	59660	
C4	Same as C1				
C5	Capacitor, Ceramic, Monolithic: 47 pF, 5%, 100 V	1	8121-100-COGO-470J	59660	
C6	Same as C1				
C7	Same as C1				
C8	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	5	34452-1	14632	
C9	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	1	8121-050-651-104M	59660	
C10	Same as C8				
C11	Same as C8				
C12 Thru C18	Same as C1				
C19	Same as C8				
C20	Same as C1				
C21	Same as C8				
C22	Same as C1				
C23	Same as C1				
C24	Same as C1				
C25	Not Used				
C26 Thru C44	Same as C1				
E1	Terminal, Forked	2	140-1941-02-01	71279	
E2	Same as E1				
FL1	Filter		Customer Option		
FL2 Thru FL4	Same as FL1				
J1	Terminal, Strip	1	65500-106	22526	
L1	Coil, Fixed, Molded: 8.2 µH	1	1025-42	99800	
L2	Coil, Variable: 6.8 MH	1	6740-23	04213	
L3	Coil, Fixed: 3.9 µH, 10%	3	1025-34	99800	
L4	Coil, Fixed: 18 µH, 10%	4	1025-50	99800	
L5	Same as L4				
L6	Same as L3				

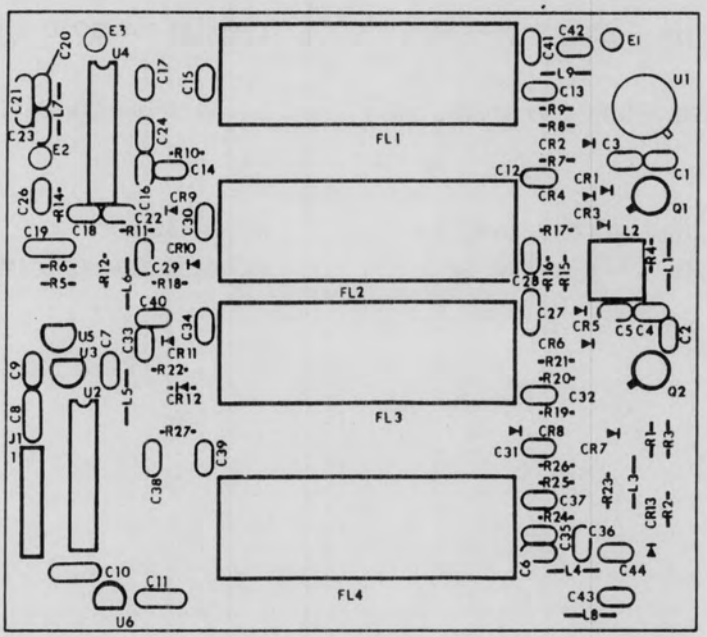

Figure 5-12. Type 371150-1 21.4 MHz Bandpass Amplifier (A2A1), Location of Components

REF DESIG PREFIX A2A1

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
L7	Same as L4				
L8	Same as L3				
L9	Same as L4				
P1	Pin Socket	1	NS-441-B1	06776	
Q1	Transistor	1	CP643	12498	
Q2	Transistor	1	2N2222A	80131	
R1	Resistor, Fixed, Film: 47 Ω, 5%, 1/8 W	2	CF1/8-47 OHMS/J	09021	
R2	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	2	CF1/8-470 OHMS/J	09021	
R3	Resistor, Fixed, Film: 6.8 kΩ, 5%, 1/8 W	5	CF1/8-6.8K/J	09021	
R4	Resistor, Fixed, Film: 1.2 kΩ, 5%, 1/8 W	1	CF1/8-1.2K/J	09021	
R5	Same as R2				
R6	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	1	CF1/8-2.2K/J	09021	
R7	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	5	CF1/8-1.5K/J	09021	
R8	Resistor, Fixed, Film: 39 Ω, 5%, 1/8 W	4	CF1/8-39 OHMS/J	09021	
R9	Resistor, Fixed, Film: 18 kΩ, 5%, 1/8 W	4	CF1/8-18K/J	09021	
R10	Same as R3				
R11	Same as R1				
R12	Resistor, Fixed, Film: 160 Ω, 5%, 1/8 W	1	CF1/8-160 OHMS/J	09021	
R13	Not Used				
R14	Resistor, Fixed, Film: 680 Ω, 5%, 1/8 W	1	CF1/8-680 OHMS/J	09021	
R15	Same as R7				
R16	Same as R8				
R17	Same as R9				
R18	Same as R3				
R19	Same as R7				
R20	Same as R8				
R21	Same as R9				
R22	Same as R3				
R23	Same as R7				
R24	Same as R7				
R25	Same as R8				
R26	Same as R9				
R27	Same as R3				
U1	Attenuator	1	G1	27956	
U2	Integrated Circuit	1	MC14052BCP	04713	
U3	Voltage Regulator	1	MC78L15ACP	04713	
U4	Integrated Circuit	1	SL550D	52648	
U5	Integrated Circuit	1	LM317LZ	27014	
U6	Voltage Regulator	1	MC79L15ACP	04713	

5.5.2.2 **Type 371151-1 AM/SSB/CW Demodulator** REF DESIG PREFIX **A2A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
AT1	Attenuator	1	9950-1050	84048	
CR1	Diode	5	1N4446	80131	
CR2	Diode	6	5082-3188	28480	
CR3 Thru CR7	Same as CR2				
CR8	Diode	1	5082-2800	28480	
CR9	Not Used				
CR10	Same as CR1				
CR11	Not Used				
CR12	Same as CR1				
CR13	Same as CR1				
CR14	Not Used				
CR15	Same as CR1				
C1	Capacitor, Ceramic, Disc: 4700 pF, 10%, 50 V	27	8111-050-X7RO-472K	59660	
C2	Not Used				
C3 Thru C7	Same as C1				
C8	Capacitor, Variable, Ceramic: 5-25 pF, 100 V	4	518-000A5-25	59660	
C9	Capacitor, Ceramic, Disc: 4.7 pF ±0.25 pF, 100 V	1	8101-100-COHO-479C	59660	
C10	Same as C8				
C11	Same as C1				
C12	Capacitor, Electrolytic, Aluminum: 0.47 µF ±20%, 16 Vdc	2	ECE-A1CK470	54473	
C13	Same as C1				
C14	Same as C1				
C15	Capacitor, Ceramic, Disc: 680 pF, 5%, 100 V	1	8121-100-COGO-681J	59660	
C16	Same as C1				
C17	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	12	34452-1	14632	
C18 Thru C21	Same as C1				
C22	Same as C8				
C23	Capacitor, Ceramic, Disc: 56 pF, 5%, 100 V	2	8121-100-COGO-560J	59660	
C24	Capacitor, Ceramic, Disc: 750 pF, 5%, 50 V	1	8121-050-COGO-751J	59660	
C25	Capacitor, Composition, Tubular: 0.75 pF, 10%, 500 V	1	QCC-75PFP	95121	
C26	Same as C8				
C27	Same as C23				
C28	Capacitor, Ceramic, Disc: 390 pF, 5%, 100 V	2	8121-100-COGO-391J	59660	
C29 Thru C32	Same as C1				

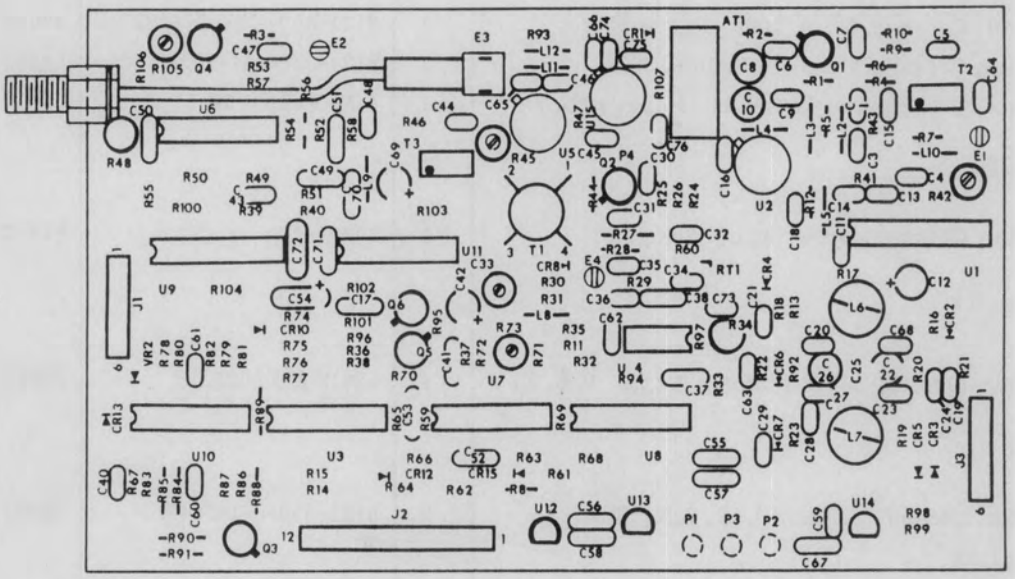

Figure 5-13. Type 371151-1 AM/SSB/CW Demodulator (A2A2), Location of Components

REF DESIG PREFIX **A2A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C33	Capacitor, Variable, Ceramic: 1-3 pF, 100 V	1	518-000A1-3	59660	
C34	Same as C1				
C35	Capacitor, Ceramic, Monolithic: 1 pF ±0.1 pF, 100 V	2	8102-100-COKO-109B	59660	
C36	Same as C35				
C37	Same as C17				
C38	Same as C17				
C39	Not Used				
C40	Capacitor, Ceramic, Disc: 1000 pF, 5%, 50 V	1	8121-050-COGO-102J	59660	
C41	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	3	8131-050-651-105M	59660	
C42	Capacitor, Electrolytic, Tantalum: 15 µF, 10%, 25 V	1	ECS-F1EE156K		
C43 Thru C48	Same as C1				
C49	Capacitor, Ceramic, Disc: .01 µF, 20%, 50 V	1	34453-1	14632	
C50 Thru C53	Same as C17				
C54	Capacitor, Electrolytic, Tantalum: 2.2 µF, 20%, 35 V	1	196D225X0035JE3	56289	
C55 Thru C58	Same as C17				
C59	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	3	8121-050-651-104M	59660	
C60	Same as C59				
C61	Same as C59				
C62	Capacitor, Ceramic, Monolithic: 5.6 pF ±0.25 pF, 100 V	1	100-100-NPO-569C	51642	
C63	Same as C1				
C64	Same as C28				
C65	Capacitor, Ceramic, Disc: 150 pF ±5%, 100 V	1	200-100-NPO-151J	51642	
C66	Capacitor, Ceramic, Monolithic: 75 pF ±2%, 100 V	1	200-100-NPO-750G	51642	
C67	Same as C17				
C68	Same as C1				
C69	Same as C12				
C70	Same as C41				
C71	Same as C41				
C72	Capacitor, Ceramic, Disc: 3.3 µF, 20%, 25 V	1	8141-050-651-335M	59660	
C73	Capacitor, Ceramic, Monolithic: 10 pF ±0.5 pF, 100 V	1	8101-100-COGO-100D	59660	
E1	Terminal/Forked	3	140-1941-02-01	71279	
E2	Same as E1				
E3	Terminator/Coax	1	D-607-10	06090	
E4	Same as E1				
J1	Terminal Strip	2	65500-106	22526	
J2	Terminal Strip	1	65500-112	22526	

REF DESIG PREFIX **A2A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
J3	Same as J1				
J4	Connector, Jack: SMA Series	1	9023-9023-005	19505	
L1	Not Used				
L2	Coil, Fixed: 18 µH, 10%	3	1025-50	99800	
L3	Coil, Fixed: 3.3 µH	1	1025-32	99800	
L4	Coil, Fixed, Molded: 1.8 µH, 10%	1	1025-26	99800	
L5	Same as L2				
L6	Coil, Toridal	2	20681-257	14632	
L7	Same as L6				
L8	Coil, Fixed, Molded: 150 µH, 10%	1	1025-72	99800	
L9	Same as L2				
L10	Coil, Fixed: 0.15 µH	1	1025-00	99800	
L11	Coil, Fixed, Molded: 0.33 µH, 10%	2	1025-08	99800	
L12	Same as L11				
P1	Pin Socket	4	NS-441-B1	06776	
P2 Thru P4	Same as P1				
Q1	Transistor	1	3N211	80131	
Q2	Transistor	1	2N2857	80131	
Q3	Transistor	2	2N3251	80131	
Q4	Transistor	2	2N2222A	80131	
Q5	Same as Q3				
Q6	Same as Q4				
RT1	Thermistor	1	1B102	14193	
R1	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	4	CF1/8-100K/J	09021	
R2	Resistor, Fixed, Film: 30 kΩ, 5%, 1/8 W	1	CF1/8-30K/J	09021	
R3	Resistor, Fixed, Film: 4.3 kΩ, 5%, 1/8 W	1	CF1/8-4.3K/J	09021	
R4	Resistor, Fixed, Film: 6.2 kΩ, 5%, 1/8 W	2	CF1/8-6.2K/J	09021	
R5	Same as R4				
R6	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	6	CF1/8-100 OHMS/J	09021	
R7	Resistor, Fixed, Film: 220 Ω, 5%, 1/8 W	1	CF1/8-220 OHMS/J	09021	
R8	Resistor, Fixed, Film: 330 Ω, 5%, 1/8 W	3	CF1/8-330 OHMS/J	09021	
R9	Resistor, Fixed, Film: 910 Ω, 5%, 1/8 W	1	CF1/8-910 OHMS/J	09021	
R10	Resistor, Fixed, Film: 120 Ω, 5%, 1/8 W	3	CF1/8-120 OHMS/J	09021	
R11	Resistor, Fixed, Film: 2.7 Ω, 5%, 1/8 W	1	CF1/8-2.7 OHMS/J	09021	
R12	Resistor, Fixed, Film: 180 Ω, 5%, 1/8 W	1	CF1/8-180 OHMS/J	09021	
R13	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	5	CF1/8-1.5K/J	09021	
R14	Resistor, Fixed, Film: 680 Ω, 5%, 1/8 W	2	CF1/8-680 OHMS/J	09021	
R15	Same as R14				
R16	Same as R13				

REF DESIG PREFIX **A2A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R17	Same as R6				
R18	Same as R13				
R19	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	6	CF1/8-2.2K/J	09021	
R20	Resistor, Fixed, Film: 18 kΩ, 5%, 1/8 W	3	CF1/8-18K/J	09021	
R21	Same as R19				
R22	Same as R20				
R23	Resistor, Fixed, Film: 3.9 kΩ, 5%, 1/8 W	2	CF1/8-3.9K/J	09021	
R24	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/8 W	9	CF1/8-4.7K/J	09021	
R25	Same as R6				
R26	Same as R24				
R27	Resistor, Fixed, Film: 330 Ω, 5%, 1/4 W	1	CF1/4-330 OHMS/J	09021	
R28	Same as R10				
R29	Resistor, Fixed, Film: 200 kΩ, 5%, 1/8 W	1	CF1/8-200K/J	09021	
R30	Resistor, Fixed, Film: 8.2 kΩ, 5%, 1/8 W	1	CF1/8-8.2K/J	09021	
R31	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	3	CF1/8-3.3K/J	09021	
R32	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	7	CF1/8-10K/J	09021	
R33	Resistor, Fixed, Film: 12 kΩ, 5%, 1/8 W	2	CF1/8-12K/J	09021	
R34	Resistor, Trim, Film: 200 kΩ, 10%, 1/2 W	1	62PR200K	73138	
R35	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	3	CF1/8-1.0K/J	09021	
R36	Same as R32				
R37	Same as R6				
R38	Resistor, Fixed, Film: 3.3 Ω, 5%, 1/8 W	1	CF1/8-3.3 OHMS/J	09021	
R39	Same as R1				
R40	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	4	CF1/8-47K/J	09021	
R41	Same as R6				
R42	Resistor, Trim, Film: 20 kΩ, 10%, 1/2 W	1	62PR20K	73138	
R43	Resistor, Fixed, Film: 3.6 kΩ, 5%, 1/8 W	1	CF1/8-3.6K/J	09021	
R44	Resistor, Fixed, Film: 22 Ω, 5%, 1/8 W	1	CF1/8-22 OHMS/J	09021	
R45	Resistor, Trim, Film: 50 Ω, 10%, 1/2 W	1	62PR50	73138	
R46	Same as R10				
R47	Resistor, Fixed, Film: 360 Ω, 5%, 1/8 W	1	CF1/8-360 OHMS/J	09021	
R48	Resistor, Variable, Film: 500 Ω, 10%, 1/2 W	1	62PR500	73138	
R49	Same as R19				
R50	Same as R19				
R51	Resistor, Fixed, Film: 1.2 kΩ, 5%, 1/8 W	2	CF1/8-1.2K/J	09021	
R52	Same as R35				
R53	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	2	CF1/8-470 OHMS/J	09021	
R54	Same as R33				
R55	Same as R1				
R56	Same as R31				
R57	Same as R31				

REF DESIG PREFIX **A2A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R58	Same as R13				
R59	Same as R24				
R60	Resistor, Fixed, Film: 20 Ω, 5%, 1/8 W	1	CF1/8-20 OHMS/J	09021	
R61	Same as R13				
R62	Same as R20				
R63	Resistor, Fixed, Film: 27 kΩ, 5%, 1/8 W	1	CF1/8-27K/J	09021	
R64	Resistor, Fixed, Film: 91 kΩ, 5%, 1/8 W	1	CF1/8-91K/J	09021	
R65	Same as R24				
R66	Same as R40				
R67	Same as R63				
R68	Same as R32				
R69	Resistor, Fixed, Film: 43 kΩ, 5%, 1/8 W	1	CF1/8-43K/J	09021	
R70	Resistor, Fixed, Film: 1.0 MΩ, 5%, 1/8 W	1	CF1/8-1M/J	09021	
R71	Same as R40				
R72	Same as R23				
R73	Resistor, Variable, Film: 5 kΩ, 10%, 1/2 W	1	62PR5K	73138	
R74	Same as R1				
R75	Resistor, Fixed, Film: 2 kΩ, 5%, 1/8 W	2	CF1/8-2K/J	09021	
R76	Same as R32				
R77	Same as R32				
R78	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	1	CF1/8-22K/J	09021	
R79	Same as R32				
R80	Same as R24				
R81	Same as R32				
R82	Same as R24				
R83	Same as R19				
R84	Resistor, Fixed, Film: 23.7 kΩ, 1%, 1/10 W	1	RN55C2372F	81349	
R85	Resistor, Fixed, Film: 9.09 kΩ, 1%, 1/10 W	1	RN55C9091F	81349	
R86	Same as R35				
R87	Same as R75				
R88	Resistor, Fixed, Film: 2.21 kΩ, 1%, 1/10 W	1	RN55C2211F	81349	
R89	Resistor, Fixed, Film: 6.81 kΩ, 1 %, 1/10 W	1	RN55C6811F	81349	
R90	Resistor, Fixed, Film: 20 kΩ, 1%, 1/10 W	1	RN55C2002F	81349	
R91	Resistor, Fixed, Film: 10 kΩ, 1%, 1/10 W	1	RN55C1002F	81349	
R92	Same as R40				
R93	Same as R6				
R94	Same as R8				
R95	Same as R24				
R96	Resistor, Fixed, Film: 330 kΩ, 5%, 1/8 W	1	CF1/8-330K/J	09021	
R97	Same as R24				
R98	Same as R53				

REF DESIG PREFIX **A2A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R99	Same as R19				
R100	Resistor, Fixed, Film: 2.7 kΩ, 5%, 1/8 W	1	CF1/8-2.7K/J	09021	
R101	Resistor, Fixed, Composition: 10 MΩ, 5%, 1/8 W	1	RCR05G106JS	81349	
R102	Same as R51				
R103	Resistor, Fixed, Film: 220 kΩ, 5%, 1/8 W	1	CF1/8-220K/J	09021	
R104	Same as R8				
R105	Resistor, Variable, Film: 20 kΩ, 10%, 1/2 W	1	62PR20K	73138	
R106	Same as R24				
T1	Transformer Assembly	1	22295-74	14632	
T2	Transformer	2	T16-1	15542	
T3	Same as T2				
U1	Integrated Circuit	1	TDA1576	52648	
U2	Integrated Circuit	2	MWA110	04713	
U3	Integrated Circuit	3	DG303CJ	17856	
U4	Integrated Circuit	1	LM318N	27014	
U5	Same as U2				
U6	Integrated Circuit	1	MC1496P	04713	
U7	Integrated Circuit	2	NE5514N	18324	
U8	Same as U3				
U9	Integrated Circuit	1	DG212CJ	17856	
U10	Same as U7				
U11	Same as U3				
U12	Voltage Regulator	1	MC78L15ACP	04713	
U13	Voltage Regulator	1	MC79L15ACP	04713	
U14	Integrated Circuit	1	LM317LZ	27014	
VR1	Not Used				
VR2	Diode, Zener: 6.2 V	1	1N753A	80131	
W1	Cable Assembly	1	17300-353-1	14632	

5.5.2.3 **Type 371152-1 Video/Audio/COS** REF DESIG PREFIX **A2A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	5	1N4446	80131	
CR2 Thru CR5	Same as CR1				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	12	8121-050-651-104M	59660	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 390 pF, 5%, 100 V	4	8121-100-COGO-391J	59660	
C4	Same as C1				
C5	Same as C3				
C6 Thru C8	Same as C1				
C9	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	6	34452-1	14632	
C10	Same as C9				
C11	Same as C3				
C12	Same as C1				
C13	Same as C1				
C14	Same as C3				
C15	Capacitor, Electrolytic, Tantalum: 3.3 µF, 20%, 35 V	1	196D335X0035JE3	56289	
C16	Capacitor, Ceramic, Disc: 27 pF, 5%, 50 V	1	8111-050-COGO-270J	59660	
C17	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	2	8131-050-651-105M	59660	
C18	Same as C17				
C19	Capacitor, Ceramic, Disc: 0.015 µF, 10%, 100 V	1	8121-100-X7R0-153K	59660	
C20	Same as C1				
C21	Same as C1				
C22 Thru C25	Same as C9				
C26	Not Used				
C27	Capacitor, Ceramic, Disc: 2.7 pF ±0.1 pF, 100 V	2	8101-100-COJO-2798	59660	
C28	Same as C27				
C29	Capacitor, Electrolytic, Aluminum: 10 µF ±20%, 25 V	2	ECE-A1EK100	54473	
C30	Same as C29				
C31	Same as C1				
C32	Same as C1				
E1	Terminal, Forked	9	140-1941-02-01	71279	
E2 Thru E9	Same as E1				
J1	Terminal, Strip	1	65500-109	22526	
J2	Terminal, Strip	1	65500-106	22526	
L1	Coil, Fixed: 120 µH, 10%	3	1025-70	99800	
L2	Coil, Fixed: 2.2 µH, 10%	1	1025-28	99800	

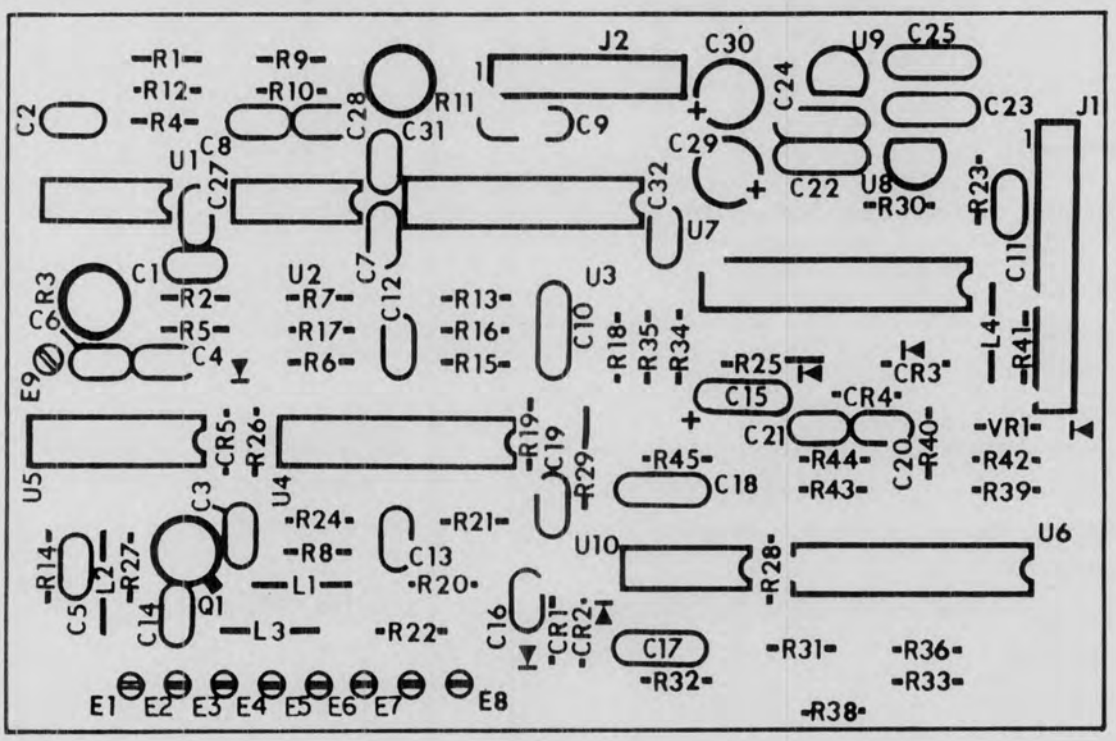

Figure 5-14. Type 371152-1 Video/Audio/COS (A2A3), Location of Components

REF DESIG PREFIX **A2A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
L3	Same as L1				
L4	Same as L1				
Q1	Transistor	1	2N2222A	80131	
R1	Resistor, Fixed, Film: 330 Ω, 5%, 1/8 W	2	CF1/8-330 OHMS/J	09021	
R2	Resistor, Fixed, Film: 2.7 Ω, 5%, 1/8 W	1	CF1/8-2.7 OHMS/J	09021	
R3	Resistor, Variable, Film: 2 kΩ, 10%, 1/2 W	1	62PR2K	73138	
R4	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	2	CF1/8-470 OHMS/J	09021	
R5	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	2	CF1/8-1.0K/J	09021	
R6	Resistor, Fixed, Film: 910 Ω, 5%, 1/8 W	1	CF1/8-910 OHMS/J	09021	
R7	Resistor, Fixed, Film: 3.6 kΩ, 5%, 1/8 W	1	CF1/8-3.6K/J	09021	
R8	Resistor, Fixed, Film: 560Ω, 5%, 1/8 W	3	CF1/8-560 OHMS/J	09021	
R9	Same as R1				
R10	Resistor, Fixed, Film: 1.8 kΩ, 5%, 1/8 W	1	CF1/8-1.8K/J	09021	
R11	Resistor, Variable, Film: 5 kΩ, 10%, 1/2 W	1	62PR5K	73138	
R12	Same as R4				
R13	Same as R5				
R14	Resistor, Fixed, Film: 68 Ω, 5%, 1/8 W	1	CF1/8-68 OHMS/J	09021	
R15	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	5	CF1/8-10K/J	09021	
R16	Resistor, Fixed, Film: 56 Ω, 5%, 1/8 W	1	CF1/8-56 OHMS/J	09021	
R17	Resistor, Fixed, Film: 8.2 kΩ, 5%, 1/8 W	2	CF1/8-8.2K/J	09021	
R18	Same as R8				
R19	Same as R15				
R20	Resistor, Fixed, Film: 36 kΩ, 5%, 1/8 W	1	CF1/8-36K/J	09021	
R21	Same as R17				
R22	Same as R8				
R23	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	2	CF1/8-2.2K/J	09021	
R24	Same as R15				
R25	Resistor, Fixed, Film: 5.6 MΩ, 5%, 1/4 W	1	CF1/8-5.6M/J	09021	
R26	Same as R23				
R27	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	1	CF1/8-100 OHMS/J	09021	
R28	Same as R15				
R29	Resistor, Fixed, Film: 10 MΩ, 5%, 1/4 W	1	CF1/4-10M/J	09021	
R30	Resistor, Fixed, Film: 270 Ω, 5%, 1/8 W	1	CF1/8-270 OHMS/J	09021	
R31	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/8 W	8	CF1/8-4.7K/J	09021	
R32	Resistor, Fixed, Film: 13 kΩ, 5%, 1/8 W	1	CF1/8-13K/J	09021	
R33	Resistor, Fixed, Film: 2.7 kΩ, 5%, 1/8 W	2	CF1/8-2.7K/J	09021	
R34	Same as R31				
R35	Resistor, Fixed, Film: 2.4 kΩ, 5%, 1/8 W	1	CF1/8-2.4K/J	09021	
R36	Same as R15				
R37	Not Used				
R38	Same as R31				

REF DESG PREFIX **A2A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R39	Same as R31				
R40	Resistor, Fixed, Film: 51 kΩ, 5%, 1/8 W	1	CF1/8-51K/J	09021	
R41 Thru R44	Same as R31				
R45	Same as R33				
U1	Integrated Circuit	3	LM318N	27014	
U2	Same as U1				
U3	Integrated Circuit	1	DG303CJ	17856	
U4	Integrated Circuit, OP AMP	2	NE5514N	18324	
U5	Integrated Circuit	1	LH0002CN	27014	
U6	Same as U4				
U7	Integrated Circuit	1	DG212CJ	17856	
U8	Voltage Regulator	1	MC79L15ACP	04713	
U9	Voltage Regulator	1	NC78L15ACP	04713	
U10	Same as U1				
VR1	Diode, Zener: 5.6 V	1	1N752A	80131	

5.5.2.4 **Type 371153-1 Digital Interface** REF DESIG PREFIX **A2A4**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	9	34452-1	14632	
C2	Capacitor, Cermaic, Disc: 0.1 µF, 20%, 50 V	14	34475-1	14632	
C3 Thru C5	Same as C1				
C6	Capacitor, Electrolytic, Tantalum: 22 µF, 20%, 10 V	1	196D226X0010JE3	56289	
C7 Thru C9	Same as C2				
C10	Capacitor, Ceramic, Disc: 33 pF, 5%, 100 V	2	8121-100-COGO-330J	59660	
C11	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	1	8131-050-651-105M	59660	
C12	Same as C2				
C13	Same as C1				
C14	Same as C2				
C15	Same as C1				
C16 Thru C19	Same as C2				
C20	Same as C10				
C21 Thru C23	Same as C1				
C24 Thru C27	Same as C2				
E1	Terminal, Forked	3	140-1019-02-01	71279	
E2	Same as E1				
E3	Not Used				
E4	Same as E1				
J1	Connector, Plug	1	65820-003	22526	
J2	Terminal Strip	1	65500-109	22526	
J3	Terminal Strip	1	65500-112	22526	
J4	Terminal Strip	1	65500-114	22526	
RN1	Resistor, Network	1	4306R-101-103	80294	
R1	Resistor, Fixed, Film: 120 Ω, 5%, 1/4 W	3	CF1/4-120 OHMS/J	09021	
R2	Same as R1				
R3	Same as R1				
R4	Resistor, Fixed, Film: 510 kΩ, 5%, 1/8 W	2	CF1/8-510K/J	09021	
R5	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	2	CF1/8-100K/J	09021	
R6	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	2	CF1/8-10K/J	09021	
R7	Resistor, Fixed, Film: 33 kΩ, 5%, 1/8 W	2	CF1/8-33K/J	09021	
R8	Same as R5				
R9	Resistor, Fixed, Film: 24 kΩ, 5%, 1/8 W	1	CF1/8-24K/J	09021	
R10	Resistor, Fixed, Film: 56 kΩ, 5%, 1/8 W	1	CF1/8-56K/J	09021	

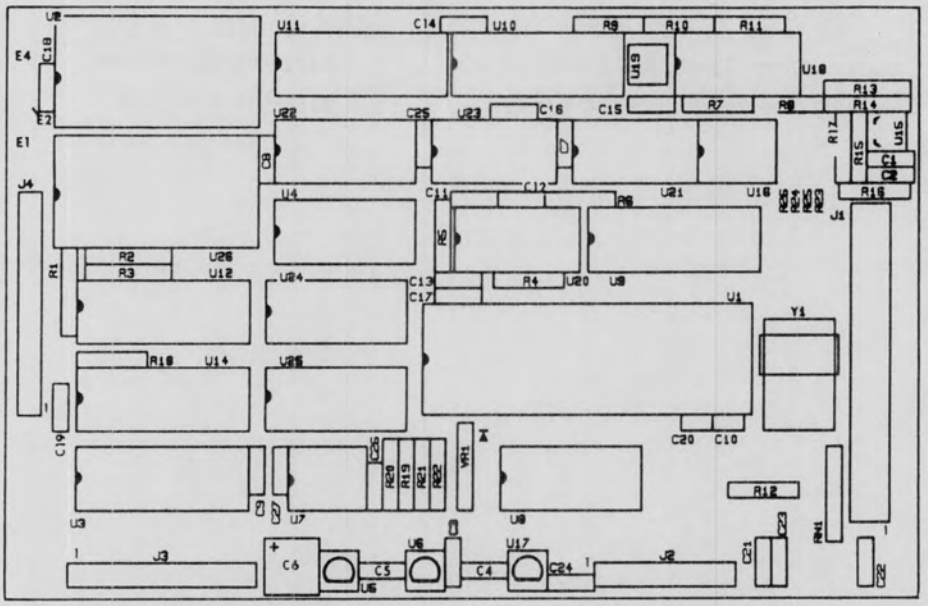

Figure 5-15. Type 371153-1 Digital Interface (A2A4), Location of Components

REF DESIG PREFIX **A2A4**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R11	Resistor, Fixed, Film: 20 kΩ, 5%, 1/8 W	1	CF1/8-20K/J	09021	
R12	Resistor, Fixed, Film: 560 kΩ, 5%, 1/8 W	2	CF1/8-560 OHMS/J	09021	
R13	Resistor, Fixed, Film: 12.1 kΩ, 1%, 1/10 W	1	RN55C1212F	81349	
R14	Resistor, Fixed, Film: 100 kΩ, 1%, 1/10 W	5	RNC55H1003FM	81349	
R15	Resistor, Fixed, Film: 4.7 kΩ, 5%, 1/8 W	1	CF1/8-4.7K/J	09021	
R16	Resistor, Fixed, Film: 240 Ω, 5%, 1/8 W	1	CF1/8-240 OHMS/J	09021	
R17	Resistor, Fixed, Film: 270 Ω, 5%, 1/8 W	2	CF1/8-270 OHMS/J	09021	
R18	Same as R6				
R19	Resistor, Fixed, Film: 62 kΩ, 5%, 1/8 W	2	CF1/8-62K/J	09021	
R20	Same as R14				
R21	Same as R19				
R22	Same as R14				
R23	Same as R17				
R24	Same as R7				
R25	Same as R14				
R26	Same as R14				
U1	Integrated Circuit	1	P80C31BH	34649	
U2	Integrated Circuit	1	D2732A	34649	
U3	Integrated Circuit	2	MM74C374N	27014	
U4	Integrated Circuit	1	MC14161BCP	04713	
U5	Integrated Circuit	1	MC78L05ACP	04713	
U6	Voltage Regulator	1	MC78L15ACP	04713	
U7	Integrated Circuit	2	TL062CP	01295	
U8	Integrated Circuit	1	DG212CJ	17856	
U9	Same as U3				
U10	Integrated Circuit	1	AD7226KN	04713	
U11	Integrated Circuit	1	MM74HC373N	27014	
U12	Integrated Circuit	2	MM74C244N	27014	
U13	Not Used				
U14	Same as U12				
U15	Integrated Circuit	1	LM317LZ	27014	
U16	Same as U7				
U17	Voltage Regulator	1	MC79L15ACP	04713	
U18	Integrated Circuit	1	TL064CN	01295	
U19	Integrated Circuit	1	AD580JH	24355	
U20	Integrated Circuit	1	MM74C14N	27014	
U21	Integrated Circuit	1	MM74HC08N	27014	
U22	Integrated Circuit	1	MM74HC138N	27014	
U23	Integrated Circuit	1	MM74HC04N	27014	
U24	Integrated Circuit	1	CD4021BE	02735	
U25	Integrated Circuit	1	CD4094BE	02735	

REF DESIG PREFIX **A2A4**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U26	Integrated Circuit	1	HM6116LP-4	62786	
VR1	Diode, Zener: 10 V	1	1N758A	80131	
XU1	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	
XU3	Socket, Integrated Circuit	1	ICN-246-S5-T	06776	
Y1	Crystal, Quartz	1	CR64U 10.000 MHz	80058	

5.5.2.5 **Type 371154-1 FM Demodulator Motherboard** REF DESIG PREFIX **A2A5**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	IF Bandwidth Option		WJ-9928-XXXX	14632	
A2 Thru A4	Same as A1				
C1	Capacitor, Ceramic, Disc: 4700 pF, 10%, 50 V	12	8111-050-X7RO-472K	59660	
C2 Thru C10	Same as C1				
C11	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	4	8121-050-651-104M	59660	
C12	Same as C11				
C13	Capacitor, Ceramic, Disc: 0.1 µF, 10%, 100 V	5	CK06BX104K	81349	
C14	Same as C11				
C15	Same as C11				
C16	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	4	34452-1	14632	
C17	Same as C16				
C18	Capacitor, Electrolytic, Aluminum: 10 µF ±20%, 25 V	2	ECE-A1EK100	54473	
C19	Same as C16				
C20	Same as C16				
C21	Same as C18				
C22	Same as C1				
C23	Same as C1				
J1	Terminal Strip	1	65500-114	22526	
J2	Connector	1	65624-103	22526	
J3	Interconnect Strip	4	170554-1	14632	
J4	Interconnect Strip	8	170554-2	14632	
J5	Same as J4				
J6	Interconnect Strip	8	170554-3	14632	
J7	Same as J6				
J8	Same as J3				
J9	Same as J4				
J10	Same as J4				
J11	Same as J6				
J12	Same as J6				
J13	Same as J3				
J14	Same as J4				
J15	Same as J4				
J16	Same as J6				
J17	Same as J6				
J18	Same as J3				
J19	Same as J4				
J20	Same as J4				
J21	Same as J6				

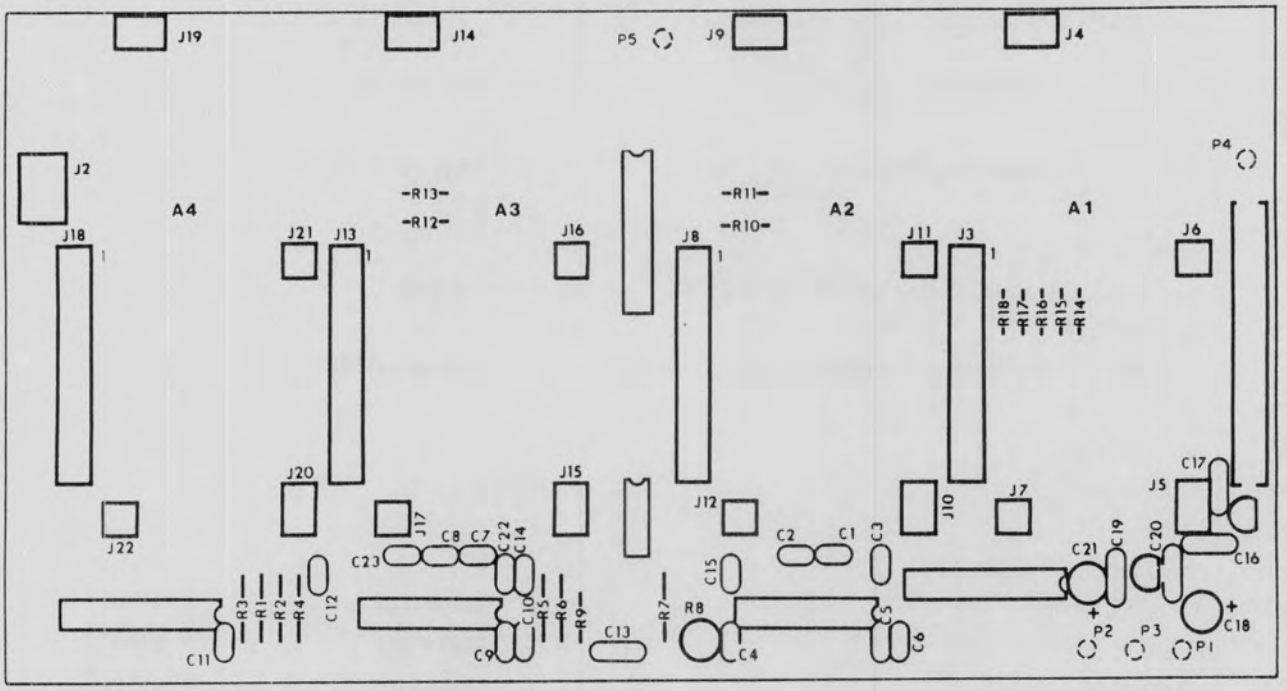

Figure 5-16. Type 371154-1 FM Demodulator Motherboard (A2A5), Location of Components

REF DESIG PREFIX **A2A5**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
J22	Same as J6				
P1	Pin Socket	5	NS-441-B1	06776	
P2	Same as P1				
P3 Thru P5	Same as P1				
R1	Resistor, Fixed, Film: 9.1 kΩ, 5%, 1/4 W	2	CF1/4-9.1K/J	09021	
R2	Resistor, Fixed, Film: 5.6 kΩ, 5%, 1/4 W	2	CF1/4-5.6K/J	09021	
R3	Same as R1				
R4	Same as R2				
R5	Resistor, Fixed, Film: 12 kΩ, 5%, 1/4 W	1	CF1/4-12K/J	09021	
R6	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/4 W	1	CF1/4-1K/J	09021	
R7	Resistor, Fixed, Film: 47 kΩ, 5%, 1/4 W	1	CF1/4-47K/J	09021	
R8	Resistor, Variable, Film: 100 kΩ, 10%, 1/2 W	1	62PR100K	73138	
R9	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	1	CF1/8-1.5K/J	09021	
R10	Resistor, Fixed, Composition: 47 kΩ, 5%, 1/8 W	4	RCR05G473JS	81349	
R11 Thru R13	Same as R10				
R14	Resistor, Fixed, Composition: 100 kΩ, 5%, 1/8 W	5	RCR05G104JS	81349	
R15 Thru R18	Same as R14				
U1	Integrated Circuit	2	DG302CJ	17856	
U2	Integrated Circuit	3	MC14052BCP	04713	
U3	Same as U1				
U4	Same as U2				
U5	Same as U2				
U6	Integrated Circuit	1	TL061ACP	01295	
U7	Voltage Regulator	1	MC78L15ACP	04713	
U8	Voltage Regulator	1	MC79L15ACP	04713	

5.5.3 **TYPE 794447-1 SYNTHESIZER MODULE** REF DESIG PREFIX **A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Connector Interface	1	371159-1	14632	
A2	Time Base	1	371160-1	14632	
A3	2nd LO VCO	1	371161-1	14632	
A4	2nd LO PLL	1	371162-1	14632	
A5	Auxiliary,PLL Phase Detector	1	371163-1	14632	
A6	Auxiliary, VCO	1	371164-1	14632	
A7	BFO Assembly	1	371165-1	14632	
A8	Reference Mixer	1	371166-1	14632	
A9	1st LO Phase Detector/Divider	1	371167-1	14632	
A10	1st LO VCO	1	470958-1	14632	
C1	Capacitor, Ceramic, Feedthru: 33 pF, 10%, 500 V	1	54-794-001-3301	33095	
C2	Capacitor, Ceramic, Feedthru: 0.05 µF, GMV, 300 V	12	54-785-002-503P	33095	
C3 Thru C13	Same as C2				
C14	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	1	34475-1	14632	
E1	Connector, Terminal	2	8044-1551-003	19505	
E2	Same as E1				
E3	Terminal, Feedthru, Insulated	5	SFU16Y	04013	
E4 Thru E7	Same as E3				
J1	Connector, Plug	1	DBSPRB25P	71468	
J2	Connector, Jack: SMA Series	1	2004-7188	26805	
J3	Connector, Receptacle: SMB Series	3	2012-1511-000	19505	
J4	Same as J3				
J5	Same as J3				
J6	Connector, Receptacle: SMB Series	1	2004-1511-000	19505	
P1	Not Used				
P2	Housing, Connector	1	86427-1	00779	
W1	Cable Assembly	1	271370-1	14632	
W2	Cable Assembly	1	17300-346-1	14632	
W3	Cable Assembly	1	17300-346-2	14632	
W4	Cable Assembly	1	271371-1	14632	
W1P1	Connector Plug	4	IDD-7-G	55322	
W1P2 Thru W1P4	Same as W1P1				
W3P1	Connector Plug	1	2002-1551-003	19505	
W4P1	Connector, Multipin, PL	1	66900-026	22526	

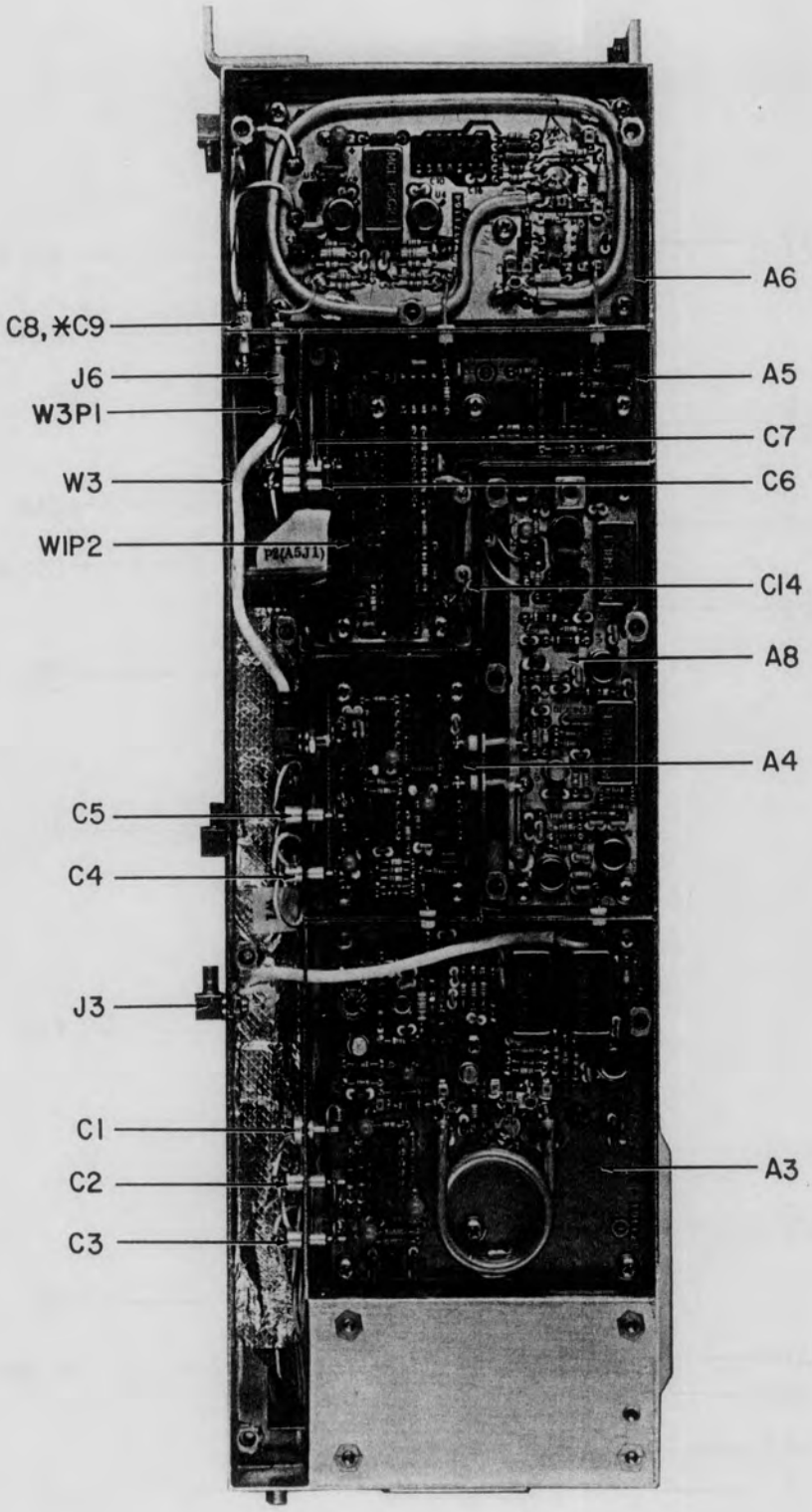

Figure 5-17. Type 794447-1 Synthesizer Module (A3), Top View, Location of Components

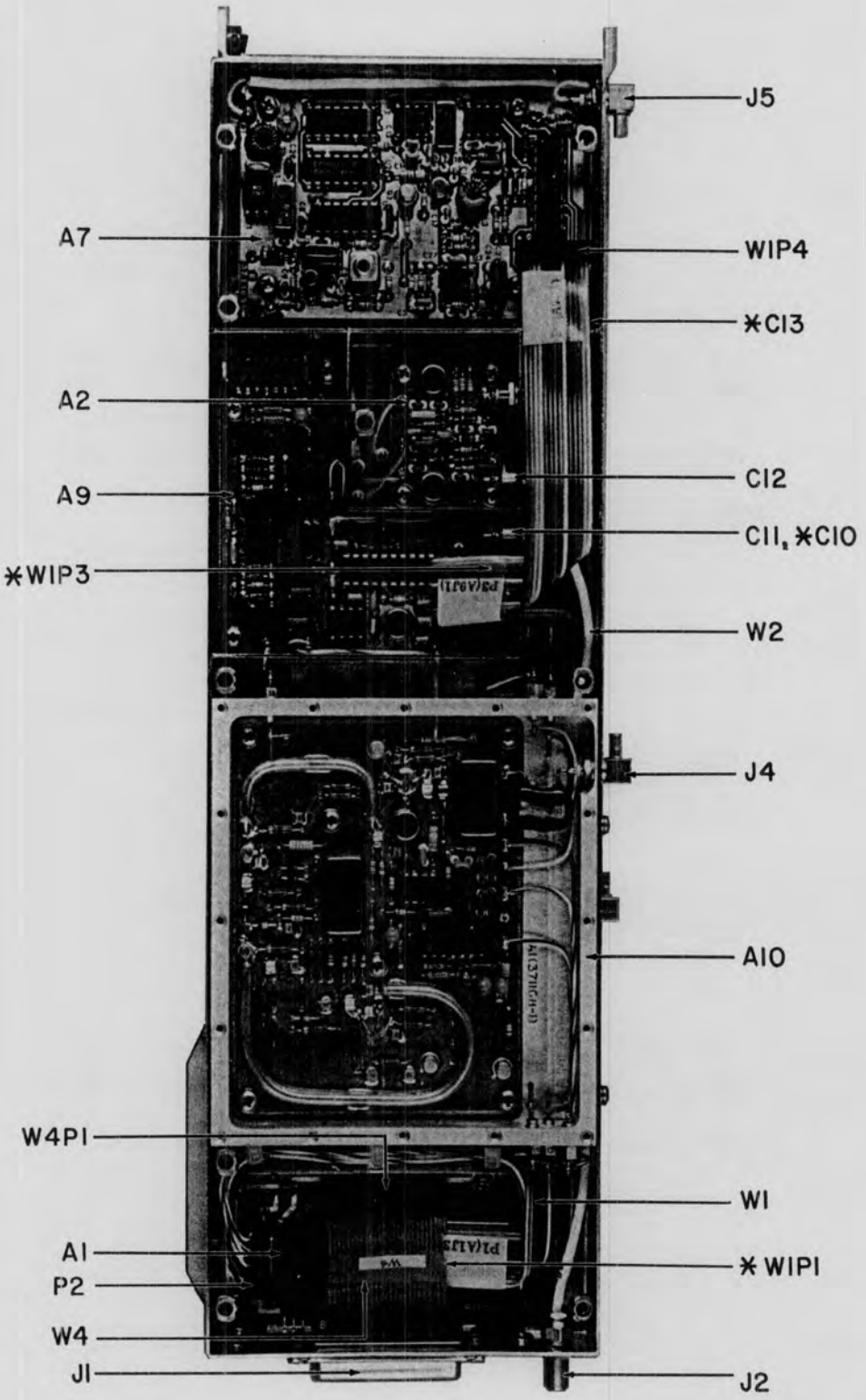

Figure 5-17. Type 794447-1 Synthesizer Module (A3), Bottom View, Location of Components

5.5.3.1 **Type 371159-1 Connector Interface** REF DESIG PREFIX **A3A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	1	34475-1	14632	
J1	Connector Plug	1	65820-003	22526	
J2	Terminal Strip	1	65610-126	22526	
J3	Connector, Receptacle	1	65610-114	22526	
J4	Connector, Receptacle	1	87224-7	00779	
R1	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	1	CF1/8-10K/J	09021	
U1	Integrated Circuit	2	DG202BJ	17856	

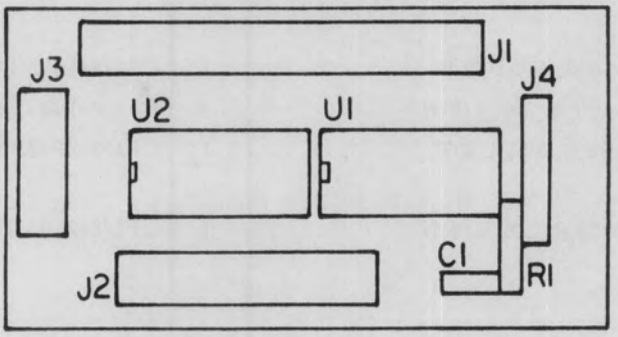

Figure 5-18. Type 371159-1 Connector Interface (A3A1), Location of Components

5.5.3.2 **Type 371160-1 Time Base** REF DESIG PREFIX **A3A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 68 pF, 5%, 100 V	5	8121-100-COGO-680J	59660	
C2	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	34475-1	14632	
C3 Thru C5	Same as C1				
C6	Same as C2				
C7	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	2	8131-050-651-105M	59660	
C8	Same as C7				
C9	Same as C1				
C10	Capacitor, Ceramic, Monolithic: 47 pF, 5%, 100 V	1	8121-100-COGO-470J	59660	
E1	Terminal Forked	5	140-1941-02-01	71279	
E2 Thru E5	Same as E1				
L1	Coil, Fixed, Molded: 12 µH, 10%	1	1025-46	99800	
L2	Coil, Fixed, Molded: 0.33 µH, 10%	1	1025-08	99800	
L3	Coil, Fixed: 0.15 µH	2	1025-00	9980	
L4	Same as L3				
R1	Resistor, Fixed, Film: 150 Ω, 5%, 1/8 W	2	CF1/8-150 OHMS/J	09021	
R2	Resistor, Fixed, Film: 36 Ω, 5%, 1/8 W	1	CF1/8-36 OHMS/J	09021	
R3	Same as R1				
R4	Resistor, Fixed, Film: 10 Ω, 5%, 1/8 W	1	CF1/8-10 OHMS/J	09021	
R5	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	3	CF1/8-100 OHMS/J	09021	
R6	Resistor, Fixed, Film: 68 Ω, 5%, 1/8 W	1	CF1/8-68 OHMS/J	09021	
R7	Same as R5				
R8	Resistor, Fixed, Film: 220 Ω, 5%, 1/8 W	1	CF1/8-220 OHMS/J	09021	
R9	Same as R5				
U1	Not Used				
U2	Integrated Circuit	1	MWA120	04713	
U3	Integrated Circuit	1	MWA110	04713	
U4	Integrated Circuit	1	MC78L05ACP	04713	

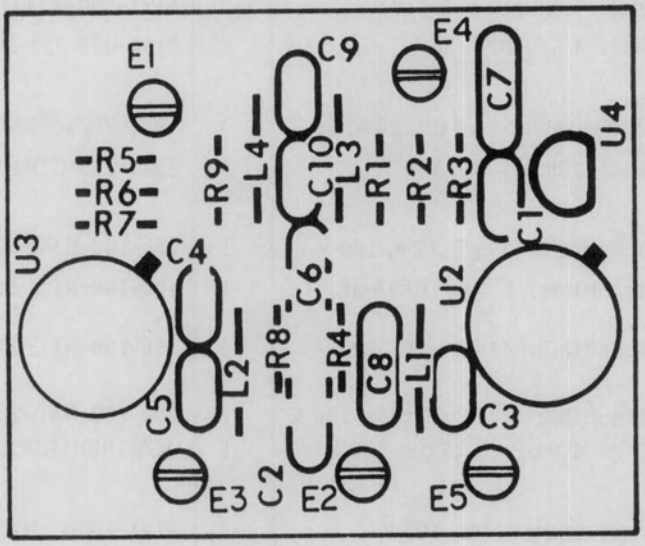

Figure 5-19. Type 371160-1 Time Base (A3A2), Location of Components

5.5.3.3 **Type 371161-1 2nd LO VCO** REF DESIG PREFIX **A3A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Not Used				
CR2	Diode	3	U11-3102	52673	
CR3	Same as CR2				
CR4	Same as CR2				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	1	8121-050-651-104M	59660	
C2	Capacitor, Ceramic, Disc: 15 pF, 5%, 50 V	1	8101-050-COGO-150J	59660	
C3	Capacitor, Ceramic, Monolithic: 37 pF ±2%, 100 V	1	150-100-NPO-360G	51642	
C4	Caapcitor, Ceramic, Disc: 12 pF, 5%, 100 V	1	8111-100-COGO-120J	59660	
C5	Capacitor, Ceramic, Disc: 1000 pF, 10%, 100 V	3	8121-100-X7RO-102K	59660	
C6	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	3	8131-050-651-105M	59660	
C7	Same as C6				
C8	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	4	196D475X0035JE3	56289	
C9	Capacitor, Ceramic, Disc: 100 pF, 5%, 100 V	1	8121-100-COGO-101J	59660	
C10	Same as C5				
C11	Capacitor, Ceramic, Monolithic: 30 pF ±2%, 100 V	1	150-100-NPO-300G	51642	
C12	Capacitor, Ceramic, Monolithic: 8.2 pF ±0.25 pF, 100 V	1	100-100-NPO-829C	51642	
C13	Capacitor, Ceramic, Monolithic: 47 pF ±2%, 100 V	2	150-100-NPO-470G	51642	
C14	Same as C13				
C15	Capacitor, Ceramic, Monolithic: 2200 pF ±2%, 100 V	2	200-100-NP0-222G	51642	
C16	Capacitor, Ceramic, Chip: 1.0 pF ±0.25 pF, 500 V	1	ATC100B1R0CP500X	29990	
C17	Same as C15				
C18	Capacitor, Ceramic, Disc: 680 pF, 5%, 100 V	2	8121-100-COGO-681J	59660	
C19	Same as C18				
C20	Capacitor, Ceramic, Chip: 6.8 pF ±.25 pF, 500 V	1	ATC100B6R8CP500X	29990	
C21	Capacitor, Variable, Air: 0.6-4.5 pF, 500 V	1	27273	91293	
C22	Capacitor, Ceramic, Chip: 24 pF, 5%, 500 V	1	ATC100B240JP500X	29990	
C23	Capacitor, Ceramic, Chip: 10 pF, 2%, 500 V	1	ATC100B100GP500X	29990	
C24	Capacitor, Ceramic, Chip: 4.7 pF ±.25 pF, 500 V	1	ATC100B4R7CP500X	29990	
C25	Same as C8				
C26	Same as C5				
C27	Same as C6				
C28	Same as C8				
C29	Same as C8				
C30	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	1	34452-1	14632	
C31	Capacitor, Ceramic, Chip: 470 pF, 10%, 500 V	1	ATC100B471KP500X	29990	
DL1	Transformer	1	271414-1	14632	
E1	Terminal, Forked	7	140-1941-02-01	71279	
E2 Thru E7	Same as E1				
L1	Coil, Mounted	1	271423-12	14632	
L2	Coil, Fixed: 1.2 µH, 10%	1	1025-22	99800	

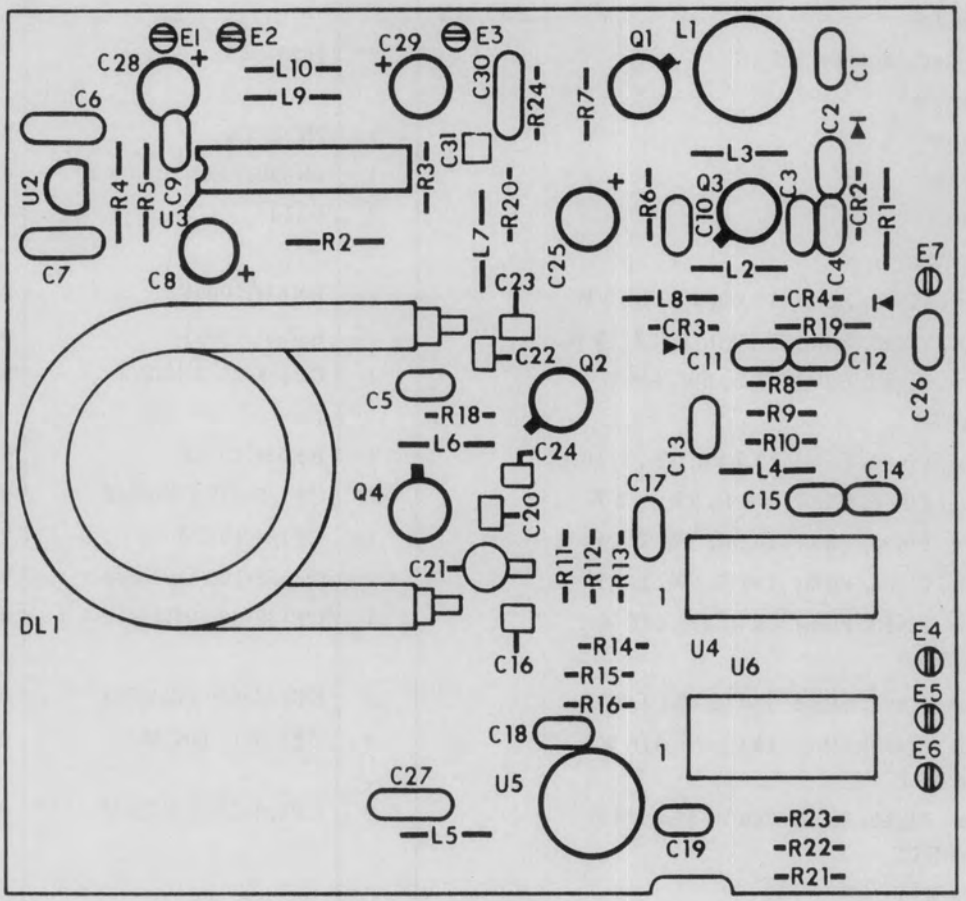

Figure 5-20. Type 371161-1 2nd LO VCO (A3A3), Location of Components

REF DESIG PREFIX **A3A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
L3	Coil, Fixed, Molded: 10 µH	1	1025-44	99800	
L4	Coil, Fixed, Molded: 0.1 µH	1	1025-94	99800	
L5	Coil, Fixed, Molded: 1.5 µH, 10%	2	1025-24	99800	
L6	Coil, Fixed: 0.27 µH	1	1025-06	99800	
L7	Coil, Fixed: 0.15 µH	1	1025-00	99800	
L8	Same as L5				
L9	Coil, Fixed, Molded: 10 µH	2	1025-44	99800	
L10	Same as L9				
Q1	Transistor	1	2N2222A	80131	
Q2	Transistor	1	2N2907/JAN	81350	
Q3	Transistor	2	U310	17856	
Q4	Same as Q3				
R1	Resistor, Fixed, Film: 10 kΩ, 1%, 1/10 W	2	RN55C1002F	81349	
R2	Resistor, Fixed, Film: 7.5 kΩ, 1%, 1/10 W	2	RN55C7501F	81349	
R3	Resistor, Fixed, Film: 22 Ω, 5%, 1/8 W	1	CF1/8-22 OHMS/J	09021	
R4	Same as R2				
R5	Resistor, Fixed, Film: 13.7 kΩ, 1%, 1/10 W	1	RN55C1372F	81349	
R6	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	1	CF1/8-470 OHMS/J	09021	
R7	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	1	CF1/8-10K/J	09021	
R8	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	2	CF1/8-100 OHMS/J	09021	
R9	Resistor, Fixed, Film: 68 Ω, 5%, 1/8 W	1	CF1/8-68 OHMS/J	09021	
R10	Same as R8				
R11	Resistor, Fixed, Film: 330 Ω, 5%, 1/8 W	2	CF1/8-330 OHMS/J	09021	
R12	Resistor, Fixed, Film: 18 Ω, 5%, 1/8 W	2	CF1/8-18 OHMS/J	09021	
R13	Same as R11				
R14	Resistor, Fixed, Film: 300 Ω, 5%, 1/8 W	2	CF1/8-300 OHMS/J	09021	
R15	Same as R12				
R16	Same as R14				
R17	Not Used				
R18	Resistor, Fixed, Film: 270 Ω, 5%, 1/8 W	1	CF1/8-270 OHMS/J	09021	
R19	Same as R1				
R20	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	1	CF1/8-2.2K/J	09021	
R21	Resistor, Fixed, Film: 180 Ω, 5%, 1/8 W	2	CF1/8-180 OHMS/J	09021	
R22	Resistor, Fixed, Film: 33 Ω, 5%, 1/8 W	1	CF1/8-33 OHMS/J	09021	
R23	Same as R21				
R24	Resistor, Fixed, Film: 220 Ω, 5%, 1/8 W	1	CF1/8-220 OHMS/J	09021	
U1	Not Used				
U2	Integrated Circuit	1	MC78L05ACP	04713	
U3	Integrated Circuit	1	723DC	07263	
U4	Divider, Power	2	PSC2-1	15542	
U5	Integrated Circuit	1	MWA120	94713	
U6	Same as U4				

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5.5.3.4 **Type 371162-1 2nd LO PLL** REF DESIG PREFIX **A3A4**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	2	1N4446	80131	
CR2	Same as CR1				
C1	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	5	8131-050-651-105M	59660	
C2	Capacitor, Ceramic, Disc: 68 pF, 5%, 100 V	1	8121-100-COGO-680J	59660	
C3	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	2	196D475X0035JE3	56289	
C4	Capacitor, Ceramic, Monolithic: 150 pF, 5%, 100 V	1	8121-100-COGO-151J	59660	
C5	Same as C1				
C6	Capacitor, Electrolytic, Tantalum: 15 µF, 20%, 15 V	1	196D156X0015JE3	56289	
C7	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	1	34452-1	14632	
C8	Capacitor, Ceramic, Disc: 1000 pF, 5%, 100 V	2	8121-100-COGO-102J	59660	
C9	Same as C8				
C10	Same as C1				
C11	Same as C3				
C12	Same as C1				
C13	Same as C1				
C14	Capacitor, Ceramic, Monolithic: 10 pF ±0.5 pF, 100 V	1	8101-100-COGO-100D	59660	
E1	Terminal, Forked	6	140-1941-02-01	71279	
E2 Thru E6	Same as E1				
R1	Resistor, Fixed, Film: 2.0 kΩ, 5%, 1/8 W	1	CF1/8-2.0K/J	09021	
R2	Resistor, Fixed, Film: 110 kΩ, 5%, 1/8 W	1	CF1/8-110K/J	09021	
R3	Resistor, Fixed, Film: 56 kΩ, 5%, 1/8 W	1	CF1/8-56K/J	09021	
R4	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	1	CF1/8-100K/J	09021	
R5	Resistor, Fixed, Film: 51 kΩ, 5%, 1/8 W	2	CF1/8-51K/J	09021	
R6	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	3	CF1/8-10K/J	09021	
R7	Same as R6				
R8	Same as R5				
R9	Same as R6				
U1	Integrated, Circuit	1	NE5534AN	18324	
U2	Integrated, Circuit	1	MM74C932N	27014	
U3	Integrated, Circuit	1	MM74HC390N	27014	
U4	Integrated, Circuit	1	SP8792	52648	
U5	Voltage Regulator	1	MC78L15ACP	04713	
U6	Integrated Circuit	1	MC78L05ACP	04713	

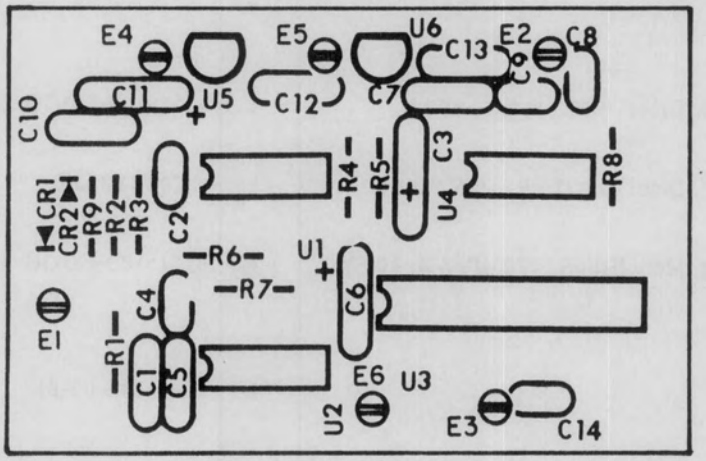


Figure 5-21. Type 371162-1 2nd LO PLL (A3A4), Location of Components

5.5.3.5 **Type 371163-1 AUX/PLL Phase Detector** REF DESIG PREFIX **A3A5**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	5	1N4446	80131	
CR2 Thru CR5	Same as CR1				
C1	Capacitor, Ceramic, Disc: 1000 pF, 5%, 100 V	3	8121-100-COGO-102J	59660	
C2	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	7	8131-050-651-105M	59660	
C3	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	3	34452-1	14632	
C4	Same as C1				
C5	Same as C1				
C6	Capacitor, Ceramic, Monolithic: 150 pF, 5%, 100 V	1	8121-100-COGO-151J	59660	
C7	Not Used				
C8	Not Used				
C9	Capacitor, Ceramic, Disc: 0.01 µF, 5%, 100 V	1	8131-100-COGO-103J	59660	
C10	Same as C3				
C11	Capacitor, Ceramic, Disc: 0.033 µF, 10%, 100 V	1	CK06BX333K	81349	
C12	Same as C2				
C13	Capacitor, Ceramic, Monolithic: 470 pF, 5%, 100 V	1	8121-100-COGO-471J	59660	
C14 Thru C18	Same as C2				
E1	Terminal, Forked	7	140-1941-02-01	71279	
E2 Thru E7	Same as E1				
J1	Connector, Receptacle	1	65610-114	22526	
R1	Resistor, Fixed, Film: 36 kΩ, 5%, 1/8 W	1	CF1/8-36K/J	09021	
R2	Resistor, Fixed, Film: 9.1 kΩ, 5%, 1/8 W	1	CF1/8-9.1K/J	09021	
R3	Resistor, Fixed, Film: 330 kΩ, 5%, 1/8 W	1	CF1/8-330K/J	09021	
R4	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	1	CF1/8-22K/J	09021	
R5	Resistor, Fixed, Film: 200 kΩ, 5%, 1/8 W	2	CF1/8-200K/J	09021	
R6	Resistor, Fixed, Film: 82.5 kΩ, 1%, 1/10 W	1	RN55C8252F	81349	
R7	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	3	CF1/8-10K/J	09021	
R8	Not Used				
R9	Resistor, Fixed, Film: 150 kΩ, 5%, 1/8 W	1	CF1/8-150K/J	09021	
R10	Resistor, Fixed, Film: 22.1 kΩ, 1%, 1/10 W	1	RN55C2212F	81349	
R11	Same as R7				
R12	Same as R7				
R13	Same as R5				
R14	Resistor, Fixed, Film: 68.1 kΩ, 1%, 1/10 W	1	RN55C6812F	81349	
U1	Integrated Circuit	1	74F162PC	07261	
U2	Integrated Circuit	1	NJ8821DG	52648	
U3	Integrated Circuit	1	SP8792	52648	
U4	Integrated Circuit	1	CA3140AE	02735	
U5	Integrated Circuit	1	MC78L05ACP	04713	
U6	Integrated Circuit	1	MC78L24ACP	04713	

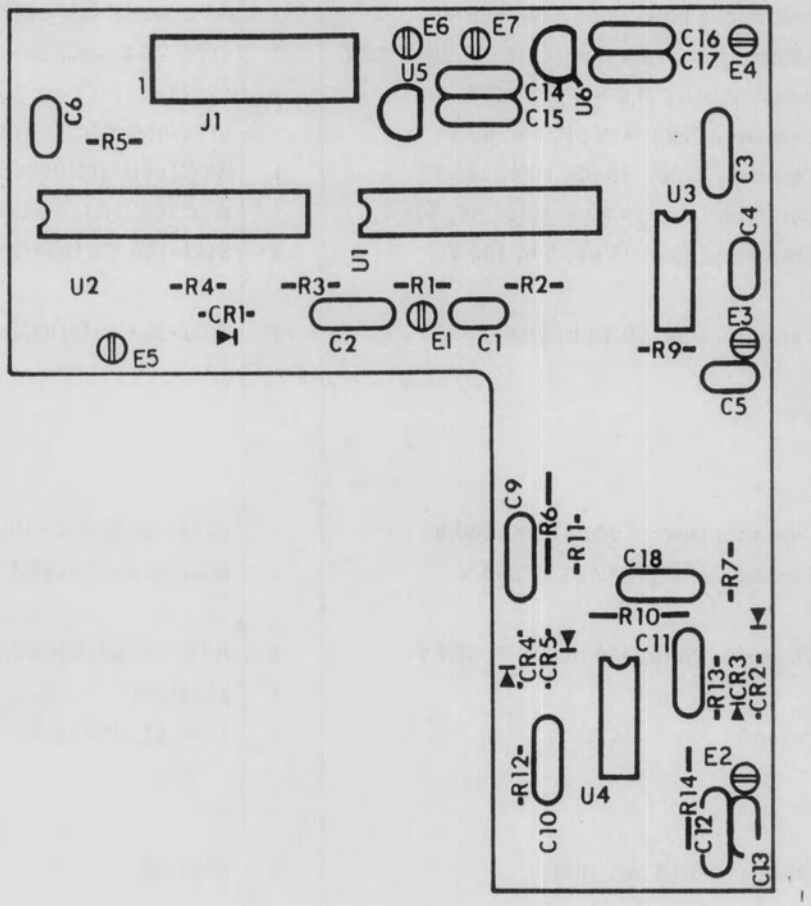


Figure 5-22. Type 371163-1 AUX/PLL Phase Detector (A3A5), Location of Components

5.5.3.6 **Type 371164-1 AUX VCO** REF DESIG PREFIX **A3A6**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode, Variable, Capacitance	4	KV3901	52673	
CR2 Thru CR4	Same as CR1				
C1	Capacitor, Ceramic, Chip: 22.0 pF ±2%, 500 V	1	ATC100B220GP500X	29990	
C2	Capacitor, Ceramic, Chip: 10 pF, 2%, 500 V	1	ATC100B100GP500X	29990	
C3	Capacitor, Ceramic, Chip: 33 pF, 2%, 500 V	1	ATC100B330GP500X	29990	
C4	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	2	196D475X0035JE3	56289	
C5	Capacitor, Variable, Air: 0.6-4.5 pF, 500 V	1	27273	91293	
C6	Capacitor, Ceramic, Disc: 470 pF, 5%, 50 V	1	8121-050-COGO-471J	59660	
C7	Capacitor, Ceramic, Chip: 68 pF, 10%, 500 V	1	ATC100B680KP500X	29990	
C8	Capacitor, Ceramic, Chip: 5.1 pF ±0.25 pF, 500 V	1	ATC700B5R1CP500X	29990	
C9	Capacitor, Ceramic, Disc: 33 pF, 5%, 100 V	4	8121-100-COGO-330J	59660	
C10	Same as C9				
C11	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	8121-050-651-104M	59660	
C12	Same as C9				
C13	Same as C11				
C14	Same as C9				
C15	Same as C4				
C16	Capacitor, Ceramic, Disc: 100 pF, 5%, 100 V	1	8121-100-COGO-101J	59660	
C17	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	2	8131-050-651-105M	59660	
C18	Same as C17				
C19	Capacitor, Ceramic, Chip: 470 pF, 10%, 500 V	1	ATC100B471KP500X	29990	
DL1	Delay Line	1	271413-1	14632	
E1	Terminal, Forked	5	140-1941-02-01	71279	
E2 Thru E5	Same as E1				
L1	Coil, Fixed, Molded: 0.18 µH, 10%	4	1025-02	99800	
L2	Same as L1				
L3	Coil, Fixed, Molded: 0.1 µH	1	1025-94	99800	
L4	Same as L1				
L5	Same as L1				
Q1	Transistor	1	U310	17856	
R1	Resistor, Fixed, Film: 220 Ω, 5%, 1/8 W	3	CF1/8-220 OHMS/J	09021	
R2	Resistor, Fixed, Film: 10 kΩ, 1%, 1/10 W	1	RN55C1002F	81349	
R3	Resistor, Fixed, Film: 7.5 kΩ, 1%, 1/10 W	2	RN55C7501F	81349	
R4	Resistor, Fixed, Film: 22 Ω, 5%, 1/8 W	1	CF1/8-22 OHMS/J	09021	
R5	Same as R3				
R6	Resistor, Fixed, Film: 13.7 kΩ, 1%, 1/10 W	1	RN55C1372F	81349	
R7	Resistor, Fixed, Film: 82 Ω, 5%, 1/8 W	2	CF1/8-82 OHMS/J	09021	

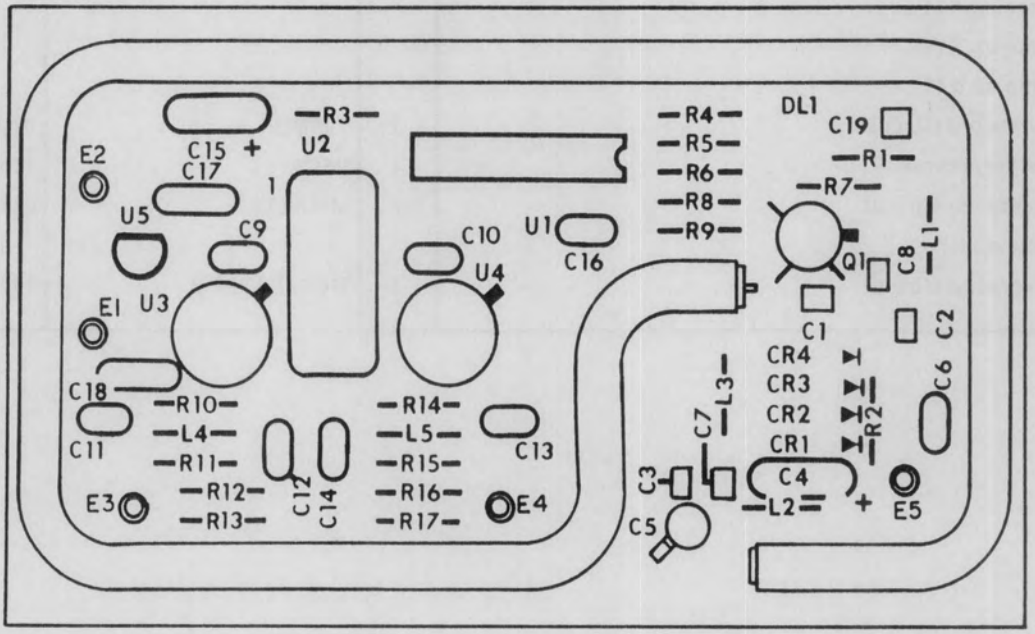


Figure 5-23. Type 371164-1 AUX VCO (A3A6), Location of Components

REF DESIG PREFIX **A3A6**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R8	Resistor, Fixed, Film: 91 Ω, 5%, 1/8 W	1	CF1/8-91 OHMS/J	09021	
R9	Same as R7				
R10	Same as R1				
R11	Resistor, Fixed, Film: 300 Ω, 5%, 1/8 W	4	CF1/8-300 OHMS/J	09021	
R12	Resistor, Fixed, Film: 18 Ω, 5%, 1/8 W	2	CF1/8-18 OHMS/J	09021	
R13	Same as R11				
R14	Same as R1				
R15	Same as R11				
R16	Same as R12				
R17	Same as R11				
U1	Integrated Circuit	1	723DC	07263	
U2	Divider/Power	1	PSC2-1	15542	
U3	Integrated Circuit	2	MWA110	04713	
U4	Same as U3				
U5	Integrated Circuit	1	MC78L05ACP	04713	

5.5.3.7 **Type 371165-1 BFO Assembly** REF DESIG PREFIX A3A7

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode, Variable, Capacitance	2	KV3901	52673	
CR2	Not Used				
CR3	Not Used				
CR4	Same as CR1				
CR5	Diode	3	1N4446	80131	
CR6	Same as CR5				
CR7	Same as CR5				
C1	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	4	8131-050-651-105M	59660	
C2	Capacitor, Ceramic, Disc: 100 pF, 5%, 100 V	1	8121-100-COGO-101J	59660	
C3	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	3	34475-1	14632	
C4	Not Used				
C5	Capacitor, Ceramic, Monolithic: 22 pF, 5%, 100 V	3	8111-100-COGO-220J	59660	
C6	Capacitor, Ceramic, Chip: 330 pF, 5%, 50 V	2	8121-050-COGO-331J	59660	
C7	Capacitor, Ceramic, Chip: 150 pF, 5%, 50 V	2	8121-050-COGO-151J	59660	
C8	Same as C6				
C9	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 50 V	4	8121-050-651-103M	59660	
C10	Same as C9				
C11	Same as C9				
C12	Capacitor, Ceramic, Disc: 100 pF, 5%, 50 V	3	8121-050-COGO-102J	59660	
C13	Same as C3				
C14	Same as C7				
C15	Capacitor, Ceramic, Monolithic: 15 pF, 5%, 100 V	1	8111-100-COGO-150J	59660	
C16	Same as C5				
C17	Same as C5				
C18	Capacitor, Ceramic, Disc: 6.8 pF ±0.25 pF, 100 V	1	8101-100-COHO-689C	59660	
C19	Not Used				
C20	Capacitor, Ceramic, Disc: 47 pF, 5%, 50 V	1	8111-050-COGO-470J	59660	
C21	Same as C12				
C22	Same as C12				
C23 Thru C25	Same as C1				
C26	Capacitor, Variable, Ceramic: 5-25 pF, 100 V	1	518-000A5-25	59660	
C27	Same as C3				
C28	Same as C9				
E1	Terminal, Forked	4	140-1941-02-01	71279	
E2 Thru E4	Same as E1				
FL1	Filter	1	XF-212	KVG	
J1	Connector, Receptacle	1	65610-114	22526	

REF DESIG PREFIX **A3A7**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
L1	Coil, Variable	1	6740-21	04213	
L2	Coil, Fixed: 18 µH, 10%	1	1025-50	99800	
L3	Coil, Mounted	1	271423-1	14632	
L4	Coil, Fixed, Molded: 1.0 µH, 10%	1	1025-20	99800	
Q1	Transistor	1	2N3478	80131	
Q2	Transistor	1	U310	17856	
Q3	Transistor	1	2N2222A	80131	
R1	Resistor, Fixed, Film: 3.9 kΩ, 5%, 1/8 W	1	CF1/8-3.9K/J	09021	
R2	Resistor, Fixed, Film: 12 kΩ, 5%, 1/8 W	2	CF1/8-12K/J	09021	
R3	Resistor, Fixed, Film: 150 kΩ, 5%, 1/8 W	3	CF1/8-150K/J	09021	
R4	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	6	CF1/8-10K/J	09021	
R5	Same as R4				
R6	Not Used				
R7	Not Used				
R8	Same as R4				
R9	Resistor, Fixed, Film: 2.7 kΩ, 5%, 1/8 W	1	CF1/8-2.7K/J	09021	
R10	Resistor, Fixed, Film: 15 kΩ, 5%, 1/8 W	1	CF1/8-15K/J	09021	
R11	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	3	CF1/8-100K/J	09021	
R12	Resistor, Fixed, Film: 220 Ω, 5%, 1/8 W	2	CF1/8-220 OHMS/J	09021	
R13	Not Used				
R14	Same as R3				
R15	Same as R4				
R16	Same as R12				
R17	Same as R4				
R18	Not Used				
R19	Same as R3				
R20	Not Used				
R21	Same as R4				
R22	Same as R11				
R23	Same as R11				
R24	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	1	CF1/8-22K/J	09021	
R25	Resistor, Fixed, Film: 470 kΩ, 5%, 1/8 W	1	CF1/8-470K/J	09021	
T1	Transformer	1	T36-1	15542	
T2	Transformer	1	271423-11	14632	
U1	Integrated Circuit	1	MM74HC390N	27014	
U2	Integrated Circuit	1	MC14568BCP	04713	
U3	Integrated Circuit	1	LM358AN	27014	
U4	Integrated Circuit	1	SN74LS393N	01295	
U5	Mixer, Balanced	1	MCL TFM-3	15542	
U6	Integrated Circuit	1	SP8793A	52648	
U7	Integrated Circuit	1	TSC-2-1	15542	

REF DESIG PREFIX **A3A7**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
U8	Integrated Circuit	1	SP8792	52648	
U9	Integrated Circuit	1	NJ8821DP	52648	
U10	Integrated Circuit	1	MC78L05ACP	04713	
Y1	Crystal	1	XS2803	99999	

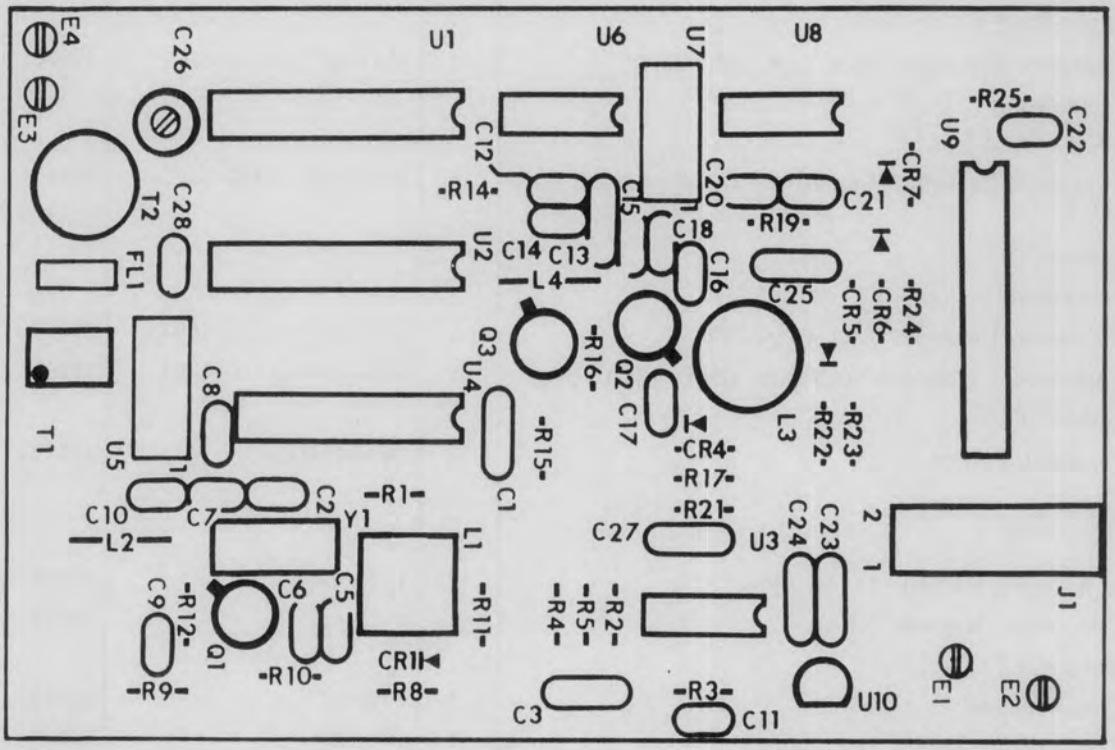


Figure 5-24. Type 371165-1 BFO Assembly (A3A7), Location of Components

5.5.3.8 **Type 371166-1 Reference Mixer** REF DESIG PREFIX **A3A8**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Electrolytic, Tantalum: 15 µF, 20%, 15 V	2	196D156X0015JE3	56289	
C2	Capacitor, Ceramic, Disc: 1000 pF, 5%, 100 V	8	8121-100-COGO-102J	59660	
C3 Thru C6	Same as C2				
C7	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	3	34452-1	14632	
C8	Same as C2				
C9	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 50 V	2	8121-050-651-103M	59660	
C10	Capacitor, Ceramic, Monolithic: 15 pF, 5%, 100 V	3	8111-100-COGO-150J	59660	
C11	Capacitor, Ceramic, Monolithic: 22 pF, 5%, 100 V	1	8111-100-COGO-220J	59660	
C12	Same as C10				
C13	Same as C2				
C14	Same as C7				
C15	Same as C2				
C16	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	2	8131-050-651-105M	59660	
C17	Same as C1				
C18	Same as C10				
C19	Capacitor, Ceramic, Monolithic: 5.6 pF ±0.5 pF, 100 V		8101-100-COHO-569D	59660	
C20	Same as C7				
C21	Same as C9				
C22	Capacitor, Ceramic, Disc: 68 pF, 5%, 50 V	1	8121-050-COGO-680J	59660	
C23	Capacitor, Ceramic, Monolithic: 47 pF, 5%, 100 V	1	8121-100-COGO-470J	59660	
C24	Same as C16				
E1	Terminal, Forked	5	140-1941-02-01	71279	
E2 Thru E5	Same as E1				
L1	Coil, Fixed, Molded: 12 µH, 10%,	2	1025-46	99800	
L2	Coil, Fixed, Molded: 0.1 µH	1	1025-94	99800	
L3	Same as L1				
L4	Coil, Variable	1	6740-01	04213	
L5	Coil, Fixed, Molded: 180 µH, 10%	1	1025-74	99800	
L6	Coil, Fixed: 0.15 µH	2	1025-00	99800	
L7	Same as L6				
Q1	Transistor	1	2N2222A	80131	
R1	Resistor, Fixed, Film: 150 Ω, 5%, 1/8 W	4	CF1/8-150 OHMS/J	09021	
R2	Resistor, Fixed, Film: 36 Ω, 5%, 1/8 W	2	CF1/8-36 OHMS/J	09021	
R3	Same as R1				
R4	Resistor, Fixed, Film: 220 Ω, 5%, 1/8 W	1	CF1/8-220 OHMS/J	09021	
R5	Same as R1				
R6	Same as R2				
R7	Same as R1				

REF DESIG PREFIX A3A8

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R8	Resistor, Fixed, Film: 33 kΩ, 5%, 1/8 W	1	CF1/8-33K/J	09021	
R9	Resistor, Fixed, Film: 3.3 K, 5%, 1/8 W	1	CF1/8-3.3K/J	09021	
R10	Resistor, Fixed, Film: 15 kΩ, 5%, 1/8 W	1	CF1/8-15K/J	09021	
R11	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	2	CF1/8-1.0K/J	09021	
R12	Resistor, Fixed, Film: 510 Ω, 5%, 1/8 W	1	CF1/8-510 OHMS/J	09021	
R13	Resistor, Fixed, Film: 2.7 kΩ, 5%, 1/8 W	1	CF1/8-2.7K/J	09021	
R14	Resistor, Fixed, Film: 12 Ω, 5%, 1/8 W	1	CF1/8-12 OHMS/J	09021	
R15	Same as R11				
R16	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	1	CF1/8-100 OHMS/J	09021	
T1	Transformer	1	T4-1	15542	
U1	Integrated Circuit	1	SP8607B	52648	
U2	Integrated Circuit	1	MWA110	04713	
U3	Mixer, Double Balanced	2	SBL-1	15542	
U4	Integrated Circuit	1	MWA120	04713	
U5	Same as U3				
U6	Integrated Circuit	1	CA3028AF	02735	

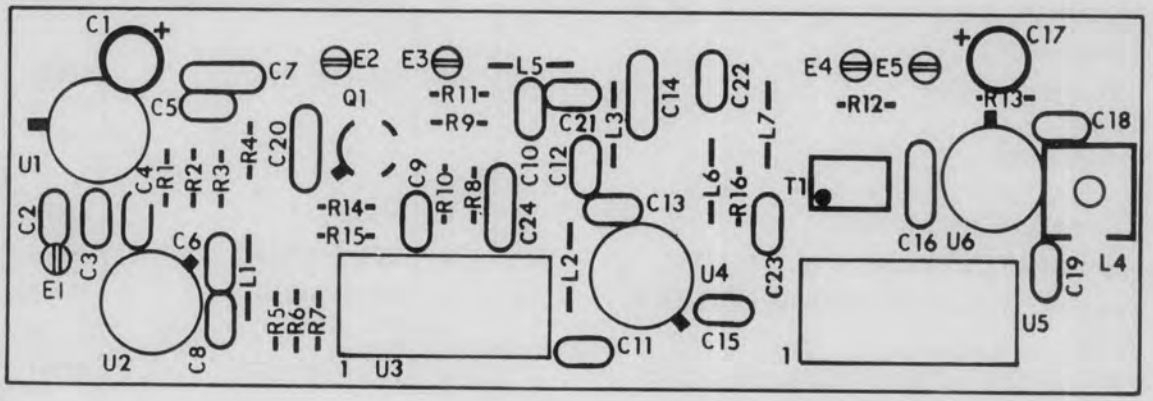


Figure 5-25. Type 371166-1 Reference Mixer (A3A8), Location of Components

5.5.3.9 **Type 371167-1 1st LO Phase Detector/Divider** REF DESIG PREFIX **A3A9**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	1	1N4449	80131	
CR2	Diode	4	1N4446	80131	
CR3 Thru CR5	Same as CR2				
C1	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	5	8131-050-651-105M	59660	
C2	Capacitor, Ceramic, Disc: 1000 pF, 5%, 100 V	7	8121-100-COGO-102J	59660	
C3	Not Used				
C4	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	34475-1	14632	
C5	Same as C1				
C6	Capacitor, Ceramic, Disc: 0.015 µF, 10%, 100 V	1	CK06BX153K	81349	
C7	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	1	34452-1	14632	
C8	Same as C1				
C9	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	1	196D475X0035JE3	56289	
C10	Same as C2				
C11	Capacitor, Ceramic, Monolithic: 15 pF, 5%, 100 V	1	8111-100-COGO-150J	59660	
C12	Same as C2				
C13	Not Used				
C14	Same as C4				
C15 Thru C18	Same as C2				
C19	Same as C1				
C20	Same as C1				
C21	Capacitor, Ceramic, Monolithic: 330 pF, 5%, 100 V	2	8121-100-COGO-331J	59660	
C22	Same as C21				
E1	Terminal, Forked	5	140-1941-02-01	71279	
E2 Thru E5	Same as E1				
J1	Connector, Receptacle	1	65610-114	22526	
R1	Resistor, Fixed, Film: 22 kΩ, 5%, 1/8 W	2	CF1/8-22K/J	09021	
R2	Resistor, Fixed, Film: 5.62 kΩ, 1%, 1/10 W	1	RN55C5621F	81349	
R3	Not Used				
R4	Resistor, Fixed, Film: 270 kΩ, 5%, 1/8 W	1	CF1/8-270K/J	09021	
R5	Not Used				
R6	Not Used				
R7	Same as R1				
R8	Resistor, Fixed, Film: 12 kΩ, 5%, 1/8 W	1	CF1/8-12K/J	09021	
R9	Resistor, Fixed, Film: 1.5 kΩ, 5%, 1/8 W	1	CF1/8-1.5K/J	09021	
R10	Not Used				
R11	Resistor, Fixed, Film: 220 kΩ, 5%, 1/8 W	1	CF1/8-220K/J	09021	
R12	Resistor, Fixed, Film: 39 kΩ, 5%, 1/8 W	1	CF1/8-39K/J	09021	

REF DESIG PREFIX A3A9

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R13	Not Used				
R14	Not Used				
R15	Resistor, Fixed, Film: 15 kΩ, 5%, 1/8 W	1	CF1/8-15K/J	09021	
R16	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	1	CF1/8-10K/J	09021	
R17	Resistor, Fixed, Film: 18 Ω, 5%, 1/8 W	1	CF1/8-18 OHMS/J	09021	
R18	Resistor, Fixed, Film: 34.0 kΩ, 1%, 1/10 W	1	RN55C3402F	81349	
R19	Resistor, Fixed, Film: 13.7 kΩ, 1%, 1/10 W	1	RN55C1372F	81349	
R20	Resistor, Fixed, Film: 12 kΩ, 5%, 1/8 W	1	CF1/8-12K/J	09021	
U1	Integrated Circuit	1	NJ8821DP	52648	
U2	Integrated Circuit	1	SP8716	52648	
U3	Integrated Circuit	1	CA3140AE	02735	
U4	Not Used				
U5	Integrated Circuit	1	SP86078	52648	
U6	Integrated Circuit	1	723DC	07263	
U7	Not Used				
U8	Integrated Circuit	1	MC78L05ACP	04713	
Y1	Crystal	1	XS2703A	99999	

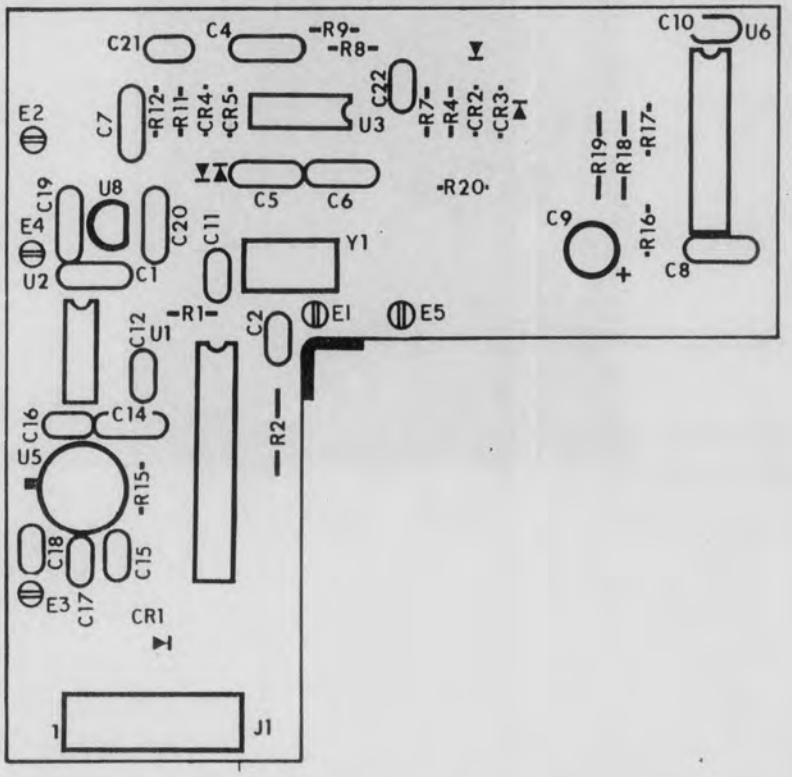


Figure 5-26. Type 371167-1 1st LO Phase Detector/Divider (A3A9), Location of Components

5.5.3.10 **Type 470958-1 1st LO Assembly** REF DESIGN PREFIX **A3A10**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	1st LO/VCO	1	371168-1	14632	
C1	Capacitor, Ceramic, Feedthru: 0.05 µF, GMV, 300 V	3	54-785-005-503P	33095	
C2	Same as C1				
C3	Capacitor, Ceramic, Feedthru: 100 pF, ±20%, 200 V	3	54-713-001-101M	33095	
C4	Same as C3				
C5	Same as C1				
C6	Same as C3				
C7	Capacitor, Mica, Dipped: 100 pF, 2%, 100 V	1	CM06FD102G03	81349	

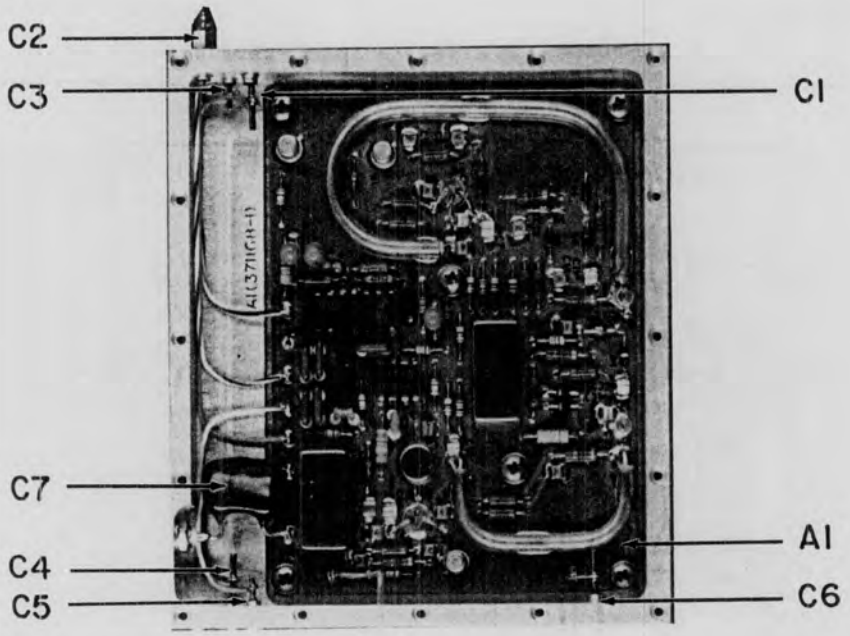


Figure 5-27. Type 470958-1 1st LO Assembly (A3A10), Location of Components

5.5.3.10.1 **Type 371168-1 1st LO VCO** REF DESIG PREFIX **A3A10A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode, Variable, Capacitance	5	KV3901	52673	
CR2	Not Used				
CR3	Same as CR1				
CR4	Not Used				
CR5	Not Used				
CR6	Same as CR1				
CR7	Diode	2	KS3542	52673	
CR8	Same as CR1				
CR9	Same as CR1				
CR10	Diode	1	U11-3102	52673	
CR11	Same as CR7				
C1	Capacitor, Ceramic, Disc: 1 µF, 20%, 50 V	5	8131-050-651-105M	59660	
C2 Thru C4	Same as C1				
C5	Capacitor, Ceramic, Chip: 510 pF, 10%, 100 V	2	ATC100B511KP100X	29990	
C6	Capacitor, Ceramic, Chip: 6.8 pF ±0.25 pF, 500 V	2	ATC100B6R8CP500X	29990	
C7	Capacitor, Ceramic, Chip: 4.7 pF ±0.1 pF, 500 V	1	ATC100B4R7BP500X	29990	
C8	Capacitor, Ceramic, Chip: 470 pF, 20%, 200 V	7	ATC100B471MP200X	29990	
C9	Same as C8				
C10	Capacitor, Variable, Air: 0.6-4.5 pF, 500 V	2	GT-24T	73899	
C11*	Capacitor, Ceramic, Chip: 12 pF, 2%, 500 V	1	ATC100B120GP500X	29990	
C12*	Capacitor, Ceramic, Chip: 13 pF, 5%, 500 V	1	ATC100B130JC500X	29990	
C13	Same as C8				
C14	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	3	196D475X0035JE3	56289	
C15	Capacitor, Ceramic, Disc: 100 pF, 10%, 200 V	1	CK05BX101K	81349	
C16	Same as C14				
C17	Capacitor, Ceramic, Chip: 1.0 pF ±0.25 pF, 500 V	1	ATC100B1R0CP500X	29990	
C18	Capacitor, Ceramic, Chip: 0.7 pF ±10%, 500 V	1	ATC100B0R7BP500 X	29990	
C19	Capacitor, Ceramic, Chip: 330 pF, 10%, 200 V	2	ATC700B331KP200X	29990	
C20	Same as C8				
C21	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	34475-1	14632	
C22	Same as C19				
C23	Same as C1				
C24	Same as C21				
C25	Same as C5				
C26	Capacitor, Ceramic, Chip: 3.6 pF ±.1 pF, 500 V	1	ATC100B3R6BP500X	29990	
C27	Capacitor, Ceramic, Chip: 3.3 pF, 10%, 500 V	1	ATC100B3R3KP500X	29990	
C28	Same as C8				
C29	Same as C8				
C30	Same as C10				
	*Nominal Value, Final Value Factory Selected				

REF DESIG PREFIX **A3A10A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C31*	Capacitor, Ceramic, Chip: 2.7 pF ±0.1 pF, 500 V	1	ATC100B2R7BP500X	29990	
C32*	Same as C6				
C33	Same as C8				
C34	Same as C14				
DL1	Delay Line	1	271415-1	14632	
DL2	Delay Line	1	271416-1	14632	
E1	Terminal, Forked	9	140-1941-02-01	71279	
E2 Thru E9	Same as E1				
L1	Coil, Fixed: 0.12 µH, 10%	7	1025-96	99800	
L2 Thru L4	Same as L1				
L5	Coil, Fixed: 0.39 µH, 10%	1	1025-10	99800	
L6	Same as L1				
L7	Same as L1				
L8	Coil, Fixed, Molded: 0.56 µH, 10%	1	1025-14	9980	
L9	Same as L1				
L10	Coil, Fixed, Molded: 100 µH, 10%	1	1025-68	99800	
Q1	Transistor	3	2N2222A	80131	
Q2	Same as Q1				
Q3	Same as Q1				
Q4	Transistor	2	U310	17856	
Q5	Same as Q4				
R1	Resistor, Fixed, Film: 15 kΩ, 1%, 1/10 W	2	RN55C1502F	81349	
R2	Resistor, Fixed, Film: 5.62 kΩ, 1%, 1/10 W	2	RN55C5621F	81349	
R3	Resistor, Fixed, Film: 562 Ω, 1%, 1/10 W	2	RN55C5620F	81349	
R4	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	6	CF1/8-10K/J	09021	
R5	Resistor, Fixed, Film: 10 kΩ, 1%, 1/10 W	5	RN55C1002F	81349	
R6	Same as R5				
R7	Resistor, Fixed, Film: 470 Ω, 5%, 1/8 W	2	CF1/8-470 OHMS/J	09021	
R8	Same as R5				
R9	Resistor, Fixed, Film: 12 Ω, 5%, 1/8 W	1	CF1/8-12 OHMS/J	09021	
R10	Resistor, Fixed, Film: 27.4 kΩ, 1%, 1/10 W	1	RN55C2742F	81349	
R11	Resistor, Fixed, Film: 14.3 kΩ, 1%, 1/10 W	1	RN55C1432F	81349	
R12	Resistor, Fixed, Film: 300 Ω, 5%, 1/8 W	4	CF1/8-300 OHMS/J	09021	
R13	Resistor, Fixed, Film: 18 Ω, 5%, 1/8 W	2	CF1/8-18 OHMS/J	09021	
R14	Same as R12				
R15	Same as R12				
R16	Same as R13				
R17	Same as R12				
	*Nominal Value, Final Value Factory Selected				

REF DESIG PREFIX **A3A10A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R18	Resistor, Fixed, Film: 100 Ω, 5%, 1/8 W	1	CF1/8-100 OHMS/J	09021	
R19 Thru R22	Same as R4				
R23	Same as R1				
R24	Same as R2				
R25	Same as R3				
R26	Same as R4				
R27	Same as R5				
R28	Same as R5				
R29	Same as R7				
R30	Resistor, Fixed, Film: 39 kΩ, 5%, 1/8 W	1	CF1/8-39K/J	09021	
U1	Integrated Circuit	1	NE5534AN	18324	
U2	Voltage Regulator	1	MC79L15ACP	04713	
U3	Integrated Circuit	1	MC78L05ACP	04713	
U4	Integrated Circuit	1	723DC	07263	
U5	Divider/Power	1	PSC-2-1W	15542	
U6	Amplifier	1	MWA-220	04713	
U7	Coupler	1	PDC-10-22	15542	

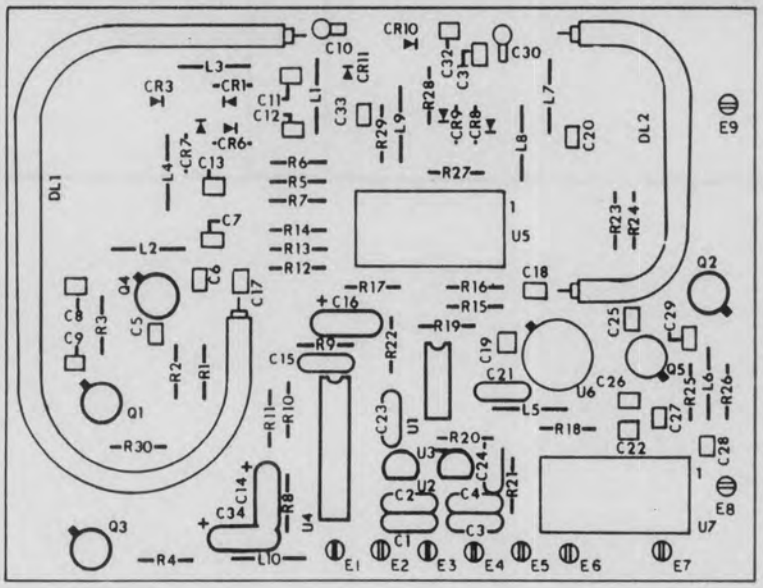
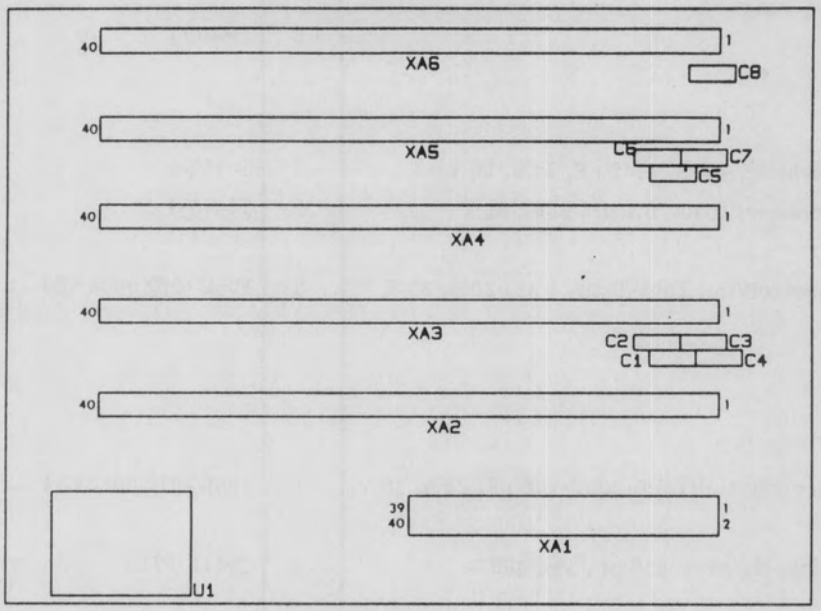


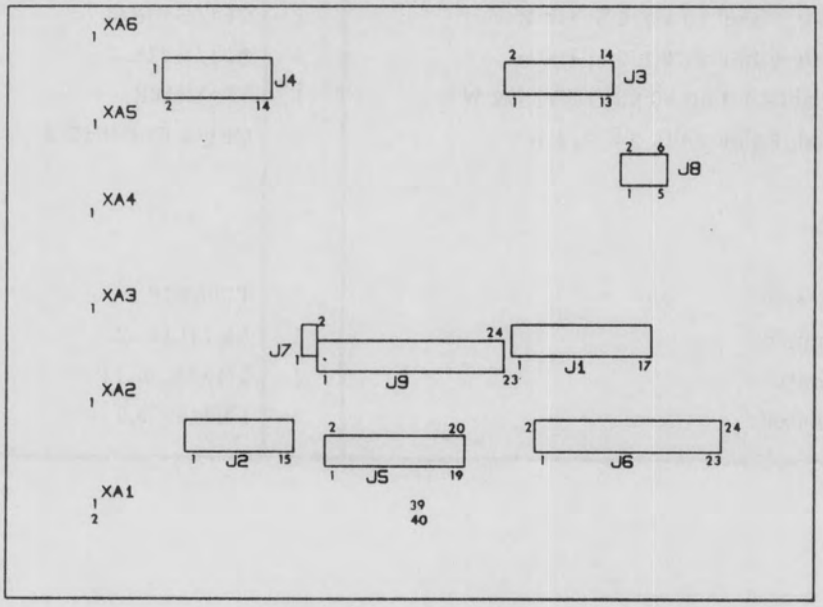
Figure 5-28. Type 371168-1 1st LO VCO (A310A1), Location of Components

5.5.4 **TYPE 794431-2 CONTROLLER MOTHERBOARD** REF DESIG PREFIX **A4**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
A1	Voltage Regulator	1	794432-1	14632	
A2	Remote I/O Option		794437-1	14632	
A3	Extended CPU Option		794444-X	14632	
A4	Customer Option				
A5	Receiver, EF Interface		794421-1	14632	
A6	Front Panel Interface		794433-1	14632	
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	8	34475-1	14632	
C2 Thru C8	Same as C1				
J1	Connector, Receptacle	2	65610-218	22526	
J2	Connector, Receptacle	3	65610-214	22526	
J3	Same as J2				
J4	Same as J2				
J5	Same as J1				
J6	Connector, Receptacle	1	65610-224	22526	
J7	Terminal Strip	1	65500-202	22526	
J8	Connector, Receptacle	1	65610-106	22526	
J9	Terminal Strip	1	65610-124	22526	
P1	Connector, Plug	2	65474-001	22526	
P2	Same as P1				
U1	DC-AC Inverter	1	DAS5V7	62483	
XA1	Connector, Receptacle	1	65610-240	22526	
XA2	Terminal Strip	10	65500-220	22526	
XA3 Thru XA6	Same as XA2				



Top View



Bottom View

Figure 5-29. Type 794431-2 Controller Motherboard (A4), Location of Components

5.5.4.1 **Type 794432-1 Voltage Regulator** REF DESIG PREFIX **A4A1**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	6	1N4003	80131	
CR2 Thru CR6	Same as CR1				
C1	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	3	34452-1	14632	
C2	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	2	34475-1	14632	
C3	Same as C1				
C4	Capacitor, Electrolytic, Tantalum: 1 µF, 20%, 35 V	5	196D105X0035HE3	56289	
C5	Same as C1				
C6	Same as C2				
C7	Same as C4				
C8	Not Used				
C9	Capacitor, Electrolytic, Tantalum: 100 µF, 20%, 20 V	1	196D107X0020TE4	56289	
C10	Same as C4				
C11	Capacitor, Mica, Dipped: 820 pF, 5%, 300 V	1	DM15-821J	72136	
C12	Same as C4				
C13	Same as C4				
C14	Capacitor, Ceramic, Disc: 2.2 µF, 10%, 50 V	1	8141-050-651-225M	59660	
P1	Connector, PC Board	1	65000-026	22526	
Q1	Transistor	1	2N2222A	80131	
R1	Resistor, Fixed, Film: 10 kΩ, 5%, 1/4 W	1	CF1/4-10K/J	09021	
R2	Resistor, Fixed, Film: 22 kΩ, 5%, 1/4 W	3	CF1/4-22K/J	09021	
R3	Resistor, Variable, Film: 50 kΩ, 10 %, 1/2 W	1	62PAR50K	73138	
R4	Resistor, Fixed, Film: 68 Ω, 5%, 1/4 W	2	CF1/4-68 OHMS/J	09021	
R5	Same as R4				
R6	Same as R2				
R7	Same as R2				
U1	Integrated Circuit	1	TL062CP	01295	
U2	Voltage Regulator	1	LM78L12CZ	27014	
U3	Voltage Regulator	1	LM320L Z-12	27014	
U4	Voltage Regulator	1	LM340T-5.0	27014	

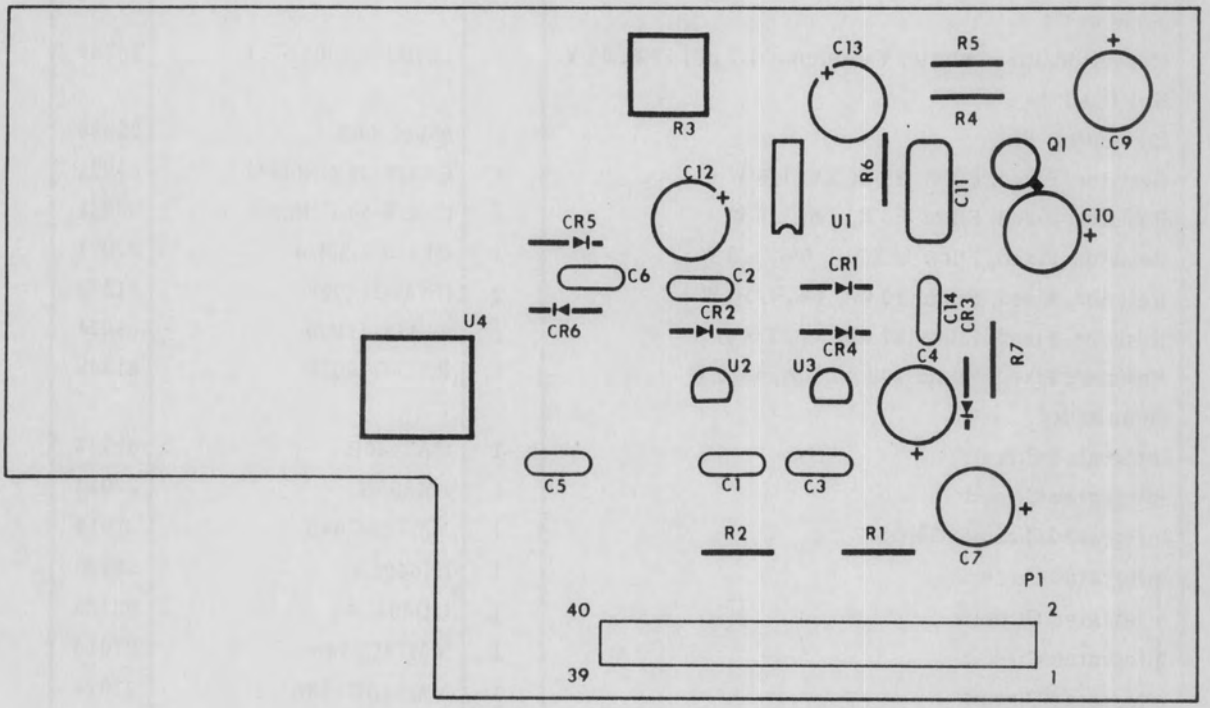


Figure 5-30. Type 794432-1 Voltage Regulator (A4A1), Location of Components

5.5.4.2 **Type 794437-1 Remote I/O Interface (Option)** REF DESIG PREFIX **A4A2**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	1	1N4449	80131	
CR2	Diode	1	1N746A	80131	
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	4	34475-1	14632	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 50 V	1	34452-1	14632	
C4	Same as C1				
C5	Same as C1				
C6	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	1	196D475X0035JE3	56289	
JW1	Not Used				
P1	Connector, Plug	1	65001-066	22526	
R1	Resistor, Fixed, Film: 39 Ω, 5%, 1/8 W	1	CF1/8-39 OHMS/J	09021	
R2	Resistor, Fixed, Film: 56 Ω, 5%, 1/8 W	1	CF1/8-56 OHMS/J	09021	
R3	Resistor, Fixed, Film: 2.2 MΩ, 5%, 1/8 W	1	CF1/8-2.2M/J	09021	
R4	Resistor, Fixed, Film: 10 kΩ, 1%, 1/10 W	2	RN55C1002F	81349	
R5	Resistor, Fixed, Film: 47 kΩ, 5%, 1/8 W	1	CF1/8-47K/J	09021	
R6	Resistor, Fixed, Film: 100 kΩ, 1%, 1/10 W	1	RN55C1003F	81349	
R7	Same as R4				
U1	Integrated Circuit	1	CA3140E	02735	
U2	Integrated Circuit	1	LM393N	27014	
U3	Integrated Circuit, CMOS	1	MM74HC04N	27014	
U4	Integrated Circuit	1	IM6402A	32293	
U5	Integrated Circuit	1	CD4011AE	02735	
U6	Integrated Circuit	1	MM74C374N	27014	
U7	Integrated Circuit	1	MM74HC138N	27014	
U8	Integrated Circuit	1	MM74HC373N	27014	
U9	Integrated Circuit	1	MM74HC08N	27014	
U10	Integrated Circuit	1	MM74C244N	27014	
U11	Integrated Circuit	1	MM74HC32N	27014	

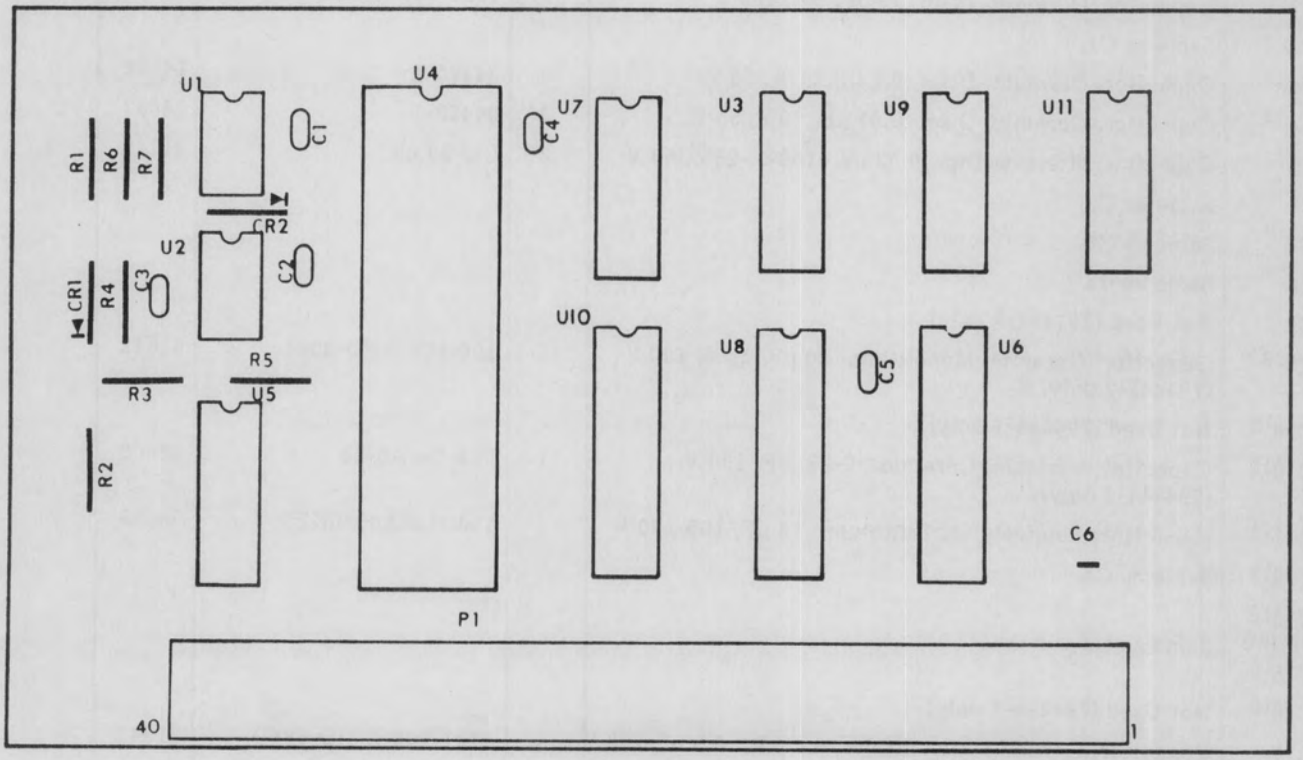


Figure 5-31. Type 794437-1 Remote I/O Interface (Option), (A4A2), Location of Components

5.5.4.3 **Type 794444-1 & 2 Extended CPU** REF DESIG PREFIX **A4A3**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
BT1	Battery, Lithium	1	2736	00681	
CR1	Diode	2	1N4449	80131	
CR2	Same as CR1				
CR3	Diode	2	5082-2800	28480	
CR4	Same as CR3				
C1	Capacitor, Ceramic, Disc: 39 pF, 5%, 100 V	2	8121-100-COGO-390J	59660	
C2	Same as C1				
C3	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	5	34475-1	14632	
C4	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 50 V	2	34453-1	14632	
C5	Capacitor, Micro-Q-Dip: 0.03 µF +100% -25%, 50 V	3	UQ-28.03	31745	
C6	Same as C5				
C7	Same as C5				
C8	Same as C3				
C9	Not Used (794444-1 only)				
C9	Capacitor, Ceramic, Monolithic: 20 pF, ±5%, 100 V (794444-2 only)	1	100-100-NPO-200J	51642	
C10	Not Used (794444-1 only)				
C10	Capacitor, Variable, Ceramic: 5-25 pF, 100 V (794444-2 only)	1	518-000A5-25	59660	
C11	Capacitor, Electrolytic, Tantalum: 18 µF, 10%, 20 V	1	196D186X9020KE3	56289	
C12	Same as C4				
C13 Thru C15	Same as C3				
C16	Not Used (794444-2 only)				
C17	Capacitor, Ceramic, Monolithic: 6.8 pF, ±0.5 pf, 100 V (794444-2 only)	1	8101-100COHO-689D	51642	
JW1	Terminal Strip	2	65500-103	22526	
JW2A	Same as JW1				
JW2B	Terminal	1	65500-101	22526	
P1	Connector, Plug	1	65001-066	22526	
P2	Connector, Plug (794444-1 only)	2	65474-001	22526	
P3	Same as P2 (794444-1 only)				
Q1	Transistor	2	2N3251	80131	
Q2	Transistor	1	2N2222A	80131	
Q3	Same as Q1				
RN1	Resistor, Network	1	L08-1C104	73138	
R1	Resistor, Fixed, Film: 1 MΩ, 5%, 1/4 W	2	CF1/4-1M/J	09021	
R2	Same as R1				
R3	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	7	CF1/8-10K/J	09021	
R4	Same as R3				
R5	Resistor, Fixed, Film: 2.2 MΩ, 5%, 1/4 W	1	CF1/4-2.2M/J	09021	
R6	Same as R3				

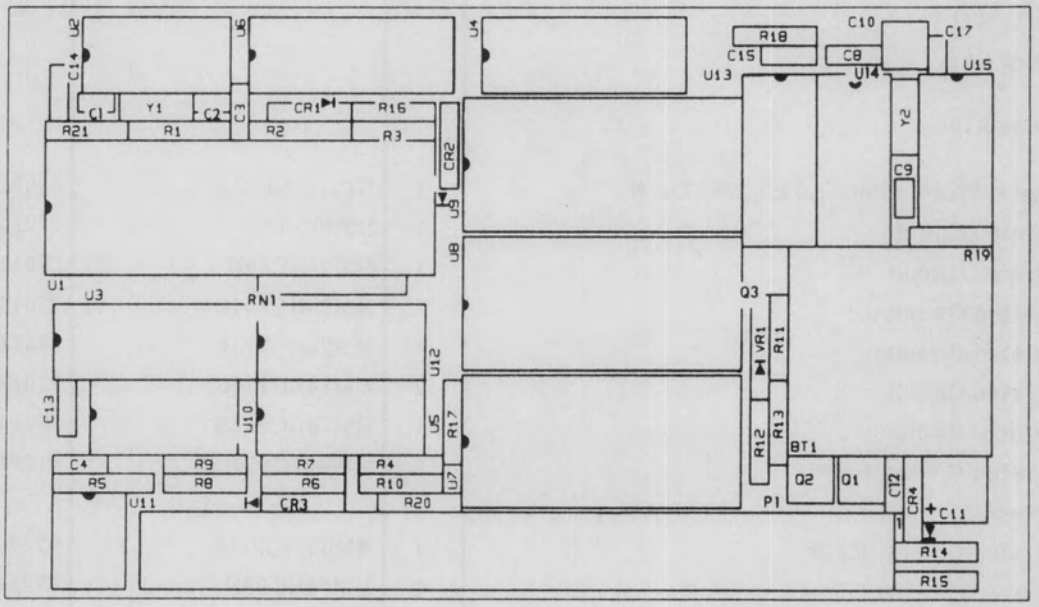


Figure 5-32. Type 794444-1 Extended CPU (A4A3), Location of Components

REF DESIG PREFIX A4A3

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R7	Same as R3				
R8	Resistor, Fixed, Film: 3.3 kΩ, 5%, 1/8 W	1	CF1/8-3.3K/J	09021	
R9	Same as R3				
R10	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	6	CF1/8-100K/J	09021	
R11	Resistor, Fixed, Film: 2.2 kΩ, 5%, 1/8 W	3	CF1/8-2.2K/J	09021	
R12	Same as R11				
R13	Same as R3				
R14	Same as R11				
R15	Same as R3				
R16 Thru R20	Same as R10				
R21	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	1	CF1/8-1.0K/J	09021	
U1	Integrated Circuit	1	NSC800N	27014	
U2	Integrated Circuit	1	MM74HC00N	27014	
U3	Integrated Circuit	1	MM74HC244N	27014	
U4	Integrated Circuit	1	MM74HC373N	27014	
U5	Integrated Circuit	2	MM74HC138N	27014	
U6	Integrated Circuit	1	MM74HC245N	27014	
U7	Integrated Circuit PROM	2	MBM27C256-25	61271	
U8	Same as U7				
U9	Integrated Circuit, RAM	1	HM6264LP-15	62786	
U10	Integrated Circuit	1	MM74HC08N	27014	
U11	Integrated Circuit	1	LM393N	27014	
U12	Same as U5				
U13	Integrated Circuit	1	MM74C174N	27014	
U14	Not Used (794444-1 only)				
U14	Integrated Circuit (794444-2 only)	1	MM58274N	27014	
U15	Integrated Circuit	1	MM74HC32N	27014	
VR1	Diode, Zener: 3.3 V	1	1N746A	80131	
XU1	Socket, Integrated Circuit	1	ICN-406-S5-T	06776	
XU7	Socket, Integrated Circuit	3	ICN-286-S5-T	06776	
XU8	Same as XU7				
XU9	Same as XU7				
Y1	Crystal Quartz (794444-1 only)	1	CSA4.91MG	72982	
Y1	Crystal Quartz (794444-2 only)	1	CX-.03	51791	

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5.5.4.4 **Type 794421-1 Receiver/EF Interface** REF DESIG PREFIX **A4A5**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	4	344575-1	14632	
C2	Not Used				
C3 Thru C5	Same as C1				
P1	Connector, Plug	1	65001-066	22526	
Q1	Transistor	2	2N2222A	80131	
Q2	Same as Q1				
R1	Resistor, Fixed, Film: 100 kΩ, 5%, 1/8 W	2	CF1/8-100K/J	09021	
R2	Same as R1				
R3	Resistor, Fixed, Film: 100 Ω, 5%, 1/4 W	1	CF1/4-100 OHMS/J	09021	
R4	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	2	CF1/8-1.0K/J	09021	
R5	Resistor, Fixed, Film: 10 kΩ, 5%, 1/8 W	1	CF1/8-10K/J	09021	
R6	Same as R4				
U1	Integrated Circuit	2	MM74C74N	27014	
U2	Integrated Circuit	1	MM74C161N	27014	
U3	Integrated Circuit	2	CD4094BE	02735	
U4	Same as U3				
U5	Same as U1				
U6	Integrated Circuit	1	MM74C374N	27014	
U7	Integrated Circuit	1	MM74C373N	27014	
U8	Integrated Circuit	1	MM74HC138N	27014	
U9	Integrated Circuit	1	MM74HC08N	27014	
U10	Integrated Circuit	1	MM74C240N	27014	
U11	Integrated Circuit	2	MM74C165N	27014	
U12	Same as U11				
U13	Integrated Circuit	1	DG212CJ	17856	
U14	Integrated Circuit	1	TL062CP	01295	
U15	Integrated Circuit	1	MC14503BCP	04713	

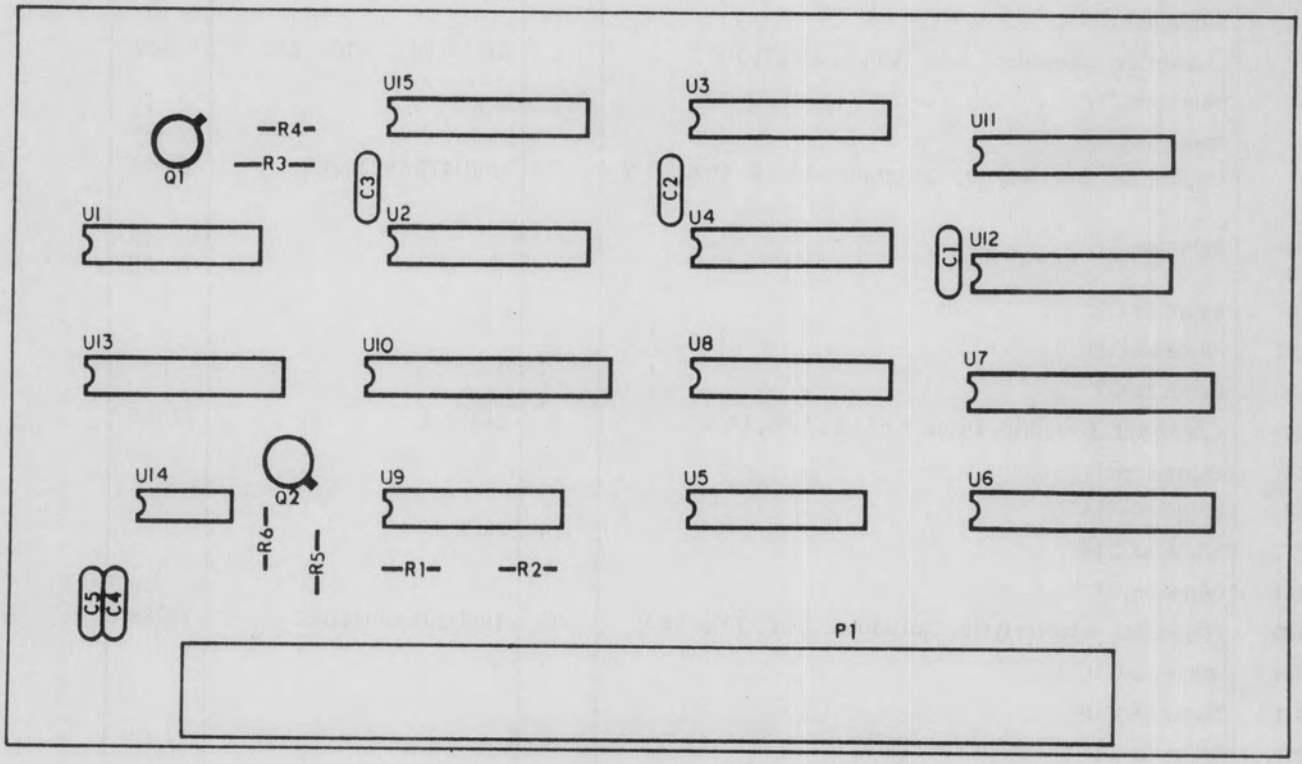


Figure 5-33. Type 794421-1 Receiver/EF Interface (A4A5), Location of Components

5.5.4.5 **Type 794433-1 Front Panel Interface** REF DESIG PREFIX **A4A6**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
CR1	Diode	2	5082-2800	28480	
CR2	Same as CR1				
C1	Capacitor, Ceramic, Disc: 0.1 µF, 20%, 50 V	11	34475-1	14632	
C2	Same as C1				
C3	Same as C1				
C4	Capacitor, Ceramic, Disc: 100 pF, 5%, 100 V	1	8121-100-COGO-101J	59660	
C5	Same as C1				
C6	Same as C1				
C7	Capacitor, Electrolytic, Tantalum: 4.7 µF, 20%, 35 V	5	196D475X0035JE3	56289	
C8 Thru C10	Same as C7				
C11	Same as C1				
C12	Same as C1				
C13	Same as C7				
C14	Capacitor, Ceramic, Disc: 0.01 µF, 20%, 50 V	3	34453-1	14632	
C15	Same as C1				
C16	Same as C14				
C17	Same as C14				
C18	Same as C1				
C19	Capacitor, Electrolytic, Tantalum: 1 µF, 20%, 35 V	2	196D105X0035HE3	56289	
C20	Same as C1				
C21	Same as C19				
C22	Same as C1				
P1	Connector, Plug	1	65001-066	22525	
R1	Resistor, Fixed, Film: 12 kΩ, 5%, 1/8 W	6	CF1/8-12K/J	09021	
R2	Same as R1				
R3	Resistor, Fixed, Film: 9.09 kΩ, 1%, 1/10 W	1	RN55C9091F	81349	
R4	Resistor, Fixed, Film: 28.7 kΩ, 1%, 1/10 W	1	RN55C2872F	81349	
R5	Resistor, Fixed, Film: 15 kΩ, 1%, 1/10 W	2	RN55C1502F	81349	
R6	Resistor, Fixed, Film: 1.0 kΩ, 5%, 1/8 W	2	CF1/8-1.0K/J	09021	
R7	Resistor, Fixed, Film: 7.5 kΩ, 5%, 1/8 W	2	CF1/8-7.5K/J	09021	
R8	Same as R5				
R9	Resistor, Fixed, Film: 120 kΩ, 5%, 1/4 W	1	CF1/4-120K/J	09021	
R10	Same as R1				
R11	Same as R1				
R12	Resistor, Fixed, Film: 40.2 kΩ, 1%, 1/10 W	1	RN55C4022F	81349	
R13	Resistor, Fixed, Film: 8.66 kΩ, 1%, 1/10 W	1	RN55C8661F	81349	
R14	Resistor, Variable, Film: 5 kΩ, 10%, 1/2 W	1	62PAR5K	73138	
R15	Same as R6				
R16	Same as R1				

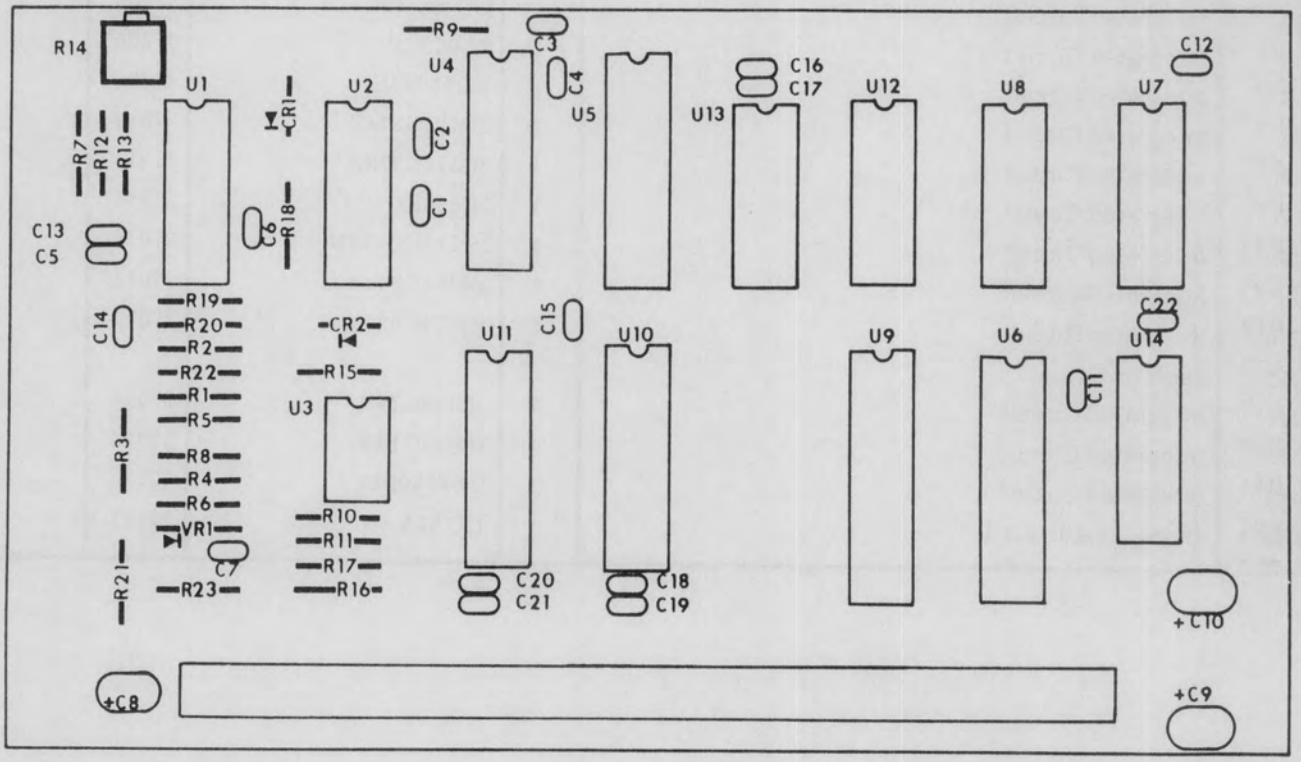


Figure 5-34. Type 794433-1 Front Panel Interface (A4A6), Location of Components

REF DESIG PREFIX **A4A6**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
R17	Same as R1				
R18	Resistor, Fixed, Film: 27 kΩ, 5%, 1/8 W	5	CF1/8-27K/J	09021	
R19 Thru R22	Same as R18				
R23	Same as R7				
U1	Integrated Circuit	1	TL064CN	01295	
U2	Integrated Circuit	1	CD4051BE	02735	
U3	Integrated Circuit	1	TL062CP	01295	
U4	Integrated Circuit	1	AD7574JN	24355	
U5	Integrated Circuit	1	MM74C374N	27014	
U6	Integrated Circuit	1	MM74C373N	27014	
U7	Integrated Circuit	1	MM74HC00N	27014	
U8	Integrated Circuit	1	MM74HC138N	27014	
U9	Integrated Circuit	1	MM74C244N	27014	
U10	Integrated Circuit	2	MM74C922N	27014	
U11	Same as U10				
U12	Integrated Circuit	1	MM74C74N	27014	
U13	Integrated Circuit	1	MM74C14N	27014	
U14	Integrated Circuit	1	CD4020BE	02735	
VR1	Diode, Zener: 5.1 V	1	1N751A	80131	

5.5.5 **TYPE 794457-1 CONTROLLER/RECEIVER INTERFACE** REF DESIG PREFIX **A5**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
C1	Capacitor, Ceramic, Disc: 0.47 µF, 20%, 100 V	3	8131M100-651-474M	59660	
C2	Same as C1				
C3	Same as C1				
J1	Connector, Plug	1	65820-003	22526	
J2	Connector, Plug	1	65820-011	22526	
J3	Connector, Receptacle	1	65610-114	22526	
J4	Terminal Strip	1	65610-118	22526	
J5	Terminal Strip	1	65610-126	22526	

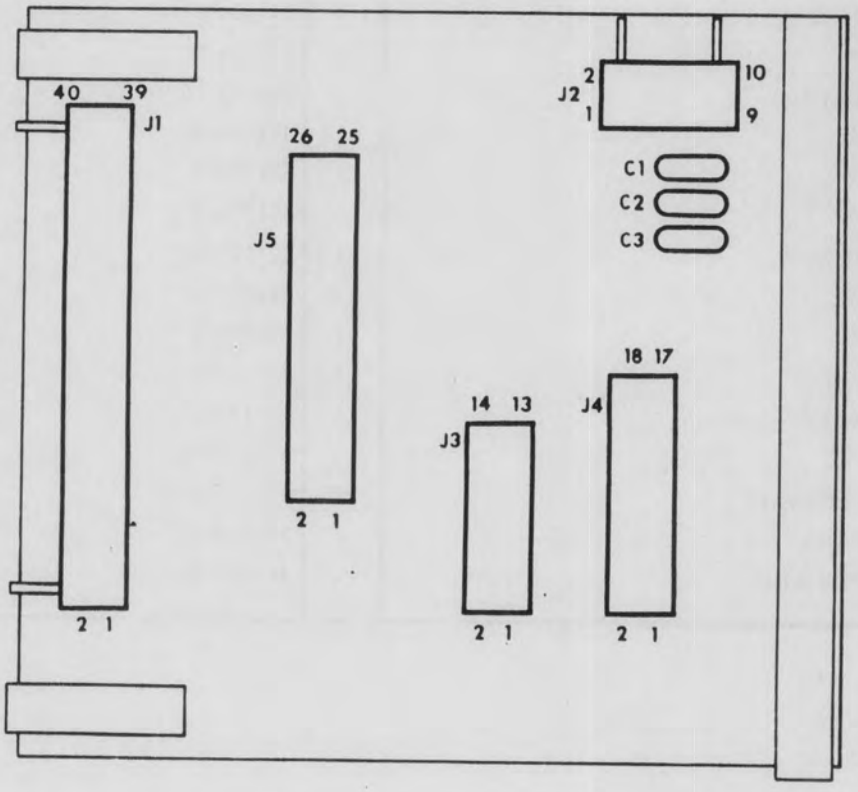


Figure 5-35. Type 794457-1 Controller/Receiver Interface (A5), Location of Components

5.5.6 **TYPE 371037-2 KEYBOARD ASSEMBLY** REF DESIG PREFIX **A8**

REF DESIG	DESCRIPTION	QTY PER ASSY	MANUFACTURER'S PART NO.	MFR. CODE	RECM VENDOR
J1	Connector, Receptacle	1	65610-214	22526	
S1	Switch, PB "DET Mode"	1	371126-17	14632	
S2	Switch, PB "IF BW"	1	371126-18	14632	
S3	Switch, PB "GAIN Mode"	1	371126-19	14632	
S4	Switch, PB "STO"	1	371126-32	14632	
S5	Switch, PB "RCL"	1	371126-33	14632	
S6	Switch, PB "EXEC"	1	371126-34	14632	
S7	Switch, PB "R/LCL, COS"	1	371126-23	14632	
S8	Switch, PB "DWL, AFC"	1	371126-24	14632	
S9	Switch, PB "SET, SCAN"	1	371126-25	14632	
S10	Switch, PB "SYS CLR"	1	371126-26	14632	
S11	Switch, PB "INCL, L/OUT"	1	371126-27	14632	
S12	Switch, PB "ARROW UP/DN"	1	371126-15	14632	
S13	Switch, PB "7"	1	371126-7	14632	
S14	Switch, PB "8"	1	371126-8	14632	
S15	Switch, PB "9"	1	371126-9	14632	
S16	Switch, PB "BFO +/-"	1	371126-16	14632	
S17	Switch, PB "4"	1	371126-4	14632	
S18	Switch, PB "5"	1	371126-5	14632	
S19	Switch, PB "6"	1	371126-6	14632	
S20	Switch, PB "KHZ"	1	371126-13	14632	
S21	Switch, PB "1"	1	371126-1	14632	
S22	Switch, PB "2"	1	371126-2	14632	
S23	Switch, PB "3"	1	371126-3	14632	
S24	Switch, PB "MHZ"	1	371126-4	14632	
S25	Switch, PB "0"	1	371126-10	14632	
S26	Switch, PB "DECIMAL"	1	371126-11	14632	
S27	Switch, PB "CLR"	1	371126-12	14632	
S28	Switch, PB "OPR AID"	1	371126-28	14632	

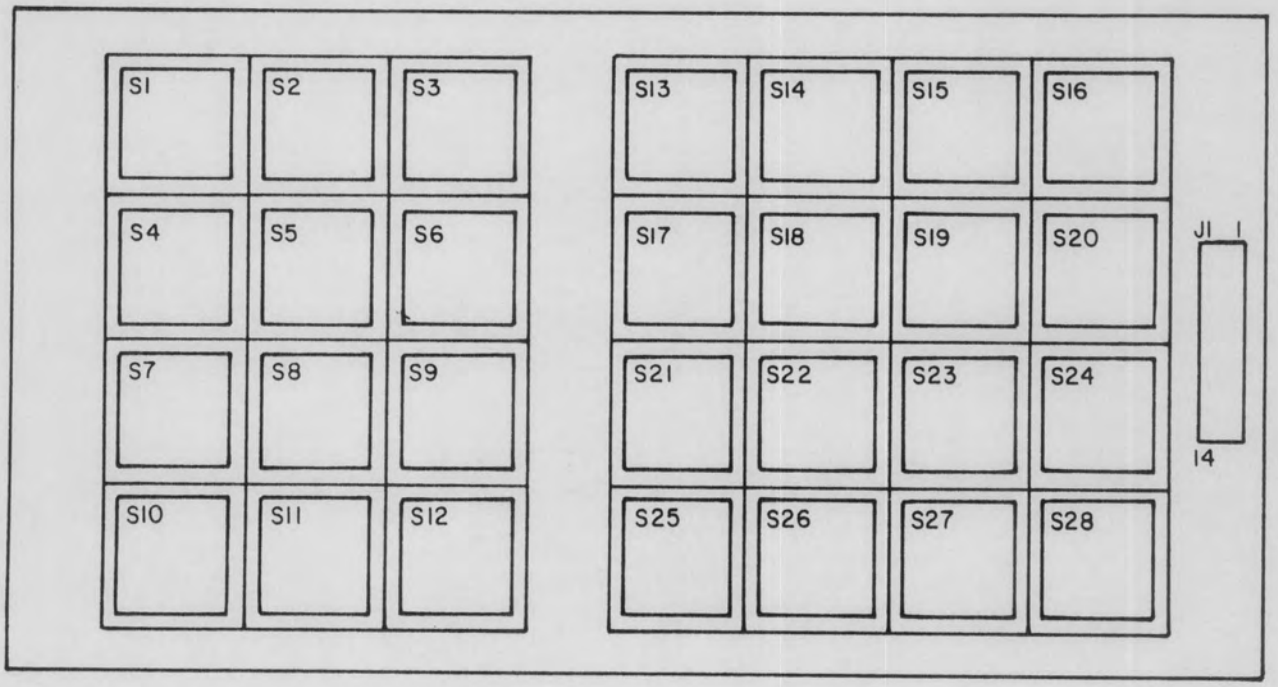


Figure 5-36. Type 371037-2 Keyboard Assembly (A8), Location of Components

SECTION VI

SCHEMATIC DIAGRAMS

NOTES
1. UNLESS OTHERWISE SPECIFIED,
   a) FEED-THRU CAPACITORS ARE 100pF.
   b) INDUCTANCE IS 1000 uH.
2. FOR DIFFERENT DASH NUMBERS, SEE TABULATION.

TABULATION

TYPE NUMBER	A4 PART NUMBER	A6 PART NUMBER
794445-1	371137-1	371285-1
794445-2	371137-2	371285-2

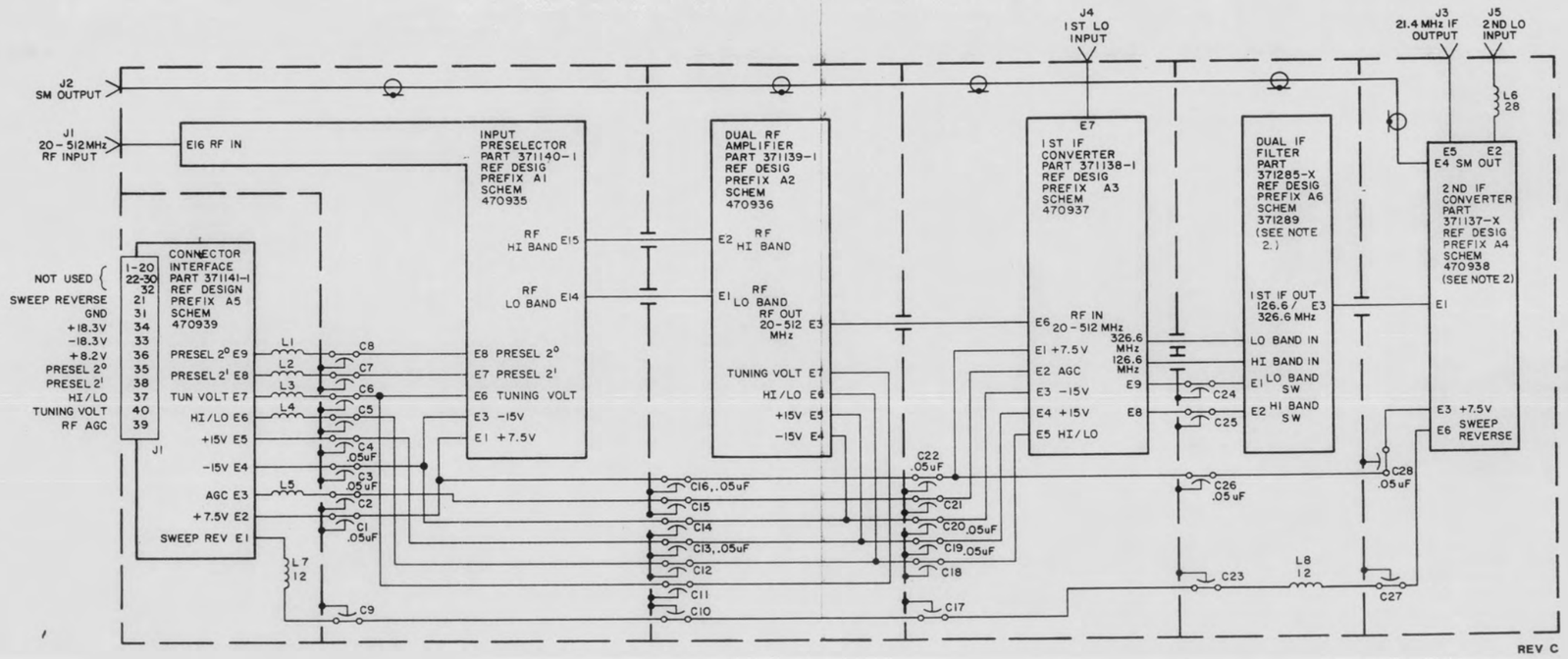


Figure 6-1. Type 794445-2 RF Tuner 20-512 MHz (A1), Schematic Diagram 470932

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN µF.
   c) INDUCTANCE IS IN µH.
2. FOR DASH NO. DIFFERENCES SEE TABULATION.
3. NOMINAL VALUE, FINAL VALUE FACTORY SELECT, INSTALL WHEN THE VARACTORS WILL NOT TRACK PROPERLY.

TABULATION		
DASH NUMBER	CR39	CR40
371140 – 1	NOT USED	NOT USED
371140 – 2	UM9401	5082-2800

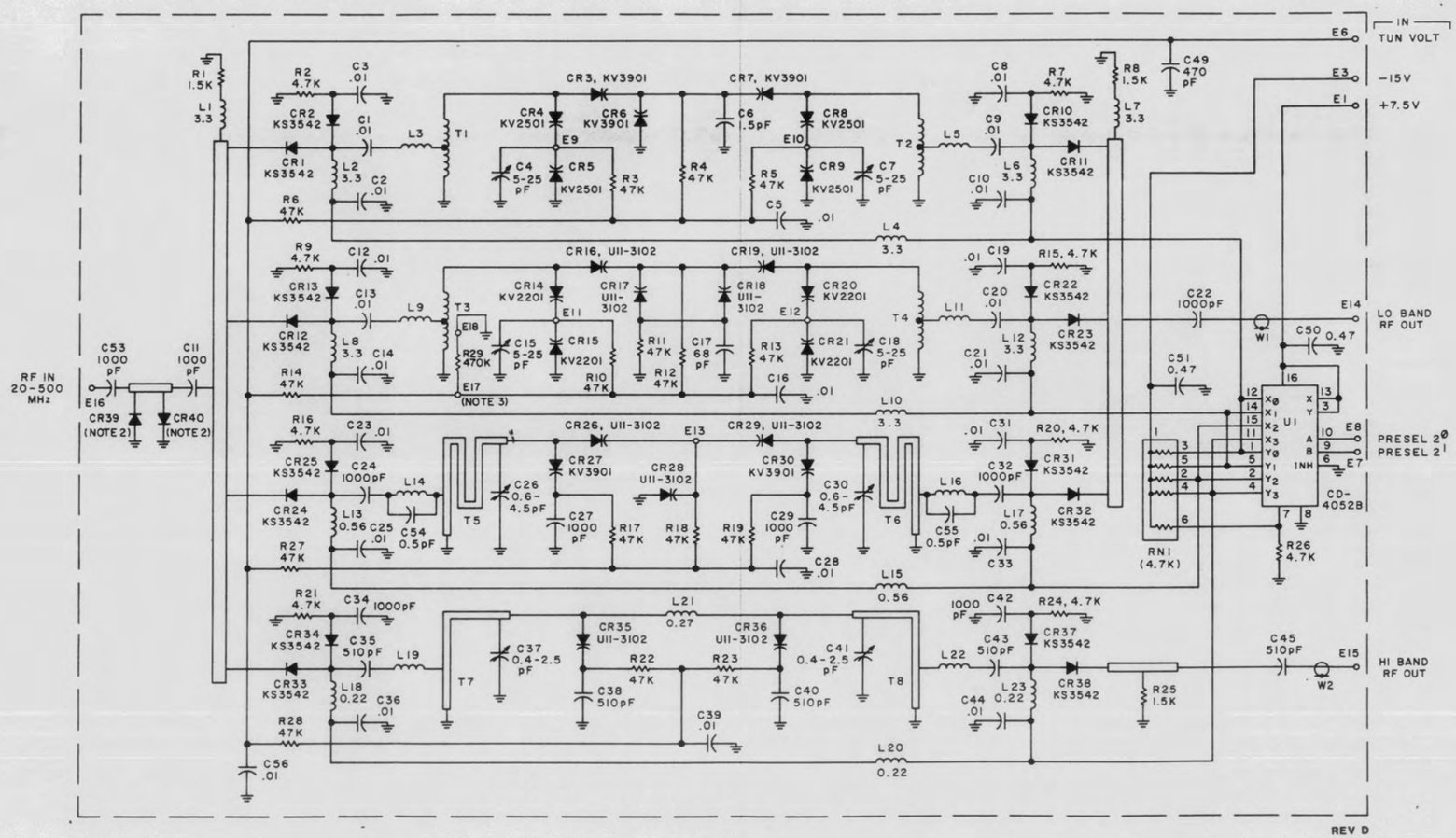


Figure 6-2. Type 371140-1 Preselector (A1A1), Schematic Diagram 470935

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ± 5%, 1/8 W.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.
2. U3/U4 SWITCH STATES SHOWN FOR LOGIC "0" INPUT.

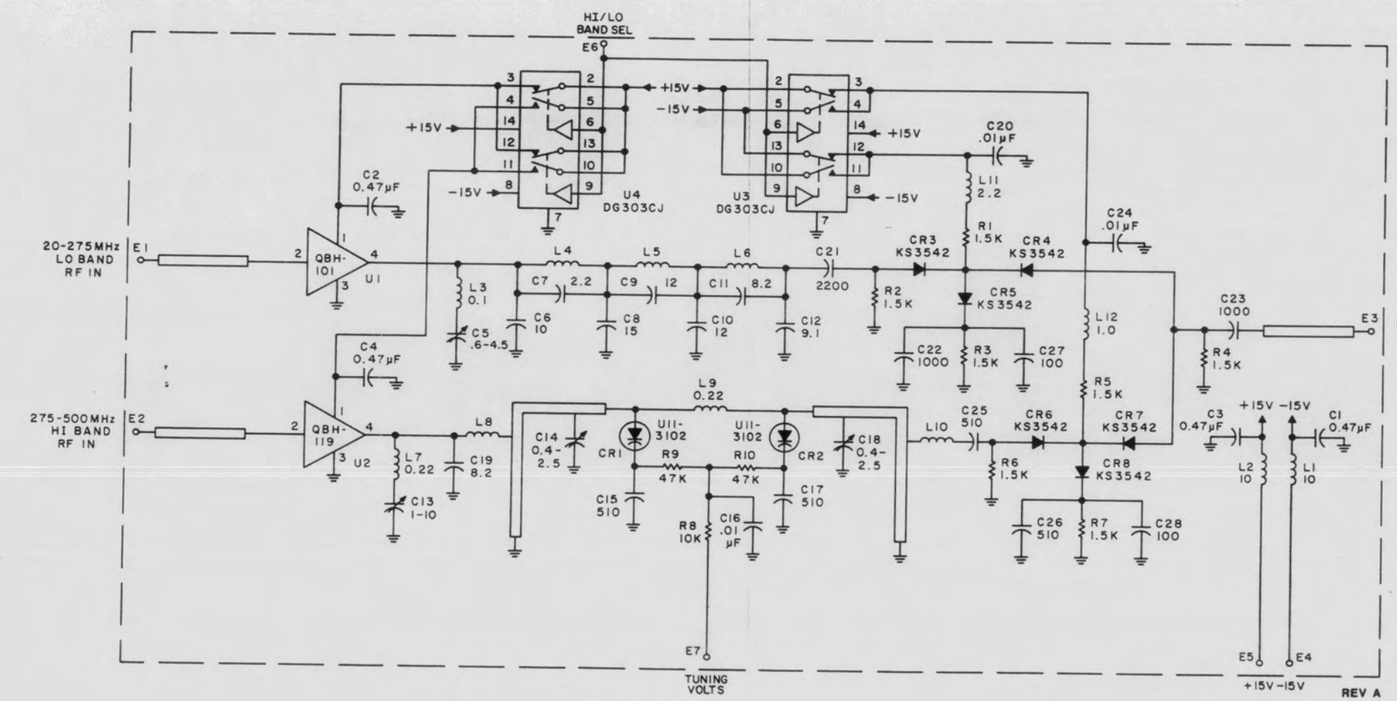


Figure 6-3. Type 371139-1 Dual RF Amplifier (A1A2), Schematic Diagram 470936

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.

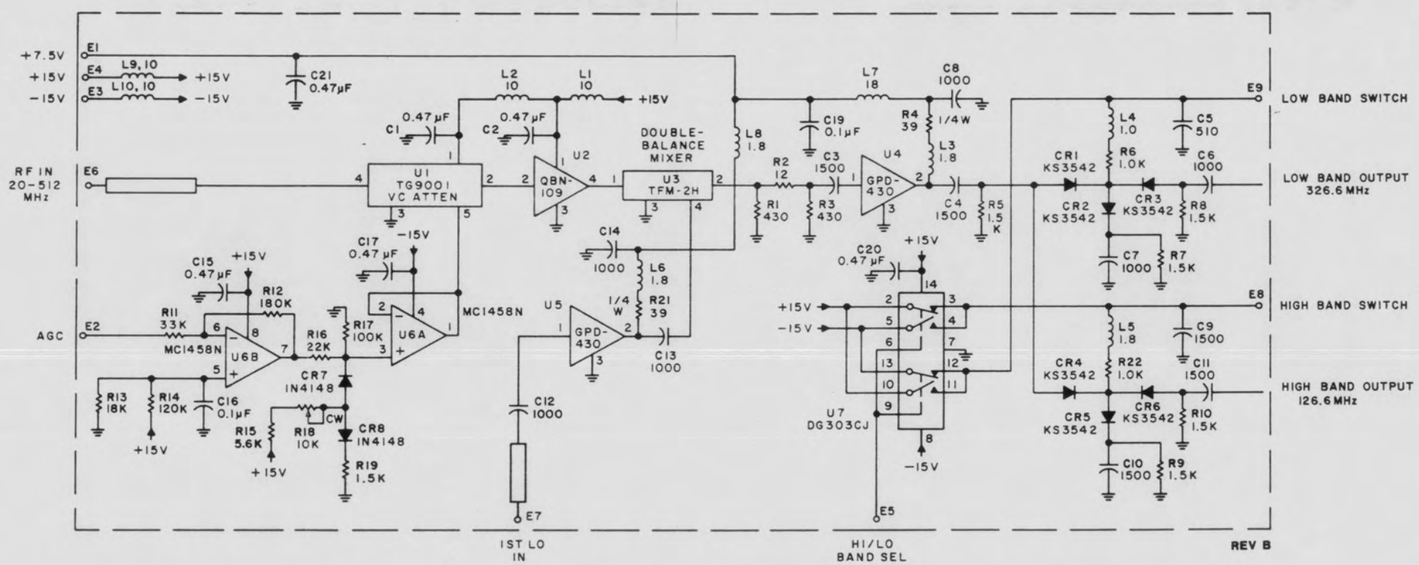


Figure 6-4. Type 371138-1 1st Converter (A1A3), Schematic Diagram 470937

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 5%, 1/8W.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.
2. DIFFERENCES IN TYPE NUMBERS IS SHOWN IN TABULATION.

TABULATION

TYPE NUMBER	C12	C13	C14	U4
371137-1	100	220	100	DIR CPLR 10dB TDC 10-1
371137-2	75	240	75	DIR CPLR 10dB TDC 10-1
371137-3	75	240	75	POWER SPLITTER TSC 2-1

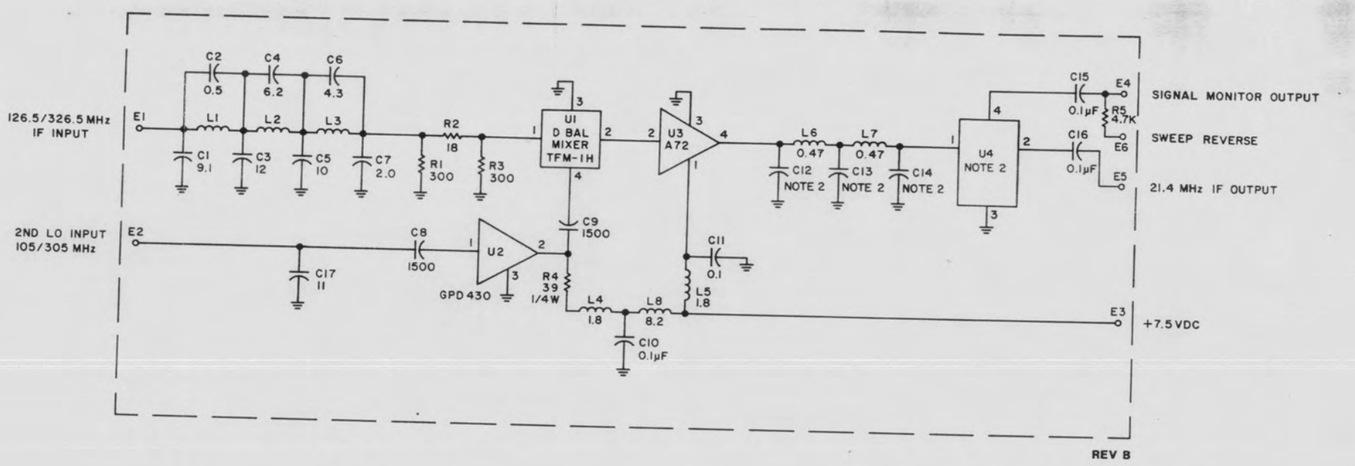


Figure 6-5. Type 371137-2 2nd Converter (A1A4), Schematic Diagram 470938

NOTES:
UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
b) CAPACITANCE IS IN µF.

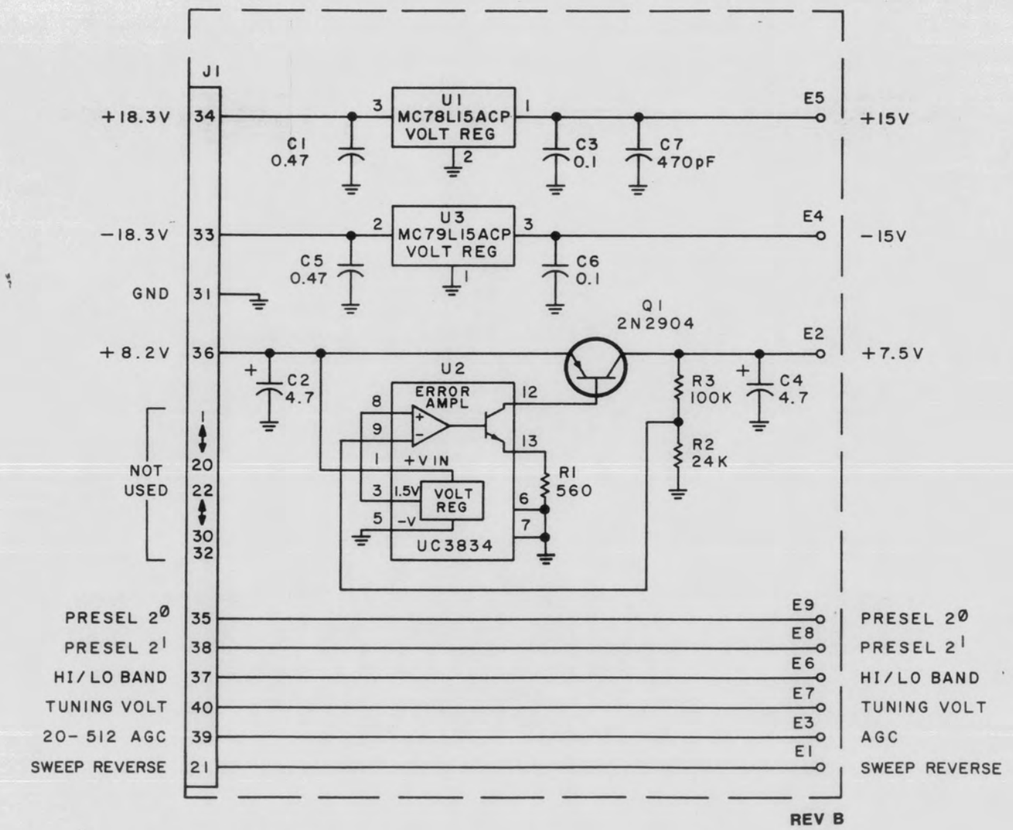


Figure 6-6. Type 371141-1 Connector Interface (A1A5), Schematic Diagram 470939

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.
2. FOR DIFFERENT DASH NUMBERS, SEE TABULATION.

PART NUMBER	FL2 (BW)
371285-1	6.32MHz BW
371285-2	13.5 MHz BW

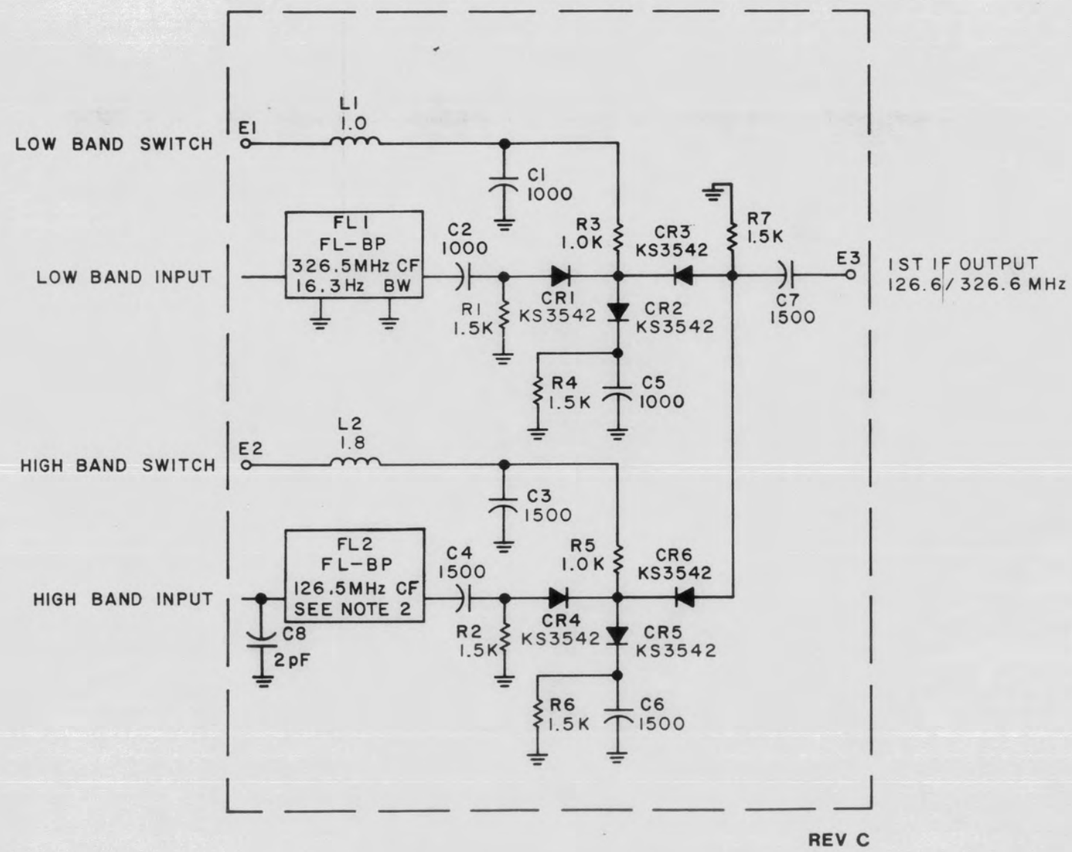


Figure 6-7. Type 371285-2 Dual IF Converter (A1A6), Schematic Diagram 371289

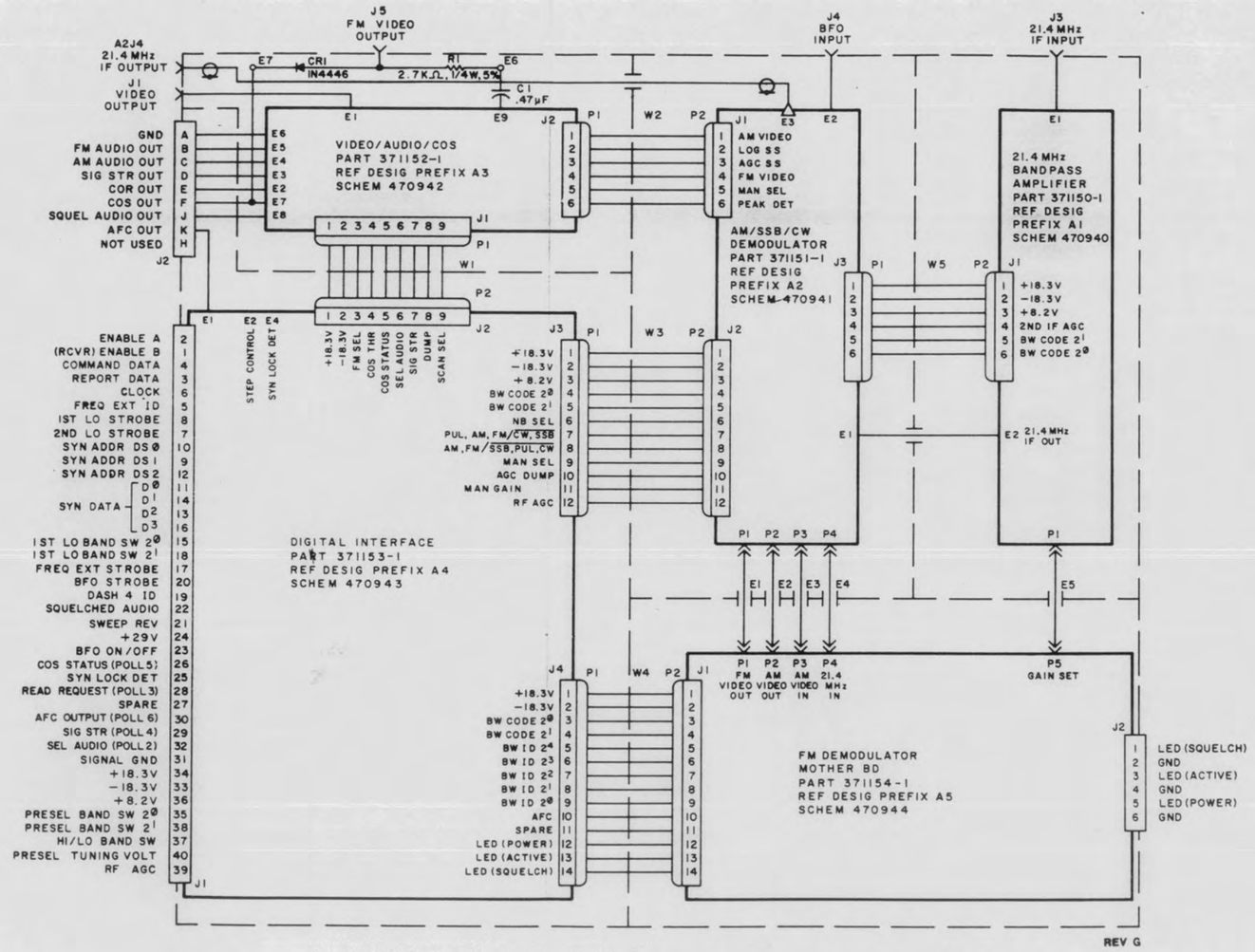


Figure 6-8. Type 794446-1 21.4 MHz IF Demodulator (A2), Schematic Diagram 470933

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/8W
   b. CAPACITANCE IS IN pF
   c. INDUCTANCE IS IN µH

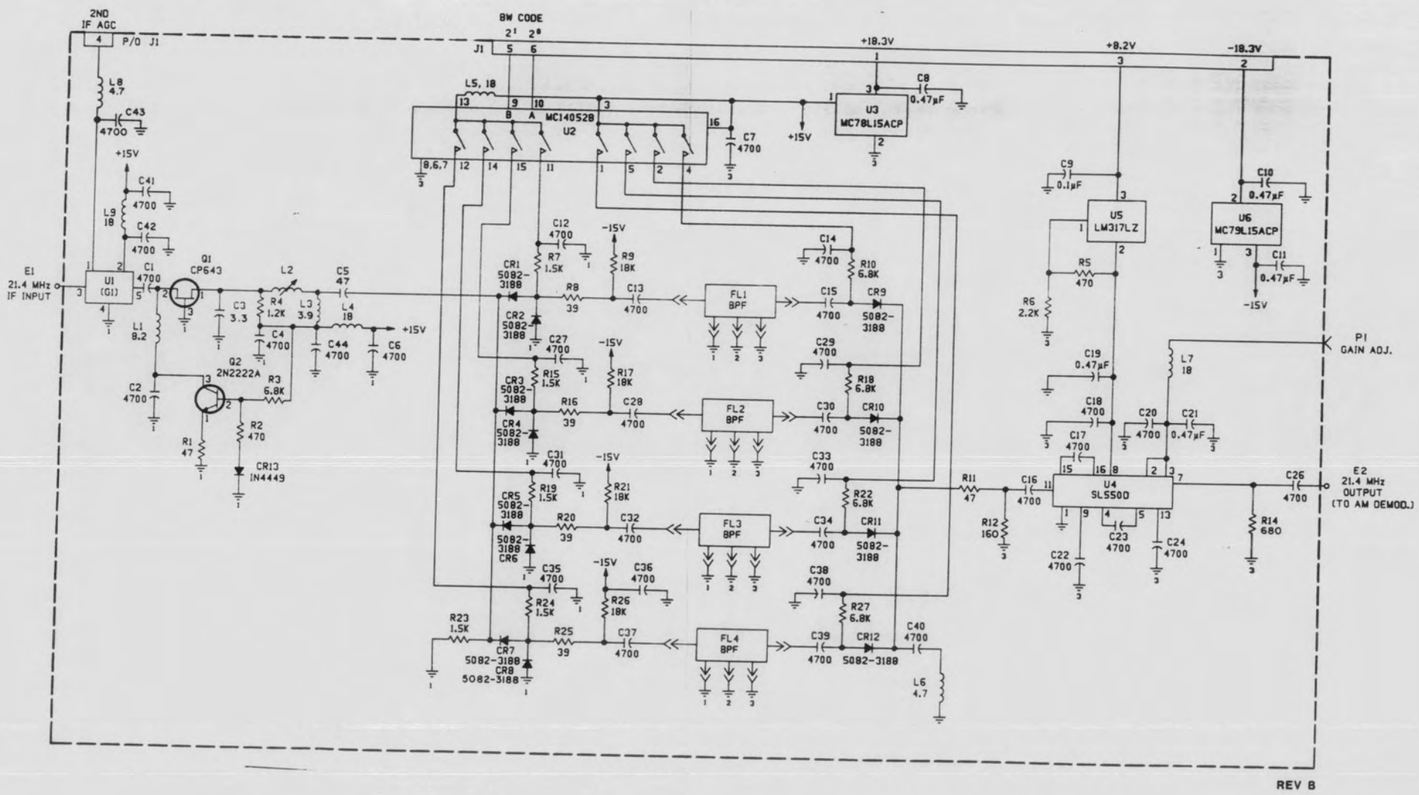


Figure 6-9. Type 371150-1 21.4 MHz Bandpass Amplifier (A2A1), Schematic Diagram 470940

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.

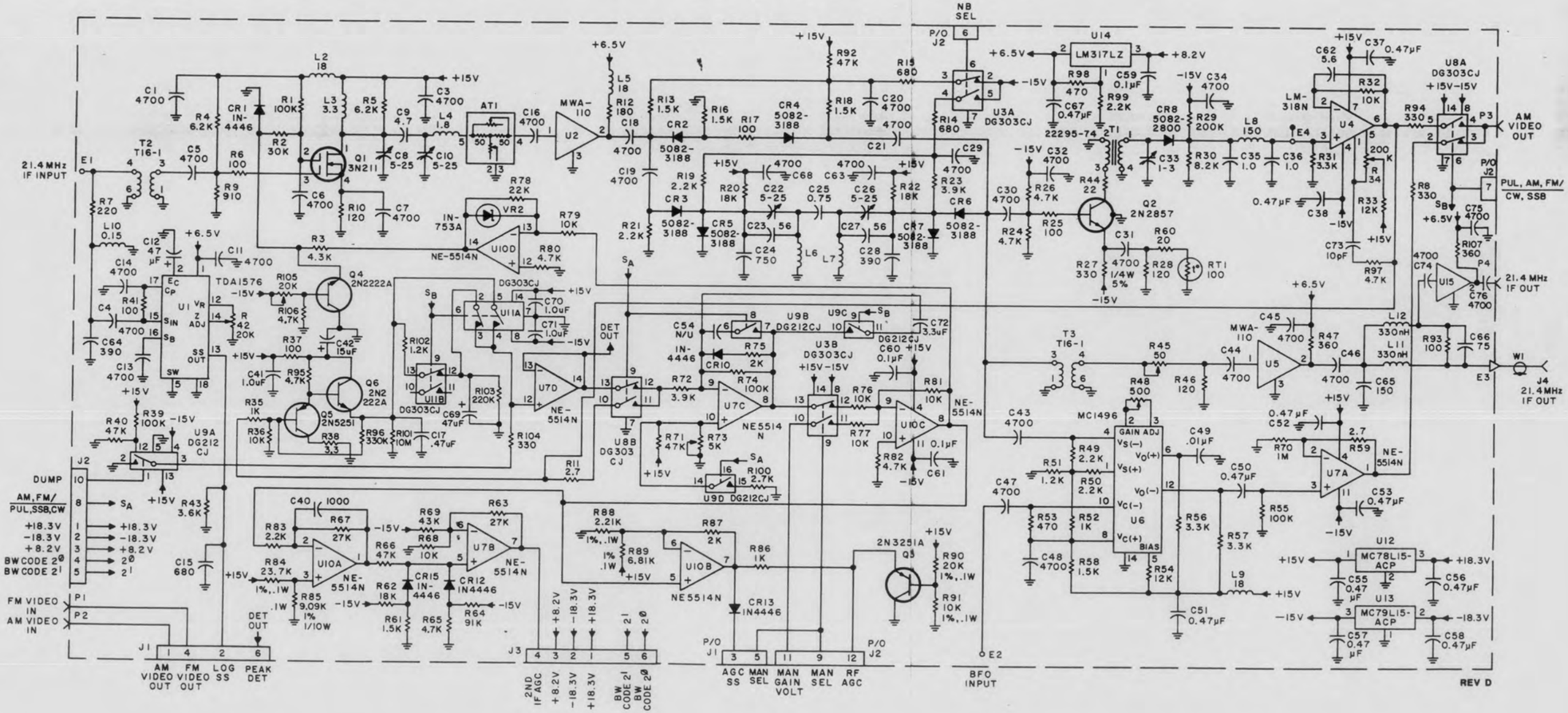


Figure 6-10. Type 371151-1 AM/SSB/CW Demodulator (A2A2), Schematic Diagram 470941

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/8W
   b. CAPACITANCE IS IN µF
   c. INDUCTANCE IS IN µH
2. SEE TABULATION FOR DIFFERENCE IN DASH NUMBERS.

LAST REF. DES. USED	NOT USED
C32	R37
R45	
CR5	C26
VR1	
L4	
U10	
J2	
E9	
Q1	

TABULATION				
DASH NO.	C3	C11	L1	L4
-1	390pF	390pF	120	120
-2	0.1	0.1	68mH	68mH

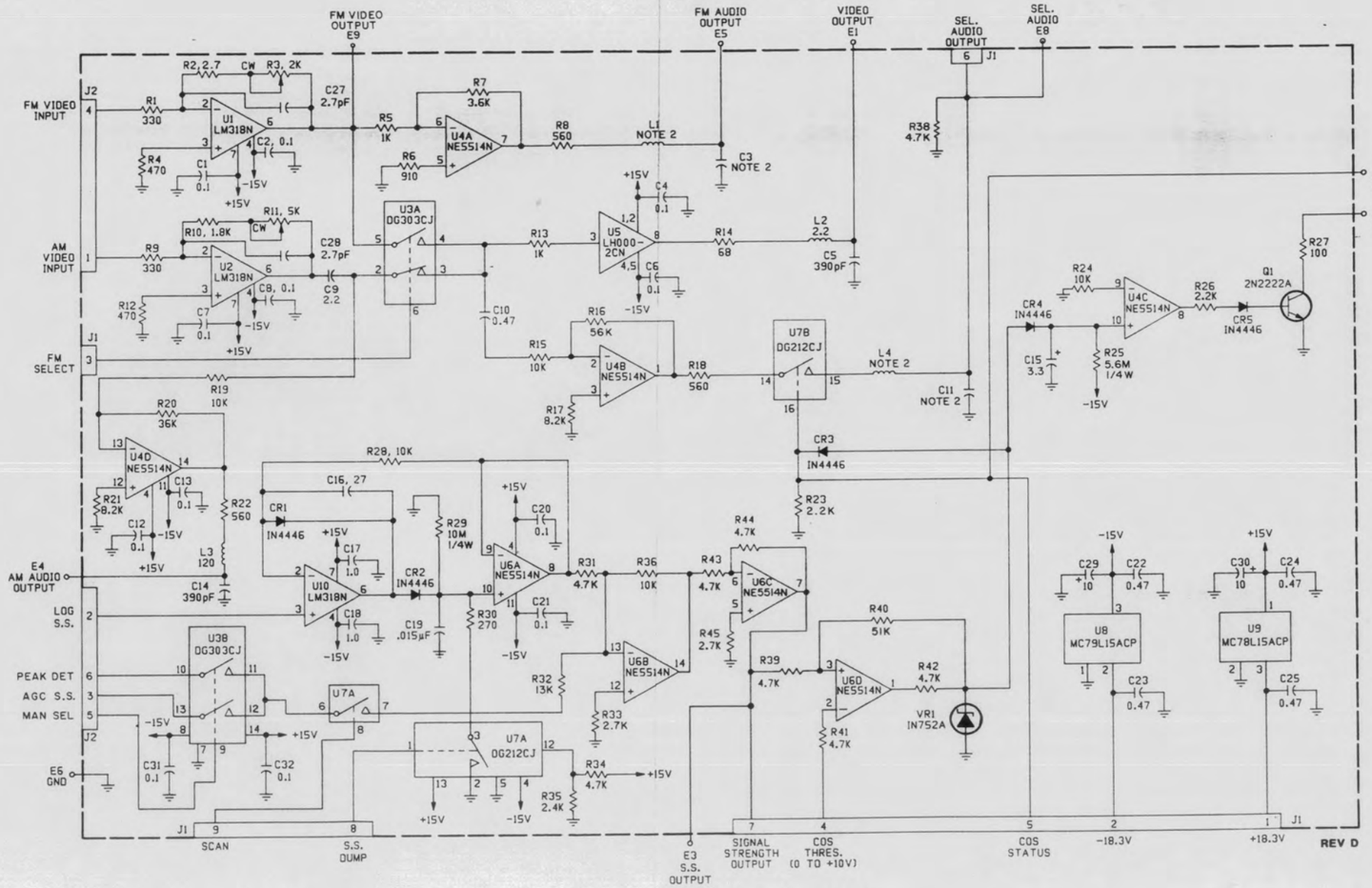


Figure 6-11. Type 371152-1 Video/Audio/COS (A2A3), Schematic Diagram 470942

NOTES:
UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
b) CAPACITANCE IS IN µF.

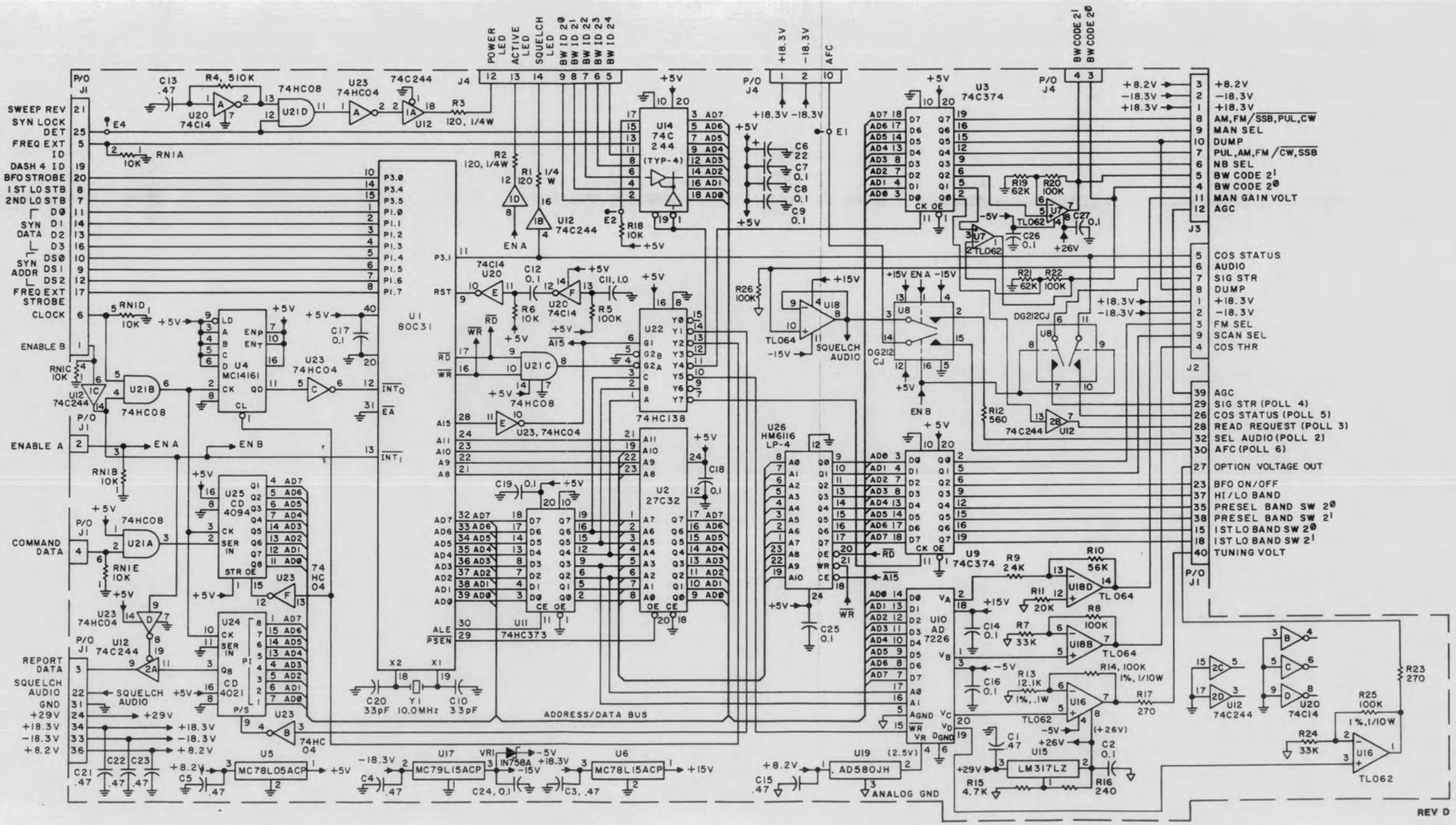


Figure 6-12. Type 371153-1 Digital Interface (A2A4), Schematic Diagram 470943

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%. 1/4 W.
   b. CAPACITANCE IS IN μF.
   c. INDUCTANCE IS IN μH.
2. TYPE IS SELECTED FROM TABLE I AS A FUNCTION OF DESIRED IF BANDWIDTH.

TABLE I

IF BW	TYPE NO.
10kHz	371155-1
20kHz	371155-2
50kHz	371156-1
100kHz	371156-2
200kHz	371156-3
500kHz	371157-1
1 MHz	371158-1
2 MHz	371158-2
4 MHz	371158-3
150kHz	371156-4
2.85kHz/SSB	371155-3

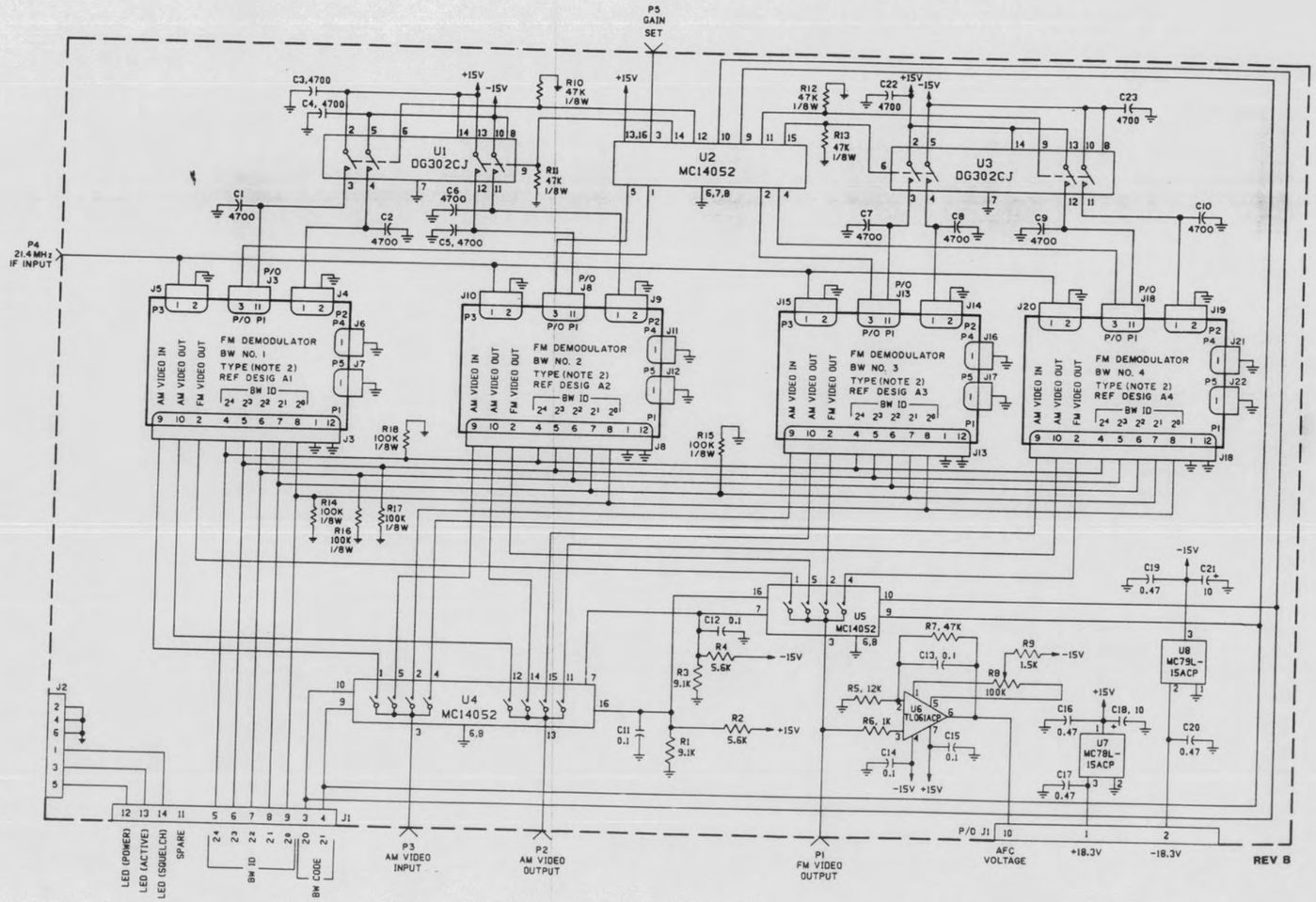


Figure 6-13. Type 371154-1 FM Demodulator Motherboard (A2A5), Schematic Diagram 470944

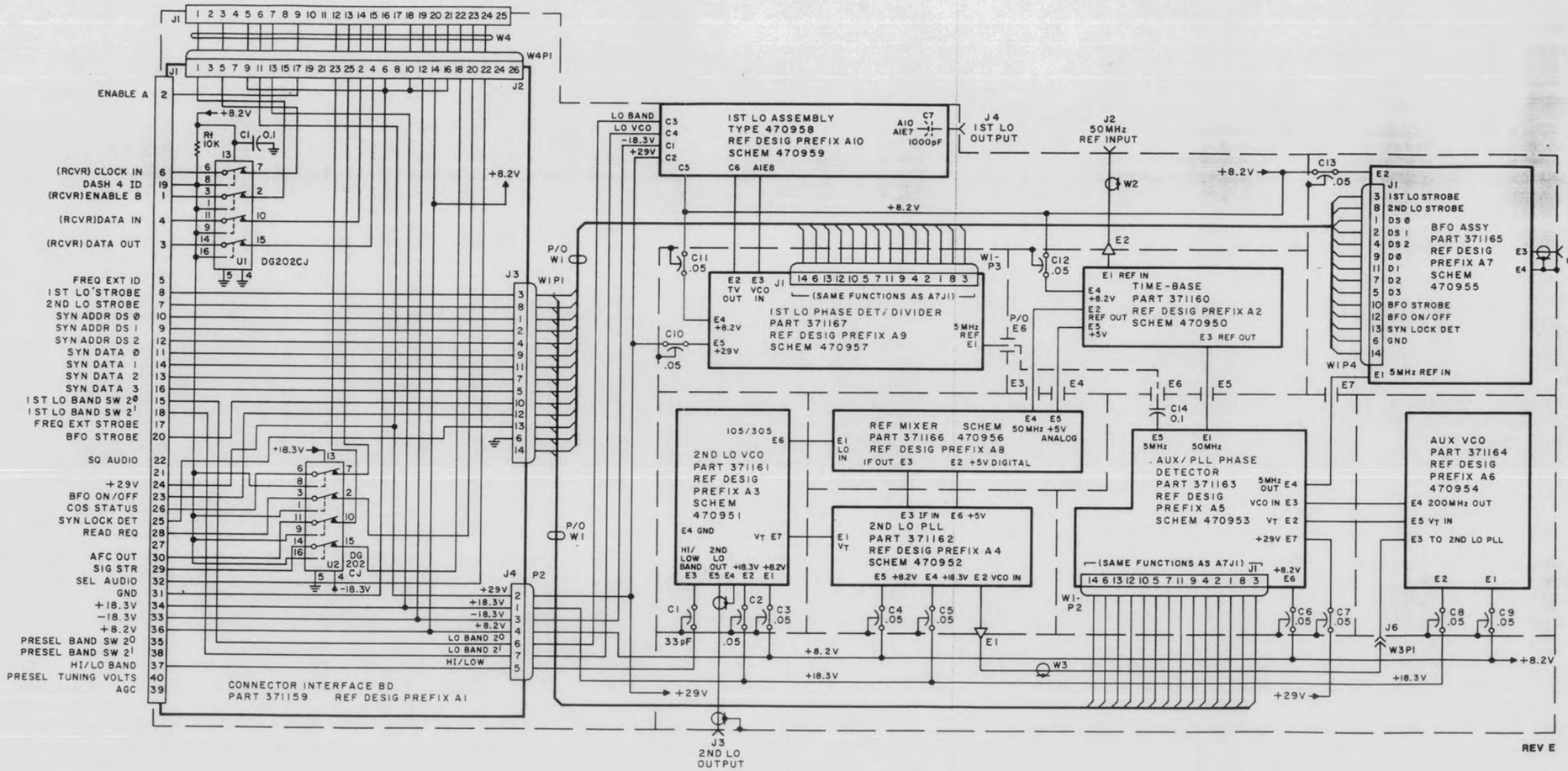


Figure 6-14. Type 794447-1 Synthesizer Module (A3), Schematic Diagram 470934

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/8W
   b. CAPACITANCE IS IN pF
   c. INDUCTANCE IS IN µH

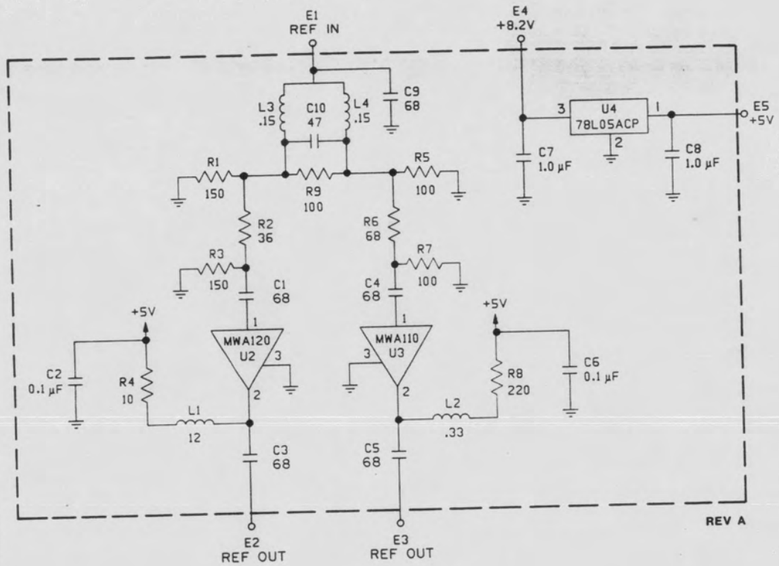


Figure 6-15. Type 371160-1 Time Base (A3A2), Schematic Diagram 470950

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, +5%, 1/8 W.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.
2. FINAL VALUE FACTORY SELECTED.

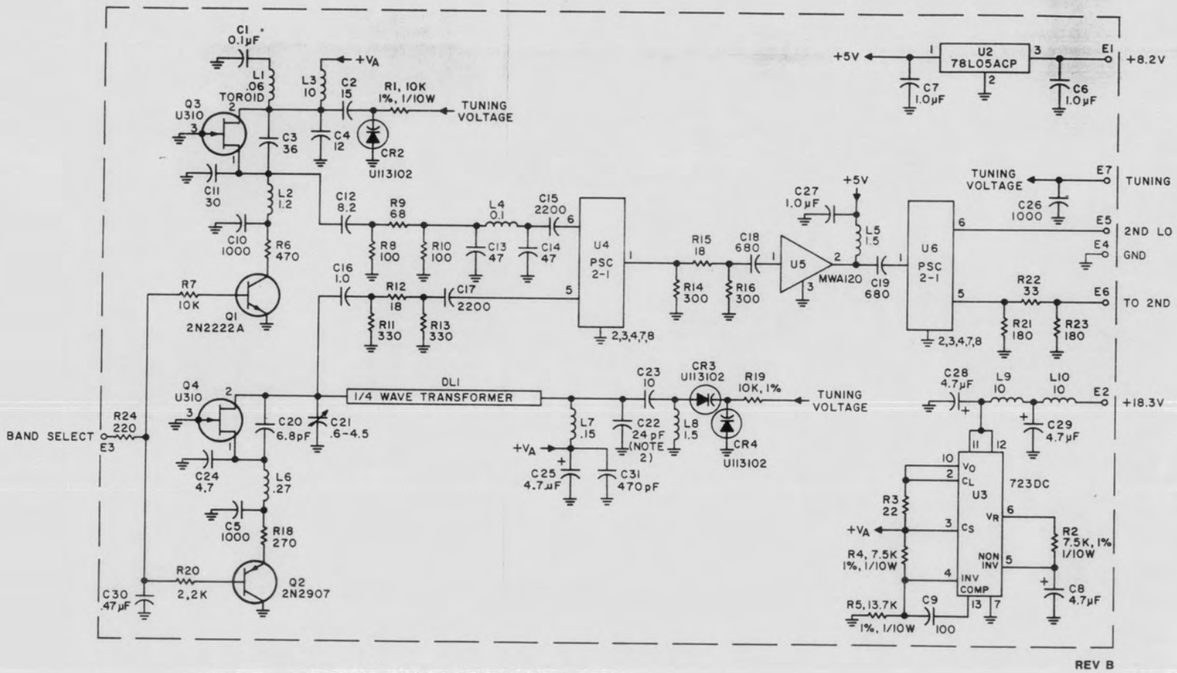


Figure 6-16. Type 371161-1 2nd LO VCO (A3A3), Schematic Diagram 470951

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/8W
   b. CAPACITANCE IS IN pF
   c. INDUCTANCE IS IN µH

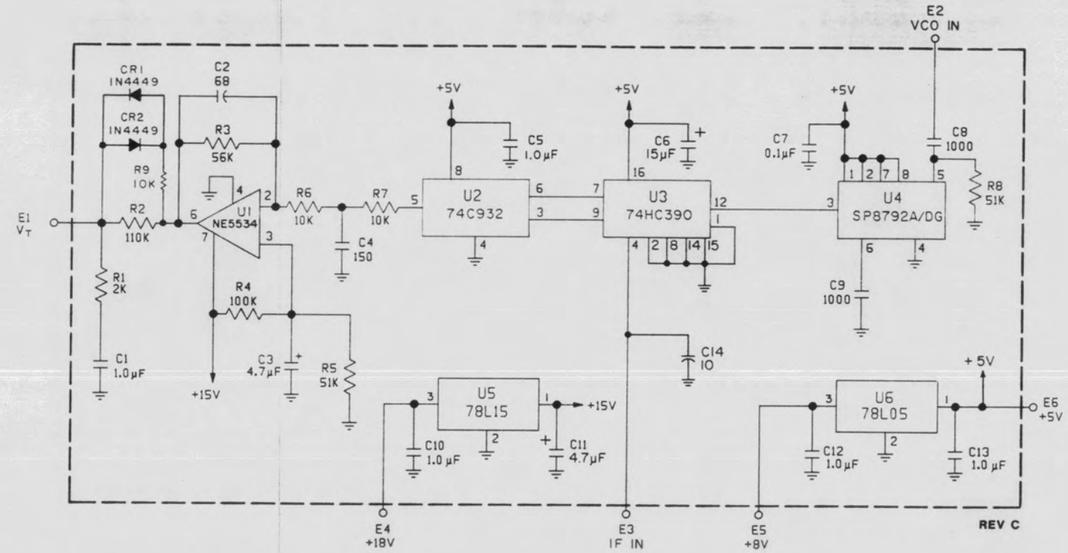


Figure 6-17. Type 371162-1 2nd LO PLL (A3A4), Schematic Diagram 470952

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/8 W.
   b. CAPACITANCE IS IN µF

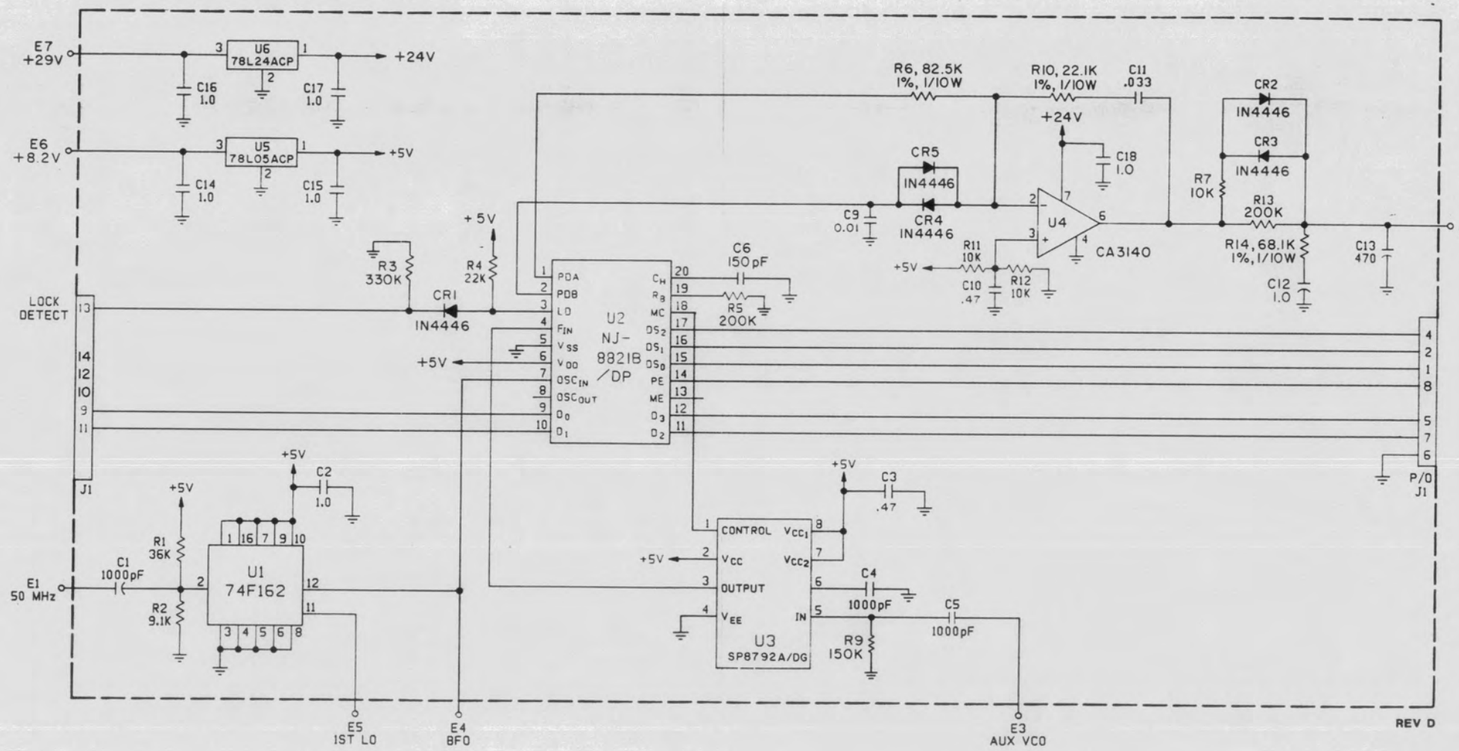


Figure 6-18. Type 371163-1 AUX/PLL Phase Detector (A3A5), Schematic Diagram 470953

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4 W.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.
2. NOMINAL VALUE, FINAL VALUE FACTORY SELECT

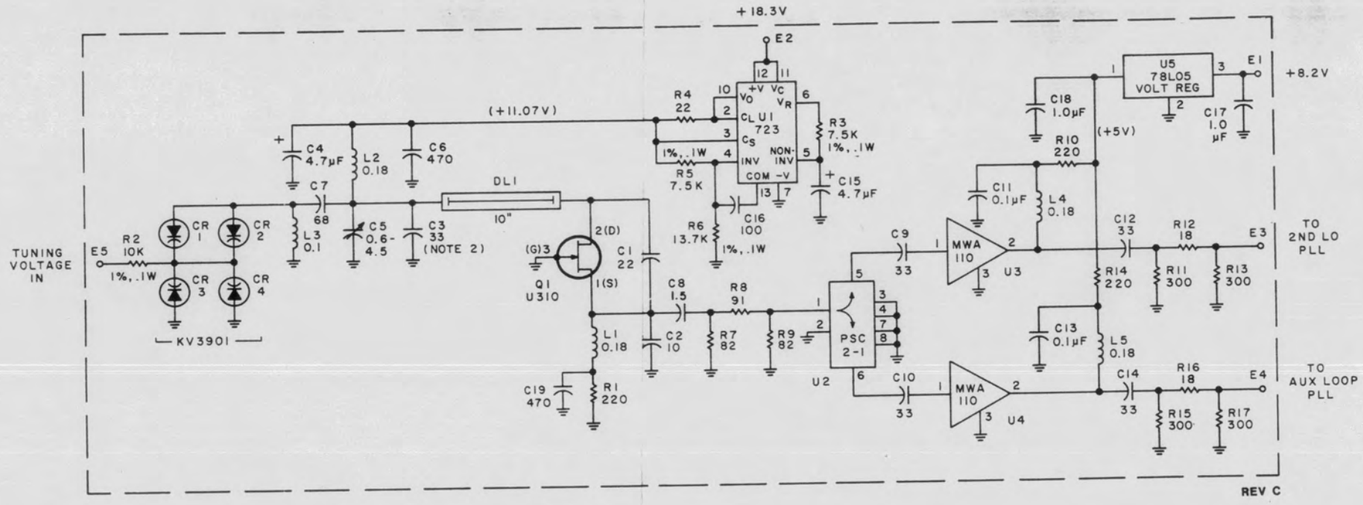


Figure 6-19. Type 371164-1 AUX VCO (A3A6), Schematic Diagram 470954

NOTES:
UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
b) CAPACITANCE IS IN µF.
c) INDUCTANCE IS IN µH.

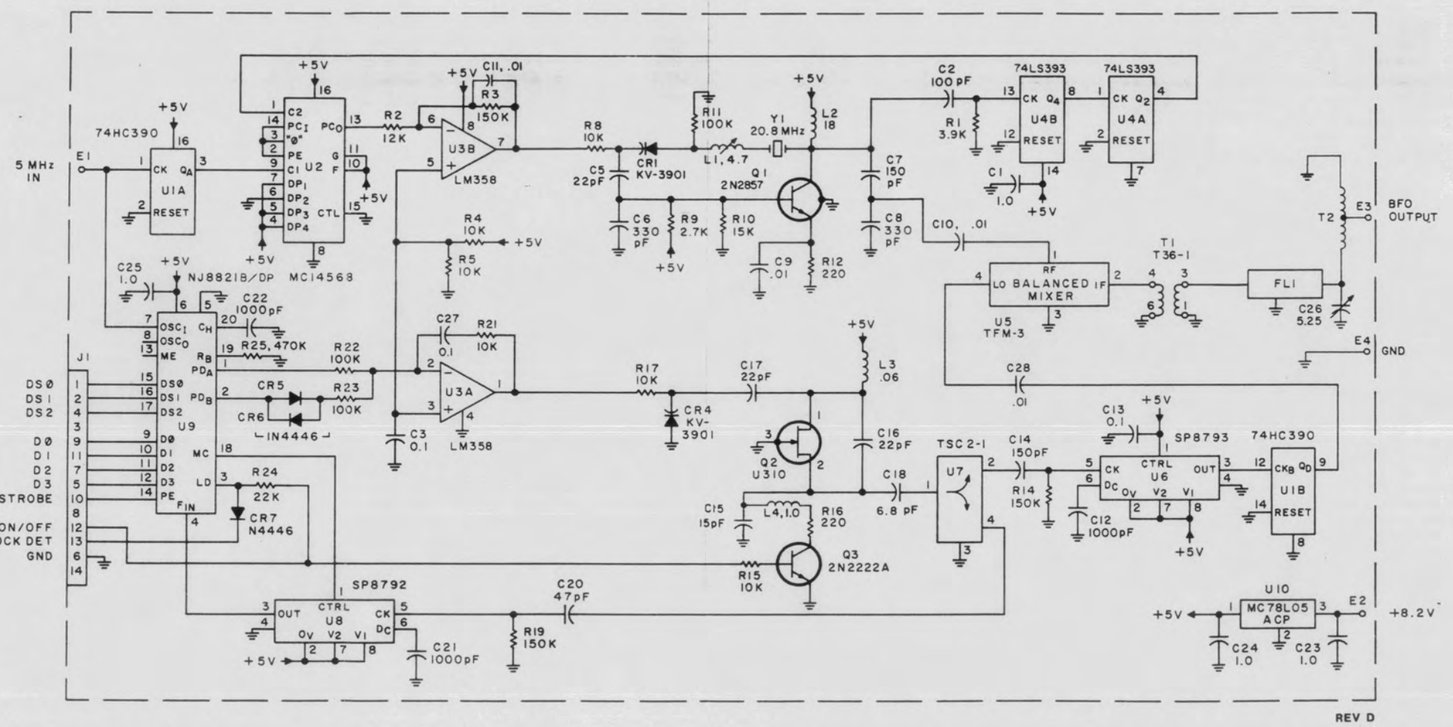


Figure 6-20. Type 371165-1 BFO Assembly (A3A7), Schematic Diagram 470955

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/8W
   b. CAPACITANCE IS IN pF
   c. INDUCTANCE IS IN µH

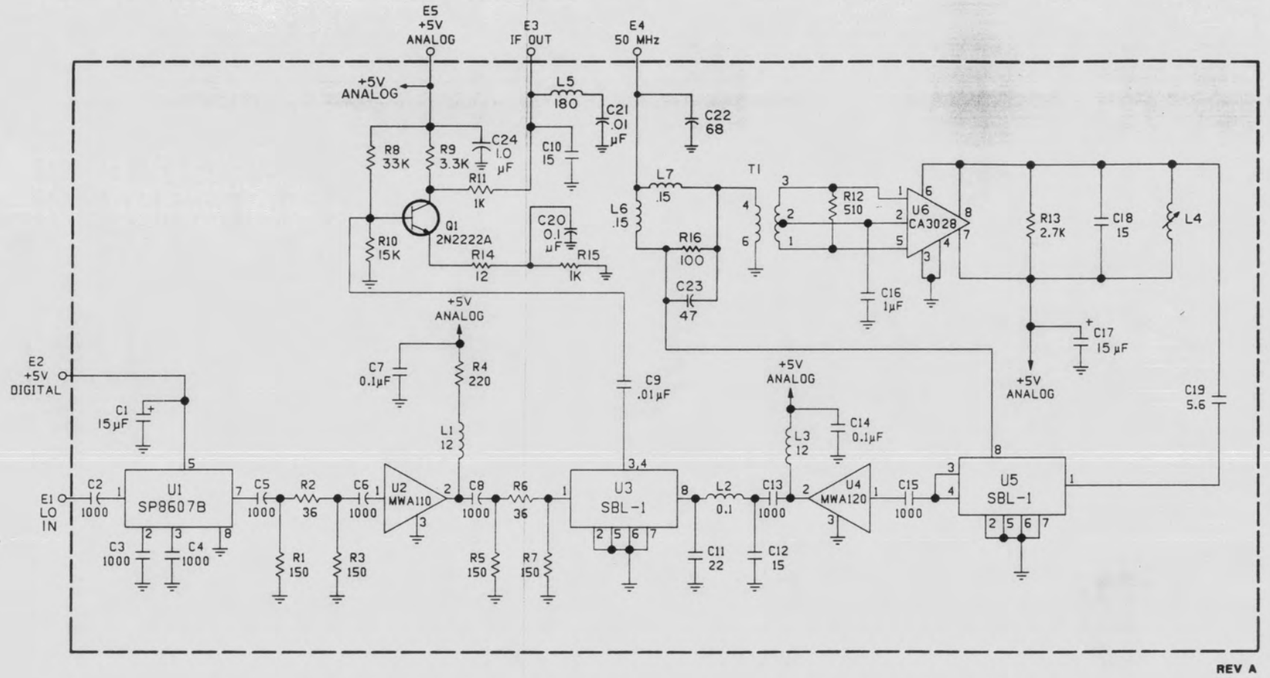


Figure 6-21. Type 371166-1 Reference Mixer (A3A8), Schematic Diagram 470956

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5%, 1/8 W.
   b. CAPACITANCE IS IN μF

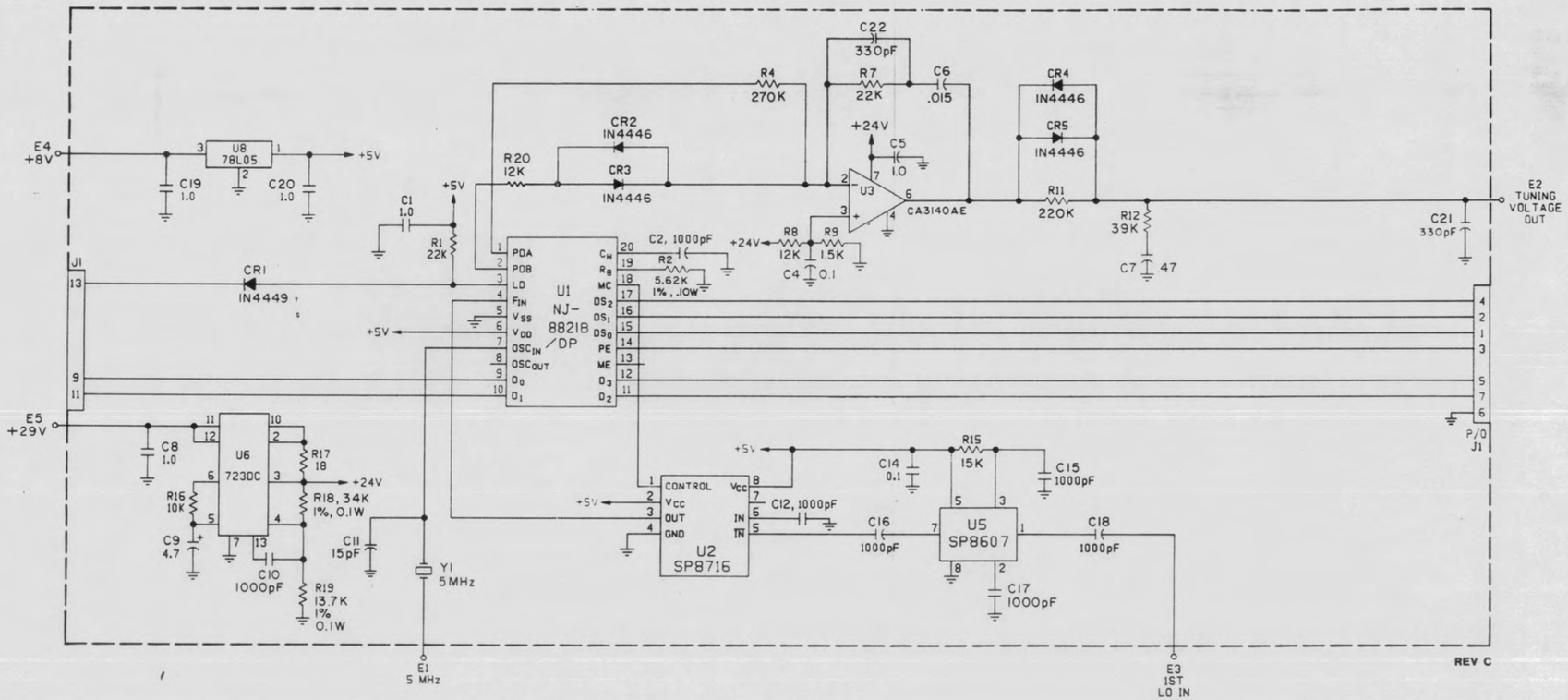


Figure 6-22. Type 371167-1 1st LO Phase Detector/Divider (A3A9), Schematic Diagram 470957

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8 W.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.
2. NOMINAL VALUE, FINAL VALUE TO BE FACTORY SELECTED

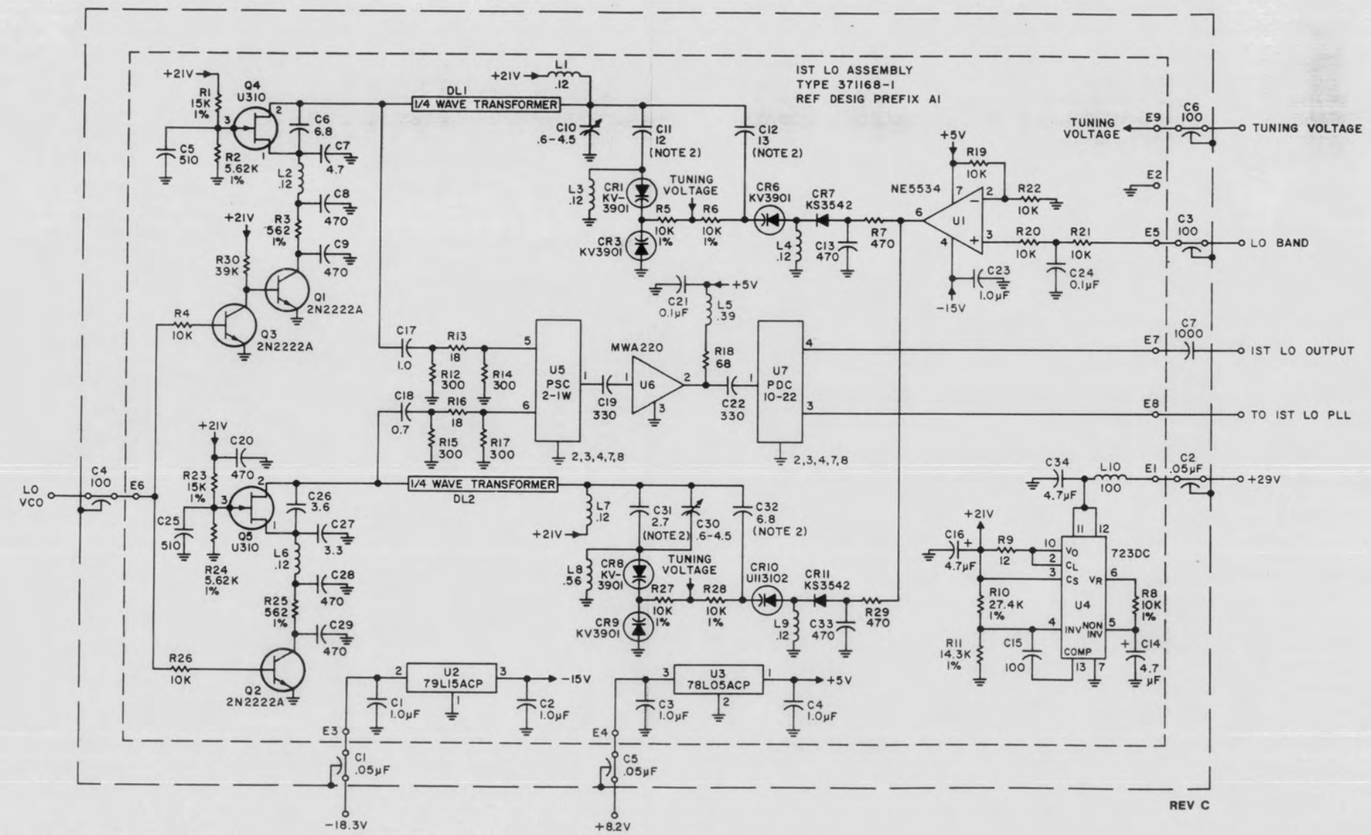


Figure 6-23. Type 470958-1 1st LO Assembly (A3A10), Schematic Diagram 470959

TABULATION

TYPE NO.	JW1	JW2	P1	P2	J8	J9
794431-1	USE	USE	N/U	N/U	N/U	N/U
794431-2	N/U	N/U	USE	USE	USE	USE

	TITLE	TYPE	SCHEM
XA1	VOLTAGE REGULATOR MODULE	794432-1	470889
XA2	I/O OPTION		
XA3	EXTENDED CPU	794444-X	570353
XA4	OPTION		
XA5	RECEIVER/EF INTERFACE	794421-1	470894
XA6	FRONT PANEL INTERFACE	794433-1	470895

NOTES:
1. UNLESS OTHERWISE SPECIFIED: CAPACITANCE IS IN µF.
2. FOR DIFFERENCES IN TYPE NUMBER SEE TABULATION.

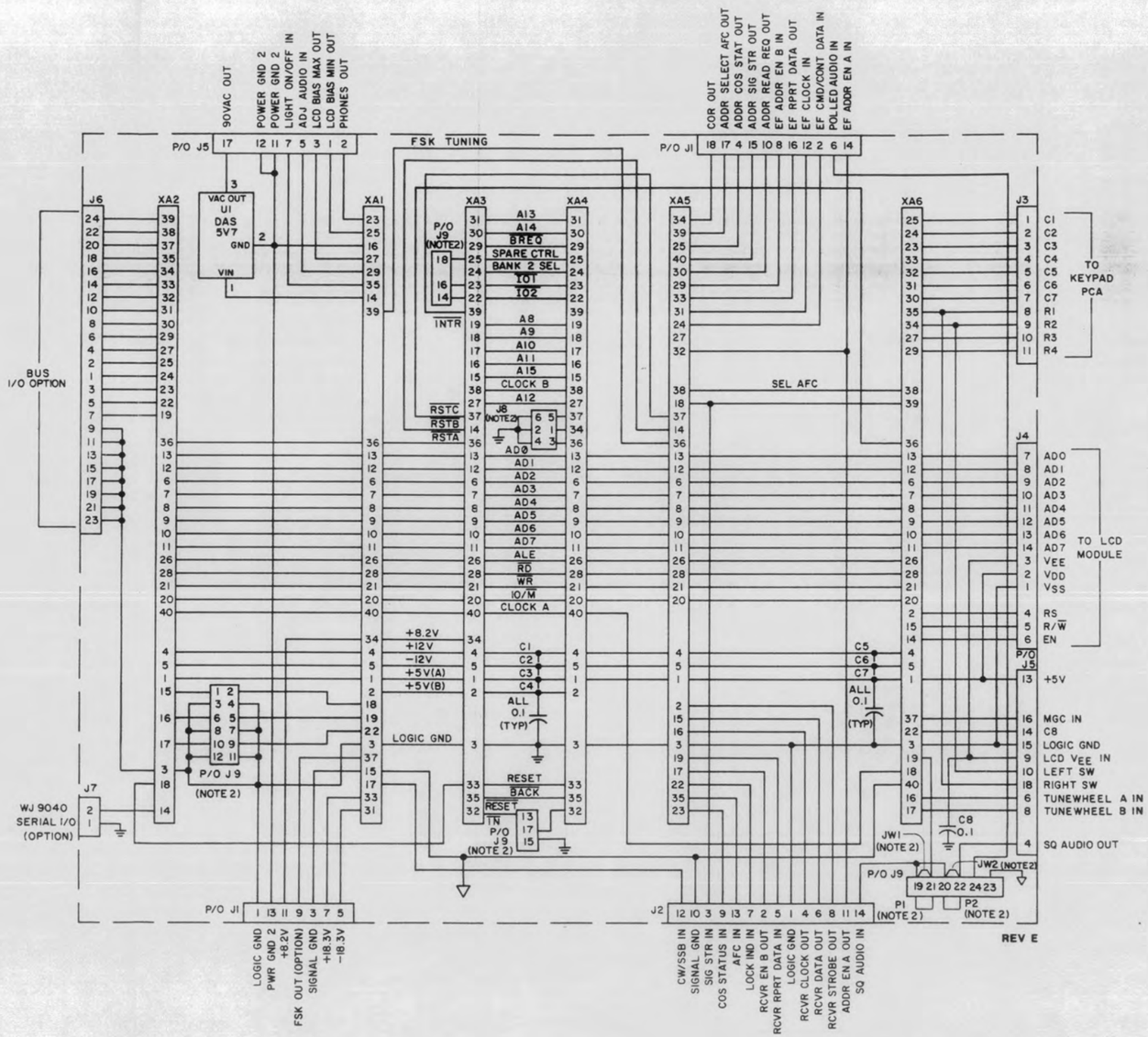


Figure 6-24. Type 794431-2 Controller Motherboard (A4), Schematic Diagram 470890

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS IN μF.

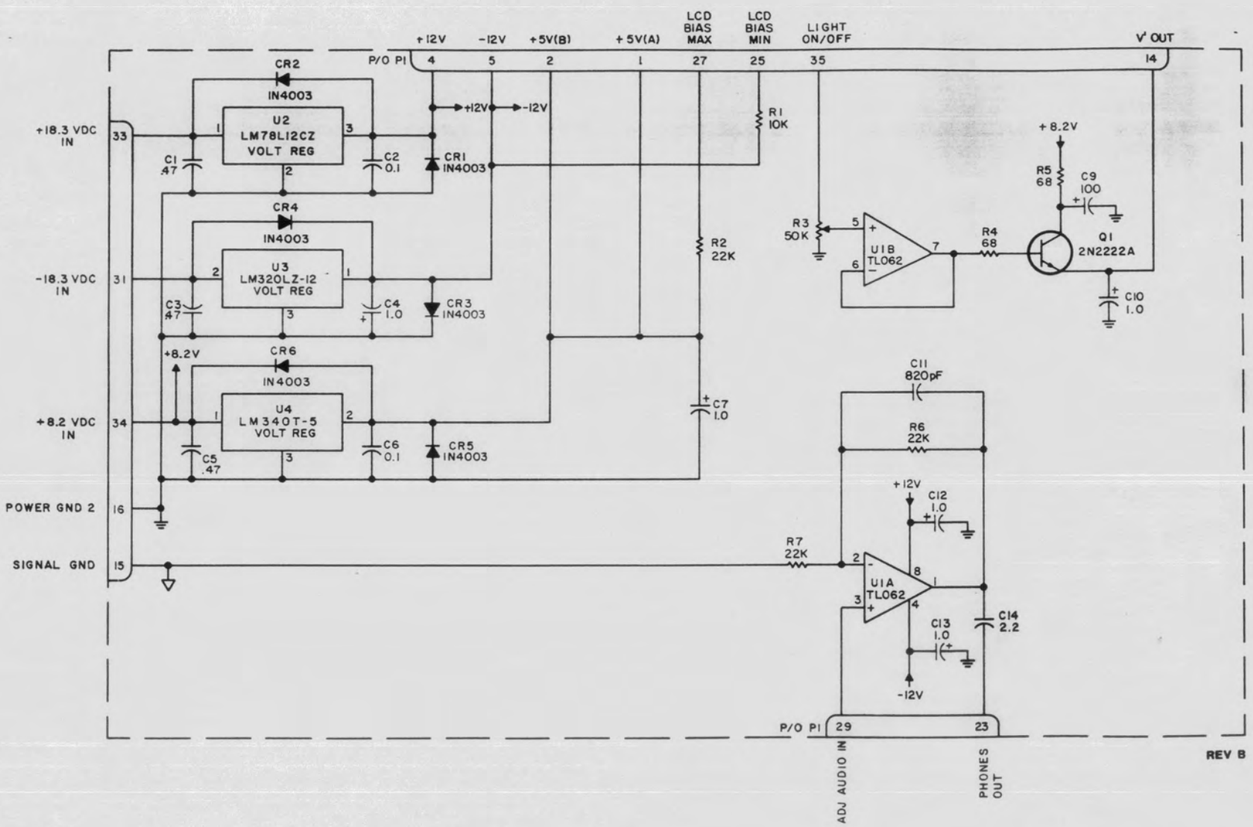


Figure 6-25. Type 794432-1 Voltage Regulator (A4A1), Schematic Diagram 470889

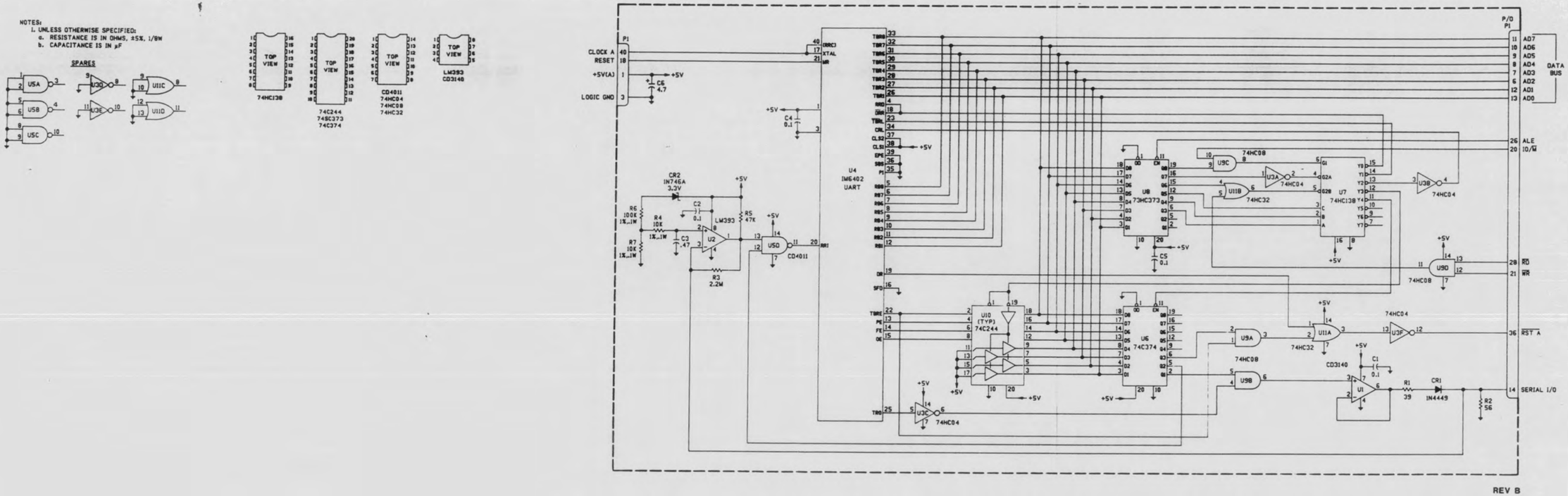


Figure 6-26. Type 794437-1 Remote I/O Interface Option (A4A2), Schematic Diagram 470969

Figure 6-27. Type 794444-X Extended CPU Option (A4A3), Schematic Diagram 570353

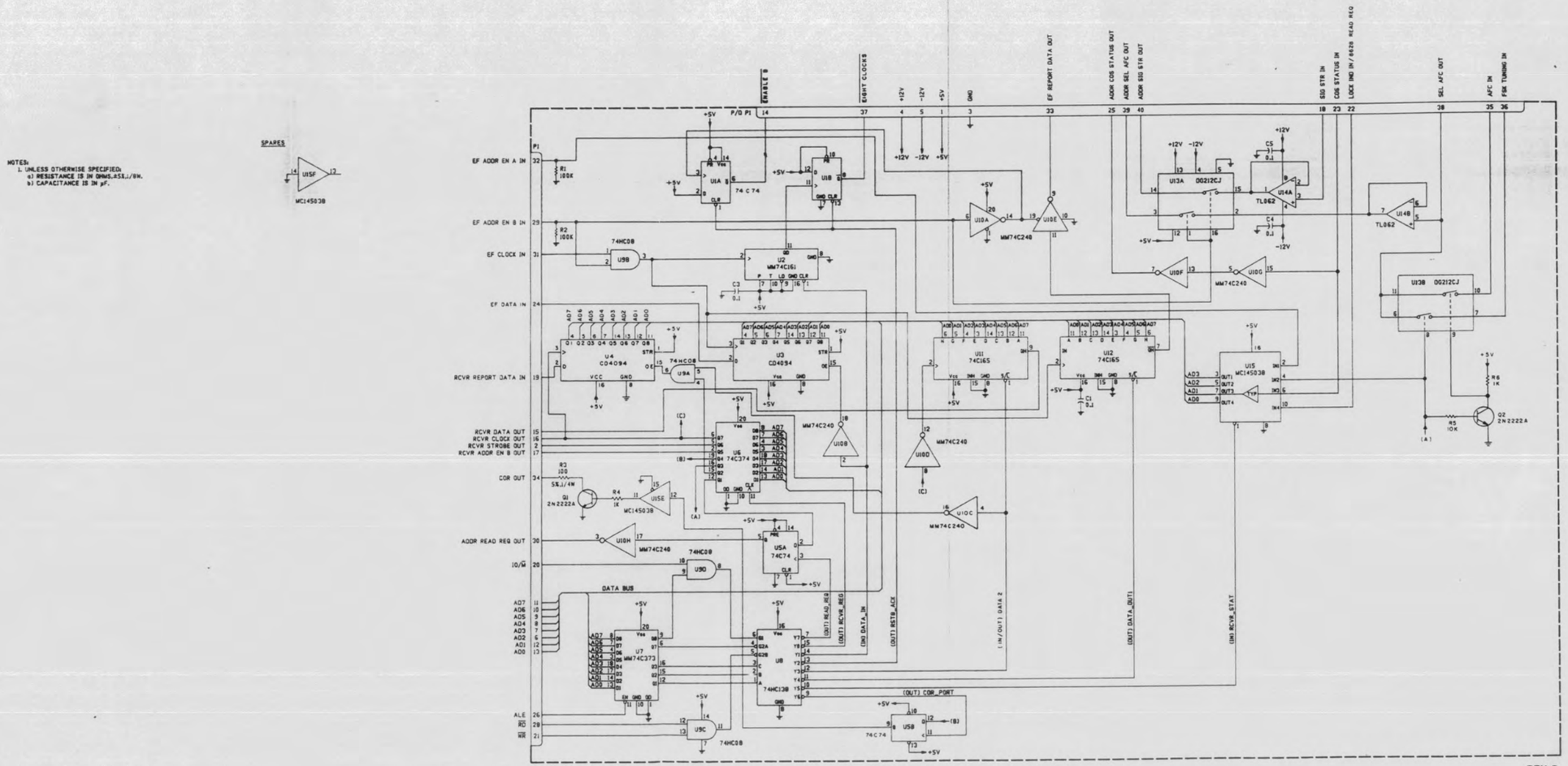


Figure 6-28. Type 794421-1 Receiver EF/Interface (A4A5), Schematic Diagram 470894

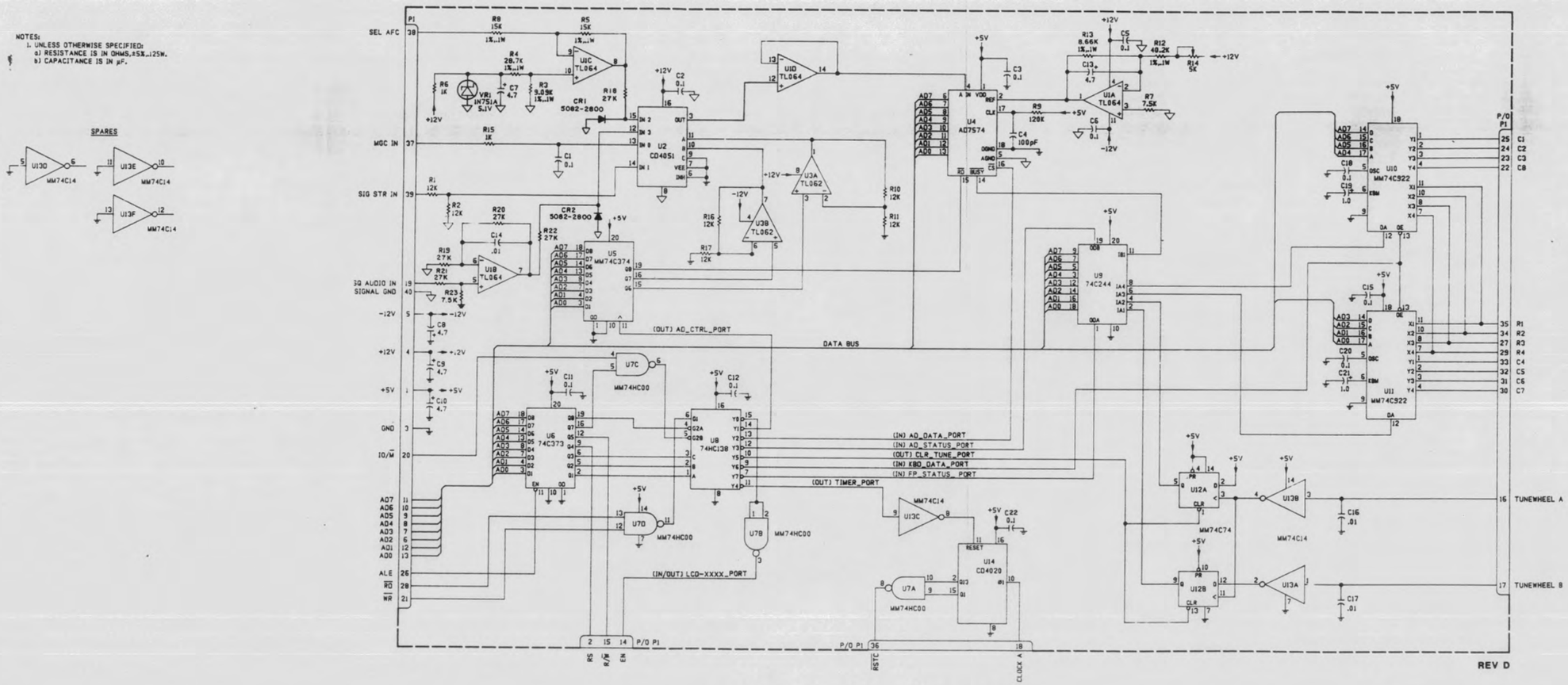


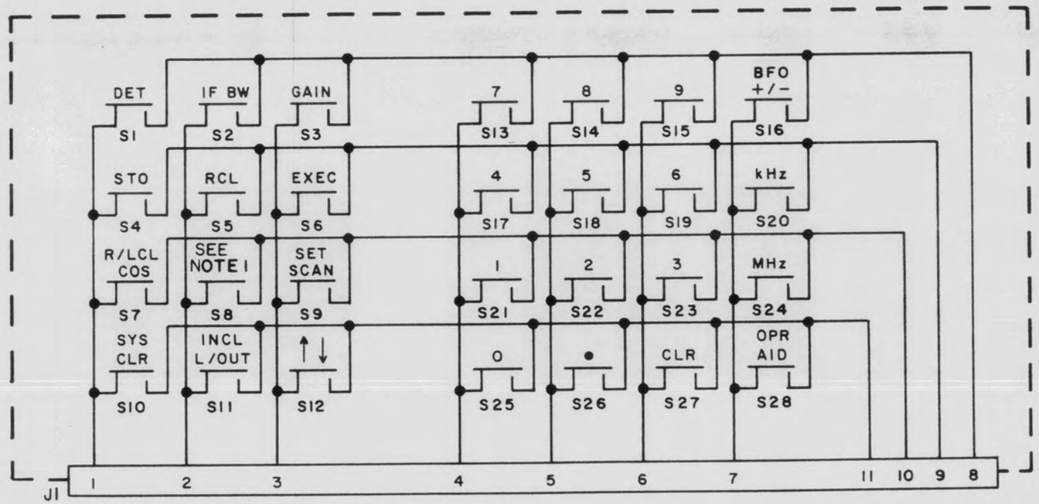
Figure 6-29. Type 794433-1 Front Panel Interface (A4A6), Schematic Diagram 470895

TABLE I

PART	S8
371037-2	DWL AFC
371037-3	DWL

NOTES:

1. DIFFERENCE BETWEEN PARTS IS SHOWN IN TABLE I.



REV C

Figure 6-30. Type 371037-2 Keyboard Assembly (A8), Schematic Diagram 371045

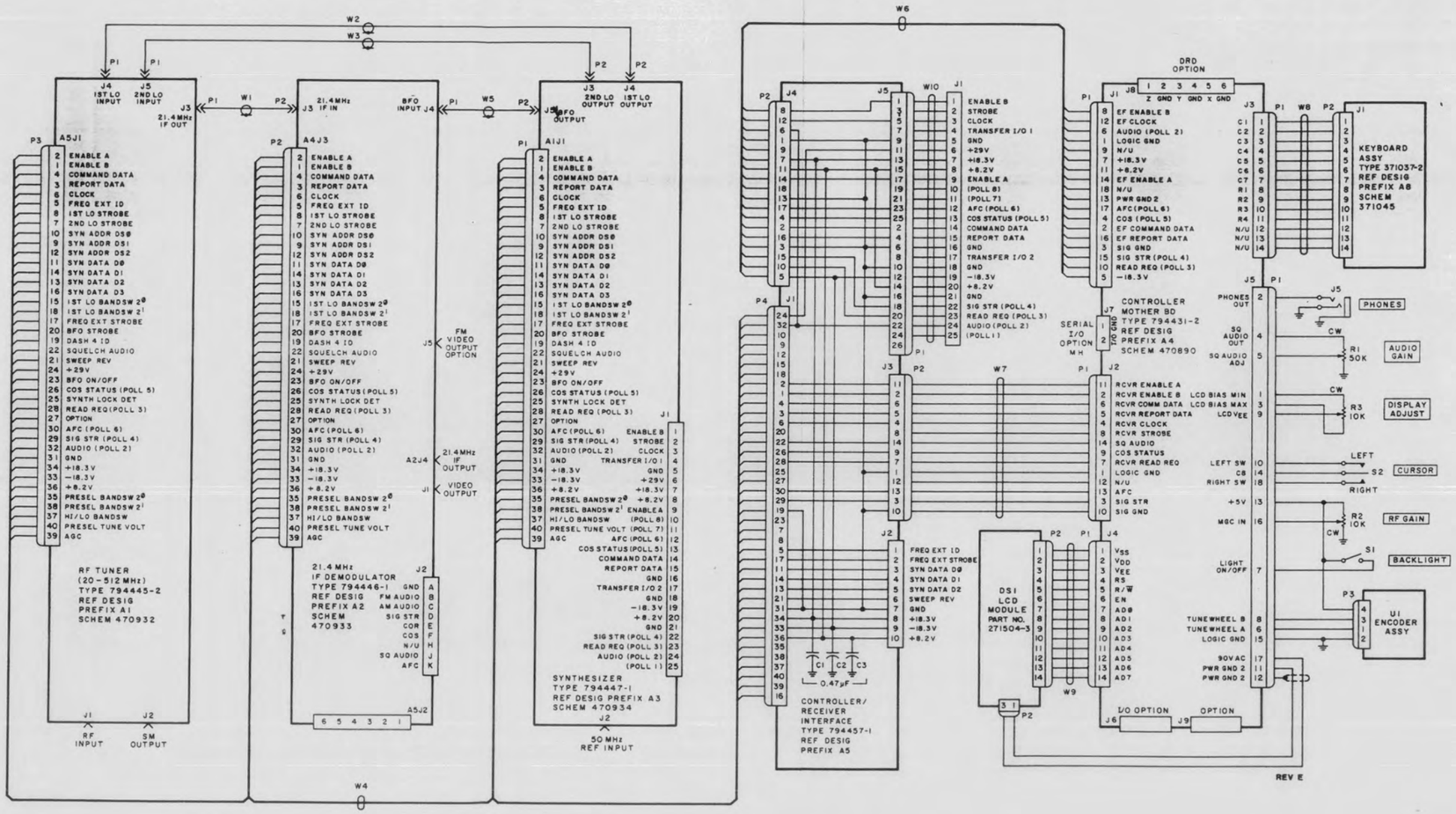


Figure 6-31. Type WJ-8628-4 VHF/UHF Receiver Main Chassis, Schematic Diagram 570342