SECTION III

CIRCUIT DESCRIPTION

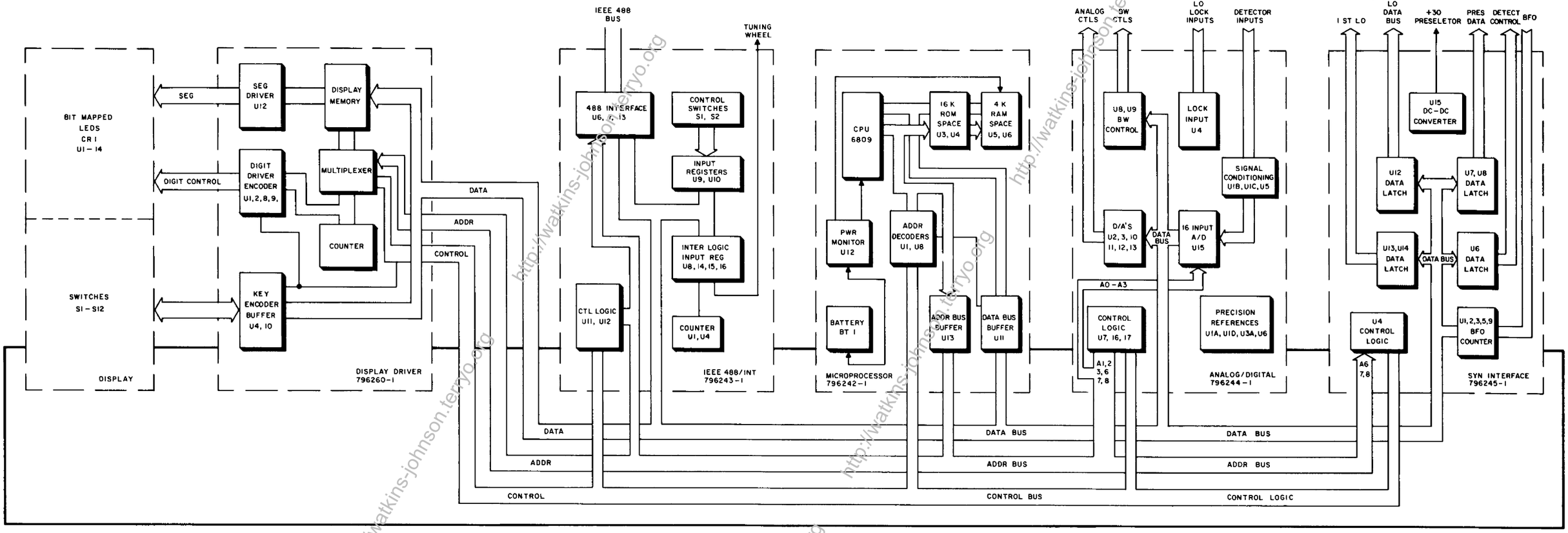


Figure 3-1. Digital Control Section Functional Block Diagram 580205

SECTION III

CIRCUIT DESCRIPTION

3.1 GENERAL

The operating circuitry of the WJ-8615D Compact Receiver is contained in three main sections. Each section contains the circuitry required to perform specific portions of the overall receiver operation. The sections are interconnected via a common Motherboard (A1) which permits the various sections to perform as a single unit under the control of the Digital Control Section. Operation of the Digital Control, Synthesizer and RF/IF Sections are described in the following paragraphs. Reference to the Functional Block Diagrams in this section and to the Schematic Diagrams in Section VI supplement the following circuit descriptions.

3.2 DIGITAL CONTROL SECTION

3.2.1 FUNCTIONAL DESCRIPTION

This microprocessor controlled Digital Control Section continuously monitors the operation of the receiver and provides control signals directing its operation. The primary subassemblies responsible for controlling the receiver are the Microprocessor (A1A3), IEEE-488/Interrupt (A1A2), Analog/Digital (A1A4), Synthesizer Interface (A1A5) and Front Panel Display (A1A1). These subassemblies and their interconnections are illustrated in the Digital Control Section Functional Block Diagram, **Figure 3-1.** In addition to the primary control subassemblies, an option slot is provided to extend the control capabilities and provide enhancements to the operation of the receiver.

The Microprocessor (A1A3) performs the task of controlling the operation of the receiver by providing control signals to the various receiver circuits and monitoring the receiver operation. This subassembly consists of a microprocessor, a list of operating instructions contained in ROM (Read-Only-Memory) and 2 k bytes of RAM (Random-Access-Memory) where the microprocessor stores and retrieves variable data as required, as it performs its control function. Under the direction of the program, the microprocessor continuously monitors the receiver operation and performs tasks as required. Communication between the microprocessor and the other subassemblies within the Digital Control Section is established utilizing the 16-line address bus and the 8-line data bus of the microprocessor. Each of the input and output circuits on the Synthesizer Interface, Analog/Digital, IEEE-488 Interrupt and Front Panel Display as well as the option slot are assigned specific addresses. By placing the appropriate address on the address bus, the microprocessor communicates with the desired location via the data bus. The control bus which is comprised of the I/O enable, Read/Write and IRQ lines permit the microprocessor to activate the required circuit by controlling the direction and timing of the data flow and to sense when a circuit is exercising the IRQ line (request service by the microprocessor).

Analog/Digital subassembly (A1A4) is utilized to convert analog data from various receiver circuits such as LO Lock inputs and Detector inputs into digital form to be read by the microprocessor. These signals are conditioned and applied to D to A converters to be read by the microprocessor when address lines A0 through A3 are enabled. Control data is applied to the other receiver circuits via the analog control lines and the bandwidth control lines.

IEEE-488 Interrupt subassembly (A1A2) provides interfacing between the receiver and external controlling devices and provides interrupt latching circuitry that generates interrupt requests (IRQ) which are applied to the microprocessor. Interrupt requests are generated by the front panel when a detection mode is changed, an IF bandwidth is changed or when the tuned frequency is changed. This subassembly provides control logic to the 1st LO and 2nd LO/3rd Synthesizer and to the BFO counter. When interrupts occur, this subassembly alerts the microprocessor via the $\overline{IRQ}$ line that a service request has been made.

Synthesizer Interface subassembly (A1A5) is utilized to provide interface between the microprocessor and the 1st LO and 2nd LO/3rd Synthesizer. The data latches on this subassembly provide the BCD words for tuned frequency information, detection mode information and optional Tracking Preselector information. Also included on this subassembly are printer and RS-232 compatible printer outputs.

Front Panel Display subassembly (A1A1) contains hardware generated refresh logic. Data written by the microprocessor is hardware refreshed by the Display Driver subassembly (A1A1A1). This subassembly consists of a dual ported memory which comprises 16 bytes of bit-mapped LED display. Switch matrix encoders, upon a key closure, set the key available line to the microprocessor along with the key code and is made available to the data bus via data bus buffers.

3.2.2 DETAILED CIRCUIT DESCRIPTION

3.2.2.1 Type 796242-1 Microprocessor (A1A3)

The reference designation for the microprocessor subassembly is (A1A3). Refer to **Figure 6-4** for the Type 796242-1 Microprocessor schematic diagram.

Y1, a 4.9152 MHz crystal oscillator establishes the microprocessor (U7) internal clock frequency. The circuit comprised of capacitors C1 and C2 assures that the crystal oscillates at its fundamental frequency. U12A and U12B create a time delay circuit to allow the power supply to settle before enabling the reset circuitry of the microprocessor. Capacitor C3 creates a time delay, due to its charge time, for the +5 Vdc to settle before the microprocessor is reset. The microprocessor must see 4.8 V, minimum for power up. Power down conditions exists when the dc level is 4.7 V or less.

Integrated circuit U7 is the MC68B09 microprocessor. Pins 2 ($\overline{NMI}$), and 40 ($\overline{HLT}$) are not utilized under normal operating conditions and are terminated high, disabling these inputs. $\overline{NMI}$ (Non Maskable Input), pin 2, is utilized to start the signature analysis program when pulled low. $\overline{HLT}$ (Halt), pin 40, is utilized to stop the microprocessor activity when pulled low. $\overline{IRQ}$ and $\overline{FIRQ}$ are the interrupt request lines which receive inputs from the IEEE-488 Interrupt subassembly (A1A2) when an interrupt is requested. Data I/O lines consists of D0 through D7. These lines connect to the memories and to the data bus on the motherboard to read from and write data into the input and output circuits of the Digital Control Section. Pin 32, the Read/Write line of the microprocessor indicates whether the microprocessor is in a Read (High) or a Write (Low) state. A0 through A8 are connected to the Address Bus of the motherboard and to the memories. Address lines A13, A14 and A15 go to a 4 to 10 decoder (U1), which decodes the address lines to divide the address space into 8K byte blocks.

The lowest 8 K block (0000-1FFF) from U1, pin 1 is applied to decoder U8B where the address space is further divided into 2 K blocks. The first 2 K block (0000-07FF) is applied to RAM U6 via inverter U12B. The second 2 K block (0800-0FFF) is applied to RAM U5 via inverter U12C. The last 2 K block (1800-1FFF) is the I/O block which is divided into four 512 byte block, via U8A, for I/O control. I/O 1 controls the operation of the IEEE-488 subassembly (A1A2) and the Front Panel Display (A1A1). I/O 2 goes to the Synthesizer Interface subassembly (A1A5) and I/O 3 goes to the Analog/Digital subassembly (A1A4). I/O 4 is not utilized in the present configuration. When these control lines are pulled low, the respective subassemblies are activated.

U5 and U6 comprise the RAM's. These integrated circuits each contain 2048 memory locations 8 bits wide. The RAM's connect to the data bus lines D0 through D7 and address lines A0 through A10. The chip select inputs $\overline{CS}$ permit selection of each RAM in accordance with the address. The $\overline{CS}$ lines are enabled via U12B and U12C in accordance with address lines A11 and A12. U5 is not utilized in the present receiver configuration, but is available to provide expansion capabilities. JW3 and JW4 allow the use of an EPROM instead of a RAM in the U5 location. U12B and U12C provide data retention logic for the RAM's. The $\overline{CS}$ (chip select) lines remain high which prevents RAM access during power interruptions.

The read-only-memory is comprised of EPROM's U3 and U4. Each EPROM connects to address lines A0 through A12 providing 8 K memory locations each for a total of 16 K bytes of read-only-memory. These EPROM's are sequentially enabled in accordance with address lines A13, A14 and A15 via decoder U1. Each select output of U1 goes to the $\overline{CS}$ and $\overline{OE}$ inputs of one of the EPROM's enabling it when the line is pulled low. JW1 is utilized to decide what size memory chips are in U3 and U4 locations by jumping the select lines to the output of U1. JW5 allows the use of a RAM instead of an EPROM in the U4 location. Address line A13, pin 26 is utilized if a type 27128 EPROM is used.

Integrated circuit U11 connects to the data bus and is enabled by the I/O enable line. This bidirectional transceiver transfers data between and the microprocessor and the motherboard of the receiver. The direction of the data flow is controlled by the R/$\overline{W}$ line of the microprocessor. U13A supplies address lines A0 through A3 and U13B supplies address lines A5 through A8. Address line A4 is not buffered. Integrated circuits U11, U13A and U13B provide buffering to prevent excessive loading of the data and address busses.

When the receiver is powered up, +5 Vdc is applied to RAM's U5 and U6 via board terminals 49 and 50. When power is removed, the backup battery BT1 applies a nominal voltage of 2.8 Vdc, supplying approximately 1 µA of standby current to the RAM's. This prevents stored data in the RAM's from being lost when power is removed. Additional battery current drain is prevented by R9. CR5 isolates the battery, BT1 from the +5 V power supply line during normal receiver operation. In the absence of +5 V, CR5 is forward biased by BT1 providing backup power to the RAM circuitry.

NOTE

BT1 is a primary lithium cell which under normal operating conditions, is expected to last 10 years. When the microprocessor board is removed, the battery is disconnected. DO NOT place this assembly on a metallic surface.

3.2.2.2 Type 796244-1 Analog/Digital (A1A4)

The reference designation for the Analog/Digital subassembly is (A1A4). Refer to **Figure 6-5** for the Type 796244-1 Analog/Digital schematic diagram.

Integrated circuit U6 provides the precision 10 Vdc reference. From this circuit, U1A and Q1 provide the 10 Vdc reference for digital to analog converters U10, U11, U12 and U13. Integrated circuit U1D and Q2 provide the -13 Vdc reference for level shifter U8 so that the bandwidth code can be read on the Audio/Video subassembly. U3A provides the 4.95 Vdc reference for analog to digital converter U15.

Address converter U7 takes the I/O 3 line from the microprocessor and further decodes it with address lines A6, A7 and A8 yielding 64 byte blocks for this subassembly. These blocks are write lines thus U7 is enabled on a write cycle. A read on the I/O 3 line causes the output of inverter U17B to become active which reads the last result of conversion occurring in analog to digital converter U15.

Analog to digital converter U15 is selected by writing 1D40 into the address to start conversion. The leading edge of 1D40 latches the ALE input and the trailing edge of 1D40 starts the conversion process. When conversion is complete EOC signals the microprocessor that conversion is complete. U15 runs with $\overline{E}$ clock and its conversion time is less than 30 µsec. Connector pin 39, AM/PEAK is the dc representation of the peak component seen on the AM Demodulator. This is utilized for sideband and pulse AGC operations. Pin 40, AM/AC is the dc representation of the ac component seen on the AM Demodulator. Pin 41, AM/DC is the dc component seen on the AM Demodulator. This is utilized for AM and FM AGC operations. Pin 42, FM/AC is the dc representation of the ac component seen on the FM Discriminator. Pin 43, FM/DC is the dc component seen on the FM Discriminator. This is utilized for AFC operation and for the tuning meter. Pin 44, LOG/VIDEO is the dc component seen on the LOG Detector. Pin 46. FP USB is the upper channel audio for the front panel. This is half-wave rectified so that U15 sees the dc representation. Pin 47, FP LSB is the lower channel audio, also half-wave rectified. Connector pins 45 and 48 are not utilized in the present configuration. U15, pin 14, is a sense point for the microprocessor for testing power supply voltages. R-C filters are incorporated at pins 39 through 42 and pin 44 to strip off high frequency noise from these lines. Pin 43 also has an R-C filter and a clamping diode, CR5 to make certain that the FM dc level does not go negative. The 2nd LO fine tune voltage applied to connector pin 6 is a range between 2 to 10 V buffered via U1C and converted via U5B to a 0 to 5 V signal to be applied to U15. This is for future receiver diagnostic tests. The bandwidth code enters connector pin 4 as a current source. U1B converts this to a voltage of 0 to 10 V and converted again to 0 to 5 V via U5A before being applied to U15. Integrated circuits U5A and U5B protect U15 from seeing ground or voltage levels greater than 5 V.

Analog to digital converters U10, U11 and U12 are dual 8 bit converters. The A half of the converters are selected by writing 1C00 in the address and the B half is selected by writing 1C01 in the address. Since the operation of these converters is similar, U10 will be discussed in detail. The current output of U10A and U10B is converted to a voltage via U2B and U2C. An internal latch within U10 maintains the last seen voltage. Connector pin 14 (IF NORM) is a voltage between 0 to 13 V which selects the amount of attenuation for the IF normalization on the IF bandwidth subassembly for the selected bandwidth. This is also utilized to add attenuation for AGC operation. Pin 16 (IF AGC) is a voltage between 0 to 13 V utilized for controlling the amount of IF attenuation on the bandwidth subassembly. Pin 18 (DET AGC) is a voltage between 0 to 13 V, utilized for controlling the amount of AM Demodulator

attenuation. Pin 20 (BFO TV) is a voltage between 0 to 10 V utilized the 21.4 MHz variable oscillator on the Reference Generator subassembly. Pin 25 (AUX D/A) is applied to rear panel connector J13 and is intended for future use. Pin 22 (VHF AGC) is a voltage between 0 to 13 V utilized to control the amount of attenuation for the RF Converter subassembly. Pin 24 (UHF AGC) is a voltage between 0 to 13 V, utilized to control the amount of attenuation for the optional Frequency Extender subassembly.

The 12 bit digital to analog converter (U13) provides a current output which is converted to 0 to 13 V via U3D. This controls the coarse tune voltage for the 2nd LO Synthesizer subassemby. The two byte address of U13 is 1CC1 and 1CC0.

Data bus latch U14 provides an output from information at D5 to select FM $\overline{\text{NAR}}$/MID (narrow/midband) discriminators as required by the size of the selected IF bandwidth. D6 selects FM WIDE (wideband) discriminator as required by the size of the selected IF bandwidth.

Bandwidth and COR data latch U9 provides IF bandwidth selection via data bus lines D0 through D4. Also provided is the wideband/narrowband control line via D5. These lines, D0 through D5 are level shifted to the precision reference voltage via U8. A logic "1" is 13 V, and a logic "0" is 0 V. D6 is the spare driver line intended for future use and D7 is the external COR control line. Both D6 and D7 are open collector transistor pulled-up to +5 V in order to drive TTL devices directly. CR1 and CR2 provide voltage spike protection for relay switching.

Inverters U16C and U16F are utilized to pulse the 2nd LO/3rd Synthesizer clock lines. U16E provides a buffered direction finder control line to the rear panel connector J13 derived from the UHF/VHF control line. A logic "1" indicates the receiver is tuned between 20 and 500 MHz and logic "0" represents tuned frequencies greater than 500 MHz.

Integrated circuit U4B is the unlock sensor for the 1st LO Synthesizer subassembly. R1 and C2 form the low pass filter. Resistors R2 through R5 form a hysteresis loop around comparator U4B to compare the 1st LO lock line with the reference of U5. A logic "1" indicates unlock and a logic "0" indicates lock. U4A is the 2nd LO/3rd Synthesizer subassembly unlock sensor. R6 and C1 form the low-pass filter. Resistors R7 through R10 form a hysteresis loop around comparator U4A to compare the 2nd LO/3rd Synthesizer lock line with the reference of U5. A logic "1" indicates unlock and a logic "0" indicates lock.

3.2.2.3 Type 796243-1 IEEE-488/Interrupt (A1A2)

The reference designation for the IEEE-488/Interrupt subassembly is (A1A2). Refer to **Figure 6-3** for the Type 796243-1 IEEE-488/Interrupt schematic diagram.

Address decoder U12 provides four 64 byte write address blocks and four 64 byte read address blocks. The third write block from U12 enables address decoder U11 which provides eight single address control lines. Writing address 1800 enables interrupt latch U16. Addresses 1800-18BF write the front panel control signals. The single byte address decoder U11 is enabled by writing addresses 1900-191F. Outputs of U11 are utilized as interrupt reset and start signals and LO clock signals. Writing 1903 creates a 407 µsec. negative going pulse utilized to strobe data into the 2nd LO divider logic. Writing 1906 creates a 407 µsec. negative going pulse utilized to strobe data into the 3rd Synthesizer divider logic. Writing 1907 creates a 407 µsec. negative going pulse utilized to start the BFO counter on the Synthesizer Interface subassembly.

Address decoder U5D decodes the read and write address from 19C0 to 19FF for the IEEE-488 interface integrated circuit, U13. U13 has eight internal registers which are selected by address lines A0 through A12. U13 provides IEEE-488 interface logic along with control of switch register U10 which is utilized for 488 address information. Integrated circuits U6 and U7 are 488 interface buffers utilized to obtain the proper drive characteristics for IEEE-488 standard operation. U13 is capable of generating interrupts via interrupt comparator U14.

The 1.2 kHz Q10 output of interrupt timer and frequency divider U1 provides an .833 msec. interrupt clock to the $\overline{IRQ}$ interrupt on the microprocessor subassembly via interrupt latch U4B. U4B is reset by writing address 1905 via U11. The .833 msec. clock signal drives the front panel refresh logic to update the front panel display. U1 generates a 3.33 msec. clock which generates an interrupt via interrupt latch U4A. U4A is reset by writing address 1900 via U11. The 3.33 msec clock signal indicates key closures when a front panel pushbutton is depressed.

Integrated circuit U2B, (BFO counter interrupt latch) generates a single counter up signal, 50 msec. after the start signal of the counter. U2B is reset by writing to address 1904 via U11. The keyboard available line from the front panel generates an interrupt on key closures via interrupt latch U2A. U2A is reset by writing to address 1902 via U11.

Input register U8A shows the following status when an output is enabled:

D7 indicates analog to digital conversion is complete.
D6 indicates tuning wheel quadrature signals.
D5 indicates tuning wheel movement and direction.
D4 indicates key available.

Tuning wheel inputs TW1 and TW2 utilize schmitt triggers U3A and U3B for input filtering and hysteresis. U8B is a spare input register which responds to reading address 1980 on data lines. D0 and D1. Switch register U9 is accessed by reading address 1900.

Integrated circuit U16 is a hardware interrupt mask register, with each of its six outputs allowing enabling/disabling of interrupt signals. U16 is accessed by writing 1800 on data lines D0 through D5. These data lines enable the following:

D0 enables the 3.33 msec. interrupt from U4.
D1 enables the SPR (spare) interrupt from U3E (SPR IN 1).
D2 enables the front panel keyboard interrupts from U2A.
D3 enables the 488 interrupts from U13.
D4 enables the BFO counter interrupts from U2B.
D5 enables the 833 msec. clock interrupts from U4B to the $\overline{FIRQ}$ line to the microcprocessor subassembly.

Interrupt comparator U14 compares interrupt mask register U16 with interrupt latches. Upon finding a logic "1" in both U16 and a latch for a given interrupt generates $\overline{IRQ}$ to the microprocessor subassembly.

Interrupt status register U15 allows the microprocessor to read the current interrupt latches. Data lines D0 through D7 are accessed by R1800 and indicate the following:

D0 indicates active 3.33 msec. interrupt from U4A.
D1 indicates active SPR (spare) interrupt from U3E.
D2 indicates active keyboard interrupt from U2A.

D3 indicates active 488 interrupt from U13.
D4 indicates active BFO counter interrupt from U2B.
D5 indicates active $\overline{\text{FIRQ}}$ interrupt from U4B.
D6 indicates active 1st LO lock from Analog/Digital subassembly.
D7 indicates active 2nd LO/3rd Synthesizer lock from Analog/Digital subassembly.

3.2.2.4 Type 796245-1 Synthesizer Interface (A1A5)

The reference designation for the Synthesizer Interface subassembly is (A1A5). Refer to **Figure 6-6** for the Type 796245-1 Synthesizer Interface schematic diagram.

Address decoder U4 provides eight 64 byte write address blocks selected via the I/O 2 control line from the microprocessor. Data latch U14 is enabled by writing to address 1A00. This latch contains the 100 MHz digit (in BCD form) for the 1st LO, on data lines D0 through D3 (2^1 through 2^8). Data line D4 is the 1st LO load signal. D5 and D6 are the UHF LO control lines (U^1 and U^2) and the UHF/$\overline{\text{VHF}}$ control line is D7. Data latch U13 is enabled by writing to address 1A40. This latch contains the 10 MHz digit (in BCD form) for the 1st LO, on data lines D4 through D7 (1^1 through 1^8). Data line D3 is the 7/$\overline{2}$ control line for the 1st LO. Data latch U12 is enabled by writing address 1A80. This latch controls the 2nd LO/3rd Synthesizer data/address bus and fine tune control. Data lines D0 through D3 form a 4 bit data bus to both LO's. D4, D5 and D6 form the LO address lines for the 2nd LO/3rd Synthesizer. D7 controls the 2nd LO fine tune off/on. Data latch U8 is enabled by writing address 1B40. This latch controls the optional Tracking Preselector subassembly. Data lines D0 and D1 form the address lines for the Tracking Preselector. D2, D3 and D4 form the preselector band code signals. D5 forms the preselector strobe control line. D6 forms the serial output line via TTL to 232 converter U10. D7 forms the printer out line via U10. Data latch U7 is enabled by writing address 1B80. This latch is also utilized for the optional Tracking Preselector subassembly. Data lines D0 through D7 form the frequency control lines. Data latch U6 is enabled by writing address 1BC0. This latch controls the demodulator and squelch circuitry of the receiver. D0 forms the $\overline{\text{FM}}$/AM control line which selects AM or FM detection mode. D1 enables CW, selects CW audio and gates the 21.4 MHz oscillator on the Reference Generator subassembly. D2 enables CW or SSB, selects SSB audio and gates the 10.7 MHz fixed and variable oscillators on the Reference Generator subassembly. D3 enables USB/$\overline{\text{LSB}}$ and selects the USB or LSB filter on the CW/ISB Demodulator subassembly along with the appropriate audio channel. D4 enables ISB and selects both upper and lower ISB and audio channels. D5 enables the squelch circuitry and disables the audio output. D6 is not used in the present configuration. D7 enables the AM peak dump control line which allows dumping of the AM peak detector onto the Audio/Video subassembly. Resistor pack R7 is the data bus pull-up.

Integrated circuits U5, U1, U3 and U9 form the BFO counter logic circuitry. Counter U5A provides a 50 msec. pulse, initiated by the counter start signal from the microprocessor. On time out, a counter done signal from U5A is applied to the 488 Interrupt subassembly. Schmitt triggers U1A and U1B make up the input conditioning circuitry for VBFO High/Low signals, from the phase comparator on the Reference Generator subassembly. U1C and U1D allow gating under the control of U5A of the difference frequency from the VBFO High/Low into 256 bit counter U3. U9 responds to R1A00 to read the number of counts in U3. Logic for U9 is provided via U5B.

DC-DC converter U15 provides 5 to 30 V for the optional Tracking Preselector subassembly when this option is installed in the receiver.

3.2.2.5 Type 796260-1 Front Panel Display (A1A1)

The reference designation for the Front Panel Display subassembly is (A1A1). Refer to **Figure 6-2** for the Type 796260-1 Front Panel Display schematic diagram.

The front panel logic contains hardware generated refresh logic. LED bar display U13 is the front panel tuning meter. Integrated circuits U1 through U5 and U8 through U11 are front panel indicators nomenclated on **Figure 6-2.** A 3 digit, seven segment LED (U6) is the signal strength indicator. A 2 digit, seven segment LED (U7) is the COR level indicator. U12 and U14, 4 digit, seven segment LED's provide the tuned frequency display. Integrated circuits U6, U7, U12 and U14 share a common cathode. The front panel display is mapped into a 16 x 8 matrix of multiplexed refreshed LED's. The switch bank is mapped into a 3 x 4 matrix of normally open, close on contact switches.

3.2.2.5.1 Part 380411-1 Display Driver (A1A1A1)

Data written by the microprocessor is hardware refreshed by this subassembly. A dual ported memory, U11 and U5 make up 16 bytes for the bit mapped display. The microprocessor accesses the memory by creating a "write front panel signal" on U3, pin 1 which maps address lines A0 through A3 which is applied to U5 and U11. A delayed write signal via R1, CR1 and C10 is applied to memories U11 and U5. Display data is stored in the 16 x 8 memory via the microprocessor.

When not interrupted by the microprocessor, the display creates a self refresh. Address counter U6 is mapped to the address lines of U11 and U5 via U3. These address lines are applied to 3 to 8 decoders, U1 and U2 for digit selection. The most significant address line of address counter U6 controls the access of either U1 or U2 depending on the state of the line. U1 is accessed when the line is high, U2 is accessed when the line is low. At each address that U6 cycles through, data is obtained from RAM's U11 and U5 and is applied to the source driver U12 as anode information. One of the outputs of U1 and U2 is enabled, selecting one of sixteen digits via current drivers U8 and U9. Duty cycle control for display intensity is maintained via U7A and U7B, which are one shots and are fired at the beginning of each display address. U4B and U10 become the switch matrix encoders upon a key closure. U10 sets the key available line to the microprocessor, along with a key code on outputs 20 through 23, making them available to the data bus via data bus buffer U4B, on data lines D0 through D3.

3.3 RF/IF SECTION

3.3.1 FUNCTIONAL DESCRIPTION

Refer to the RF/IF Section Functional Block Diagram (**Figure 3-2**) for the following function description.

The incoming 20 to 500 MHz RF signal enters the receiver via the ANTENNA input connector (J10) and is applied to the (A1A14) module. This module is either the Input Filter subassembly or the optional Tracking Preselector. Refer to the optional Tracking Preselector instruction manual for its description. Another available option in this signal path is the Frequency Extender. Refer to the optional Frequency Extender instruction manual for its description. This discussion deals with the Input Filter subassembly. This filter functions as a

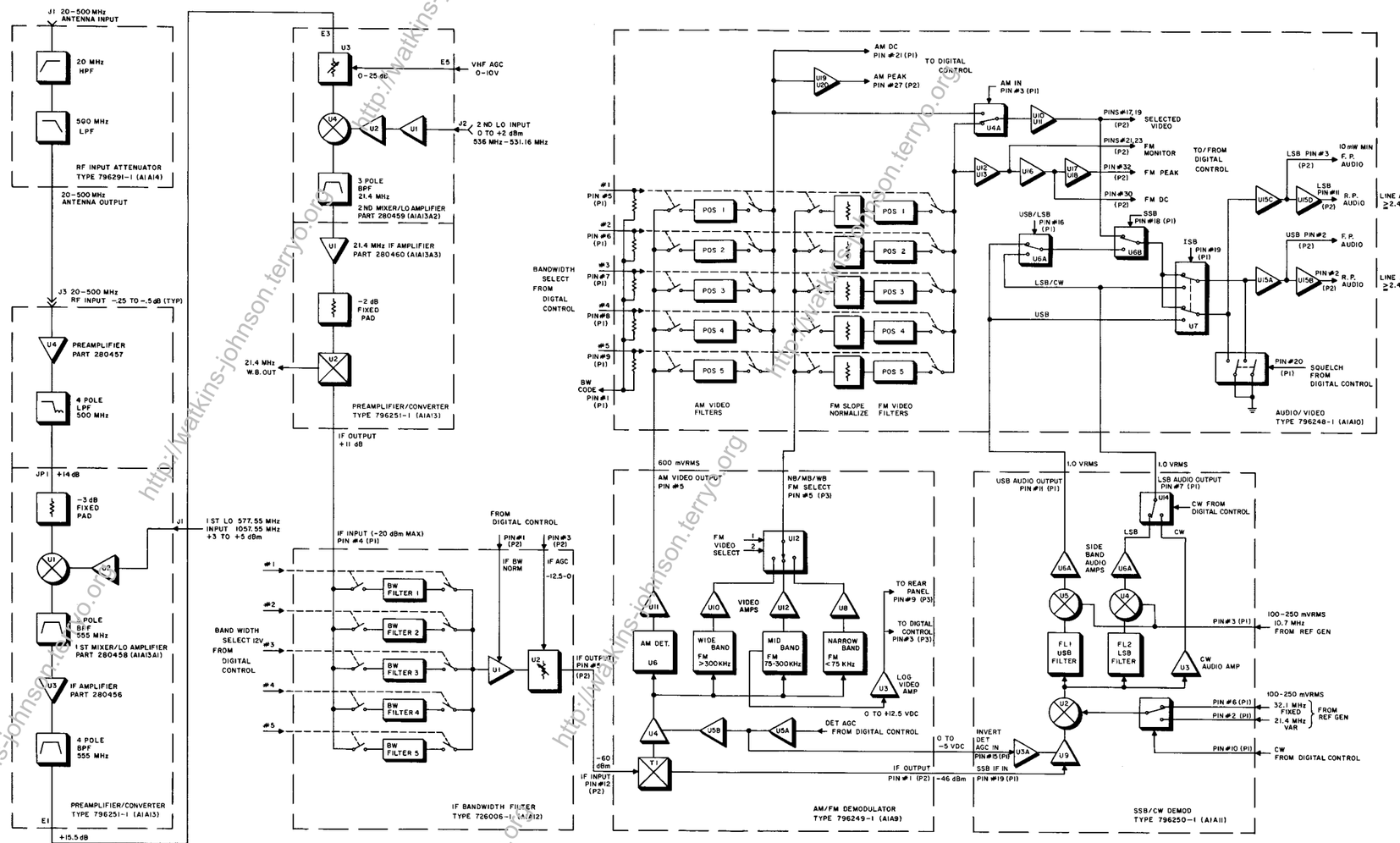


Figure 3-2. WJ-8615 RF/IF Section Functional Block Diagram 580243

wide bandpass filter, rejecting signals below 20 MHz and above 500 MHz. From this subassembly, the 20 to 500 MHz RF signal is applied to the Preamplifier/Converter subassembly (A1A13).

Amplification of the incoming RF signal and conversion to a fixed 21.4 MHz IF is the primary function of this subassembly. This subassembly is comprised of four sections: Preamplifier/Low pass filter, 1st Mixer/LO Amplifier, Gain Control and 2nd Mixer/LO Amplifier. Within the 1st Mixer/LO Amplifier, the RF signal is mixed with a 577.5501 to 1057.5501 MHz 1st LO signal from the Synthesizer Section. The LO frequency varies 5 MHz with a 10 kHz offset in 100 Hz steps. The output of the 1st mixer is a band of frequencies with center frequencies from 557.5501 to 552.5501 MHz. For example, when the receiver is tuned to 120.0000 or 125.0000, the IF output frequency is centered at 557.5501 MHz. When the receiver is tuned to 124.9999 or 129.9999, the IF output frequency is centered at 552.5501 MHz. The output is filtered and amplified restoring the signal level lost in the conversion process.

The output of the 1st Mixer/LO Amplifier is applied to the 2nd Mixer/LO Amplifier where the 557.5501 to 552.5501 MHz 1st IF is mixed with the 2nd LO signal from the Synthesizer Section, providing a 21.4 MHz 2nd IF. Gain control is also provided in this stage via the Digital Control Section. The 2nd LO signal varies from 531.1501 to 536.1501 MHz in 10 kHz steps, providing a 10 kHz tuning resolution. The 21.4 MHz IF signal is then amplified and applied to the IF BW Filter Amplifier subassembly (A1A12). Samples of the IF signal are also applied to the SM/IF OUTPUT connector J9 and to the SW IF OUTPUT connector J8 on the receiver rear panel. The 21.4 MHz IF output to the IF BW Filter subassembly is applied to the appropriate filter via switching signals provided by the Digital Control Section.

The IF OUTPUT of the selected IF BW Filter is applied to the AM/FM Demodulator subassembly (A1A9) where the IF signal is amplified linearily and logarithmically for video detection and signal strength representation. IF AGC is applied to the Analog/Digital subassembly (A1A4) in the Digital Control Section for AGC (automatic gain control) or MGC (manual gain control) operation. IF NORM is the normalized gain of the product of the bandwidth through the RF/IF signal path depending on the selected IF bandwidth, which is applied to the Digital Control Section.

AM/FM Demodulator subassembly (A1A9) amplifies the IF output of the IF BW Filter subassembly (A1A12) both linearly and logarithmically. Linear amplification of the 21.4 MHz IF is applied to the FM Demodulator circuitry for detection of FM video and to the AM Demodulator circuitry for detection of AM video. A logarithmic amplifier circuit provides a dc output voltage that varies logarithmically with the signal strength. This dc voltage is summed with a sample of the detected AM video providing an indication of the signal strength to the Digital Control Section. FM video is applied to the FM video filters on the Audio/Video subassembly (A1A10). Log video is applied to the Digital Control Section and to the auxiliary connector J13 on the rear panel representing the video signal from 0 to approximately 60 dB above the noise floor of the receiver. AGC from the Digital Control Section is applied to this subassembly for AGC (automatic gain control) or MGC (manual gain control) operation.

Detected FM video is amplified and applied to the FM MON connector (J4) on the receiver rear panel via the Audio/Video subassembly (A1A10). AM and FM video is applied to the appropriate video response modules according to the selected IF bandwidth via the Digital Control Section. Depending on the detection mode selected, the AM or FM video is amplified and applied to the SEL VIDEO connector (J5) on the receiver rear panel. The video signal is also applied to the audio circuitry where the signal is amplified and applied to the REAR PANEL AUDIO connectors (J6 and J7) and to the front panel PHONES jack (J12), under the control of the Digital Control Section. LOG video from the AM/FM Demodulator subassembly

(A1A9) and the COR level from the Digital Control Section are applied to this subassembly to activate the COR circuitry. When the LOG video level is greater than the COR reference level from the Digital Control Section, the COR circuitry is activated. This activates the audio outputs and provide a 100 mA current-sink via the COR connector (J3 on the receiver rear panel) to ground, activating external equipment.

3.3.2 DETAILED CIRCUIT DESCRIPTION

3.3.2.1 Type 796251-1 Preamplifier/Converter Assembly (A1A13)

The reference designation for the Preamplifier/Converter Assembly is (A1A13). Refer to **Figure 6-16** for the Type 796251-1 Preamplifier/Converter Assembly schematic diagram.

RF signals enter the Preamplifier/Converter subassembly via connector (A1A13J3) from the A1A4 module and are applied to the input of preamplifier/low pass filter (U4). The signal is amplified by U4, a low-noise, broad-band amplifier, which provides 15 dB of gain to RF signals from 20-500 MHz. The amplified output at U4 (pin 4) is applied to the low pass filter comprised of L10 through L14 and C15 through C18. This circuit has an insertion loss of .75 dB for frequencies below 500 MHz. This filter is an elliptic four-pole low pass filter that increases attenuation rapidly for frequencies above 500 MHz. This filter attenuates RF signals in close proximity to the receiver's 1st IF frequency, image frequencies and additionally rejects conducted LO signals from the 1st mixer (U1). Variable capacitors C15 through C18 provide a means of tuning the filter for the best response.

From the 500 MHz low pass filter, the RF signal is applied to the 1st Mixer/LO Amplifier subassembly (A1A13A1) via JP1. Bias for the RF signal attenuated approximately 30 dB via R1, R2 and R3 and the signal is applied to the RF port of mixer U1. The 577.5501 to 1057.5501 MHz LO is input from the Synthesizer Section at the 1st LO IN (A1A13J1) and is applied to broad-band amplifier U2. U2 provides +12 dB of gain, increasing the LO signal level to +15 dBm at the LO port of mixer U1. Double-balanced mixer U1 combines the RF signal with the 577.5501 to 1057.5501 MHz LO signal providing a difference frequency of from 552.5501 to 557.5501 MHz which is within the 1st IF of the receiver. This difference frequency is selected via the bandpass filter comprised of L3, L4 and L5, and C3, C4 and C5, at the mixer output. The signal enters the filter via a matching network comprised of L2, C24, L19 and the tap in inductor L3, which matches the filter impedance to 50 ohms, the nominal output impedance of mixer, U1. This filter is a three-pole bandpass filter with an insertion loss of approximately 2 dB. The bandwidth of this filter is 25 MHz centered at 555.5 MHz. Variable capacitors, C3, C4 and C5 provide a means of tuning each filter pole for the best overall response and capacitors C10 and C11 provide coupling between the poles. The filter output from the tap in inductor L5 and matching element L17 transfers the filter output to 50 ohms prior to the signal being applied to IF amplifier U3.

U3 is a broad-band amplifier providing 15 dB of gain to the IF Frequency centered at 555.5 MHz. It compensates for the conversion loss in the mixer and the loss in each of the bandpass filter networks. The output of amplifier U3 is applied to a four-pole bandpass filter via L18. This bandpass filter is comprised of L6 through L9, C6 through C9, and C12 through C14. Matching component L18 and the tap in L6 establish the 50 ohm input impedance which is the characteristic output impedance of IF amplifier U3. This filter is a four-pole bandpass filter with an approximate 20 MHz bandwidth centered at 555.5 MHz. Variable capacitors C6

through C9 provide a means of tuning each filter pole for the best overall response and capacitors C12 through C14 provide coupling between the poles. This filter output is applied via the tap in inductor L9 and C1 to match the output impedance of the filter with the input of PIN diode attenuator A2U3.

3.3.2.1.1 Part 280459-1 2nd Mixer/LO Amplifier (A1A13A2)

Part 280459-1 2nd Mixer/LO Amplifier receives the 17 MHz wide frequency spectrum from the 1st Mixer/LO Amplifier and applies it to the PIN diode attenuator (U3) which is utilized to control the module gain. It provides approximately 3 dB of fixed loss when the AGC voltage from the Digital Control Section is maximum (12.5 Vdc). When AGC voltage is minimum, attenuation provided by U3 increases to 28 dB. From U3, the signal is applied to the R port of double-balanced mixer U4. U4 has an insertion loss of approximately 6 dB.

The 2nd LO signal from the Synthesizer Section enters this subassembly via connector J2 and is amplified by broad-band amplifiers U1 and U2. Signal level of the 2nd LO at J2 is approximately 3 dB and is increased to 17 dB by U1 and U2. It is applied to the L port of U4. The R port and L port signals are combined in mixer U4 providing a difference frequency of 21.4 MHz. This 21.4 MHz difference frequency from U4 is applied to the bandpass filter comprised of L3, L4 and L5 and C9 through C13. Bandpass of this filter is 8 MHz and the 1 dB bandwidth is 6 MHz. Insertion loss is .75 dB. R3 and C8 on the output of U4 terminate the undesired mixing products, falling at frequencies higher than 21.4 MHz. Output of the bandpass filter is applied to a three-pole low pass filter comprised of C14 through C21 and L1. The 100 MHz center frequency of this filter attenuates any remaining 2nd LO harmonics before the 21.4 MHz IF signal is applied to the 21.4 MHz IF Amplifier (A1A13A3).

3.3.2.1.2 Part 280460-1 21.4 MHz IF Amplifier (1A13A3)

The 21.4 MHz IF output from C23 on the 2nd Mixer/LO Amplifier subassembly (A1A13A2) is applied to the 21.4 MHz IF Amplifier subassembly (A1A13A3). Broad-band amplifier U1 amplifies the IF signal by 18 dB and applies it to resistor network R4, R5 and R6. This network attenuates the IF signal by 2 dB before being applied to power divider U2. U2 divides the signal between the two output ports. The WB IF/SM OUT is applied to the rear panel connector J9 and the 21.4 MHz IF OUT is applied to the IF BW Filter subassembly (A1A12). The insertion loss of power divider U2 is approximately 3.75 dB.

Also contained within this module is the AGC circuitry. This circuitry consists of R1, R2 and R3, CR1 and CR2 which shapes the AGC control voltage from the Digital Control Section to contour this voltage before it is applied to the PIN diode attenuator U3 on the 2nd Mixer/LO Amplifier subassembly (A1A13A2). The overall gain of the Preamplifier/Converter subassembly (A1A13) is 17 dB.

3.3.2.2 Type 726006-1 IF BW Filter Amplifier (A1A12)

The reference designation for the IF BW Filter Amplifier subassembly is (A1A12). Refer to **Figure 6-15** for the Type 726006-1 IF BW Filter Amplifier schematic diagram.

The 21.4 MHz IF input is applied to the IF BW Filter Amplifier subassembly at connector pin 4 from the Preamplifier/Converter subassembly (A1A13). The maximum signal

level is -20 dBm, which is applied to the primary of T1. This transformer provides an impedance match between the Preamplifier/Converter subassembly and the crystal filters FL1 through FL5. Since the operation of the five IF BW filters is similar, only one will be discussed in detail. Filter FL1 band limits the 21.4 MHz IF signal to the stated bandwidth via the Digital Control Section (see **Table 3-1**) and applies the band limited signal via the voltage divider comprised of C13, CR11 and CR12 to the wideband amplifier (U1).

U1 applies the amplified IF signal for the selected bandwidth to attenuator U2. U2 provides 36 dB of attenuation before the 21.4 MHz IF is applied to connector pin 5 via C33. Transistor Q1 and its associated circuitry applies +6 Vdc to amplifier U1.

IF NORM (connector pin 1) connects to the Analog/Digital subassembly (A1A4) of the Digital Control Section to monitor the gain of the IF strip. The level of this signal increases as the bandwidth selection narrows. Bandwidth selection occurs in the Digital Control Section and is applied to connector pins 3, 5, 7, 9 and 11. IF AGC (connector pin 3) varies the level of the IF output according to the signal strength of the received signal.

Table 3-1. Available IF Bandwidths

	Bandwidth (kHz)	Bandwidth Code (Decimal) Min.	Center	Max.	A-D Volts	A1A10AX R1 Value (kΩ)	Relative IF Gain (dB)
Narrowband Discriminator	3.2	20	26	2C	.741	162	0
	6	2D	33	39	.992	121	0
	10	3A	40	46	1.259	95.3	0
	15	47	4C	52	1.489	80.6	-2
	20	53	5A	5F	1.762	68.1	-3
	50	6D	73	79	2.239	53.6	-7
Midband Discriminator	50	7A	81	87	2.526	47.5	-7
	75	88	8E	93	2.778	43.2	-8.8
	100	94	99	9E	2.985	40.2	-10
	250	9F	A4	AB	3.209	37.4	-14
	300	AD	B4	B9	3.529	34.0	-14.7
Wideband Discriminator	500	BA	BE	C4	3.704	32.4	-17
	1000	C5	CC	D2	3.987	30.1	-20
	2000	D3	DB	E0	4.286	28.0	-23
	4000	E1	E6	EB	4.494	26.7	-26

3.3.2.3 Type 796250-2 CW Demodulator/Switched IF (A1A11)

The reference designation for the CW Demodulator subassembly is (A1A11). Refer to **Figure 6-14** for the Type 796250-2 CW Demodulator/Switched IF schematic diagram.

The 21.4 MHz IF is applied to impedance matching transformer T1 via connector pin 19. From T1 the matched 21.4 MHz IF signal is applied to the balanced modulator/demodulator (U1) via amplifier U2 and impedance matching transformer T2.

AGC input from the D/A converter subassembly is applied to operational amplifier U3A via connector pin 15 at a level from 0 to approximately +12 Vdc. Gain control voltage of from 0 to 6 Vdc is applied from the output of U3A to RF/IF video amplifier U2.

U1, a balanced modulator/demodulator, produces an output voltage of up to +8 Vdc which is proportional to the 21.4 MHz IF signal (pin 1) and the 21.4 MHz VBFO signal (pin 10). Pin 12 provides the 21.4 MHz signal to the audio amplifier U3A and pin 6 provides the 21.4 MHz signal to audio amplifier U3B. Gain of U1 is adjustable via potentiometer R2. CW audio is applied from U3B to connector pin 12.

From the secondary tap of transformer T2 (pin 1), the 21.4 MHz IF signal is applied to the narrow-band/wideband filter circuitry. A TTL level "high", applied to connector pin 23 (SW IF OUT SELECT) is applied to U4, enabling the narrow band circuitry comprised of C16 through C22, L3, L4, R34 and R35. The narrow band circuitry is a 500 kHz band pass filter which provides this signal to connector J1 via current amplifier U6 and to the receiver rear panel connector SW IF OUT J8. A TTL level "low" applied to connector pin 23 enables the wideband circuitry via U4. This circuitry comprised of C23, C24, CR4, CR5, L5, L6, R38 and R39 is a wideband filter passing signals above 500 kHz to connector J1 via current amplifier U6 and to receiver rear panel connector SW IF OUT J8. Gain of current amplifier U6 is variable utilizing potentiometer R38.

Analog switch U5 is utilized to disconnect the CW audio from the receiver when CW is not selected. CW AUDIO OUT (connector pin 12 of connector P1) is externally applied to CW IN (connector pin 12 of connector P2) via the motherboard. When a TTL "high" from the Digital Control Section is applied to connector pin 18, U5 is enabled and the CW signal is applied at connector pin 14.

3.3.2.4 Type 796250-1 ISB/CW Demodulator (A1A11) (Optional)

The reference designation prefix for this optional ISB/CW Demodulator subassembly is (A1A11). Refer to **Figure 6-14** for the optional Type 796250-1 ISB/CW Demodulator schematic diagram.

This subassembly is similar to the Type 796250-2 CW Demodulator/Switched IF subassembly. The difference is the inclusion of the sideband circuitry discussed in the following paragraphs. Refer to **paragraph 3.3.2.3** for a discussion of the CW Demodulator circuitry.

The positive output of balanced modulator/demodulator U2 is applied to LSB BF filter FL1. The output signal of FL1 is 10.6977 MHz which is applied to balanced modulator/demodulator U4 via impedance matching transformer T1. 10.7 MHz from the Reference Generator subassembly is applied to U4 pin 10 via connector pin 3. The output of U4 is applied to audio amplifier U6B and also is applied to connector pin 7 as the LSB AUDIO OUTPUT. Potentiometer R34 provides gain control of the LSB audio signal level.

The negative output of balanced modulator/demodulator U2 is applied to USB BF filter FL2. The output signal of FL2 is 10.7023 MHz which is applied to balanced modulator/demodulator U5 via impedance matching transformer T2. 10.7 MHz from the Reference Generator subssembly is applied to U5 pin 10 via connector pin 3. The output of U5 is applied to audio amplifier U6A and also is applied to connector pin 11 as the USB AUDIO OUTPUT. Potentiometer R47 provides gain control of the USB audio signal level.

3.3.2.5 Type 796248-1 Audio/Video (A1A10)

The reference designation for the Audio/Video subassembly is A1A10. Refer to **Figure 6-12** for the Type 796248-1 Audio/Video schematic diagram.

FM video from the AM/FM Demodulator subassembly (A1A9) enters this subassembly at connector pin 4 and is applied to the five position BW/Video Response module. Normalized FM Video, which is the limited DC offset voltage from the FM Discriminators has a bandwidth of approximately 1/2 of the selected bandwidth. This signal is applied to the FM Video amplifier circuitry comprised of amplifier U9 and R12 through R15, C5 and C6. A sample of this signal is taken from current amplifier U8 and applied to the receiver rear panel via connector pin 23. The DC amplitude of the FM video signal is applied to the Digital Control Section at connector pin 30 via operational amplifier U15. A sample of this DC amplitude is applied to amplifier U10 and to the bridge rectifier (CR1 through CR4) removing any AC component. This signal is applied to the Digital Control Section at connector pin 32 via amplifier U11. The FM peak value is a dc level, proportional to the frequency deviation of the FM signal level applied to the receiver rear panel.

AM video from the AM/FM Demodulator subassembly (A1A9) enters this subassembly at connector pin 21 and is applied to the five position BW/Video Response module. Normalized AM Video, which is the limited DC offset voltage from the AM Discriminators has a bandwidth of approximately 1/2 of the selected bandwidth. This signal is applied to amplifier U12 which amplifies the dc signal and applies it to the bridge rectifier comprised of CR5 through CR8. This bridge rectifier removes any AC component before the signal is applied to the Digital Control Section at connector pin 34 via amplifier U13. The AM peak value is a dc level proportional to the AM signal strength.

AM/$\overline{\text{FM}}$ select line enables U4, which switches between normalized FM (TTL "low") and AM video (TTL "high"). In the AM video position (TTL "high") the AM video signal is applied to the AM Video amplifier circuitry comprised of amplifier U5, R7 and R8. The AM video signal is applied at the SELECTED VIDEO OUT (connector pins 17 and 19) via amplifier U6 and resistors R1 and R2. A sample of the AM video signal is applied to analog switch U1. Analog switches U1 and U2 are enabled by the Digital Control Section and select between AM, FM, SSB and CW, determining which audio signals are to be applied to the audio amplifier circuitry.

Audio signals are applied to amplifiers U7A and U7B via analog switch U3. U7B applies the audio signal to the left portion of the front panel audio. A sample of this audio signal is applied to the LEFT AUDIO OUT (connector pin 7) via amplifier U7D. Potentiometer R32 establishes the gain of this portion of the audio signal path. U7A applies the audio signal to the right portion of the front panel audio. A sample of this audio signal is applied to the RIGHT AUDIO OUT (connector pin 11) via amplifier U7C. Potentiometer R28 establishes the gain of this portion of the audio signal path. The overall signal response of the audio section is 700 Hz to 7 kHz at a level adjustable to 10 mW.

3.3.2.6 Type 796249-1 AM/FM Demodulator (A1A9)

The reference designation for the AM/FM Demodulator subassemby is (A1A9). Refer to **Figure 6-11** for the Type 796249-1 AM/FM Demodulator schematic diagram.

IF input signals from the IF BW Filter Amplifier subassembly (A1A12) are applied to connector pin 12, IF INPUT. The IF signal is applied to wideband amplifier U4 via C14. A sample of the amplified IF is applied to connector pin 1 via power splitter transformer T1. Transformer T4 is another power splitter that provides the IF signal to quadrature detector U1. Gain equalization is accomplished utilizing potentiometer R3. The detector output of U1 is applied to a tank circuit comprised of R1, L15, L3, C6 and C8. This tuned circuit establishes the medium band discriminator with a band break point of 75 kHz. Narrow band video is applied to operational amplifier U2 and to the analog switch U12 which applies the medium band IF signal to connector pin 4. Analog switch U12 is enabled by the Digital Control Section via connector pins 5 and 6. Potentiometer R2 provides the narrow band IF video gain adjustment. A logarighmic video sample is applied to operational amplifier U3 from quadrature detector U1. This signal is applied to connector pin 3 as the LOG VIDEO. It is a dc output voltage proportional to the log of the input signal. Potentiometer R24 provides the LOG VIDEO gain adjust.

A sample of the IF signal is applied to quadrature detector U7 via transformer T4. The tuned circuit comprised of Y1, L9 and L10 forms the narrow band portion of the AM/FM Demodulator. This filtered signal is applied to pin 5 of analog switch U12, via operational amplifier U8. The output level is adjustable via potentiometer R6. DC decoupling for the midband section is accomplished utilizing the circuit comprised of C33, C34, C19 through C21, R35 and R36 via the stabilizer output (pin 14) of video IF amplifier/demodulator U6. Supply voltage for U6 is applied to pin 13 from the narrow band section.

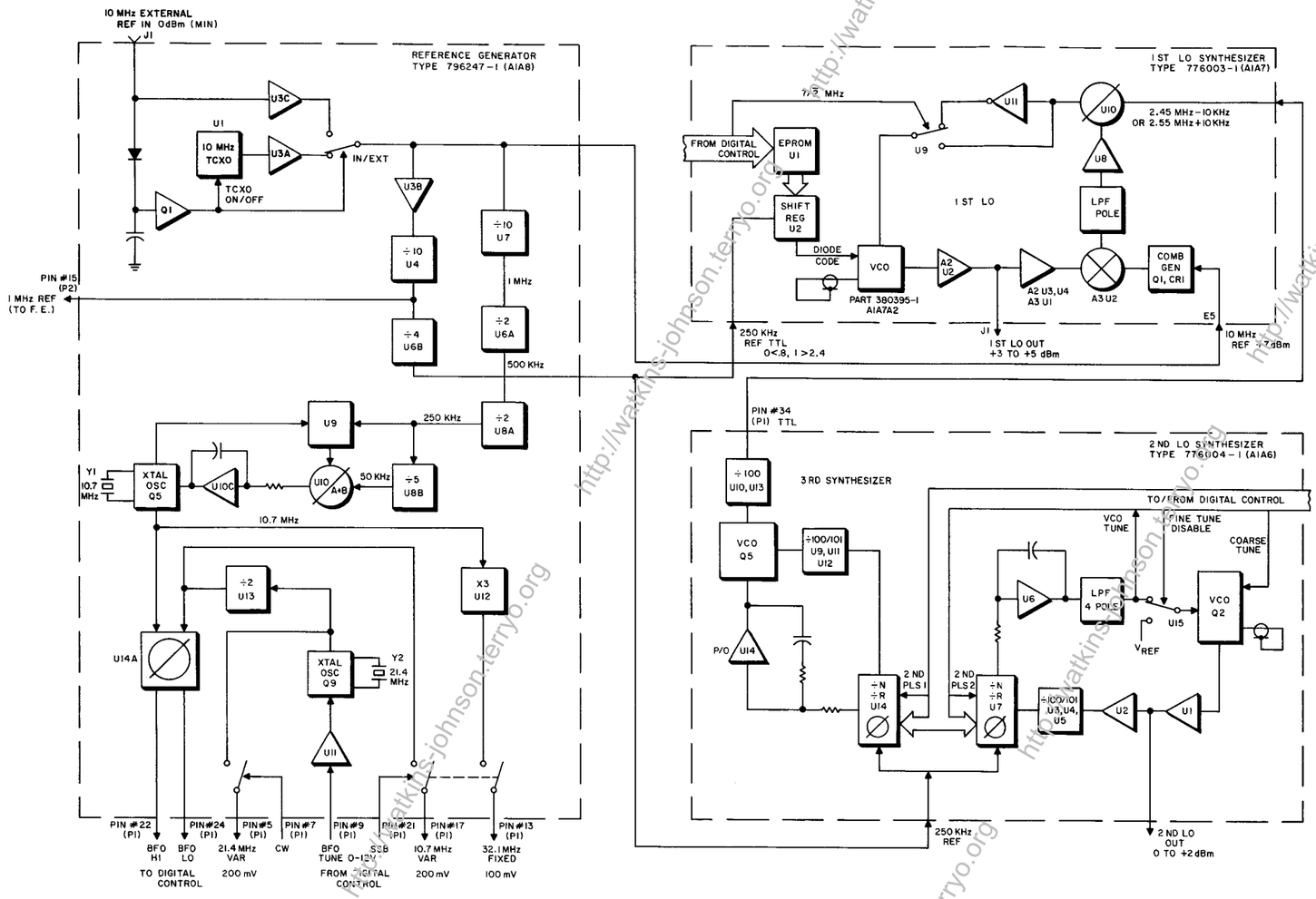
IF signals from video IF amplifier/demodulator U6 are filtered via L8, C27 and R39 before being applied to the wideband circuitry. The wideband circuitry is enabled by the Digital Control Section via analog switch U13. IF amplifier U9 applies the IF signal to the Foster-Seely discriminator L14, C48 and R55 via transformer T6. The wideband IF signal is amplified by video amplifier U10 and applied to pin 13 of analog switch U12.

3.4 SYNTHESIZER SECTION

3.4.1 FUNCTIONAL DESCRIPTION

The subassemblies that comprise the Synthesizer Section are illustrated in the Synthesizer Section Functional Block Diagram, **Figure 3-3**. Refer to **Figure 3-4** for the following functional description.

The Reference Generator (A1A8) provides the 250 kHz, 32.1 MHz, 21.4 MHz and 10.7 MHz reference signals required by the Synthesizer Section to produce the required output signals. This subassembly contains a 10 MHz temperature-compensated crystal oscillator (TCXO) which functions as the main time base of the receiver. A series of frequency dividers then divide this frequency producing the 250 kHz reference signals 32.1 MHz, 21.4 MHz and 10.7 MHz are also produced utilizing the 10 MHz TCXO as the time base. In this configuration, all of the reference signals are phase-locked to the same time base.



SYNTHESIZER TUNING SCHEME			
CARRIER FREQ.	1 ST LO	2 ND LO	3 RD LO
20.0000 – 24.9999 MHz	577.5500 – 577.5599 MHz	536.1500 – 531.1600 MHz	2.4500 – 2.4401 MHz
25.0000 – 29.9999 MHz	582.5500 – 582.5599 MHz	536.1500 – 531.1600 MHz	2.5500 – 2.5599 MHz

Figure 3-3. WJ-8615 Synthesizer Section Functional Block Diagram 480503

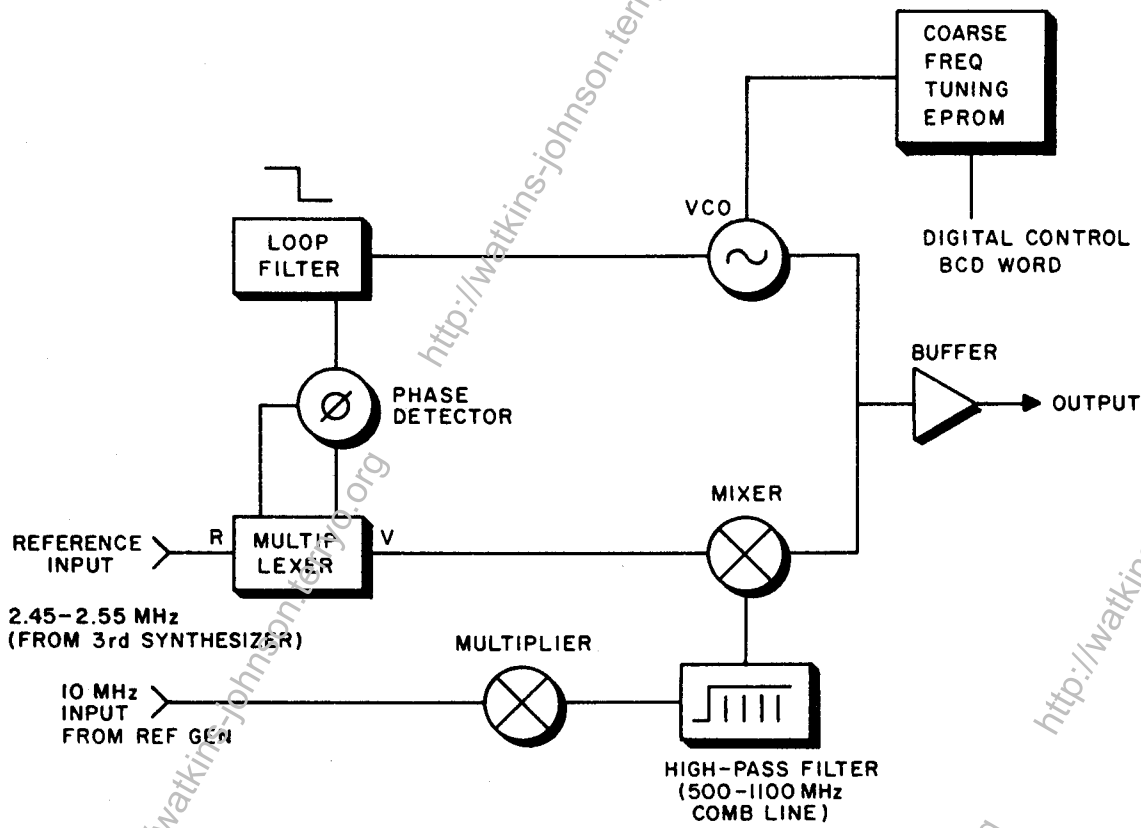


Figure 3-4. 1st LO Synthesizer Simplified Block Diagram

A connection from the Reference Generator subassembly to the rear panel of the receiver (J2) accepts a 10 MHz external reference when it is desired to reference the receiver from an external time base. The external 10 MHz reference signal, at a level of from 0 to +20 dB, then provides the time base for the receiver. Switching from internal reference to external reference is automatically transferred when the external signal level reaches 0 dB.

The 2.45 to 2.55 MHz 3rd Synthesizer loop frequency is applied to the 1st LO Synthesizer (A1A7). This input provides the reference utilized by the 1st LO Synthesizer phase-locked-loop circuitry producing the 1st LO output. The 1st LO Synthesizer is comprised of an EPROM, a shift register, a voltage controlled oscillator (VCO), a phase detector and a loop filter. From the Digital Control Section, coarse frequency information in the form of a BCD word is applied as the EPROM address. The addressed location EPROM then provides the appropriate tuning words via the shift register to update the diode code for the VCO. Refer to **Figure 3-4.**

The 3rd Synthesizer loop frequency is applied to the 1st LO Synthesizer (A1A7). This input provides the reference utilized by the 1st LO Synthesizer phase-locked-loop circuitry to produce the 1st LO output. This output frequency to the 1st LO Synthesizer provides the 100 Hz fine tune resolution. Two frequency bands are provided depending on the 5 MHz steps of the 1st LO. These bands are 2.55 to 2.56 MHz and 2.44 to 2.45 MHz.

The 10 MHz reference from the Reference Generator is applied to the comb generator via a multiplier. This provides the 500 to 1100 MHz comb line high-pass filter, frequency spaced 10 MHz apart. A sample of the VCO is mixed with the comb line and the resulting signal is phase locked to the 2.45 to 2.55 MHz 3rd Synthesizer loop. The 3rd Synthesizer signal is obtained via a 3-pole low pass filter and a multiplexer. This signal is then applied to the phase detector where a resulting error voltage is applied to the loop filter. This voltage is then applied to a varactor diode in the VCO to tune and lock the VCO onto the desired frequency. A difference between the VCO signal and the reference from the 3rd Synthesizer causes the phase detector to generate a tuning voltage to increase or decrease the VCO frequency. When the two signals are equal, the VCO is locked onto the new frequency. The 1st LO Synthesizer tunes in 5 MHz steps with 10 kHz deviation from nominal frequency in 10 Hz steps.

Integrated circuit, U7 contains a phase detector, ÷ N counter and a reference divider which is the heart of the 2nd LO Synthesizer. Refer to **Figure 3-5**. A signal in digital form from the Digital Control Section sets U7 to divide the 250 kHz reference from the Reference Generator to 10 kHz. A dual modulus prescaler and a sample of the VCO provide the 531 to 536 MHz 2nd LO output to the Preamplifier/Converter assembly in the RF/IF Section. Tuning resolution of the 2nd LO Synthesizer is 10 kHz.

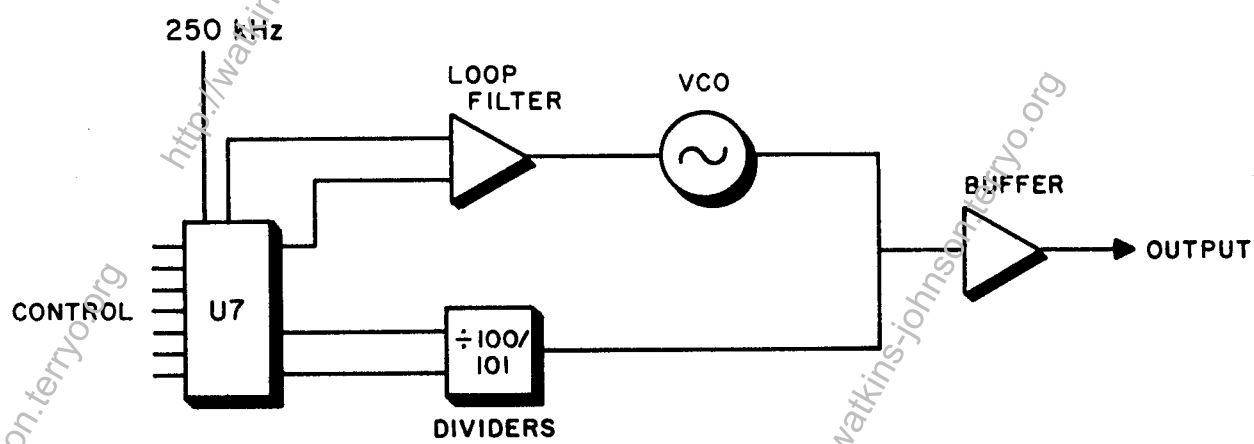


Figure 3-5. 2nd LO Synthesizer, Simplified Block Diagram

Integrated circuit U14 is the same as U7 in the 2nd LO Synthesizer, as it is the heart of the 3rd Synthesizer. The 250 kHz reference from the Reference Generator is applied to U14 and a signal in digital form from the Digital Control Section sets U14 to divide this reference down to 10 kHz. The VCO is set at 244 to 256 MHz and the output of this assembly is divided down by a factor of 10 two times yielding the 2.44 to 2.56 3rd Synthesizer output. Refer to **Figure 3-6.**

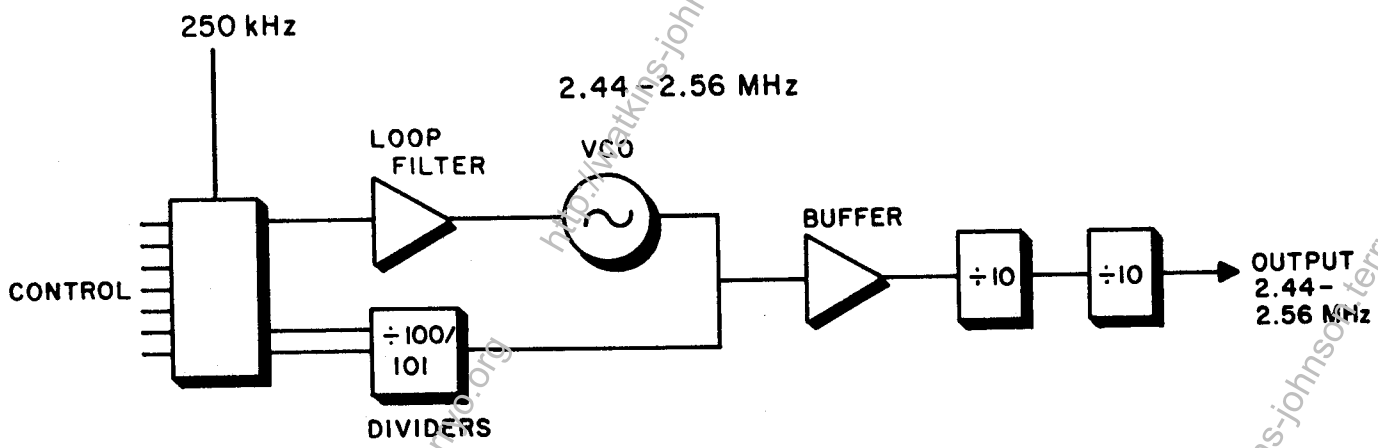


Figure 3-6. 3rd Synthesizer, Simplified Block Diagram