INSTRUCTION MANUAL
FOR
TYPES DRO-309A, DRO-302B, DRO-315, AND DRO-333
FREQUENCY COUNTERS

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700 QUINCE ORCHARD ROAD
GAITHERSBURG, MARYLAND 20760

PI/400/11/10/73/DR

WARNING

The equipment employs voltages which are dangerous and may be fatal if contacted. Extreme caution should be exercised in working with the equipment to avoid contact with primary ac power wiring.

ADDENDA

DRO-309A, DRO-302B, DRO-315 And DRO-333

The following changes should be incorporated into the Instruction Manual for the DRO-309A, DRO-302B, DRO-315 and DRO-333 Frequency Counters.

1. Section IV - Maintenance

   A. Paragraph 4.6.5.2.2 Adjustment Operations; Page 4-19

      1. In step (3) change ±1.65 V dc to: +1.65 V dc.

2. Section V - Replacement Parts List

   A. Paragraph 5.4.4 Type 76192 Switching Regulator (A2)

      1. Change C6 from: 27 μF; Part Number 196D276X9035MA3 to: 100 μF, Part Number 196D107X0020MA3. (Page 5-23)

      2. Change CR3 from: Part Number UTR3305 to: Part Number UTX4105 Mfr. Code: 12969. (Page 5-23)

      3. Change R3 from: 68 Ω; Part Number RCR07G680JS to: 47 Ω; Part Number RCR07G470JS. (Page 5-23)

3. Section VI - Schematic Diagrams

   A. Figure 6-6; Page 6-13; Type 76192 Switching Regulator (A2)

      1. Change C6 from: 27 μF, to: 100 μF.

      2. Change CR3 from: UTR3305 to: UTX4105.

      3. Change R3 from: 68 Ω to: 47 Ω.

ADDENDA
DRO-309A, DRO-302B, DRO-315, and DRO-333

The following changes should be incorporated into the Instruction Manual for the DRO-309A, DRO-302B, DRO-315, and DRO-333 Counters.

1. Section V - Replacement Parts List

   A. Paragraph 5.4.3.3; Part 16462 325 MHz ECL, Divide by 2, 4, or 8.

      1) Change R25 from: Same as R1 to: RESISTOR, FIXED, COMPOSITION: 510 Ω, 5%, 1/8W; Qty. 1; Part No. RCR05G511JS; Mfr. Code 81349. (Page 5-22)

      2) Change R26 from: RESISTOR, FIXED, COMPOSITION: 510 Ω, 5%, 1/8W; Qty. 1; Part No. RCR05G511JS; Mfr. Code 81349 to: Same as R1. (Page 5-22)

   B. Paragraph 5.4.5; Type 79907 Gate Generator and DAFC.

      1) Change Mfr. Code on Q4 (3N139) from: 80131 to: 07263 (Fairchild). (Page 5-26)

2. Section VI - Schematic Diagrams

   A. Figure 6-5; Part 16462 325 MHz Binary Divider (A1A3).

      1) Change R25 from: 100 Ω to: 510 Ω. (Page 6-13)

      2) Change R26 from: 510 Ω to: 100 Ω. (Page 6-13)

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Table 1-1. Type DRO-309A Series Frequency Counters, Specifications

Readout Frequency Range ..... 0.1 MHz to 1000 MHz in four ranges

Range Dependent Characteristics:

Nominal Readout Freq. Range (with Internal Preset)	Input Freq. Range	Input Level	BCD & DAFC	Display	Resolution
0.1-50 MHz (1)	0.1-70 MHz	250 mV rms to 1V rms (2)	80 Hz	16 Hz	±100 Hz
20-300 MHz	20-321.4 MHz	50 mV rms to 500 mV rms	100 Hz	20 Hz	±1 kHz
200-500 MHz	295-560 MHz	50 mV rms to 500 mV rms	50 Hz	10 Hz	±1 kHz
490-1000 MHz (3)	550-1060 MHz	50 mV rms to 500 mV rms	50 Hz	10 Hz	±1 kHz

NOTES: (1) With no preset; preset optional on this range.
(2) 100 mV rms to 1V rms from 0.5 rms to 50 MHz.
(3) Applies only to DRO-309A and DRO-333.

Readout Accuracy ..... Resolution, ±1PPM, 0°-50°C

Display Type ..... Six digit decimal display by shaped dot arrays of light emitting diodes

Input Impedance ..... 50 ohms, nominal

Input Connectors ..... Three, all BNC:
DIRECT 0.1-50 MHz
VHF LO (VHF/UHF)
UHF LO
(Inputs may be configured for common or separate VHF/UHF connectors by internal cabling options.)

BCD Output Characteristics:

Outputs ..... 24 lines of data; one inhibit line; one storage pulse line; two power supply lines for external readout.

Code ..... 1248 positive true logic

Data Voltages ..... 1 $\geq$ 2.4V and 0 $\leq$ 0.4V (with 1/2 standard TTL unit load).

Inhibit Command ..... Contact closure between control lines or sink inhibit lines to $\leq$ 0.4V.

Storage Pulse ..... Negative going pulse from DTL logic, positive transistion indicates new count ready.

Power Supply Voltages ..... +5V nominal at 300 mA maximum, and -5V nominal at 20 mA maximum.

DAFC Characteristics:

Digits Locked ..... Least significant digit, second digit, one BCD bit from third digit

Lock Recovery Range ..... At least ±99 counts of two least significant digits

Correction Rates ..... Two, selected by front panel switch; each rate has automatic rapid/delayed speed for large/small errors.

Table 1-1. Type DRO-309A Series Frequency Counters, Specifications (Continued)

Output Voltage	Two modes, selected by rear panel switch; Mode 1: +8V off, nominal, with a range of +5 to +15V, positive frequency/volts slope; for use primarily with tube type receiver LO. Mode 2: Zero volts off, nominal with a range of +2.5 to -3.0V, negative frequency/volts slope; for use primarily with solid-state receiver LO.
Output Impedance	2.0 ±0.5 kilohms
Stability	Holds receiver to lock frequency ±1 count of least significant digit.
Meter	Indicates direction and magnitude of DAFC frequency correction.
Preset Modes	Three modes, selected by rear panel switch; Internal: Two preset numbers for use with VHF receiver with 21.4 MHz IF or UHF receiver with 60 MHz first IF; automatically selected with range. External: Same as internal, plus two preset numbers for use with 8.0 MHz and 10.0 MHz IF (not for 0.1-50 MHz range); one customer option preset which may be substituted for one of the preceeding; preset defeat function Off: Allows unit to be used as conventional test counter.
External Range/Preset Control:	
Functions Selected	Any of the four frequency ranges; any of the four external presets; preset defeat
Selection Command	Contact closure between control lines or sink selector line to $\leq$ 0.2V.
Front Panel Controls and Indicators	POWER toggle switch, RANGE rotary switch, DAFC rotary switch, six digit numerical display, TUNING CORRECTION meter.
Input Power	115/230 Vac, 50-400 Hz
Power Consumption	13 watts, approximately
Dimensions:	
DRO-309A and DRO-302B	7.9 inches wide, 3.25 inches high, and 15.7 inches deep
DRO-333 and DRO-315	19.00 inches wide, 1.75 inches high, and 18.97 inches long
Weight:	
DRO-309A and DRO-302B	8.8 lbs., approximately
DRO-333 and DRO-315	12.5 lbs., approximately

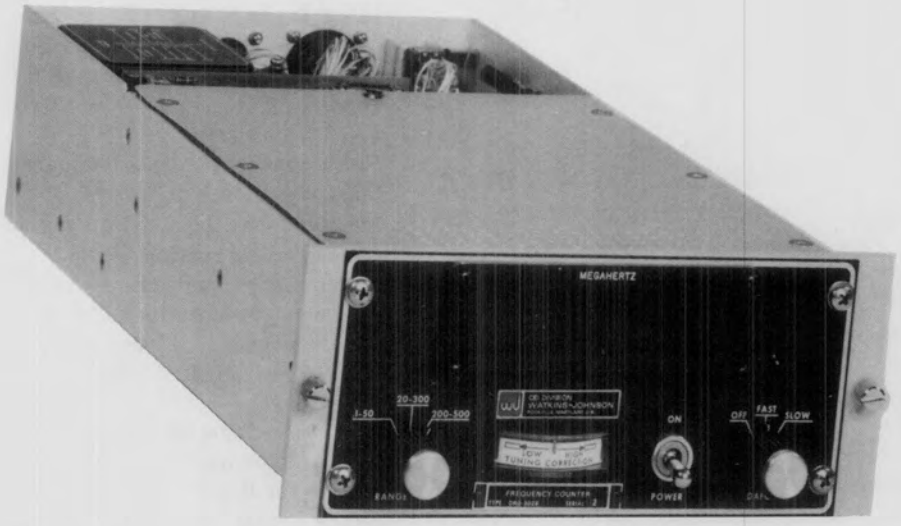


Figure 1-1. Type DRO-302B Frequency Counter, Front View

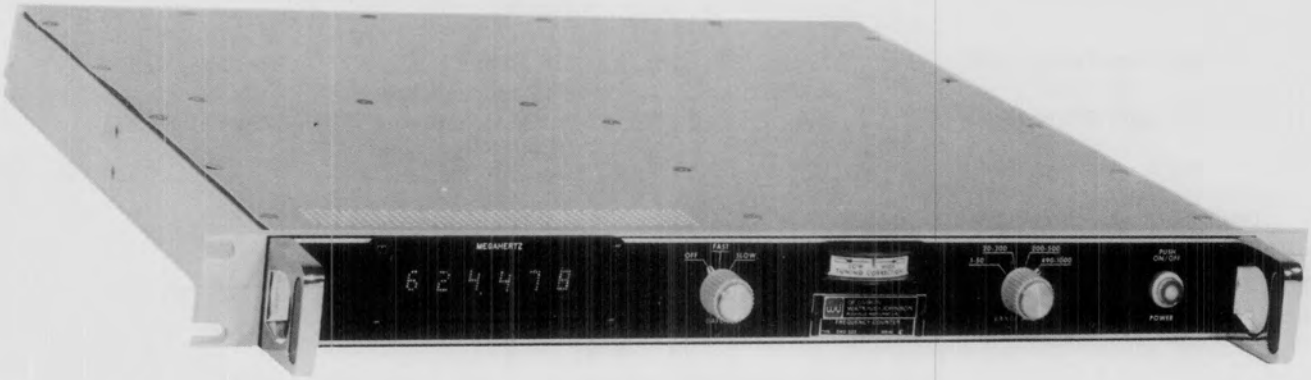


Figure 1-2. Type DRO-333 Frequency Counter, Front View

SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

1.1.1 Due to the great similarity between the Type DRO-309A Frequency Counter and the Types DRO-302B, DRO-333, and the DRO-315 Frequency Counters, they can be referred to as the DRO-309A Series as a group.

1.1.2 The Type DRO-309A Series Frequency Counter serves as an accessory to an HF, VHF, or UHF receiver, providing a highly accurate readout of the tuned frequency. The counter performs this function by counting the frequency of the LO (local oscillator) of the associated receiver and subtracting the IF frequency. The resultant count is visually displayed in six digits on shaped dot arrays of light emitting diodes. The readout has a resolution of ±100 Hz on the 0.1-50 MHz range and a resolution of ±1 kHz on the VHF and UHF ranges. Only the DRO-309A and the DRO-333 have the 490-1000 MHz UHF range. Circuit features include BCD (binary coded decimal) output, DAFC (digital automatic frequency control) to stabilize the LO frequency of the associated receiver, and the capability for external selection of ranges and presets.

1.1.3 The use of an LED (light emitting diode) visual display is updated from 10 times per second to 20 times per second. There is therefore no significant delay in obtaining a new count after the associated receiver is retuned.

1.1.4 Presetting to a number other than zero before each counting period enables the DRO-309A Series to effectively subtract the intermediate frequency of the associated receiver from the displayed count. Three preset numbers for IF frequencies of 21.4, 8.0, and 10.0 MHz are provided, normally for use on the 20-300 MHz VHF range. A preset number for an IF frequency of 60 MHz is also provided, normally for use on the 200-500, and 490-1000 MHz UHF ranges. Preset numbers for other IF frequencies may be substituted at the customer's request. These counters can be operated so that the proper preset is activated by the front panel RANGE switch (21.4 or 60 MHz IF), or the preset may be externally selected via a rear panel connector. If desired, the preset may be deactivated. The DRO-309A Series then reads out the input frequency with no offset and may be used as a conventional test counter over the range of 0.1 to 1060 MHz.

1.1.5 When the DAFC feature of the counter is utilized, the LO of the receiver associated with the DRO-309A Series can be locked to within plus or minus one count of any desired frequency in the receiver tuning range. The long term stability of the LO frequency will then approach the stability of the time base crystal oscillator of the counter. When the DAFC circuit is switched on it stores the frequency to which the receiver is tuned. If the readout frequency changes on subsequent counts, the counter will vary the analog voltage which is supplied to the receiver local oscillator to return the receiver to the desired frequency. Wide error sensing range is achieved by storing BCD information from the two least significant digits of the display, with one BCD bit from the third digit utilized. In addition to the FAST-SLOW function controlled by the front panel DAFC switch, an automatic rapid/delayed speed control which senses the magnitude of the correction is included. This feature allows the DAFC to quickly retune the receiver if a large error occurs, but minimizes incidental FM when the tuning correction is small. The wide acquisition range and automatic speed control of the DAFC circuit make these counters particularly useful in applications where the associated receiver may be subject to mechanical or thermal shock, such as in mobile installations. The DAFC output voltage is monitored by the TUNING CORRECTION meter, which indicates the magnitude and direction of the correction. If the DAFC voltage approaches the limits of the hold-in range, this will be indicated by the meter so that the receiver may be retuned before lock is broken. Two modes of DAFC voltage are provided; one for solid state receivers designed for use with DAFC, and one for tube type receivers which have been retrofitted for DAFC operation.

1.1.6 The DRO-309A Series provides a BCD output which can be connected to a remote display or printer. There are twenty-four lines of data and two supply voltages which may be used to power a remote display. The BCD is positive true logic in a 1248 code. Levels are compatible with transistor-transistor-logic. If desired, updating of the count can be inhibited while the BCD is being read out. The updating is provided at a rear panel connector.

1.1.7 The range and preset used by the DRO-309A Series can be externally controlled via selector lines available at a rear panel connector. The connector carries two sets of control lines to select which of the four frequency ranges and which of the four presets will be active.

1.1.8 The DRO-309A Series achieves measurement of input frequencies up to 1060 MHz by direct prescaling; no heterodyning techniques or transfer oscillators are employed. The three stage prescaler employs microwave transistors and stripline etched circuit board techniques to produce ultra high speed frequency dividers. Integrated circuit flip-flops capable of operating to 325 MHz are also employed. AGC circuits ensure stable counting over a wide range of input levels. Additional circuit features include the use of highly stable TCXO (temperature compensated crystal oscillator) for the time base oscillator, and a switching mode power supply regulator to minimize heat dissipation.

1.2 MECHANICAL CHARACTERISTICS

1.2.1 The Types DRO-309A and DRO-302B Frequency Counters are constructed in a half-rack package intended for installation in an equipment frame (see paragraph 1.4). The Types DRO-333 and DRO-315 are constructed as full-rack units 1.75 inches high and do not require an equipment frame. The chassis panels are fabricated of aluminum, and the front panel is a heavy machined plate. It is overlaid with a black, anodized aluminum bezel with etched markings. All subassemblies are constructed on etched circuit boards. Some plug into receptacles; other are bolted to a sub-chassis and hard wired to a cable harness.

1.2.2 The most frequently used controls are mounted on the front panel, along with the six digit display. Included are the POWER ON/OFF toggle switch (DRO-309A, DRO-302B) a push type ON/OFF switch (DRO-333, DRO-315), the RANGE rotary switch, and the DAFC OFF-FAST-SLOW rotary switch. The zero center TUNING CORRECTION meter is also on the front panel. Four option selector switches are mounted on the rear panel. Switch S2, the 115/230 Vac power selector, is a screwdriver activated slide switch; others are recessed toggle switches. Included are the PRESET INT-OFF-EXT switch, the RANGE CONT INT-EXT switch, and the DAFC 1-2 mode switch. All connectors are mounted on the rear panel. Two are multipin -- BCD OUTPUT jack J2 and RANGE/PRESET CONT jack J1. Four BNC coaxial jacks are also located on the rear panel. These are the three RF input connectors -- DIRECT 0.1-50 MHz, J6; VHF-LO (VHF-UHF) J5; UHF LO, J4; -- and one output connector, DAFC OUTPUT jack J3. Other components mounted on the rear panel are the line fuses, F1 and F2, and the permanently attached power cord.

1.3 EQUIPMENT SUPPLIED

This equipment consists only of any selected DRO-309A Series Counter with two mating multipin connectors. Dimensions and weight are given in Table 1-1.

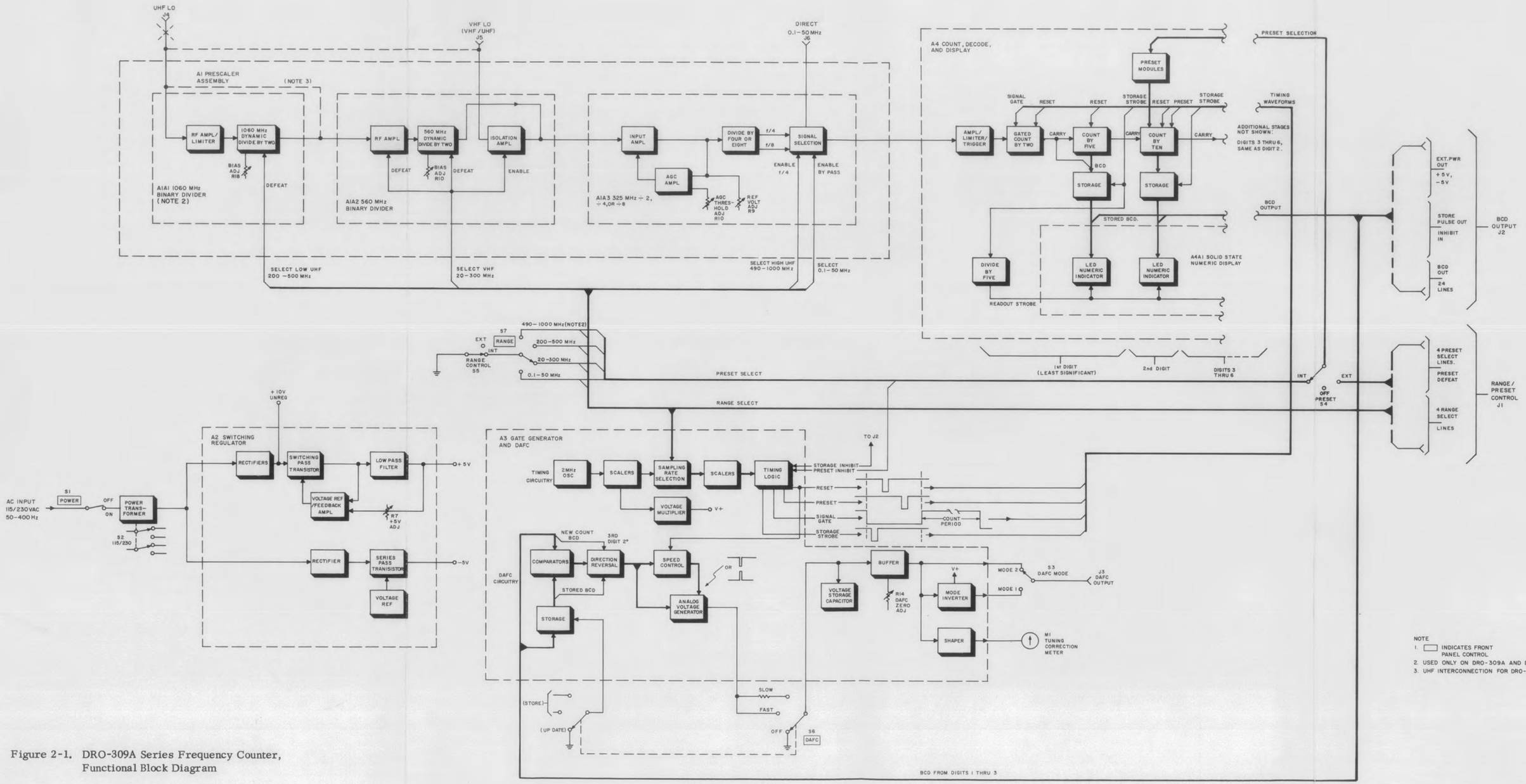
1.4 EQUIPMENT REQUIRED BUT NOT SUPPLIED

The DRO-309A Series serves as an accessory to an HF, VHF, or UHF receiver. The counter must be mounted in an equipment frame such as the WJ Type EF-101 or EF-201C, if it is a DRO-309A or DRO-302B.

Table 1-2. Type DRO-309A Series Frequency Counter Characteristics

UNIT TYPE	NOMINAL MAX FREQ READOUT	MECHANICAL PACKAGE
DRO-309A	1000 MHz	Half Rack
DRO-302B	500 MHz	Half Rack
DRO-333	1000 MHz	1.75" Full Rack
DRO-315	500 MHz	1.75" Full Rack

Figure 2-1



NOTE
1. ▭ INDICATES FRONT PANEL CONTROL.
2. USED ONLY ON DRO-309A AND DRO-333.
3. UHF INTERCONNECTION FOR DRO-302B AND DRO-

Figure 2-1. DRO-309A Series Frequency Counter, Functional Block Diagram

SECTION II

CIRCUIT DESCRIPTION

2.1 GENERAL

Operation of the various circuits in the DRO-309A Series is described in the following paragraphs. The explanation begins with the functional description which is keyed to the functional block diagram, Figure 2-1. Following sections provide detailed circuit descriptions of individual modules using the schematic diagrams, Figures 6-1 through 6-8. Note that the unit numbering method is used for electrical components. Parts on subassemblies and modules carry a prefix before the component designator. For example, A4R2 refers to a resistor in subassembly A4 and A2Q4 refers to a transistor in subassembly A2. Subassembly prefixes may be omitted in the text and on illustrations except where confusion might result from their omission. In regard to frequency ranges of these counters, it should be noted that range switching and control functions shown on the functional block diagram and main chassis schematic diagram refer to frequency readout ranges (for example, 200-500 MHz UHF Range) however, titles of prescaler modules refer to actual LO frequencies (for example, 560 MHz Binary Divider, A1A2).

2.2 FUNCTIONAL DESCRIPTION

The functional description of the DRO-309A Series is divided into six main headings:

(1) BCD Counting

(2) Digital Integrated Circuits

(3) Operating Principles

(4) DAFC

(5) External Interfacing Functions

(6) Power Supply

2.2.1 BCD Counting Description. - To aid in understanding the operation of the counter digital circuits, a brief explanation of the binary coded decimal (BCD) system of counting and waveform development follows. Only two characters, 0 or 1, are used for each binary place. BCD representation of a digit in the base ten, or decimal system, requires four binary places. The first place, or bit, represents 2^0 or 1, the second bit 2^1 or 2, the third bit 2^2 or 4, and the fourth bit 2^3 or 8. Thus, 0001 equals 1, 0010 equals 2, 0011 equals 3 and so on. Four flip-flops each representing the 0 or 1 state of each binary place, are required to count up to ten. However, a logic 1 output from each of the four flip-flops (1111) would represent 15 so a means must be provided to restrict the count to ten. A combination of four flip-flops plus an AND gate is used to count 0 through 9 and automatically reset to zero. Note that instead of the total count the value held in a decade is the least significant decimal digit. For example, the actual count of twelve results in a two in the counter. Decade counters, upon receipt of the tenth pulse, reset themselves to zero and pass a "ten" or "carry" pulse to the decade counter for the next, more significant digit. Figure 2-2 is included to show the BCD equivalent waveforms of the digits 0 through 9. The symmetrical BCD 1 waveform is exactly one-half the basic frequency. The output waveforms of the other flip-flops are modified by the feedback connections and are not symmetrical. The BCD 8 is also the carry pulse to the next decade of counting.

2.2.2 Digital Integrated Circuits. - Most circuitry in the DRO-309A Series consists of logic functions contained in integrated circuits (IC's). Three logic families are used: DTL, TTL, and ECL. For some slow speed functions, DTL (diode-transistor-logic) is employed. Where greater speed and output driving capability are required, TTL (transistor-transistor-logic) is employed. The DTL and TTL IC's include inverters. NAND gates, NOR gates, J-K flip-flops, decade counters, digital comparators, and numeric indicators. These IC's have a high, or 1, output state that is at least +3.0V and may approach the supply voltage (+5 Vdc) under light loading. The low, or 0 state, is +0.4V or less. Due to the similar voltage states, DTL and TTL gates are intermixed in some circuitry of the DRO-309A Series, where speed is not critical, as on the gate generator card (A3). Where complex functions or high speed are required, TTL circuits alone must be used, as in the counting chain on count, decode, and display board (A4). Transistors within DTL and TTL IC's operate in the saturated mode, switching

between saturation and cutoff. One type of IC using nonsaturated circuitry is employed and is designated ECL (emitter-coupled-logic). Transistors within the ECL IC's operate in the nonsaturated mode to achieve extremely high switching speeds. A smaller logic swing, 900 mV from the 0 state to the 1 state is employed. When used with a positive power supply as in the DRO-309A Series, the approximate voltages of the logic states are: 0 = +3.3V and 1 = +4.2V. The ECL device used is a type D flip-flop.

Nth NEG IN TRANSITION	1	2	3	4	5	6	7	8	9	10
COUNT VALUE	0	1	2	3	4	5	6	7	8	9	10
1 OUT	0	1	0	1	0	1	0	1	0	1	0
2 OUT	0	0	1	1	0	0	1	1	0	0	0
4 OUT	0	0	0	0	1	1	1	1	0	0	0
8 OUT	0	0	0	0	0	0	0	0	1	1	0

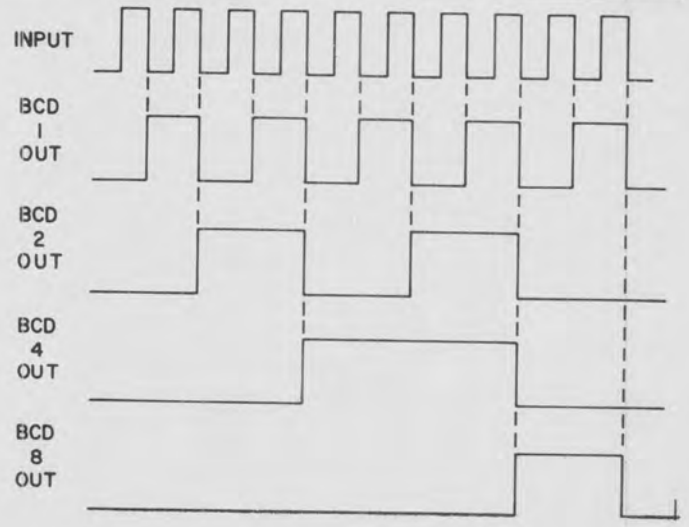


Figure 2-2. BCD Counting-Waveforms and Truth Table

2.2.2.1 Inverter. - This circuit is used in the DRO-309A Series to reverse the polarity of a pulse or waveform. When a waveform passes through the inverter the high and low states are reversed. The inverter logic symbol is shown in Figure 2-3. A small circle on the symbol indicates inversion or that the low input state is dominent. The bar over the character A in the statement $B = \overline{A}$ also indicates inversion and is read "not-A". The 9936 IC contains six inverters in one package. Inverters are contained in the 9014 and 9016 along with other functions.

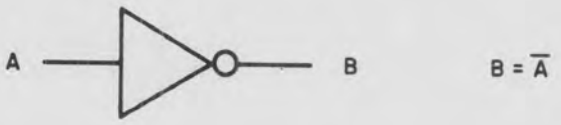


Figure 2-3. Inverter - Logic Symbol

Figure 2-4
Figure 2-5
Figure 2-6

2.2.2.2 NAND Gate. - A simple logic function used in the DRO-309A Series is the NAND (Inverting AND) gate. The NAND gate symbol and truth table refer to the high and low states of positive logic. The function of a NAND gate is this: if any input is low, the output will go high; only when all inputs are high will the output go low. The DRO-309A Series uses four types of NAND gate IC's. The 9946 contains four gates, each of which has two inputs; the 9962 contains three gates each of which has three inputs; and the 9961 contains two gates, each of which has four inputs. Another type, the 9016, contains two NAND gates along with inverters. (See Figure 2-4)

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Figure 2-4. NAND Gate - Logic Symbol and Truth Table

2.2.2.3 NOR Gate. - This logic function provides a low output if any input is high. Only when all inputs are low will the output go high. Figure 2-5 shows the logic symbol and truth table for this device. The 9015 contains four NOR gates; three have two inputs and one has four inputs.

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Figure 2-5. NOR Gate - Logic Symbol and Truth Table

2.2.2.4 Exclusive OR. - The exclusive OR gate gives a high output only if the two inputs have opposite states. If both inputs are high, or both low, the output will be low. These characteristics give the IC the capability of acting as a programmable inverter -- it may be an inverting or noninverting gate as desired. The truth table in Figure 2-6 shows, that if A is held low, C = B. If A is high, C = $\overline{B}$. Four exclusive OR gates are included in each 9014 package, along with two inverters.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Figure 2-6. Exclusive OR Gate - Logic Symbol and Truth Table

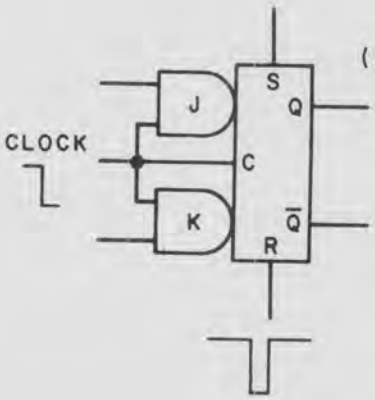
2.2.2.5 J-K Flip-Flop. - Figure 2-7 shows the logic symbol and truth tables for the J-K flip-flop. As used in the DRO-309A Series, this device has several important characteristics:

(1) When a pulse is presented to the clock input, the flip-flop switches its outputs to a state determined by the states of the J and K inputs.

(2) With J and K inputs held high, the flip-flop responds to pulses at its clock input by changing states of the Q output in a divide-by-two action. This occurs because there is internal feedback from the Q and $\overline{Q}$ outputs to the J and K inputs.

(3) When the set-reset (R and S) inputs are active, they dominate all clocked inputs (J, K, or clock).

The flip-flop changes output state on the negative-going edge of the clock pulse, depending on the state of the J and K inputs. During counting, the RS and J-K inputs are held high. Pulses to be counted are applied to the clock input. When a positive input goes high, then low, the Q output changes to the opposite state. This is shown by the last line of the clocked truth table. The negative transition of a second clock pulse will make the Q output revert to its original state. Therefore, the flip-flop divides the number of input pulses by two. When stopping the divide-by-two action is required, the J and K inputs are held low. As indicated by the first line of the clocked truth table, clock pulses can no longer change the Q output state. Before presenting a new train of clock pulses to be counted, it is necessary to set the Q output low so that the count starts from zero. The set-reset truth table shows that this is accomplished when the reset lines goes low, for any state of the clocked inputs. The $\overline{Q}$ output is then high, because its state is always opposite to that of the Q output. Two types of J-K flip-flop IC's are used in the DRO-309A Series. The 3202 contains a single TTL flip-flop for high speed counting. The 322 contains two J-K flip-flops. Additionally, all decade counter IC's include J-K flip-flops.



SET-RESET TRUTH TABLE (J&K MAY HAVE ANY STATE)

R	S	Q
0	0	NOT DEFINED
0	1	0
1	0	1
1	1	NO CHANGE

PARTIAL CLOCKED TRUTH TABLE (R & S = 1)

J	K	Qn+1
0	0	Qn
1	1	$\overline{Qn}$

Qn = INITIAL STATE OF Q OUTPUT.

Qn+1 = STATE AFTER ONE NEGATIVE TRANSITION OF CLOCK PULSE.

Figure 2-7. J-K Flip-Flop - Logic Symbol and Truth Table

2.2.2.6 Type D Flip-Flop. - The MC1671 flip-flop is an ECL master-slave type capable of operating as a frequency divider above 300 MHz. It is similar to the J-K flip-flop described in Section 2.2.2.5. However, it has a single D input with a J and K function. Thus the single input line can determine two output states. The clock input is triggered on positive transitions. When the clock is low, data is entered at the D input and stored in the master flip-flop. When the clock goes high, the data is transferred to the slave flip-flop and is available at the Q and $\overline{Q}$ outputs. Figure 2-8 shows a logic symbol and truth tables. The R and S inputs override any clocked inputs. The high input state is active at the R and S inputs, and at the clock inputs. There are two OR'ed clock inputs, C_1 and C_2. When used with the $\overline{Q}$ output tied back to the D input, the flip-flop will complement (change state) on each pulse at the clock inputs in a divide-by-two function. This is indicated by the clocked truth table. If the $\overline{Q}$ is high the D input is conditioned so that the next positive transition of the clock switches $\overline{Q}$ low. When $\overline{Q}$ goes low, it conditions the D input so that the next clock pulse will set $\overline{Q}$ high.

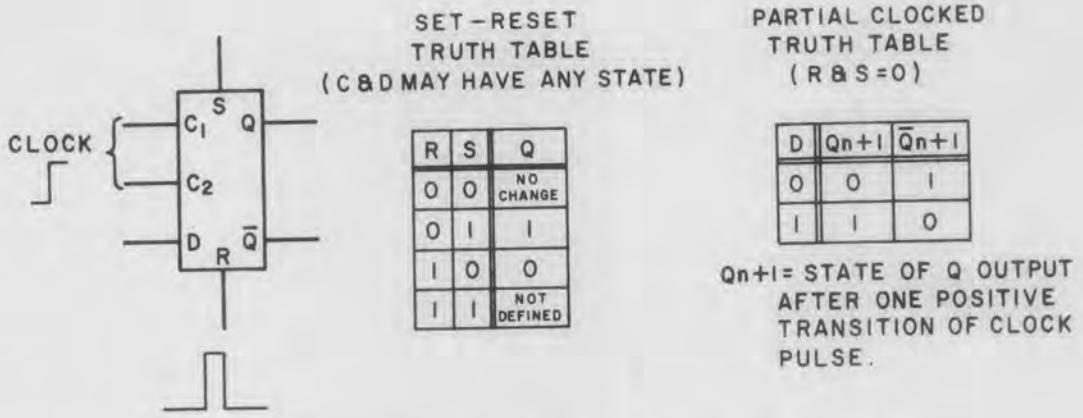


Figure 2-8. Type D Flip-Flop - Logic Symbol and Truth Table

2.2.2.7 Decade Counter. - These modules serve a variety of functions in the DRO-309A Series, including counting, scaling, and data storage. A logic symbol is shown in Figure 2-9. These devices contain four J-K flip-flops with feedback and feed forward lines to produce count-by-ten operation. In addition, a group of NAND gates allows parallel entry of 4 lines of data, which program the R and S inputs of the internal flip-flops. Two clock inputs C_1 and C_2 are provided. Input pulses may be applied directly to the first of four flip-flops at C_1, with the output of this flip-flop driving the other three via C_2. (These three flip-flops are connected in a divide-by-five configuration.) This connection is used whenever the device is used as a counter; that is, whenever its function is to provide a BCD output telling how many pulses have been presented to the input. Figure 2-2 is applicable as a truth table for the counting mode. A reset function is also provided for counting applications. When the R_D input is driven low, the outputs of all flip-flops will be set to zero in preparation for a new count. The connection to C_1 is also used when scaling by a factor of ten is needed. In scaling, the IC serves only as a frequency divider, with the input signal applied to a clock input and the output taken at the D_{OUT} pin. If the input is applied to C_2, the scaling factor is five. Entry of parallel data is effected when the S_T terminal is driven low. Under this condition the parallel data will be loaded into the flip-flops and the output terminals will be set accordingly. Use of the parallel input capability has two applications in the DRO-309A Series. One application is in presetting. It is desirable to have some of the decade counters begin their count from numbers other than zero, and the parallel entry makes loading in of these preset numbers possible. In a second application, only parallel entry occurs; the IC does not count or scale. Instead, it serves only as a storage element. It holds the BCD data from a similar IC that is used as a counter while a new count is being made. Once the data is loaded in, it will be held until another storage strobe pulse applied to the S_T input commands up-dating of the stored data. A series of similar TTL decade counters is used in the DRO-309A Series. The 8292, a low power version, is used in greatest quantity. The 8280, a medium speed version, and the 8290, a high speed version, are also used. Except for speed, all are identical.

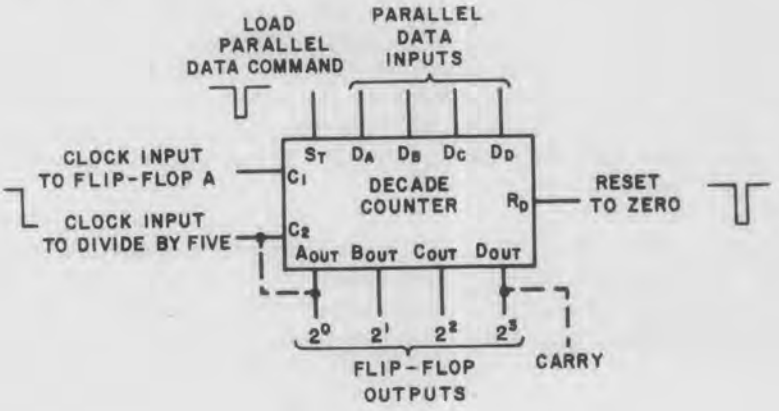
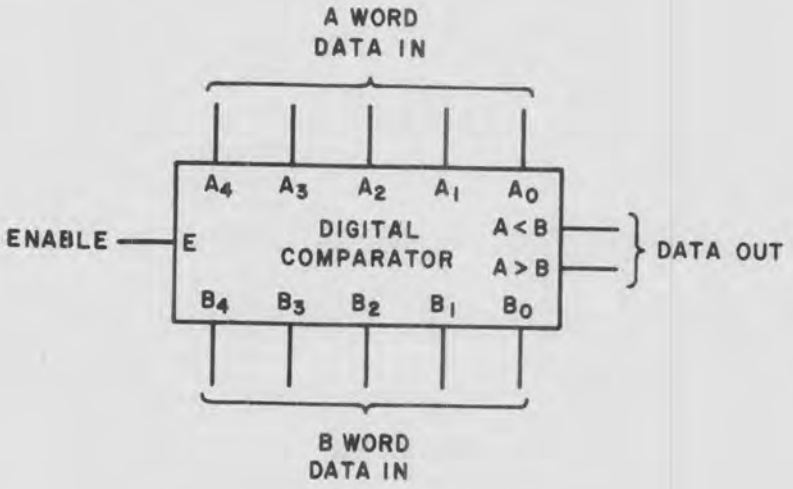


Figure 2-9. Decade Counter - Logic Symbol

2.2.2.8 Digital Comparator. - The logic symbol and truth table for the 93L24 comparator are shown in Figure 2-10. This IC compares a five bit binary word at its "A" inputs to a five bit word at its "B" inputs. Three conditions of the two outputs are generated, indicating that A is larger, B is larger, or both are equal. Each of the succeedingly more significant bits of input data carries greater weight in the comparison process. To accept more inputs bits, the IC's may be cascaded by using outputs of the IC accepting the most significant bits to drive the A_4 and B_4 inputs of the comparator for less significant bits.



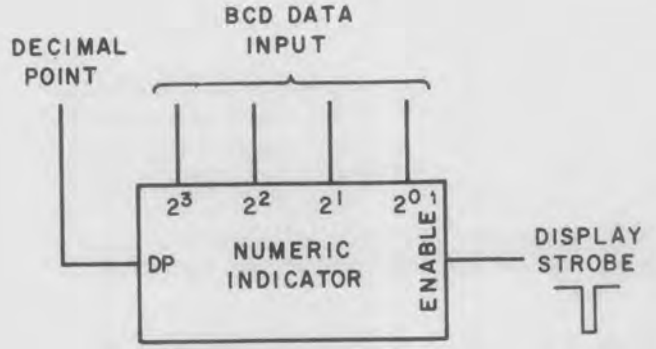
INPUT CONDITIONS	A < B OUT	A > B OUT
A WORD > B WORD	0	1
A WORD < B WORD	1	0
A WORD = B WORD	0	0

NOTE: ENABLE INPUT = 0

Figure 2-10. Digital Comparator - Logic Symbol and Truth Table

2.2.2.9 Numeric Indicator. - This IC type is used to visually display the count accumulated by the DRO-309A Series counting circuits. Each numeric indicator displays one digit of the count. A shaped numerical character is presented on a 4 x 7 dot array of light emitting diodes. The character represents the value of the BCD input data to the IC. The numeric indicator has three principal functions. First, the BCD input data is stored in latches to provide a steady readout until reading of new inputs is desired. The latches are controlled by an enable line which commands the latches to store previous data (enable line high) or to read new input (enable line low). The second major circuit function is decoding of the stored BCD to a 4 x 7 matrix dot pattern. Last, the LED's are activated to visually display the appropriate character. A right hand decimal point (also controlled by the enable line) is provided; a low input activates the decimal. A logic symbol and truth table are shown in Figure 2-11.

2.2.3 Operating Principles. - The Type DRO-309A Series Frequency Counter accepts input signals over the range of 0.1-1060 MHz, counts the signal for a precise interval, and digitally subtracts a predetermined number. Output information is a six digit visual readout on numeric indicators and 24 lines of BCD data. The following paragraphs describe the signal paths, presetting and timing functions. The description is keyed to the functional block diagram, Figure 2-1.



NUMERICAL CHARACTER TRUTH TABLE

BCD INPUTS 2^3	2^2	2^1	2^0	ENABLE	CHARACTER DISPLAYED
0	0	0	0	0	0
THROUGH				0	THROUGH
1	0	0	1	0	9
ANY				1	NO CHANGE

DECIMAL POINT TRUTH TABLE

DP INPUT	ENABLE	DECIMAL POINT
0	0	ON
1	0	OFF
ANY	1	NO CHANGE

Figure 2-11. Numeric Indicator - Logic Symbol and Truth Table

2.2.3.1 Signal Path. - Input signals pass through prescaler assembly A1 for frequency division before being applied to the counting circuits on count, decode, and display card A4. As shown in Figure 2-1, the prescaler assembly contains three modules. Several combinations exist for activation or defeat of prescaler circuits, depending on the range in use. The prescaler may pass signals with no frequency division (0.1-50 MHz range); it may divide the frequency by eight (20-300 MHz VHF range); or it may divide the frequency by sixteen (200-500 MHz, and 490-1000 MHz UHF range). The prescaling factor (and the time base) may be selected by the front panel RANGE switch or by selector lines at the rear panel RANGE CONT connector. The following description first explains prescaler function, progressing from lower to high frequencies, and then deals with basic counting circuits.

2.2.3.1.1 0.1-50 MHz Direct Range. - The LO input signal from jack J6 is applied to module A1A3 of the prescaler assembly. Signal selection diodes on this board block all outputs from the frequency dividers and route the signal directly to count, decode, and display card A4.

2.2.3.1.2 30-300 MHz VHF Range. - The VHF LO signal from jack J5 is applied to prescaler module A1A2. On this card the signal passes through a grounded base isolation amplifier. (The preceeding divide-by-two is disabled.) The amplifier output is routed to the 325 MHz divide-by-four or eight, A1A3. This module includes an amplifier with cascode and common emitter stages and an AGC feedback loop. The AGC amplifier is controlled by a reference voltage set by potentiometer A1A3R9, and an AGC threshold voltage set by potentiometer A1A3R10. The amplified signal is applied to the frequency divider, which consists of three ECL Type D flip-flops. On the VHF range, signal selection diodes route the divide-by-eight output signal to the count, decode, and display card.

2.2.3.1.3 200-500 MHz Low UHF Range. - LO input signals for both the low and high UHF ranges are received at jack J4. (As an option, internal cabling may be changed so that both VHF and UHF LO signals are received at J5.) The signals are applied to A1A1, where they pass through an RF amplifier/limiter with two common emitter stages. (Note: In the DRO-302B and DRO-315 A1A1 has been removed from the circuit and the signal goes directly to A1A2.) A defeat circuit allows the signal to pass through the dynamic divide-by-two without frequency division on the low UHF range. The low UHF signal is then applied to the 560 MHz binary divider module, A1A2. In this module, the ac voltage is applied to another common emitter RF amplifier, and then to a dynamic frequency divider. This stage divides the frequency of the incoming signal by two. Bias adjust potentiometer

A1A2R10 optimizes operation for widest frequency range. The divider changes the incoming low UHF LO signal to a frequency that can be accommodated by the following 325 MHz divide-by-four or eight module, A1A3. This module also operates in the divide-by-eight mode on the low UHF range.

2.2.3.1.4 490-1000 MHz High UHF Range (Used on DRO-309A and DRO-333 only.) - The LO input signal for this range is also received at jack J4. All frequency divider circuits are used. Following the input RF amplifier/limiter on the 1060 MHz binary divider module, A1A1, is an ultra high speed dynamic frequency divider used as a divide-by-two. Sensitivity is optimized by bias adjust potentiometer A1A1R18. The output of this flip-flop is again divided by two in A1A2, which operates in the same fashion as on the low UHF band. However, it is necessary to retain the same prescaling factor on the high UHF band as on the low UHF band. Therefore A1A3 is operated in the divide-by-four mode, as determined by the signal selection circuitry, to compensate for the added divide-by-two action of A1A1.

2.2.3.1.5 Basic Counting Circuits. - Count, decode and display card A4 receives the output from prescaler assembly A1 and performs all counting functions. Subassembly A4 contains six decades of count and readout circuitry. The input signal is first conditioned by a diode limiter, IC amplifier, and trigger transistor to give a large amplitude, fast fall time pulse to the following count-by-two IC. This J-K flip-flop is the first component of the counting chain. The flip-flop forms the first decade of counting with the divide-by-five portion of a decade counter IC. A separate high speed divide-by-two is used so that the signal can be gated at this point and to increase the highest counting frequency. This decade of counting produces the least significant digit of the readout. When the signal gate timing waveform from gate generator A3 goes high, the J and K inputs of the flip-flop are enabled for a discrete period which depends upon the range in use. A burst of pulses is then accepted by the flip-flop and the frequency divide-by-two carry pulses are passed to the count-by-five IC. These two counters produce a BCD output representing the least significant digit and carry pulses to the following decade. The BCD data is held in a storage IC so that the data is continuously available to the external BCD output connector, the DAFC circuits, and the numeric indicator which provides a visual readout of the count. To prevent operator confusion from a rapidly changing readout of the least significant digit, the divide-by-five portion of a decade counter provides one readout strobe pulse to update the numeric indicators for each five storage strobe pulses. The second decade differs from the first in that all of the count-by-ten function is contained in a single IC, and preset modules are provided to set the counter to a number other than zero before each count period begins. Following decades contain the same combination of decade counter, preset, storage, and numeric indicator modules.

2.2.3.2 Presetting. - The DRO-309A Series in effect subtracts a desired number from the count before reading it out. This is necessary because the receiver's LO frequency, which is the counted signal, is equal to the tuned frequency plus the IF frequency. Therefore, the IF frequency must be subtracted. Actually, an addition process is employed, with a carry of unused most significant digit. The preset number is loaded into the decade counters of count, decode, and display card A4 before each updating of the count. Several preset numbers are available for different IF frequencies. The range switch or selector lines at a rear panel jack determine which preset will be active. BCD data supplied by preset modules load the desired preset number into the parallel entry inputs of the decade counters. Loading occurs upon command of the gate generator, when the preset timing waveform goes low. The output lines of each decade counter will then hold the BCD code for one decimal digit of the preset number. When the count period occurs, the preset digit and the counted digit will be added. Table 2-1 illustrates the presetting process for an IF frequency of 21.4 MHz. Effectively, the counter has to count up to a readout of all zeros, and then continue to count to produce the final readout. An input of 21.4 MHz gives a readout of all zeros. A most significant digit of one would be displayed, but there is no decade to read out this digit position. Table 2-1 also shows how the tuned frequency of a receiver is converted to the LO frequency and then back to a readout of the tuned frequency on the counter.

2.2.3.3 Timing Cycle Events. - The DRO-309A Series functions by cycling many times per second through a four step timing sequence. These steps are performed in response to waveforms developed by gate generator card A3. To produce these waveforms, the output frequency from a highly stable crystal oscillator is divided by a series of decade scalers. Sampling rate selection circuitry passes waveforms from various scalers, depending on operating range. Additional decade scalers produce waveforms that are combined in NAND gates which make up the timing logic circuitry, to produce the timing waveforms. The waveforms are shown in Figure 2-1. Each timing cycle begins when the gate generator produces a negative going reset pulse. The pulse is applied to all decade counters to set their outputs to zero in preparation for a new count. Next the gate generator produces the preset pulse; it connects to all but the least significant digit decade. When the pulse goes low, the values of

the selected preset modules are loaded into the decade counter IC's. The states of the decade counter outputs then represent the desired preset in BCD format. Next the count period begins. The signal gate waveform to the count-by-two of A4 goes high. For a discrete interval the incoming signal is counted. The highest speed decade counts zero through nine many times, each time passing a carry pulse to the following decade. Each succeeding decade performs its count and supplies a carry to the decade counter which follows it. If the associated receiver is tuned to 300 MHz, the input frequency to the DRO-309A Series is 321.4 MHz. On the 20-300 MHz VHF range, the effective gate time (as determined by actual gate time and prescaling factor) is one millisecond. The number of pulses counted is 321.4×10^6 cycles per second times 10^{-3} seconds, or 321.400 pulses. When added to preset number of 978,600 the result is 1,300.000. Only the six least significant digits are readout, and one numeric indicator provides a decimal point. The resultant readout is 300.000 MHz, the correct tuned frequency. This count is left standing on the BCD output lines of the decade counters when the signal gate goes low to end the count period. The outputs of the counters connect to storage elements. As the last step in the counting cycle, the storage strobe output from the gate generator goes low, commanding the storage elements to read new input data and update their output data. The BCD outputs of the storage elements connect to numeric indicators which decode the BCD and visually display the appropriate numerical character.

Table 2-1. Presetting Subtraction

21.4	--	IF Freq
+978.600	--	Preset Number
1 000.000		
	--	Read out
	--	Not Read out
300.000	--	Receiver Tuned Freq
+21.4	--	Receiver IF Freq
321.400	--	Receiver LO Freq (Input to Counter)
+978.600	--	Counter Preset Number
1 300.000		
	--	Counter Readout = Receiver Tuned Freq

2.2.3.4 Counting Periods and Prescaling Factors. - Because the prescaler of the DRO-309A Series divides incoming frequencies by multiples of two rather than multiples of ten, corresponding adjustments must be made in the counting period to provide a readout whose digits are the same as the six most significant digits of the input frequency. Table 2-2 shows the various charactertistics that relate counting periods to prescaling factors. First consider the 0.1-50 MHz DIRECT range, where no prescaling is employed and the counting period is related to one second by a power of ten. The basic sampling rate, as determined by gate generator A3, is 80 Hz; that is 80 complete counting cycles occur each second. The period of a cycle is the reciprocal of 80 Hz, and the counting period within the cycle is 80% of the cycle time. Therefore the actual counting period is 0.010 second. Since no prescaling is employed, this period is also the effective counting period. The resolution of the readout is the reciprocal of the effective counting period. A period of one second would give a resolution of one hertz, and the effective period of 0.010 second gives a resolution of 100 Hz. A different situation exists on the 20-300 MHz VHF range. As shown in the table, a prescaling factor of eight is used. An actual counting period must be provided which gives an effective counting period that is related to one second by a power of ten. This situation is effected by choosing a sampling rate that gives an actual counting period of 0.008 second. The relationship defining the effective counting period is that it equals the actual counting period divided by the prescaling factor. Thus, the 0.008 second actual counting period and the prescaling factor of eight result in an effective counting period of 0.001 second. Since this is one tenth the effective counting period for the 0.1-50 MHz DIRECT range, the resolution is only one tenth as much; that is, 1000 Hz. Similarly, the two UHF ranges employ a prescaling factor of 16 and an actual counting period of 0.016 second, again giving an effective counting period of 0.001 second and a resolution of 1000 Hz.

2.2.4 DAFC. - The DAFC (digital automatic frequency control) circuitry is used to stabilize the local oscillator of the receiver used with the DRO-309A Series against long term drift. If the LO frequency of the receiver drifts away from a selected lock frequency, an analog voltage supplied to the receiver by the counter returns the receiver to the lock frequency. This is accomplished by having the analog voltage from the DRO-309A Series vary the reverse bias on the varactor (voltage variable capacitor diode) in the receiver's local oscillator circuit. The DAFC circuitry stores BCD data representing the desired lock frequency and compares this data to BCD data generated during each new count period. If the sets of data differ, the analog voltage is changed, with an automatic rapid/delayed feature selecting one of two correction speeds for large/small errors. As shown in Figure 2-1, most of the DAFC circuitry is on the gate generator card, A3.

2.2.4.1 Digital Comparison Circuitry. - When the front panel DAFC switch is set to OFF, the storage elements on A3 constantly update their information after each new counting period in response to BCD data from count, decode and display card A4. When the DAFC switch is set to the FAST position, the storage elements are commanded to hold the latest set of data and they store the desired DAFC lock frequency. They then control BCD for the two least significant digits of the display plus one bit from the third digit. Digital comparator IC's compare this stored BCD to the BCD generated by each new counting period. The states of the comparator outputs indicate whether the new count BCD is greater than, less than, or equal to the stored BCD. After further processing these outputs will be used to generate the analog output voltage. Exclusive OR gates provide a direction reversal for the comparator outputs. They act as inverting or noninverting gates depending on the state of the BCD 1 bit from digit three. This circuit configuration serves to provide a greater input error sensing range. Assume that the counter is reading out a frequency of XXX.050 MHz and that the receiver is in DAFC lock. If a sudden shock changes the receiver frequency to XXX.110, the DAFC would try to maintain lock for the two least significant digits by seeking a frequency of XXX.150. However, since the third digit changed from zero to one, the BCD 1 bit also changed. The stored bit is now different from the new count bit, causing a reversal of the direction of DAFC correction. The DAFC now seeks the correct lock frequency of XXX.050.

2.2.4.2 Automatic Correction Speed. - The DAFC circuitry is capable of responding to the magnitude of the required correction by switching to one of two correction speeds, rapid or delayed. If error signals from the comparator occur only occasionally, due to the plus or minus one count error inherent in a gated counter, the delayed speed is used to provide a very slow correction with minimum FM of the associated receiver's LO. If a constant error signal from the comparators exists, indicating loss of DAFC lock, the rapid speed is activated to quickly regain lock. To control which correction speed is to be used, the speed control circuitry strobes the analog voltage generator with a waveform which has a high ratio of high/low states times. The analog voltage generator can change its output while the waveform is high. For delayed correction speed, the speed control circuit strobes the analog generator with a waveform which is high for only 2% of each counting cycle (the inverted reset pulse). When the speed control circuit senses that a rapid correction speed is required, the control waveform is inverted so that its duty cycle is 98%, providing a much more rapid change of the analog output.

2.2.4.3 Analog Circuitry. - The analog voltage generator provides duty cycle controlled paths to the +5 and -5 Vdc power supplies to produce the DAFC analog correction voltage. The output voltage is used to charge a storage capacitor, whose charge is the correction voltage. Negative charging voltage increases the tuned frequency of the associated receiver. The charging current reaches the capacitor through S6. This switch selects the correction rate, and introduces a series resistor in the SLOW position to provide a longer RC time constant for charging the capacitor. When set to OFF, S6 grounds the capacitor to dump the stored voltage. The charge present on the capacitor is buffered to provide a low impedance output. A MOSFET (metal oxide silicon field effect transistor) is used in the buffer stage. The extremely high input impedance of the MOSFET prevents leaking off of the capacitive charge. The buffer stage includes a potentiometer, A3R14, which is adjusted to give zero offset between buffer input and output voltages. The buffer output is the mode 2 DAFC output voltage, which is routed directly to DAFC mode switch S3, and then to rear panel connector J3. The mode 2 voltage is also applied to a mode inverter stage which includes an operational amplifier. In this stage the mode 2 voltage, which is zero centered and has a negative slope of voltage-versus-frequency correction, is converted to a mode 1 voltage, which is centered at +8V and has a positive slope. The mode inverter requires a supply of +18 Vdc; this voltage is produced by a voltage multiplier which uses a waveform from the timing logic circuitry. The mode 1 voltage is also routed to S3. A tuning correction meter, M1, receives the mode 2 voltage through a shaper circuit which makes needle deflection conform more closely to frequency correction in the associated receiver.

2.2.5 External Interfacing Functions. - The DRO-309A Series has the capability for providing an external BCD output and associated command signals to a remote readout or printer. A capability is also provided for external control of range and preset selection.

2.2.5.1 BCD Output. - Count, decode, and display card A4 supplies a 24 line BCD output to rear panel connector J2. The BCD is 1248 code positive true logic from TTL storage IC's. Gate generator card A3 also has two connections to J2. A storage pulse output is provided whose positive transition indicates that a new count has just been completed, and an inhibit line is provided which may be set low to stop updating of the storage IC's on A4.

2.2.5.2 External Range and Preset Control. - Rear panel connector J1 has control lines which may be used to remotely select the desired range and preset. When rear panel RANGE CONT switch S5 is set to EXT, the front panel RANGE selector switch is disabled. Now one of the four selector lines in J1 may be set low to activate the proper range. When rear panel PRESET switch S4 is set to INT, one of two preset numbers for A4 is selected along with the range. But if the switch is set to EXT, any of four preset numbers may be activated by selector lines in J1. A line is also provided which when set low inhibits presetting.

2.2.6 Power Supply. - A single power supply module produces +5 Vdc and -5 Vdc output voltage to power all other subassemblies of the DRO-309A Series. The high current +5 Vdc circuit uses an efficient switching mode regulator. Positive voltage is produced by two rectifier diodes that convert the output from power transformer T1 to pulsating dc. The switching pass transistor produces a rectangular waveform that is converted to the dc output voltage by a low pass filter. An IC containing an operational amplifier and voltage reference senses the output voltage and adjusts the duty cycle of the drive waveform to the pass transistor. Potentiometer A2R7 adjusts the output voltage. In the simple -5 Vdc regulator, the dc produced by a rectifier module is applied to a pass transistor which operates as an emitter follower, receiving a reference voltage from a Zener diode.

2.3 TYPE 79904 PRESCALER ASSEMBLY

The reference designation prefix for this module is A1; its schematic diagram is Figure 6-1 or 6-2. This subassembly provides frequency division by four or eight for UHF and VHF input signals. Inputs enter the subassembly at coaxial jacks J1, J2, and J3. These jacks connect directly to the rear panel LO input connectors. Input signals pass through three modules: two UHF binary dividers, A1A1 and A1A2, and a VHF divide-by-four or eight A1A3. The frequency divided signal is available at jack J4, and is routed to count, decode and display card A4. Feedthrough capacitors C1 through C7 carry +5 Vdc and -5 Vdc supply voltages, and switching lines which select the desired frequency range, from multipin connector P1. Ferrite beads FB1 through FB16 are installed on all dc lines for RF suppression. Ferrite bead FB17 on the VHF input line increases the input impedance for frequencies above the VHF range, to preserve proper input impedance when the common connector VHF/UHF input configuration is used. In addition, components C8, C9, L1 and L2 filter the +5 Vdc lines to prevent false triggering of the logic circuitry by noise from switching regulator A2. The following paragraphs describe certain unique circuits which are used repetitively in the prescaler assembly, and then treat each module in detail.

2.3.1 Constant Current Source Amplifier Biasing. - The common emitter RF amplifier stages on binary divider modules A1A1 and A1A2 are biased by constant current sources. A separate bias transistor for each RF amplifier stage sets up a constant current through a resistor which is the collector supply to the amplifier transistor. The bias transistor also supplies base current to the RF amplifier in a configuration that establishes an equilibrium condition to regulate amplifier collector current.

2.3.1.1 Bias Equilibrium. - Figure 2-12 shows a simplified schematic diagram of an amplifier stage with its bias source. Values of resistors R1 and R2 are chosen to establish a voltage drop of 0.3 Vdc across R1. Since the forward voltage drop across CR1 equals the drop across the base-emitter junction of Q1, 0.3 Vdc is also applied to R3. The value of R3 is 30 ohms; therefore, current through it is 10 milliamperes. This current remains constant since the ends of the resistor are clamped to two fixed voltage points; the +5 Vdc supply line and +4.7 volts at the emitter of Q1. The current divides into two paths. Most of the current flows through L1 into the collector of Q2. A small amount of current flows from emitter to collector of Q1. The current flows through R4 (which prevents a shunting of the RF signal to ground) and into the base of Q2. This bias current establishes the equilibrium condition that holds the Q2 collector current constant. Assume that a rise in temperature tends to cause an increase in Q2 collector current. As Q2 attempts to draw a larger share of the current through R3, less current will be available to flow into the emitter of Q1 and the base of Q2. This decrease in base bias for Q2 effectively opposes the tendency to increase collector current.

Table 2-2. Counting Periods and Prescaling Factors

RANGE	SAMPLING RATE	ACTUAL COUNTING PERIOD = 80% x 1/ Sampling Rate	PRESCALING FACTOR	EFFECTIVE COUNTING PERIOD = Actual Counting Period/Prescaling Factor	RESOLUTION = 1/Effective Counting Period
DIRECT 0.1-50 MHz	80 Hz	0.010 sec	None	.010 sec	100 Hz
VHF 20-300 MHz	100 Hz	0.008 sec	8	.001 sec	1000 Hz
UHF 200-500 MHz 490-1000 MHz	50 Hz	0.016 sec	16	.001 sec	1000 Hz

2.3.1.2 Performance Advantages. - The configuration described allows the RF amplifier transistor to develop an output voltage swing equal to the full supply voltage and to maintain symmetry of the output waveform at high signal levels. Grounding the emitter of Q2 eliminates difficulties associated with emitter bypassing over the wide range of UHF frequencies employed. Diode CR1 stabilizes bias in two ways: the diode tracks changes in the base-emitter drop of Q1 with varying temperatures, and it maintains an almost constant drop regardless of changes in supply voltages.

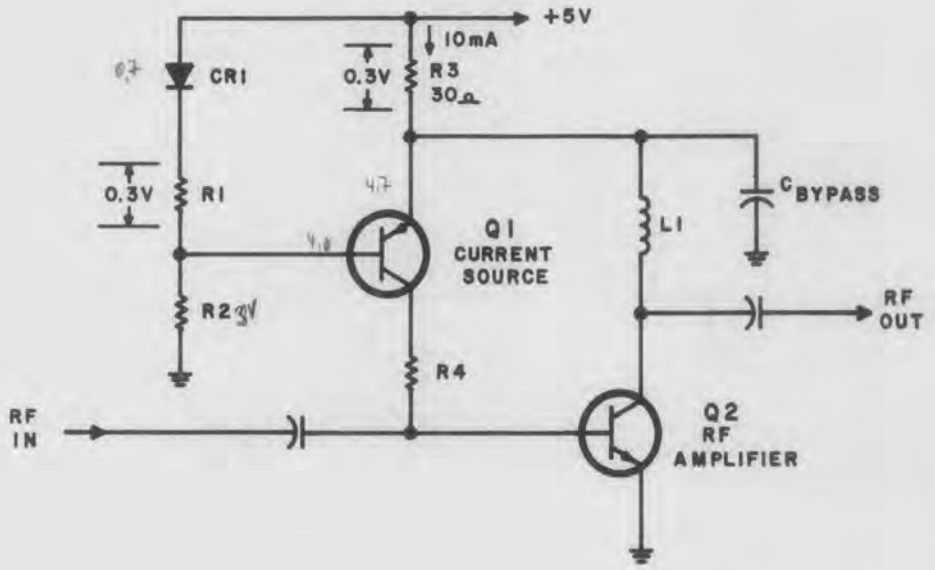


Figure 2-12. Amplifier Biasing, Simplified Schematic Diagram

2.3.2 Dynamic Frequency Dividers. - The prescaler of the DRO-309A Series achieves direct counting over its rated frequency span by use of frequency dividers capable of operating over the UHF range. A simplified schematic diagram of the dynamic frequency divider is shown in Figure 2-13. The circuit structure is similar to a conventional steered flip-flop, but there are major differences in switching operations. Determination of which transistor will be triggered by the input signal is determined not by initial conduction states of the input diodes, but by charges stored in RC networks in the emitters of the transistors. Output waveforms from the transistor collectors are not always complementary; instead, they are negative going pulses alternating between the collectors, interspersed with periods when both collectors stand high.

2.3.2.1 Switching Sequence. - Operation of the circuit can be best explained by a step-by-step consideration of switching operation, with one half cycle of the input waveform considered at a time. The following explanation is keyed to the simplified schematic diagram and idealized waveforms shown in Figure 2-13. It is assumed that Q2 was the more conducting of the two transistors in the half cycle prior to the first cycle shown in the diagram.

2.3.2.1.1 First Half Cycle. - As the input signal swings negative, it is conducted to the bases of Q1 and Q2 by the input diodes CR1 and CR2. The diodes are forward biased by R3, R4, and R6. The negative excursions on the bases of the transistors keep both cutoff, and the collectors stand high. As the voltages on C1 and C2 discharge through R1 and R2, both emitter voltages fall. Since Q1 was the less conducting transistor during the previous half cycle; its emitter capacitor has less charge. The Q1 emitter voltage falls to a minimum just prior to the second half cycle.

2.3.2.1.2 Second Half Cycle. - As the input signal swings positive both Q1 and Q2 tend to turn on. However, the emitter of Q1, and hence its base, is at a lower voltage than that of Q2. Therefore Q1 begins to conduct first, and it develops a negative-going pulse at the collector. Capacitor C3 couples the Q1 collector pulse to the base of Q2, inhibiting turn on and reverse biasing CR2 to block the input signal. As Q1 conducts through the second half cycle, the voltage drop across R1 charges C1 to its highest value.

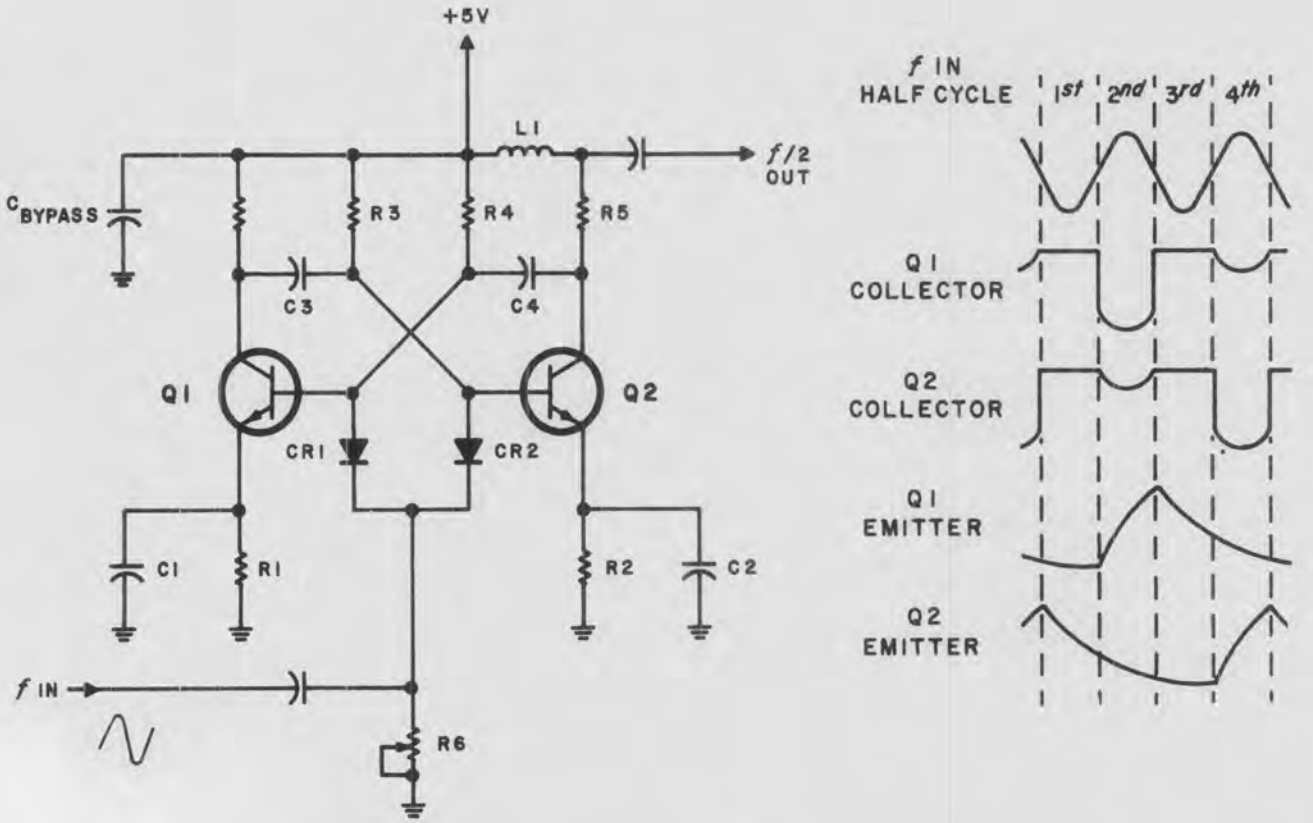


Figure 2-13. Dynamic Frequency Divider, Simplified Schematic Diagram

2.3.2.1.3 Third Half Cycle. - As the input signal swings negative, it cuts off both transistors through the forward biased diodes as in the first half cycle. But since Q2 was off in the previous half cycle, C2 has less charge than C1, and it is the Q2 emitter voltage that decays to a minimum.

2.3.2.1.4 Fourth Half Cycle. - As the input swings positive, both transistors tend to turn on as during the second half cycle. This time it is Q2 that has the lower emitter voltage and it turns on first, inhibiting Q1. The negative-going pulse which appears at the collector of Q2 has been developed in response to two cycles of the input signal, and this Q2 collector waveform is taken as the divided-by-two output signal.

2.3.2.2 Circuit Details. - To minimize loading on Q2, the output signal is taken from inductor L1 rather than directly from the Q2 collector. Potentiometer R6 allows adjustment of the base bias on the two transistors to obtain widest frequency range. There are two dynamic frequency dividers in prescaler A1, and the simplified schematic diagram shows the higher frequency divider which is used on module A1A1. The lower frequency divider, used on module A1A2, has resistors R3 and R4 returned to the transistor collectors rather than to the 5 Vdc line. However, this does not cause the dc bistable condition; both dynamic frequency dividers depend on ac characteristics for operation. Both dividers free run with no input signals and produce output frequencies in the region of 500 MHz. The extremely high frequencies achieved by the dynamic frequency dividers is obtained by use of microwave transistors, fast switching hot carrier (Shottky barrier) diodes, and stripline printed circuit boards.

2.3.3 Part 16488-1 1060 MHz Binary Divider (used only on the DRO-309A and DRO-333). - The reference designation prefix for this module is A1A1; its schematic diagram is Figure 6-3. Circuitry on this board consists mainly of two RF amplifier stages using constant source biasing and a dynamic frequency divider. Three diode limiters and a frequency divider defeat feature are also included. All UHF signals for both the 200-500 MHz and 490-1000 MHz ranges pass through this module, but the frequency divider is defeated on the low UHF range. Input signals from a rear panel input jack are received at E1 and follow a main signal path through amplifiers

Q2 and Q4 into dynamic frequency divider Q5 and Q6. The output signal from the divider connects to A1A2 via E5.

2.3.3.1 RF Amplifiers. - Common emitter RF amplifiers Q2 and Q4 with bias sources Q1 and Q3 operate as described in paragraph 2.3.1. Multiple bypass capacitors are employed on the emitters of the current source transistors and on the +5 Vdc supply line to assure rejection of power supply noise and to maintain low RF impedance across the entire UHF range. The two current source transistors share a common base bias diode, CR1. The incoming signal at E1 is applied to C2, L1, FB1, and FB2, which provide proper impedance termination across the UHF range. The amplified signal across L2 is limited to approximately 400 mV P-P by hot carrier diodes CR7 and CR8. Diode CR9 provides further limiting to reduce symmetry distortion at high signal levels. Capacitor C25 provides CR9 with an ac path to ground and R1 references the clipping point to the average signal level. The output of Q4 is also limited by CR2 and CR3 before being applied to the dynamic frequency divider. Since the divider is most sensitive to input signals in the region of 1000 MHz, it may be susceptible to false triggering on the second harmonic of input signals at the low end of the band. To prevent false triggering, the amplifier response is rolled off at the top end of the band by C26, C14, and the RC time constant of R11 and C17.

2.3.3.2 Dynamic Frequency Divider. - The amplified, limited RF signal from Q4 is coupled to the dynamic frequency divider by C15. The divider operates as described in paragraph 2.3.2. The frequency divided by two output from Q6 is coupled by C22 to terminal E5. Diode CR6, with current limiting resistor R15 and bypass capacitor C21, forms the defeat circuit. On the 200-500 MHz range, the dynamic frequency divider is disabled by application of ground to E4 by the range switch. Because CR5 is a hot carrier diode, it clamps the base of Q5 at 0.4 Vdc and the transistor is cut off. With Q5 disabled, the input signal frequency is no longer divided by two; it passes through CR5 and Q6 to E5 with no frequency change.

2.3.4 Part 16461-1 560 MHz Binary Divider. - The reference designation prefix for this module is A1A2; its schematic diagram is Figure 6-4. The UHF portion of this module includes a single amplifier stage with constant current source biasing (but without diode limiting) and a dynamic frequency divider. These circuits operate basically as previously described in paragraphs 2.3.1, 2.3.2, and 2.3.3, but with somewhat different defeat and enable circuitry. This module also contains an amplifier for the input signal on the 20-300 MHz VHF range. UHF signals are received from A1A1 at terminal E2. The signals pass through amplifier Q2, frequency divider Q3 and Q4, and through enable/defeat circuitry for range selection to output terminal E6. VHF signals enter the module at E8 directly from a rear panel input jack, are buffered by Q5, and pass through enable/defeat circuitry to E6.

2.3.4.1 VHF Amplifier. - Transistor Q5 acts as an isolation amplifier to provide a constant input impedance for the VHF signal. The transistor operates in the common base configuration. The VHF input signal from E8 is terminated by R21 and coupled to the emitter by C17. Resistor R20 supplies emitter current and R19 suppresses parasitic oscillations. Output ac voltage is developed across inductors L4 and L5. Operation of the diodes in the collector circuit is described in the following paragraphs.

2.3.4.2 UHF Enable/Defeat. - Several diodes on the module perform enable/defeat functions to select either UHF or VHF operation. On the UHF ranges, the current source biased amplifier and the dynamic frequency divider are active and the VHF amplifier is disabled. The range switch presents an open circuit to terminals E2 and E4. Diode CR9 has no effect. Since Q4 has +5 Vdc as its collector supply, diode CR5 is reverse biased from the +10 Vdc supply through R18 and R17 and also has no effect. Ferrite beads FB1 and FB2 have high impedance for fast rise times to prevent capacitive loading by CR5. However, CR4 is forward biased by being connected between +5 Vdc and +10 Vdc by L3 and R16. Output signals from the dynamic frequency divider pass through CR4 and C13 to output terminal E6. To disable Q5 during UHF operation, its output is blocked by CR6 and CR8. Both diodes are reverse biased by the dc current that flows between the +10 Vdc and +5 Vdc supplies through R18, L4, and L5. Diode CR7 is forward biased to shunt any RF leakage to ground through C15.

2.3.4.3 VHF Defeat/Enable. - When the VHF range is selected, UHF circuitry is disabled at three points. The range switch grounds E2 and E4. Diode CR9 is forward biased to clamp the base of Q2 at +0.4 Vdc and cut off the transistor to prevent any response to the free running frequency divider on A1A1; CR5 is forward biased through R12 to clamp the collector of Q4 to +0.7 Vdc to prevent free running of this dynamic frequency divider; and CR4 is reverse biased through L3 and R15 to block any output from the divider. VHF amplifier Q5 is now enabled. Diodes CR6 and CR8 are forward biased from the +5 Vdc supply through L4, L5, and R17 to connect the inductors in parallel. The shunting effect of CR7 is eliminated because it is reverse biased. The output signal from Q5 is conducted through C18 to E6.

2.3.5 Part 16462 325 MHz Divide-by-Four or Eight. - This module has the reference designation prefix A1A3; its schematic diagram is Figure 6-5. Input frequencies to this module are divided by a factor of four or eight on the VHF and UHF ranges. The input signal is received from module A1A2, and may be from the UHF dynamic frequency divider or VHF isolation amplifier. On the DIRECT range, the signal is received directly from the rear panel input jack, and prescaling is bypassed. Circuitry on A1A3 consists of three main parts; a wideband discrete component amplifier with AGC, a frequency divider composed of ECL IC's and a group of signal selection diodes to provide a divide-by-four, divide-by-eight, or bypass output.

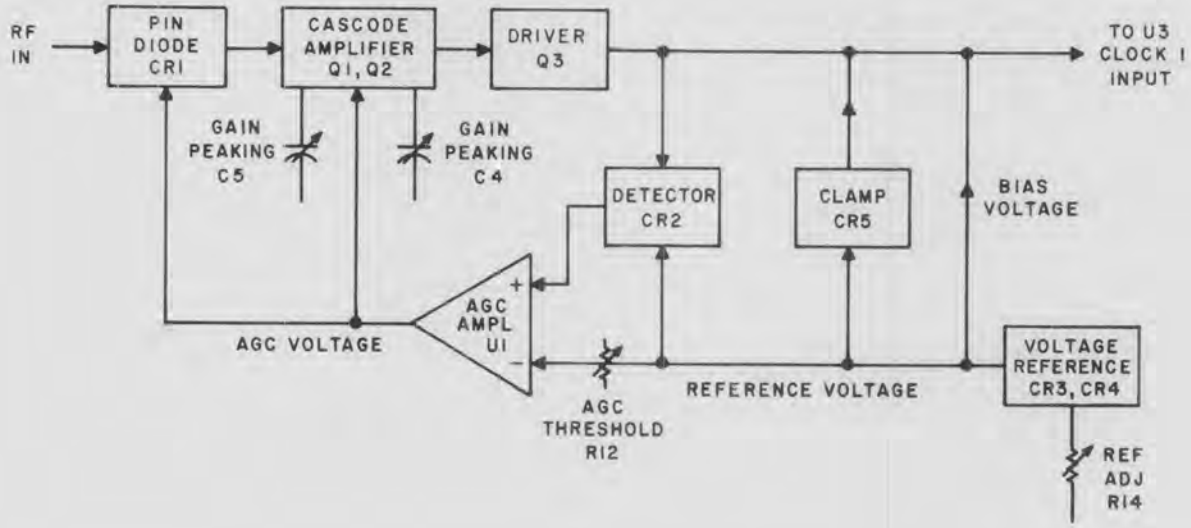


Figure 2-14. Input Amplifier, Functional Block Diagram

2.3.5.1 Input Amplifier. - Operation of the input amplifier stages can be understood by referring to the detailed block diagram shown in Figure 2-14. The main signal path through the wideband amplifier is through PIN diode CR1, high gain cascode amplifier Q1 and Q2, and driver Q3 to a clock input of U2, the first flip-flop in the frequency divider. Three other circuit functions are connected between Q3 and U2, and all are associated with the reference voltage which is supplied by CR2 and CR3 and adjusted by R9. A portion of this voltage is applied directly to the clock inputs of U2 to bias them into the center of the range of logic swing. The reference voltage also connects to CR4, which clamps off large positive excursions to U2 input to aid AGC action and protect against damage from excessive signal voltage. The reference voltage is connected to the AGC circuitry at two points. A fixed voltage is supplied to the inverting input of the AGC amplifier by AGC threshold set potentiometer R10. Detector CR5, which samples the output of driver Q3, is also connected to the reference voltage, and drives the non-inverting input of the AGC amplifier. If the output level from Q3 rises, the positive voltage detected by CR5 causes the output voltage of the AGC amplifier to go more positive. This voltage decreases the current through the PIN diode so that its RF resistance increases, and increases the current through Q1 so that its gain is reduced. The overall effect of the AGC circuit is to provide a constant input level to the frequency divider.

2.3.5.1.1 RF Amplifier Stages. - As shown in Figure 6-5, the input signal enters the board at E1 and is terminated by R1. The signal passes through CR1, a PIN diode, whose function is described in a later paragraph on AGC operation. DC blocking capacitor C1 couples the signal to the base of Q1. This transistor is a common emitter stage which is dc coupled to common base stage Q2, forming a cascode amplifier. Emitter current to Q1 is supplied by R5 and R6. Resistor R5 provides some degeneration for lower input frequencies. For higher input frequencies, variable capacitor C4 resonates with stray inductance of the emitter lead of Q1 to provide a gain peak at approximately 250 MHz. Capacitor C3 performs a similar function for Q2 at about 325 MHz. The output signal voltage from the cascode amplifier is developed across inductor L1. Capacitor C2 couples the amplified signal to the base of common emitter amplifier Q3. This stage provides additional gain and driving capability. Resistor R8 supplies emitter current to Q3 from the negative supply and is bypassed by C9 and C10.

Resistor R7 provides a dc base return for the transistor. Transformer T1 is the ac collector load for Q3; it is tapped to provide the low driving impedance needed by clock inputs of flip-flop U2. Capacitor C11 ac couples the signal to the flip-flop.

2.3.5.1.2 Voltage Reference. - Diodes CR2 and CR3 develop the voltage used in biasing and AGC operation. Diode CR2 is a silicon signal diode with a forward voltage drop of 0.75 Vdc, and CR3 is a hot carrier diode with a drop of 0.41 Vdc. The diodes are forward biased from the +5 Vdc supply through a series of resistance of R9, R10, and R11. The voltage drop across the diodes and the small drop across R9 establishes a reference voltage of approximately +3.8 Vdc at E12. Capacitor C12 places the voltage at ac ground. RF choke L3 supplies a dc path so that the reference voltage can be supplied as a bias voltage to the C_1 and C_2 inputs of U2. The high RF impedance of the inductor isolates the ac signal voltage from reference voltage. Potentiometer R9 is used to optimize the bias for the particular IC used to U2. Diode CR4, a fast switching hot carrier device, clamps positive excursions of the signal voltage to 0.41 volts above the reference voltage. The reference voltage is coupled to AGC amplifier U1 by potentiometer R10, and to AGC detector CR5 by R12.

2.3.5.1.3 AGC Circuitry. - AGC amplifier U1 receives two dc input voltages and controls current through CR1 and Q1. The IC is a high gain operational amplifier. Potentiometer R10, the AGC threshold control, applies a voltage to the inverting input of U1. Voltage to the non-inverting input is supplied by detector diode CR5. The diode is biased into conduction by R12 and R13, and rectifies signal voltage coupled from Q3 by C15. Rectified voltage is developed across dc return R13 and filtered to dc by C16. Under no signal conditions, the AGC loop seeks a maximum RF gain condition. The voltage applied to the non-inverting input of the AGC amplifier by the detector diode is less than the voltage applied to the inverting input by the threshold set potentiometer. The output voltage of U1 at E9 is then negative. The integrating feedback capacitor, C8, and the RC time constant of R31 and C28 make the amplifier immune to transients from power supply and switching voltage lines. The U1 output voltage is applied to the junction of R3 and R4. Current through R3 forward biases CR1. This device is a PIN diode (for positive, intrinsic, and negative layers) whose RF resistance varies over a wide range depending on forward dc current. (The device does not rectify the RF.) Minimum RF resistance is achieved with maximum forward bias, and this situation exists under no signal conditions. Output voltage from U1 also controls current through Q1. AGC voltage is fed to the base of Q1 by R4, and the emitter voltage tracks 0.7 Vdc more negative than the base. The difference between the emitter voltage and the -5.0 Vdc present at E2 determines the current through R6 and R5, and hence the emitter current. The nearly equal collector current determines ac gain. This transistor type operates with forward AGC; that is, increasing current past a point reduces gain. Thus gain varies according to the difference between the voltage at the junction of R3 and R4 and the voltage at E2. If an input signal is applied to the prescaler with a level above the AGC threshold, the detected output from CR5 drives the non-inverting input of U1 more positive than the inverting input. The output of the amplifier swings in a positive direction as does the junction of R3 and R4. The forward bias across CR1 decreases so that its RF resistance increases and reduces the input signal level. Since the voltage difference between the junction of R3 and R4 and terminal E2 has increased, more collector current flows through Q1, and gain drops to provide additional AGC action.

2.3.5.2 Frequency Divider. - The frequency divider uses three ECL type D flip-flops to achieve frequency division by a factor of four or eight. Each flip-flop has its D input tied to the $\overline{Q}$ output so that it operates in a divide-by-two function. The signal input is to the clock inputs and the output is taken from the Q terminal. The signal path between IC's is from a Q output to the clock input of the succeeding IC. All Q and $\overline{Q}$ outputs are provided with pull down resistors for the internal emitter followers. For U2, the IC which operates at the highest speed, RC networks such as R14-R15-C17 on the outputs optimize impedance of printed circuit lines to maintain reliable operation above 300 MHz. The divided-by-four and divided-by-eight outputs (Q of U3 and Q of U4) are taken through voltage dividers such as R19 and R20 which reduce the logic swing to prevent it from overcoming the reverse bias on the signal selection diodes.

2.3.5.3 Signal Selection Diodes. - Components CR7 through CR9 determine whether the prescaled output from this module will be divided by two, four, or eight. The diodes also bypass prescaling functions when the 0.1-50 MHz DIRECT range is selected.

2.3.5.3.1 Division by Four or Eight. - This function is determined by CR6 and CR7. On the 20-300 MHz VHF range and the 200-500 MHz UHF range, division by eight is desired. Terminal E8, which connects to the front panel RANGE switch, is an open circuit condition. Diode CR6 which has its anode tied to a Q output, is reverse biased from the +10 Vdc supply through R28 and R20 to block the divided by four signal from the Q output of U3.

However, the divided by eight signal from the Q output of U4 can pass through CR7, which has its cathode connected to a Q output and is forward biased through R28 and R29. The signal then passes through C23 and through CR8, which is conducting on all but the 0.1-50 MHz DIRECT range. Diode CR8 is forward biased by being dc connected between the +5 Vdc and the +10 Vdc supplies through R24 and R27. Capacitor C25 couples the signal to output terminal E5. On the 490-1000 MHz UHF range, division by four is desired. The range switch supplies a ground to E8. Since the output voltage from Q of U4 swings between logic levels of 3.3 and 4.2V, CR7 is reverse biased through R22 and R23. Diode CR6, however, is forward biased through R19 and R23 by the logic voltage from U3, and supplied the divided by four signal to C23.

2.3.5.3.2 Direct or Prescaled. - When operation on the 0.1-50 MHz DIRECT range is desired, the frequency divided outputs are blocked. A path is then provided for the DIRECT range signal, which enters the module at E4, to pass directly through C24 and C25 to output terminal E5. When the DIRECT range is chosen, the range switch grounds E6. Diode CR8, which was forward biased on all other ranges, is now reverse biased from the +5 Vdc supply through R24 and R26. The diode blocks both the divided by four and divided by eight outputs. Diode CR9 was reverse biased from the +10V supply by R25 and R27 on all other ranges. It is now forward biased by R25 and R26, and it provides the signal path from E4 to E5.

2.4 TYPE 79912-1 COUNT, DECODE, AND DISPLAY

The reference designation prefix for this module is A4; its schematic diagram is Figure 6-8. This card includes circuitry to amplify and shape the input waveform, and six decades of counting that provide a visual frequency readout on numeric indicator IC's.

2.4.1 Input Amplifier. - Input signals are applied to module pin 22. Resistor R1 provides a dc return for the input of IC U1. Diodes CR1 and CR2 limit the amplitude of incoming signals to avoid overloading of the amplifier IC. This device is a wideband video amplifier which provides gain needed when the DRO-309A is operating on the 0.1-50 MHz DIRECT range and low level input signals are applied directly to this card. The output from U1 is ac coupled to trigger transistor Q1. This transistor is driven from cutoff to saturation by the waveform from U1. It provides a fast fall time pulse output as required to trigger U2.

2.4.2 First Decade of Counting. - Integrated circuit U2, a J-K flip-flop, gates the input signal into bursts, and it forms the first decade of counting with divide-by-five counter U3. The signal from Q1 connects to the clock input of the J-K flip-flop. The IC divides its input frequency by two, but only when the signal gate waveform is high. This waveform, from the gate generator, enters the card at module pin 18 and connects to a J and K input of U2. Prior to each counting period, the reset pulse is applied to U2 and U3 to set them to zero. After this, the signal gate waveform goes high, and the count period occurs. The Q output of U2 drives the C_2 input of U3 for division by five. This output of U2 also connects to U4, where it is the BCD 1 bit to the low power decade counter used as a storage element. Integrated circuit U3 is a high speed decade counter which supplies the remaining BCD bits of the least significant digit to the storage element. The outputs of the storage element, which are updated upon command of the storage strobe pulse, are connected to numeric indicator IC A1U1. This IC decodes the BCD and displays the appropriate character on an array of LED's. This least significant display may flicker between two characters due to the ±1 count indeterminancy inherent in a gated counter. To prevent operation confusion (for example, flicker between 9 and 0 being interpreted as 8) the numeric indicator is updated only once for each five counting periods. The frequency of the display strobe is divided by five in decade counter U41. The display strobe enters the card at module pin 1 and is the same waveform as that at pin A. Clock input C_2 receives the input signal; the divided-by-five output is a BCD 8 waveform. The output pulse is inverted by Q2. Due to the length of the high state of the BCD 8, a second storage pulse, commanding U4 to update, might affect the readout on A1U1. Therefore the emitter of Q2 is tied to the input waveform rather than to ground, so that the negative going pulse at the collector of Q2 can be no wider than the input pulse at module pin 1. The BCD outputs from storage element U4 also connect to module pins which route them to the rear panel BCD output connector.

2.4.3 Second Decade of Counting. - The second decade contains the same basic functions as the first. However, the use of a separate J-K flip-flop for gating is not required and a single medium speed decade counter IC performs the counting function. In addition, the second decade and all following decades have presetting capability. This function is performed in the second decade by the preset modules U5 and U6. These modules are capable of loading a BCD number into the parallel data inputs of decade counter U7. Module U6 contains pull-up resistors for all parallel data inputs, and module U5 pulls down certain lines to determine the BCD number. A preset selector line determines whether U5 will be active. Figure 2-15 shows how preset operation occurs if a

preset to five module is installed for U5. Resistor R1 in each module has a very low value; resistors R2 through R5 of U6 are 10 kilohms. When the preset line for module U5 is made active (grounded) by the front panel RANGE switch or the rear panel RANGE CONT connector, germanium diodes CR1 and CR3 of U6 are forward biased and pull the BCD 2 and 8 lines down to 0.3V to set them to the 0 state. But pull-up resistors R3 and R5 of U6 hold the BCD 1 and 4 lines in the 1 state, so that parallel data inputs D_A through D_D of U7 have a BCD value of five. When the preset pulse from the gate generator drives S_T low, the parallel data is loaded into the internal flip-flops. The preset number of five will be added to the value accumulated during the following count period. Components CR4, CR5, and R8 in Figure 6-7 form a preset isolator for U7. The components form an AND function that will allow the preset line to pull down the S_T input of U7 only if the preset e selector line is low. Otherwise, a false count of BCD number 1111 would be loaded into U8 when the preset strobe goes low and a preset is selected for which this decade has no preset module.

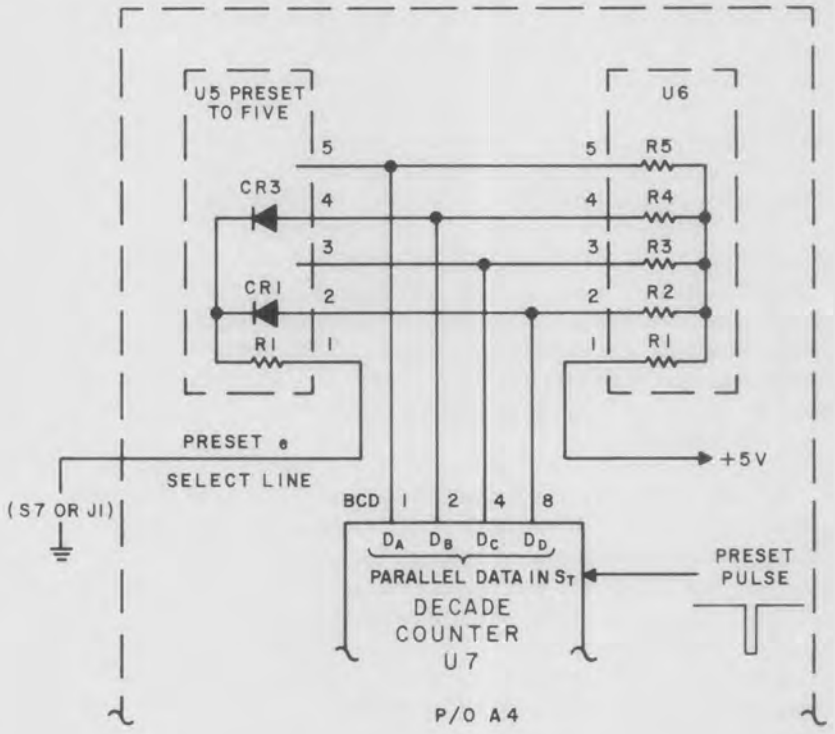


Figure 2-15. Preset Operation

2.4.4 Remaining Decades. - The third decade of counting is similar to the second decade. However, the preset isolation components are omitted and there are six preset modules. A low power decade counter IC is used. All following decades are similar to the third decade. The numeric indicator for the fourth decade displays a right hand decimal point on the VHF and UHF ranges (as in 999.999). This decimal is activated by a 0 at J3. The fifth decade displays a decimal point on the 0.1-50 MHz DIRECT range (as in 50.000), in response to a 0 at J4.

2.5 TYPE 79907 GATE GENERATOR AND DAFC

The reference designation prefix for this module is A3; its schematic diagram is Figure 6-7. This card has two principal functions: a crystal oscillator and timing circuit generate waveforms to control the counting circuitry on card A4, and storage, comparison and analog voltage generating circuits produce the two DAFC output voltages.

2.5.1 Time Base Generation. - Timing circuitry of the gate generator produces four output waveforms with three possible repetition rates. All waveforms are referenced to the output frequency of U10. This TCXO (temperature compensated crystal oscillator) is a sealed module that provides a highly stable 2 MHz output

frequency. This frequency is divided down by a chain of scalers including decade counters U1 and U2 and J-K flip-flop U4A. Output waveforms are taken from this chain at three points. NOR gates in A3 select one of the three waveforms in response to range selection circuitry of the main chassis. The output frequency from U5 is divided by a factor of 100 by U6 and U7. These two decade counters supply several BCD waveforms which are combined in NAND gates U8, U9, and U13 to produce the output timing pulses.

2.5.1.1 Sampling Rate Selection. - Range selector lines from the front panel RANGE switch or the rear panel RANGE CONT connector control NOR gates in IC U5 to determine cycling rate of the output timing waveforms from this card. For example, the 0.1-50 MHz DIRECT range sampling rate is selected by a control line connected to module pin E. If this range is not selected, module pin E will be in an open circuit condition, which NOR gate U5C accepts as a logical 1. By the basic NOR function, if any input is high, the output must stand low. Therefore U5C blocks the waveform from U3A. But if the 0.1-50 MHz DIRECT range is selected, ground is applied to module pin E and U5C. With one input at a logical 0 state, the NOR gate acts as inverter for data at the other input, and the waveform from U3A is passed on to U5D. It also passes the waveform as the outputs from U5A and U5B stand low because their respective ranges are inactive. On this range, the 2 MHz output of U10 has passed through U1, U2A, and U3A for frequency division by a factor of 250, and it will pass from U5D through U6 and U7 for division by a factor of 100. The output from U7, which determines the basic sampling rate is thus $(2 \cdot 10^6$ Hz)/(250) (100), or 80 Hz. This result is in accordance with the data tabulated in Table 2-2. Similarly, U5B selects the output of U2B and U3B, both of which divide by two to produce the 100 Hz sampling rate required on the 20-300 MHz VHF range. Gate U5A selects the output of U4A to produce the 50 Hz sampling rate required on the two UHF ranges. Inverters U13D and U13E with expansion diodes CR1 and CR2 are used to activate U5A. When the UHF ranges are inactive, R1 pulls the input of U13D up to a 1 state, which is doubly inverted and applied to U5A. Diodes CR1 and CR2 form an AND function to allow either of the two UHF control lines (module pins 1 and 2) to pull the input of U13D low while keeping the control lines isolated from each other. The low input thus supplied to U5A by U13E activates the 50 Hz sampling rate. The output of U13E also connects via module pin A to count, decode, and display card A4 to activate preset B (for 60 MHz IF frequency) when the UHF ranges and internal selection of preset are used. Inverter U13C provides a low output to enable the fourth decade decimal point of A4 on all but the 0.1-50 MHz DIRECT range, when the range selector line directly enables the fifth decade decimal point.

2.5.1.2 Timing Waveforms. - The various waveforms that are combined to produce the output timing waveforms all include the BCD 8 from U7. This waveform determines the basic sampling rate. The waveform is asymmetrical with an 80% / 20% relationship of logic states. During the 80% portion, the counting period occurs. During the 20% portion, the reset, preset, and storage strobe functions occur. Figure 2-16 shows the various BCD waveforms which are combined to produce timing pulses. The U7 BCD 8 is combined with two other waveforms to produce the reset pulse. The inverted U7 BCD 1 divides the 20% portion of the U5 BCD 8 into halves, and is high during the first half. The U6 BCD 8 is high for 20% of the time that the two previous waveforms are high. When these three waveforms are combined and inverted in NAND gate U9A, the reset pulse is the result. To produce the preset pulse, the U7 BCD 8 waveform is combined with the U7 BCD 1 without inversion, which puts the output pulse in the latter half of the 20% portion of the U7 BCD 8. These waveforms are combined with the U6 BCD 4 and the inverted BCD 2 from U6 in NAND gate U8B to produce the negative going preset pulse. To provide the signal gate waveform, it is only necessary to invert the U7 BCD 8, and this is done by NAND gate U13F. To produce storage strobe pulses, the inverted U7 BCD 1 is again used, to locate the output pulse in the first half of the 20% portion of the U7 BCD 8. Otherwise the same BCD waveforms are used as were used to produce the preset. The waveforms are combined in U8A. All of these four output timing waveforms connect directly to module pins which route them to count, decode, and display card A4 to control its function. Provision is made for disabling the storage strobe and preset pulse if desired. Diode CR4 provides the inhibit function for the storage strobe (see Figure 6-6). The diode, which is necessary to establish proper logic levels connects to an expansion node in U8A. In normal operation, the cathode of CR4 is pulled up to a 1 state by R3. But when the line that connects module pin 4 to a pin of the rear panel RANGE CONT connector is grounded, CR4 holds the expansion node in a 0 state. The storage strobe pulse stays high and no further updating of the storage elements occurs on count, decode, and display card A4. This feature may be used when the external BCD output is being readout. Components CR3 and R2 perform a similar function for disabling the preset pulse. A resistor on the main chassis sinks the inhibit line to ground when the rear panel PRESET switch is set to OFF. A preset defeat line in the rear panel RANGE CONT connector can also disable the preset pulse.

2.5.2 DAFC Circuitry. - DAFC circuitry on this module includes digital IC's to store the desired lock frequency and compare it to subsequent counts. Analog circuitry selects one of two correction speeds, generates

up and down commands, and stores and buffers the two analog output voltages.

2.5.2.1 Data Storage and Comparison. - The DAFC circuitry receives BCD data from the three least significant digits of count, decode and display card A4. The lines of BCD data connect to storage elements U17 and U18 and to one set of inputs of digital comparators U16 and U15. The outputs of the storage elements supply the other sets of inputs to the comparators. When the front panel DAFC switch is set to one of the on positions, the state of module pin X changes from ground to open circuit. The S_T inputs of storage elements U17 and U18 accept this input as a 1 state. The storage elements then stop updating and store the BCD for the frequency present when the DAFC was activated. The storage elements supply the four bits for the "A" word inputs of comparators U16 and U15. As count, decode, and display card A4 continues to update its count, the new count BCD supplies the "B" word inputs. If the tuned frequency of the receiver associated with the DRO-309A Series changes, the "B" word inputs change. The A> B and A < B outputs of the comparators indicate which of the input numbers - "A" word or "B" word - is greater. The outputs of U16 connect to the A_4 and B_4 inputs to expand the comparison greater than, equal than, or less than the value of the "B" data.

2.5.2.2 Direction Reversal. - The BCD 1 bit from the third digit of the readout is also stored. This bit determines whether the output from U15 will be inverted before reaching the analog portions of the DAFC circuitry. This feature provides capability for reversing the direction of correction, which increases the error sensing range as described in paragraph 2.2.4.1. NAND gates U9C, U12D and flip-flop U4B form a latch to store the BCD bit. The output of U19A gives an update/store command and data is entered into the latch at U9C pin 4. When the DAFC is off module pin X is at ground and the output of U19A is high, giving an update command. Gates U9C and U12D, with one input high, act as inverters. Data entered into U9C is applied to the S input of flip-flop U4B. The opposite state is applied to the R input by U12D. Depending on the data entered, either S or R will be set low to determine the state of the Q output. When the DAFC is on, the output of U19A goes low, giving a store command. Because both NAND gates have a low input, their outputs stand high. High state inputs have no effect on S and R of the flip-flop, so it remains in the previous state, storing its input data. Exclusive OR gate U11C receives both the stored third digit BCD 1 from U4B and the new count bit from module pin 12. If the bits are 11 or 00, the direction reversal command for the outputs of U15 is not needed. The output from U11C stays low, and the exclusive OR gates used as programmable inverters, U11A and U11B, pass their data without inversion. If the inputs to U11C are 01 or 10, direction reversal is required. The output of U11C will go high, and U11A and U11B will invert their input signals. Outputs of the programmable inverters connect to gates where duty cycle of the DAFC correction is controlled.

2.5.2.3 Automatic Correction Speed Control. - The decision of whether rapid or delayed DAFC correction will be enabled is made by components which process the outputs of U11A and U11B and control the duty cycle of data passing through U12B and U12C. Components U12A and Q1 charge or discharge capacitor C11 to cause rapid or delayed correction. Operational amplifier U14A acts as a high input impedance voltage follower to buffer the charge on C11. Output voltage of U14A is shifted to a voltage 0.7V less positive than voltage at the non-inverting input by diode CR7 in the negative feedback path, and this output voltage effectively supplies a 1 or 0 to control exclusive OR gate U11D. This gate operates as a programmable inverter. Its input is a positive pulse with a 2% duty cycle, obtained by inverting the reset pulse in U19B. To explain operation of the circuit the rapid speed is first considered. This speed is initiated when a constant error exists between the stored lock frequency and the new count frequency, as indicated by the outputs of comparator U15. They will be in the 10 or 01 state. The outputs may be inverted in U11A and U11B, and will be inverted by U11E and U11F; regardless, the inputs to U12A will be in opposite states. With one input low, the output of U12A will be high, and it will charge C11 positively through R7. After about 1.3 seconds the charge on C11 will rise to a value which will cause the buffered output of U14A to be accepted as a 1 by U11D. The exclusive OR will act as an inverter, and the narrow positive input pulse will be inverted to a narrow negative pulse whose voltage is high 98% of the time. This waveform is applied to NAND gates U12B and U12C so that their output data to the analog voltage generating circuitry has a very high active duty cycle. Rapid correction will occur until the desired lock frequency is acquired, at which time Q1 will discharge C11. To explain this occurence, consider that the actual counted frequency is higher than the lock frequency, so that the A < B output of U15 is in the 1 state. When rapid correction has acquired the desired lock frequency, the A < B output of U15 makes a transition from 1 to 0. At this time U11A and U11B will be operating in the non-inverting mode, so the output of U11E will make a transition from 0 to 1. Capacitor C9 and R5 differentiate this transition into a positive going spike which forward biases CR5 and momentarily causes Q1 to turn on. As Q1 conducts it quickly discharges C11 to ground. The output of U14A falls to a low voltage value which provides a 0 state to U11D. The exclusive OR gate now passes its input pulse without inversion, providing a narrow positive pulse to U12B and U12C, so that they can pass correction data for only 2% of the time. This is the delayed mode of operation. If the initial error frequency is below the lock fre-

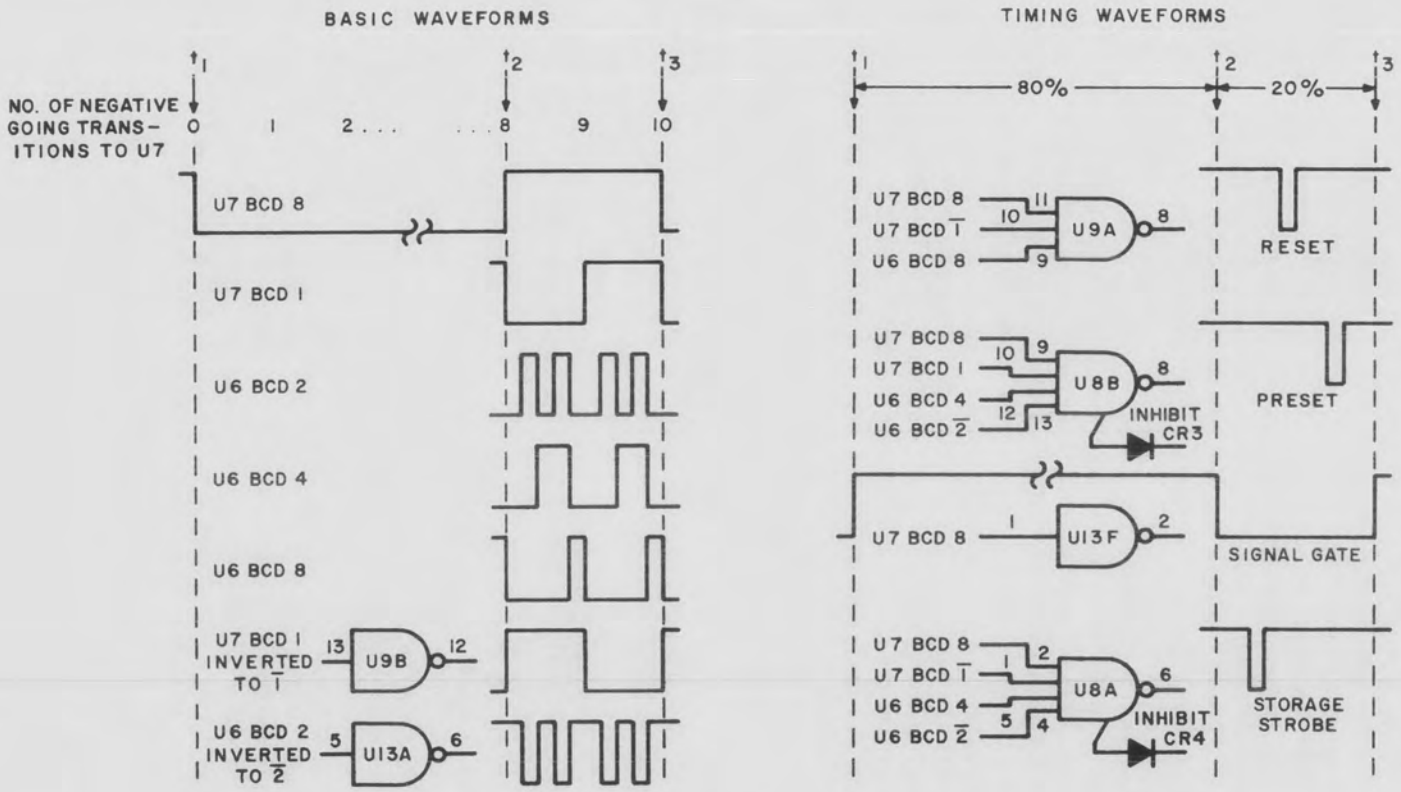


Figure 2-16. Timing Waveform Development

quency, the pulse to turn on Q1 will be provided by the output of U11F. Diodes CR5 and CR6 block the unwanted negative spikes produced when the initial error condition occurs and an output of U15 goes from 0 to 1.

2.5.2.4 Analog Voltage Generator. - Gates U12B, U12C, and U13B with transistors Q2 and Q3, convert the data originating in U15 into an analog control voltage which is stored in capacitors C13 and C14. The analog voltage may be negative or positive. Consider the case where the actual counted frequency is above the lock frequency, but with a small enough error so that U11A and U11B operate in the non-inverting mode. The A < B output of U15 will be in the 1 state. Gate U12B inverts this output to a low state, and pulls down the base of Q2 through current limiting resistor R8. Since Q2 is a PNP transistor with its emitter tied to +5 Vdc, it is turned on by the low input. Collector current for Q2 follows a path through R12 to module pin 11, through the front panel DAFC switch, back into the module at pin 10, and into storage capacitors C13 and C14. In the SLOW position the DAFC switch inserts a resistor in the current path to further increase the R12-C13-C14 time constant. The capacitors are polarized types connected back to back so that they can store either positive or negative voltage. In the case where the actual counted frequency is below the lock frequency, the A > B output of U15 will be in the 1 state. This output is doubly inverted in U12C and U13B to provide a high state to turn on Q3. Since Q3 has its emitter tied to -5 Vdc, 5.6V Zener diode CR1 is required to shift the output of U31B to negative levels. The diode is held in Zener breakdown by R10, and R9, which also limits Q3 base current. When Q3 conducts it charges C13 and C14 in a negative direction.

2.5.2.5 Buffer. - The charge stored in C13 and C14 is buffered by MOSFET Q4 to provide the mode 2 DAFC output voltage. The extremely high input impedance of the MOSFET gate prevents leaking off the charge on the capacitors. Current for Q4 is provided by a constant current source consisting of Q5, CR8, and CR9. The diodes are forward biased from the -5 Vdc supply by R15. The voltage drop across the two diodes is approximately 1.4 Vdc. Since the drop across the base emitter junction of Q5 is about 0.7 Vdc, approximately 0.7 Vdc is applied to potentiometer R14. This potentiometer can be varied to set the current through itself and the collector of Q5. The collector supplies the source current to Q4. This current through the MOSFET is set to a value that will give zero offset voltage between gate and source. Then, when the front panel DAFC switch is set to OFF, grounding module pin 10, the DAFC mode 2 output at module pin K will also be zero volts. Resistor R16 provides short circuit protection for the output at the Q4 source, and C15 filters noise from the DAFC output line.

2.5.2.6 Mode Inverter. - Operational amplifier U14B produces the mode 1 output voltage by shifting the off voltage of mode 2 from 0 to +8 Vdc, inverting the slope, and increasing the voltage swing. The IC is connected as a difference amplifier, comparing the incoming mode 2 voltage to a reference derived from the +5 Vdc power supply by R22 and R23. The mode 2 voltage is applied to the inverting input of the operational amplifier through R19. Negative feedback is supplied by R20. The ratios of R19 to R20 and R22 to R23 determine the output voltage. Output is taken through current limiting resistor R7 and RF filter C16. In order to produce the large positive excursion required, U14B receives a +18 Vdc supply voltage (V_{cc2}) from a voltage multiplies composed of Q6 and CR13 through CR18.

2.5.2.7 Meter Shaper. - Diode CR10 with R17 and R18 shapes the voltage to the TUNING CORRECTION meter so that needle swing more accurately represents the degree of DAFC frequency correction produced by the varactor in the local oscillator of the associated receiver. When the DFAC mode 2 voltage is positive and the voltage drop across R18 exceeds about 0.3 Vdc, CR10 begins to conduct to supply additional current to the meter through R17. This causes the meter needle to swing more rapidly to end of scale as the DAFC correction voltage continues to increase.

2.5.2.8 Voltage Multiplier. - Transistor Q6 and diodes CR13 through CR18 are used to produce V_{cc2}, the +18 Vdc supply required by DAFC mode inverter U14B. Transistor Q6 and inductor L1 produce a 10V P-P square wave at the transistor collector which serves as the ac input to the voltage multiplier diodes. When the transistor is driven into conduction, it provides approximately zero volts at its collector, to establish the amplitude of the negative going half cycle of the ac waveform. Inductor L1 conducts heavily from V_{cc2}, the +5 Vdc supply. When the transistor cuts off, the energy stored in L1 attempts to maintain current flow in the same direction. Since L1 now serves as a current source rather than a load, the voltage of the Q6 collector swings up to a positive voltage. This voltage equals the voltage formerly impressed across the coil, plus the voltage to which one end of the coil is clamped, for a total of +10V. The square wave peak voltages are thus zero volts and +10V. The voltage multiplier consists of five sections, CR13-CR19, etc., each of which half wave rectifies the ac. Each section produces a dc voltage equal to one half the peak to peak amplitude of the ac input signal and adds its rectified voltage to the voltages produced by the preceeding sections. For example, when the voltage at the

collector of Q6 swings positive, C19 is charged through CR13. When the collector swings low, C21 is charged through CR14. The voltage at the cathode of CR4 represents the sum of the charges on the two capacitors. This voltage is added to the charges produced by the following stages, and the voltage produced at the cathode of CR17 is several times the peak value of the input waveform. At filter section CR18-C25 the output voltage of approximately +18 Vdc is available.

2.6 TYPE 76192 SWITCHING REGULATOR

The reference designation prefix for this module is A2; its schematic diagram is Figure 6-6. This power supply has regulated outputs of +5 Vdc and -5 Vdc. The high current +5 Vdc supply uses switching mode techniques for maximum efficiency. The non-dissipative regulator utilizes a pass transistor that is always either cut off or saturated. In eight state very little power is dissipated, and the need for elaborate heat sinking is avoided. The square wave output from the switching pass transistor is converted to dc by a low pass filter. A high switching frequency, approximately 25 kHz, is employed. Filter capacitors and chokes are therefore of low value and small size. The lower current -5 Vdc supply uses a simple series regulator.

2.6.1 Basic Switching Regulator. - Figure 2-17 shows a simplified schematic diagram of the switching regulator circuitry. First consider the basic switching regulator. A rectangular wave output is present at the emitter of pass transistor Q2. During the t_{on} period, when Q2 is conducting, it supplies current to the load through L2 and C5. Diode CR3 is reversed biased. But when Q2 cuts off, the energy stored in the reactive components supplies the output current. Inductor L2 tends to sustain current through itself and it becomes a current source. The end of the inductor connected to CR3 is the negative terminal, and it is more negative than ground. Therefore the diode is forward biased, clamping the negative end of the inductor to just below ground potential. The diode provides a path for the reactive energy during t_{off}. The filter components supply a dc output voltage which is the time average of the square wave voltage. Therefore, the output voltage can be increased by increasing the time that Q2 is conducting. The higher the ratio of t_{on} to t_{off}, the higher the output voltage.

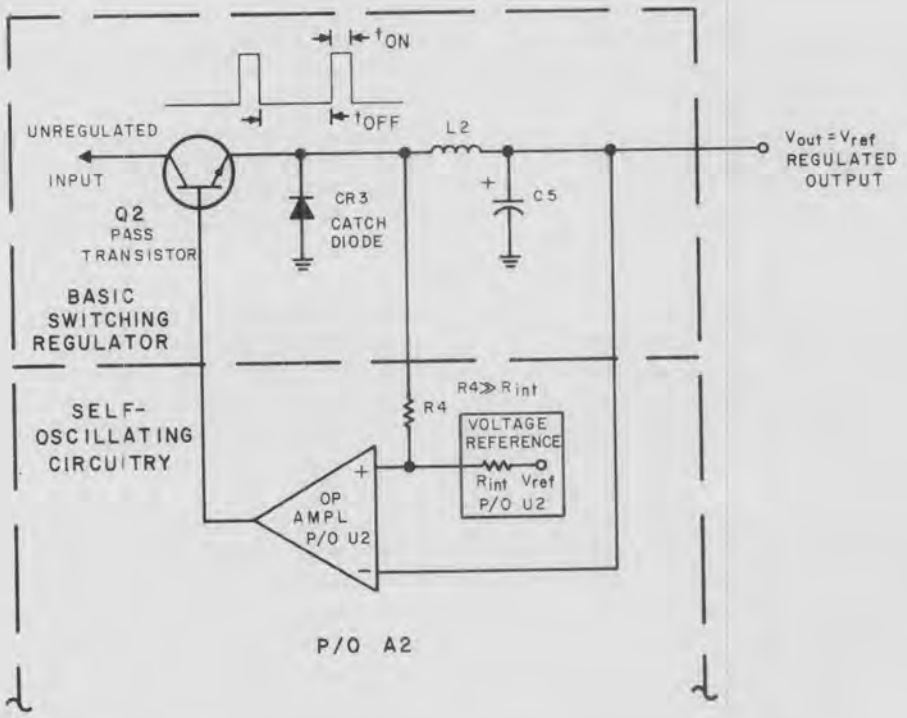


Figure 2-17. Switching Regulator, Simplified Schematic Diagram

2.6.2 Self Oscillating Regulation. - Additional components shown in Figure 2-17 give the regulator circuitry the ability to generate its own drive waveform for Q2, and to regulate the output voltage by varying the duty cycle of the square wave. The pass transistor is driven by an operational amplifier. A reference voltage and a small amount of positive feedback from the emitter of Q2 are applied to the non-inverting input of the operational amplifier. The inverting input receives the dc output voltage. When the circuit is first turned on, the reference voltage is present at the non-inverting input of the operational amplifier, but the inverting input is at ground. Therefore, the output voltage of the amplifier goes positive, turning on Q2. The small amount of positive feedback through R4 then increases the voltage at the non-inverting input to slightly above the reference voltage. The transistor stays on until the output voltage rises and becomes greater than the reference voltage plus feedback voltage at the non-inverting input of the amplifier. Now the amplifier switches its output low and Q2 cuts off. The positive feedback through R4 reduces the voltage at the non-inverting input of the amplifier to slightly below the reference voltage. The state of the amplifier remains until the output voltage falls below the reference voltage less the feedback voltage at the non-inverting input, when the cycle is repeated. Thus, it can be seen that the output oscillates around the reference voltage. The output voltage varies above and below the reference voltage by a small ripple voltage determined by the ratio of R4 to the internal resistance of the voltage reference.

2.6.3 Circuit Details. - Figure 6-5, the schematic diagram, shows additional features of the circuitry. Incoming ac from transformer T1 is full wave rectified by diodes CR1 and CR2. The output from the diodes connects to an external filter capacitor, C8, mounted on the main chassis. Unregulated dc is applied to the collector of the pass transistor after passing through a low pass filter. The filter is composed of C1, C3, L1 and C6. The function of the filter is to prevent conduction of switching transients and RF noise generated by Q2 and Q3. Integrated circuit U2 contains the differential amplifier and voltage reference required for self-oscillating operation. Resistors R6, R7, and R8 form an adjustable voltage samplign network to supply the dc input voltage to the inverting input of the operational amplifier in U2. Potentiometer R7 is adjusted to give a voltage equal to the internal reference voltage when the output of the supply is at +5 Vdc. The output of U2 is used to drive a PNP transistor connected as a common emitter amplifier, Q3, which drives pass transistor Q2. Resistor R3 provides a path for Q3 collector current. Resistor R5 determines the amount of drive current which U2 supplies to Q3. Inductor L3 reduces RF output noise. Transistor Q1 supplies the -5 Vdc output voltage. Incoming ac is rectified in diode assembly U1 and filtered by C6, a capacitor on the main chassis. Resistors R1 and R2 supply current to Zener diode VR1, with ripple filtering by C2. The diode reference voltage is 5.6 Vdc. Since Q1 is a silicon device, its base-emitter drop sets the output voltage at the emitter to -5.0 Vdc.

2.7 TYPE DRO-309A SERIES MAIN CHASSIS

Functions of the various modules, connectors, and controls of the main chassis have been discussed in previous paragraphs. Additional details are shown in Figure 6-9. A few functions which are not self-explanatory are discussed below. Switch S4 has three sections. Section S4A is concerned with the preset on/off and defeat functions. Normal operation requires that the switch be in the EXT or INT positions. In either position resistor R3 and resistor R2 (which uses module pin 18 of A2 as a tie point) are connected to form a voltage divider from the +5 Vdc supply to set the preset inhibit line to a 1 state. The preset inhibit line connects to A3 to control the expansion node of the NAND gate that produces the preset pulse. The preset pulse will be deactivated if pin A of J1 is sunk to a 0 state. Deactivation is also produced when S4 is set to OFF. In this case, the connection to R2 is broken and R3 sinks the inhibit line to a 0 state. Sections S4B and S4C control the two internal presets. When S4B is set to INT, it ties the internal preset a selector line of A4 to the 20-300 MHz range selector line in J1. Activating the desired range, by J1 or RANGE switch S7, then selects preset for a 21.4 MHz IF. When S4B is set to EXT, the preset selector lines in J1 must be used to select preset a or another VHF preset. Section S4C performs the same function for preset b, which is used with a 60 MHz IF. This preset is used with both the 200-500 MHz and 490-1000 MHz UHF ranges. Therefore S4C does not connect directly to pins of J1 in the INT position; instead it connects to module pin A of A3, which provides an AND'ed output of the two range selector lines. Diodes CR1 and CR2 prevent an undesirable condition that can occur on the 0.1-50 MHz DIRECT range. This condition would occur if the range were selected internally by the front panel RANGE switch and if S4 were set to INT or EXT. Since no preset is normally provided to this range, the preset module with pull-up resistors for each decade would enter false BCD values of 1111 into the decade counters. The numeric indicators cannot decode this value and they would go dark. To prevent this condition CR1 pulls down the preset inhibit line to a 0 state, and no presetting activity occurs. However, this preset defeat is blocked by CR2 when the 0.1-50 MHz DIRECT range is selected externally, so that a preset can be installed if desired. A 10V Zener diode, VR1, prevents excessive +10V unregulated output from the power supply if the ac line voltage rises. Excessive 10V causes poor sensitivity in the 0.1-50 MHz range because the RF switching diodes on A1A3 become improperly biased. Inductors and capacitors are installed across the ac line on the full-rack counters to prevent outward conduction of RFI.

SECTION III

INSTALLATION AND OPERATION

3.1 UNPACKING AND INSPECTION

3.1.1 Examine the shipping carton for damage before the equipment is unpacked. If the carton has been damaged, try to have the carrier's agent present when the equipment is unpacked. If not, retain the shipping carton and padding material for the carrier's inspection if damage to the equipment is evident after it has been unpacked.

3.1.2 See that the equipment is complete as listed on the packing slip. Contact Watkins-Johnson Company, CEI Division, or your Watkins-Johnson representative with details of any shortage.

3.1.3 The unit was thoroughly inspected and factory adjusted for optimum performance prior to shipment. It is, therefore, ready for use upon receipt. After uncrating and checking contents against the packing slip, visually inspect all exterior surfaces for dents and scratches. If external damage is visible, inspect the internal components for apparent damage. Check the internal cables for loose connections. See that plug-in items, such as etched circuit cards, are securely mounted in their receptacles.

3.2 INSTALLATION

3.2.1 Mounting. - The Type DRO-309A and DRO-302B Frequency Counters are designed for half-rack mounting. They can be mounted in a Type EF-101 or EF-201C Equipment Frame. The EF-101 mounts a single half-rack unit and the EF-201C can mount two half-rack units. Both equipment frames require 3.5 inches of vertical rack space and install in a standard 19-inch width rack. The DRO-333 and the DRO-315 are 1.75 inches high, 19 inches (full rack) wide, and do not require an equipment frame. These units mount in the standard 19-inch rack, and are supported by four front-panel mounting screws. If used in a mobile installation, some means should be devised to support the side and/or rear of the equipment. A brace extending along the sides from the front panel to the rear apron is preferred. Do not rely solely on the front panel mounting hardware to support the unit. It is recommended that chassis slides be added for ease of assembly, access to the unit, and to provide additional support for general installations. All installations should allow a free flow of air through the holes in the top and bottom dust covers of the equipment frame used. Forced air ventilation may be needed if equipment uses multiple stacking or close adjacent stacking. The installation should also allow access to the rear panel so that input and output connections can be made and changed if desired. The rear panel connections are described in the following paragraphs. See Figures 3-1 and 3-2 for critical dimensions.

3.2.2 Power Connection. - Before proceeding, be certain that the front panel POWER switch is set to the OFF position. Check the 115/220 Vac selector switch, S2, to determine that it is set to match the voltage of the ac power source. The switch can be actuated by a small screwdriver. Although these counters are wired for 115/220 Vac operation, it is possible to change them to 115/230 Vac operation be referencing Notes 7 and 8 of the main chassis schematic, Figure 6-9. Connect power plug P1 to a source of 115 or 220 Vac at 50-400 Hz. The third wire of the plug grounds the unit so that external bonding is not required. If the two prong to three prong adapter supplied with the unit must be used, be certain that the ground wire of the adapter is securely connected to a low impedance ground.

3.2.3 Receiver Connections. - Rear-panel BNC jacks connect the DRO-309A Series to the associated receiver. The counter receives LO signals from the receiver and provides a DAFC output voltage. Figures 3-3, 3-4, and 3-5 show typical interconnections between the counter and receiver.

3.2.3.1 LO Connection. - Separate counter connectors may be used for LO inputs on the VHF and UHF ranges, or both may be applied to a single input connector. The desired configuration is obtained by changing connections of coaxial cables beneath the chassis deck. If the DRO-309A Series are to be used with a receiver that has separate VHF and UHF LO output connectors, separate counter input connectors must be used. In this case, refer to Figure 5-4 and attach plug P8 to J10. Then connect the VHF LO signal to the counter in use at the rear-panel jack marked J5 VHF LO (VHF/UHF), and connect the UHF LO signal at the jack marked J4 LO UHF. If these counters are used with a receiver that has a single VHF/UHF LO output connector, they must be adapted for compatibility. In this case, refer to Figure 5-4 and attach plug P8 to the unused connection at J9. Then connect the VHF/UHF LO signal from the receiver to jack J5.

3.2.3.2 DAFC Connection. - Connect the DAFC OUTPUT jack, J3, of the DRO-309A Series to the DAFC INPUT or EXT AFC INPUT jack of the receiver to be stabilized. If the associated receiver has a tube type LO, set the DAFC mode switch on the rear panel of the counter to 1. If the receiver has a solid state LO, set the switch to 2. For receivers with an EXT AFC ON/OFF switch, the switch should always be set to ON when the DRO-309A Series and the receiver are interconnected. Use the DAFC switch on the front panel of the DRO-309A Series when it is desired to turn off the DAFC function. For receivers with an AFC/OFF/DAFC switch, leave the switch set to DAFC.

3.2.4 BCD Output Connections. - Multipin BCD OUTPUT jack J2 provides BCD information to a printed or remote readout. A mating connector is supplied with the DRO-309A Series. The main chassis schematic diagram, Figure 6-9, identifies the function of each pin of the BCD output connector. In addition to 24 lines of BCD data, J2 provides two power supply voltages, a storage pulse output, and an inhibit input. The BCD data lines can drive a printer or remote display capable of accepting inputs from TTL logic. Since the BCD data is stored, it may be read out at any time. The storage pulse is a negative-going pulse from a DTL output. When it goes low, the BCD output is updated. When the pulse goes high, the BCD is stored. After this positive transition of the storage pulse, the BCD data will remain stable for at least 9.8 msec, after which updating may occur. If desired, the inhibit line can be set low and updating ceases until it is retuned to a high state. Since the inhibiting count also prevents the DAFC circuitry from receiving new count frequency data, lengthy inhibiting should be avoided while the DAFC is in use.

3.2.5 Internal Range and Preset Control. - If the range and preset in use are to be determined by the front panel RANGE switch, the rear panel RANGE CONT switch and PRESET switch should be set to INT. The front panel RANGE switch then selects a preset number for a 21.4 MHz IF frequency on the 20-300 MHz VHF range, and a preset number for a 60 MHz IF frequency on the 200-500 MHz and 490-1000 MHz UHF ranges.

3.2.6 External Range and Preset Control. - The range and preset in use can be remotely controlled by sector lines in RANGE-PRESET CONT connector J1. A mating multipin plug is supplied with the DRO-309A Series Counter. Table 3-1 identifies the functions of the selector lines. Activation of a desired function may be effected by providing contact closure between the J1 control pin and pin K (ground) by lowering the control pin to ≤ 0.2 Vdc. This level guarantees a zero state.

3.2.6.1 Simultaneous Range and Preset Selection. - For this mode of operation, set the rear panel RANGE CONT switch to EXT, but set the PRESET switch to INT. Activation of a given selector line to choose a VHF or UHF range (pin B, C, or D) will also select a preset. The presets selected are for a 21.4 MHz IF on the VHF range or a 60 MHz first IF on the UHF ranges.

3.2.6.2 Independent Range and Preset Selection. - For this mode of operation set both the RANGE CONT and PRESET switches to EXT. Two separate selector lines must now be activated, one for each function. This mode of operation must be used with a VHF receiver having an IF of other than 21.4 MHz.

Table 3-1. External Control Functions

RANGE	Pin of J1 (Control)	PRESET	Pin of J1 (Control)
0.1-50 MHz	E	a. (21.4 MHz IF)	J
20-300 MHz VHF	D	b. (60 MHz IF)	F
200-500 MHz UHF	C	c. (8.0 MHz IF)	G
490-1000 MHz UHF	B	d. (10 MHz IF) (1604 Hz)	H

3.3 OPERATION

3.3.1 Frequency Indication. - The DRO-309A Series reads out the tuned frequency of the associated receiver with a resolution of ±1 kHz on the 20-1000 MHz ranges or ±100 Hz on the 0.1-50 MHz range. If DAFC operation is not desired, set the DAFC front panel switch to OFF.

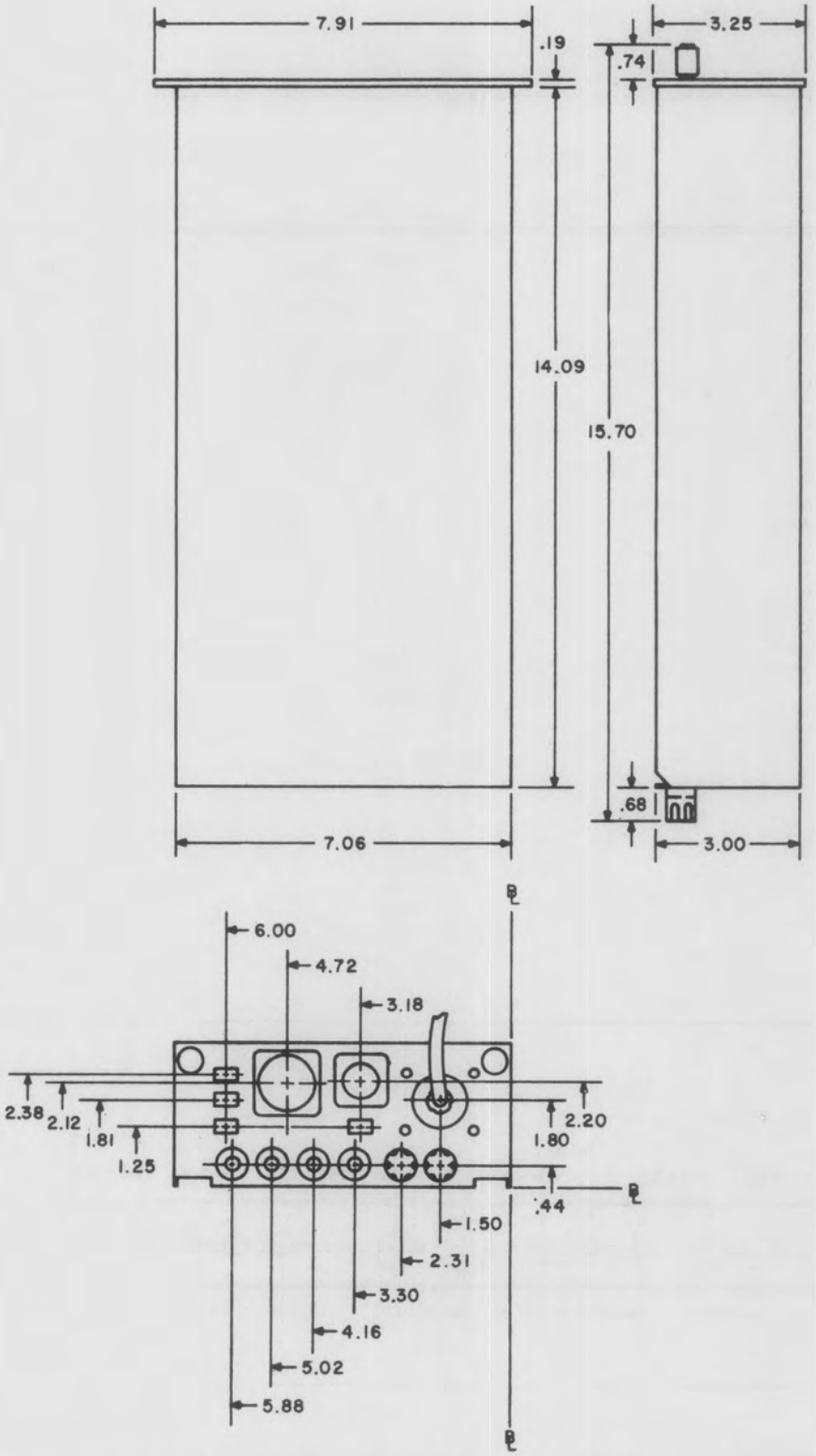


Figure 3-1. Type DRO-309A and DRO-302B Frequency Counters, Critical Dimensions

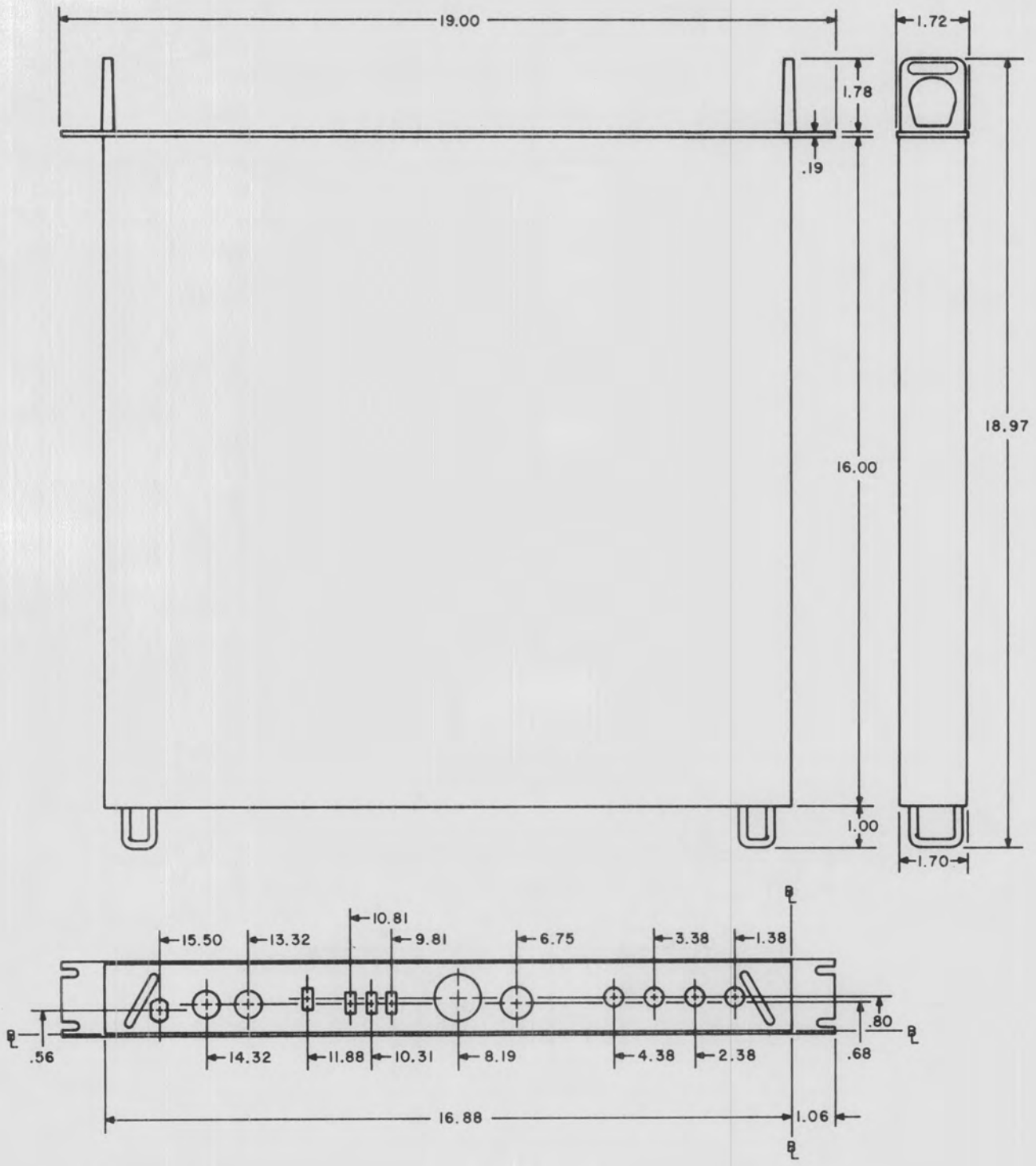
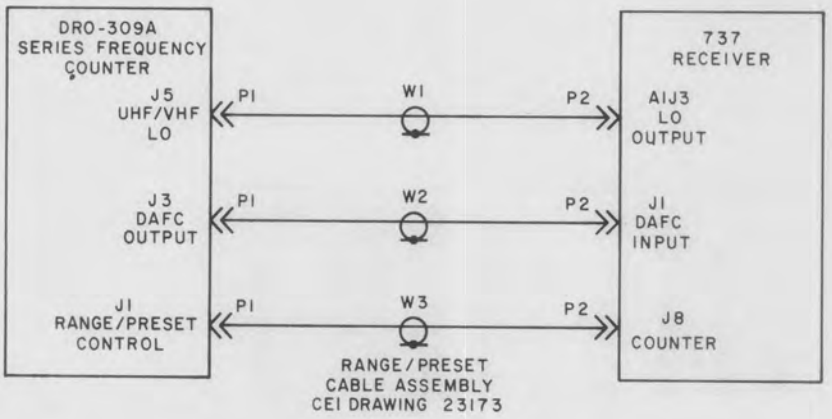
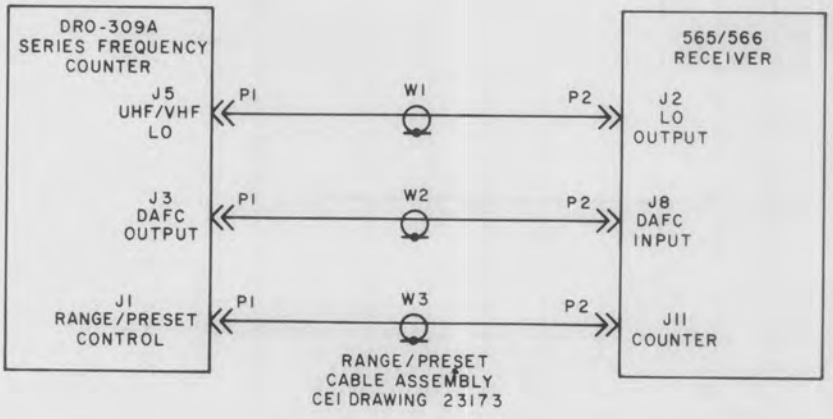


Figure 3-2. Type DRO-333 and DRO-315 Frequency Counters, Critical Dimensions



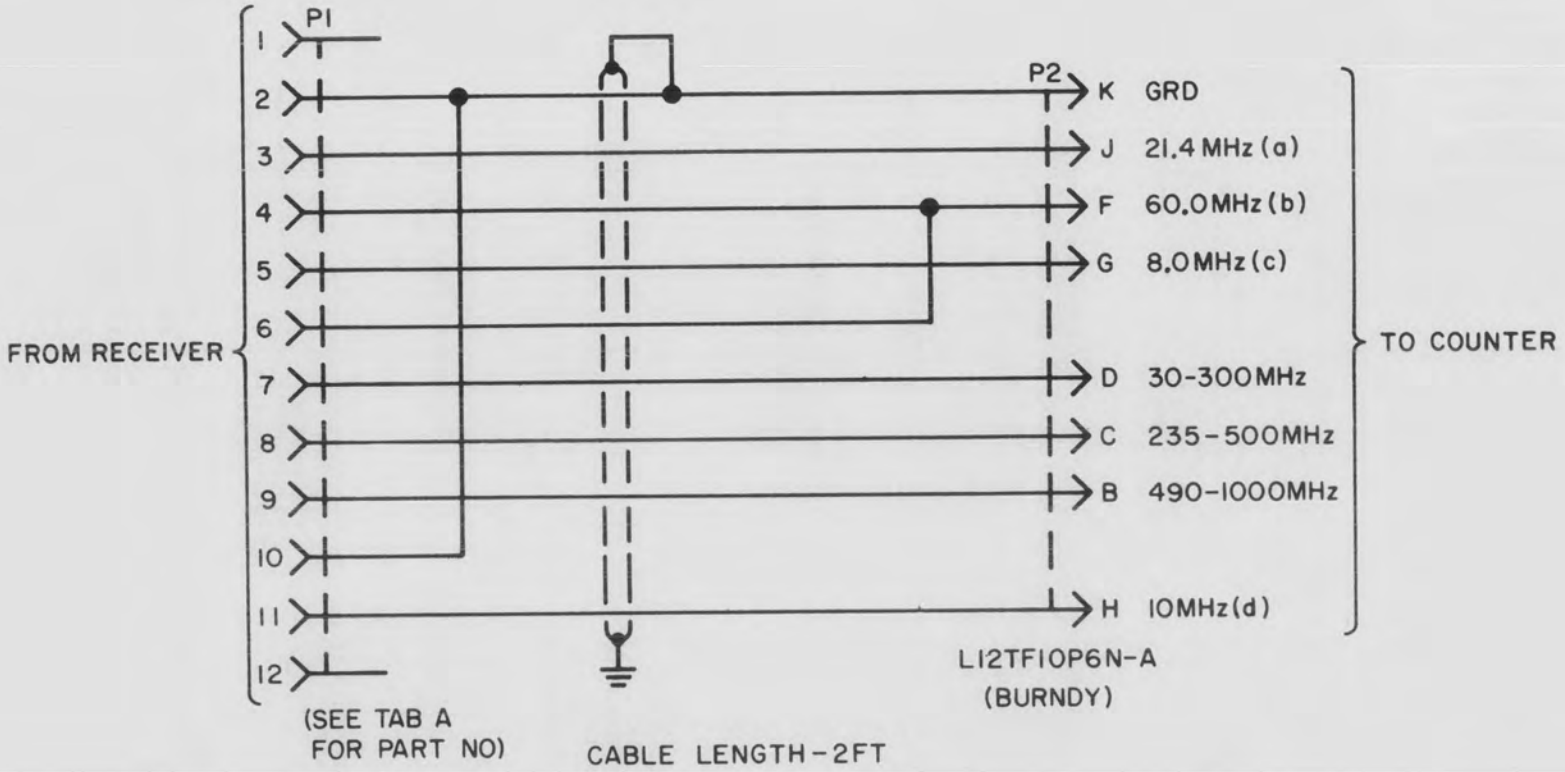
CABLE	CONNECTOR	PART NUMBER	MANUFACTURER	MFR CODE
W1	P1	BNC/UG-88U	BUNKER-RAMO/AMPHENOL	74868
W1	P2	BNC/UG-88U	BUNKER-RAMO/AMPHENOL	74868
W2	P1	BNC/UG-88U	BUNKER-RAMO/AMPHENOL	74868
W2	P2	BNC/UG-88U	BUNKER-RAMO/AMPHENOL	74868
W3	P2	DS07-12P-059	DEUTSCH.	11139
W3	P1	LI2TF10P6N-A	BURNDY	09922

Figure 3-3. DRO-309A Series and 737 Receiver, Interconnection Diagram



CABLE	CONNECTOR	PART NUMBER	MANUFACTURER	MFR CODE
W1	P1	BNC/UG-88U	BUNKER-RAMO/AMPHENOL	74868
W1	P2	BNC/UG-88U	BUNKER-RAMO/AMPHENOL	74868
W2	P1	BNC/UG-88U	BUNKER-RAMO/AMPHENOL	74868
W2	P2	BNC/UG-88U	BUNKER-RAMO/AMPHENOL	74868
W3	P2	DS07-12S-059	DEUTSCH	11139
W3	P1	LI2TF10P6N-A	BURNDY	09922

Figure 3-4. DRO-309A Series and 565/566 Receiver, Interconnection Diagram



TABULATION A

	DEUTSCH PART NO FOR P1
23173-1	DS07-12S-059
23173-2	DS07-12P-059

Figure 3-5. Range/Preset Cable, DRO-309A Series, Schematic Diagram

3.3.2 Range Selection. - The front panel rotary RANGE switch selects the range on which the DRO-309A Series will operate if internal range and preset control is employed. For the VHF and UHF bands, preset numbers for IF frequencies of 21.4 MHz and 60 MHz are automatically activated.

3.3.3 DAFC Operation. - The DAFC feature of the DRO-309A Series may be used to lock the local oscillator of the associated receiver for reception of an acquired signal, or to any arbitrary frequency within the tuning range of the receiver.

3.3.3.1 Locking to the Frequency of a Signal. - With the DAFC switch set to OFF, tune in the desired signal as accurately as possible, using the tuning meter of the receiver. Set the DAFC switch to FAST and the LO frequency will be locked. The DAFC will store the lock frequency and oppose any tendency of the receiver to drift away from it. The automatic dual correction speed will provide rapid correction if a large tuning error occurs, or delayed correction for small errors to minimize incidental FM of the receiver local oscillator. If FM is apparent when receiving CW or FSK signals, set the DAFC switch to SLOW.

3.3.3.2 Locking to an Arbitrary Frequency. - Any frequency within the tuning range of the receiver may be locked. With the DAFC switch set to OFF, tune the receiver until the readout indicates the desired frequency. Set the DAFC switch to FAST and the frequency will be locked. The DAFC switch may then be set to SLOW if desired.

3.3.3.3 Retuning. - When a change of lock frequency is desired, or when the TUNING CORRECTION meter indicates end of range, retuning is required. The TUNING CORRECTION meter shows the magnitude and direction of DAFC correction. When the pointer of the meter reaches end of scale in either direction the DAFC circuit has developed its maximum output voltage. Retuning is required to prevent loss of DAFC lock. To retune, set the DAFC switch to OFF, and follow the procedures described above. As an alternate method, the fine tuning control of the receiver may be slowly adjusted to bring the counter DAFC meter back to center of scale without switching off the DAFC.

3.4 PREPARATION FOR RESHIPMENT AND STORAGE

3.4.1 If the unit must be prepared for reshipment, the packaging methods should follow the pattern established in the original shipment. If retained, the original materials can be reused to a large extent or will at a minimum provide excellent guidance for the repackaging effort.

3.4.2 Conditions during storage and shipment should normally be limited as follows:

(1) Maximum humidity: 95% (no condensation)

(2) Temperature range: -30°C to +85°C.

SECTION IV
MAINTENANCE

4.1 GENERAL

The Type DRO-309A Series Frequency Counter has been conservatively designed to operate for extended periods of time with little or no routine maintenance. An occasional cleaning and inspection are the only preventive maintenance operations recommended. The intervals for these operations should be based on the operating environment. Should trouble occur, repair time will be minimized if the maintenance technician is familiar with the circuit descriptions found in Section II. Reference should also be made to the functional block diagram, Figure 2-1, and to the schematic diagrams found in Section VI. A complete parts list and illustrations showing part locations can be found in Section V.

4.2 CLEANING AND LUBRICATION

The unit should be kept free of dust, moisture, grease, and foreign matter to ensure trouble-free operation. If available, use low velocity compressed air to blow accumulated dust from the exterior and interior of the unit. A clean dry cloth, a soft bristled brush, or a cloth saturated with cleaning compound may also be used. These counters do not require lubrication.

4.3 INSPECTION FOR DAMAGE OR WEAR

Many potential or existing troubles can be detected by a visual inspection of the unit. For this reason, a complete visual inspection should be made for indications of mechanical and electrical defects on a periodic basis, or whenever the unit is inoperative. Electronic components that show signs of deterioration should be checked and a thorough investigation of the associated circuitry should be made to verify proper operation. Plug-in modules should be firmly mounted in their sockets, and connectors on cables should make secure contact. Damage to parts due to heat is often the result of other less apparent troubles in the circuit. It is essential that the cause of over-heating be determined and corrected before replacing the damaged parts. Mechanical parts, and front panel controls and switches should be inspected for excessive wear, looseness, misalignment, corrosion, and other signs of deterioration.

4.4 PERFORMANCE TESTS

4.4.1 General. - Selected performance tests for the DRO-309A Series Frequency Counters are presented in the following paragraphs. The tests are useful in determining that performance is adequate to meet factory test standards. The tests are also of value in troubleshooting, and can be used to verify satisfactory performance of a repaired unit. All tests are performed with the unit configured for separate VHF and UHF input connectors; that is, internal plug P8 connects to J10 (see paragraph 3.2.3.1.). If the limits and tolerances specified cannot be met, refer to the alignment and adjustment procedures in subsection 4.6.

4.4.2 Equipment Required. - The following instruments, or their equivalents, are required to execute performance tests on the Type DRO-309A Frequency Counter:

(1) Signal Generator, Hewlett Packard Model 606B.

(2) Signal Generator, Hewlett Packard Model 608E.

(3) Signal Generator, Hewlett Packard Model 612A.

(4) Oscilloscope, Hewlett Packard Model 180A, with Model 1801A Dual Channel Vertical Amplifier and 1821A Time Base.

(5) Digital Multimeter, Fluke 8100A.

(6) Frequency Counter, Computer Measurements Corporation Type 738A.

(7) VHF or UHF receiver with DAFC capability, such as CEI Division Type 977A, 555, etc.

(8) External readout or printout device capable of handling 24 lines of positive true 1248 BCD data at TTL logic levels, such as Digital Recorder, Hewlett Packard Model 5050B.

(9) Stopwatch, Micronta Corporation Model 63-635.

(10) Assorted cables and connectors.

4.4.3 Sensitivity and Overload. - These tests determine that the DRO-309A Series produces stable counting for all its rated input frequencies and levels.

4.4.3.1 Initial Equipment Setup. -

(1) Refer to Table 4-1 to determine the proper signal generator for the range to be tested. Interconnect the counter and the signal generator as shown in Figure 4-1.

(2) Set the front panel RANGE switch to the range to be tested. Set the rear panel PRESET switch of the counter to OFF, and set the RANGE CONT switch to INT.

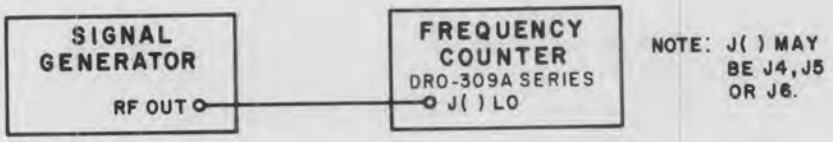


Figure 4-1. Equipment Setup for Count Input

4.4.3.2 Test Operations. -

(1) Refer to Table 4-1 to determine test frequencies for sensitivity checks. Successively tune the signal generator to the frequencies listed.

(2) At each frequency, adjust the output attenuator of the signal generator for a decreasing signal amplitude to determine the lowest level that will enable stable counting. The level must not exceed the "Maximum Sensitivity Level" shown by the table.

(3) Increase the signal generator output to the overload level indicated in Table 4-1.

(4) Successively tune the signal generator to the test frequencies shown in the table. At each frequency, verify that stable counting can be obtained.

4.4.4 Numerical Sequence. - This test verifies that all characters for each digit position of the display of the DRO-309A Series readout are in correct sequence. Proceed as follows:

4.4.4.1 Initial Equipment Setup. -

(1) Interconnect the counter and the Hewlett Packard Model 606B Signal Generator as shown in Figure 4-1. Make connection to J6 of the counter.

(2) Set the front panel RANGE switch of the counter to 0.1-50 MHz. Set the rear panel PRESET switch to OFF, and set the RANGE CONT switch to INT.

(3) Set the signal generator controls for a CW output signal at 100 kHz with a level of 250 mV rms.

4.4.4.2 Test Operations. -

(1) Slowly tune the signal generator upward in frequency to 50 MHz. Observe each digit of the display, beginning with the least significant digit. Each digit should display the characters 0 through 9 in sequence, except 0 through 5 for the most significant digit. Characters should be brightly lit and legible.

(2) Substitute the Hewlett Packard Model 612A Signal Generator for the 606B and make connection to J4 of the counter.

(3) Set the front panel switch of the counter to 490-1000 MHz.

(4) Vary the input signal frequency from 500 to 900 MHz and verify that the most significant digit displays the characters 5 through 9 in sequence.

Table 4-1. Test Frequencies

Range	0.1-50 MHz	20-300 MHz	200-500 MHz	490-1000 MHz (DRO-309A and DRO-333)
Signal Generator	H-P 606B, 608E	H-P 608E	H-P 608E, 612A	H-P 612A
Test Frequencies MHz	Max. Sensitivity Level 100 mV rms except *250 mV rms Overload Level 1V rms	Maximum Sensitivity Level, 50 mV rms Overload Level, 500 mV rms		
	0.1* 0.5 1.0 10 30 50 70*	20 60 100 150 200 250 300 325	260 350 400 450 500 560	560 600 700 800 900 1000 1060

4.4.5 Presets. - This test determines that the counter activates the proper preset numbers to provide a frequency offset for the readout.

4.4.5.1 Initial Equipment Setup. -

(1) Remove any connections to the LO input jacks of the counter.

(2) Set the rear panel RANGE CONT and PRESET switches to INT.

(3) Disconnect plug P5 of cable W4 to disable the prescaler.

Table 4-2. Preset Test Data

Preset Desig.	Internal Preset - Range	External Preset - Pin of J1	Preset Number
a	20-300	J	978.600
c	---	G	992.000
d	---	H	840.00 900.000
b	200-500 490-1000	F	940.000

4.4.5.2 Internal Presets. - Preset numbers are selected internally by the front panel RANGE switch.

Test Operations. -

(1) Using the front panel RANGE switch, successively select the ranges listed in the "Internal Preset - Range" column of Table 4-2.

(2) Verify that the corresponding numbers shown in the "Preset Number" column are obtained.

4.4.5.3 External Presets. - Preset numbers are selected externally by grounding control lines at rear panel multipin connector J1.

Test Operations. -

(1) Set the rear panel RANG CONT and PRESET switches to EXT.

(2) Successively ground the contacts listed in the "External Preset - Pin of J1" column of Table 4-2.

(3) Verify that the corresponding numbers listed in the "Preset Number" column of Table 4-2 are obtained.

4.4.5.4 Preset Defeat. - "A" pin of J1 is capable of deactivating all presets.

Test Operations. -

(1) Perform paragraph 4.4.5.3 and obtain any preset readout.

(2) Ground pin A of J1.

(3) Verify a readout of all zeros.

4.4.6 External Range Selection. - This test determines that selector lines at rear panel jack J1 can activate the desired counting range.

4.4.6.1 Initial Equipment Setup. -

(1) Refer to Table 4-1 to determine the proper signal generator for use on the 0.1-50 MHz range of the DRO-309A Series.

(2) Interconnect the signal generator and the DRO-309A as shown in Figure 4-1. Make connection to J6 of the DRO-309A Series.

(3) Set the rear panel RANGE CONT switch on the counter to EXT, and set the PRESET switch to OFF.

(4) Tune the signal generator to the highest frequency listed in Table 4-1 for sensitivity checks on the 0.1-50 MHz range, at the indicated "Max Sensitivity Level".

4.4.6.2 Test Operations. -

(1) Ground pin E of rear panel connector J1.

(2) Verify that a stable readout of the input frequency is displayed by the counter.

(3) Repeat steps (1), (2), and (4) of paragraph 4.4.6.1 and steps (1) and (2) above, but refer to the indications of Table 4-1 for the 20-300 MHz range, connect to J5, and ground pin D of J1.

(4) Repeat steps (1), (2), and (4) of paragraph 4.4.6.1 and steps (1) and (2) above, but refer to the indications of Table 4-1 for the 200-500 MHz range, connect to J4, and ground pin C of J11.

(5) Repeat steps (1), (2), and (4) of paragraph 4.4.6.1 and steps (1) and (2) above, but refer to the indications of Table 4-1 for the 490-1000 MHz range and ground pin B of J1 (DRO-309A and DRO-333).

4.4.7 Readout Accuracy. - This test determines that the maximum readout error of the counter is ±1 count of the least significant digit for the highest input frequency ever applied to the basic counter.

4.4.7.1 Initial Equipment Setup. -

(1) Interconnect the counter with the H-P 608E Signal Generator and the test counter as shown in Figure 4-2.

(2) Set the front panel RANGE switch of the counter to 0.1-50 MHz. Set the rear panel RANGE CONT switch to INT, and set the PRESET switch to OFF.

(3) Tune the signal generator to approximately 70 MHz. Set the attenuator for an output of 500 mV rms.

(4) Set the range switch of the test counter to 100 MHz. Set the GATE INTERVAL switch to X1.

(5) Energize all equipments and allow one half hour of warmup for frequency stabilization.

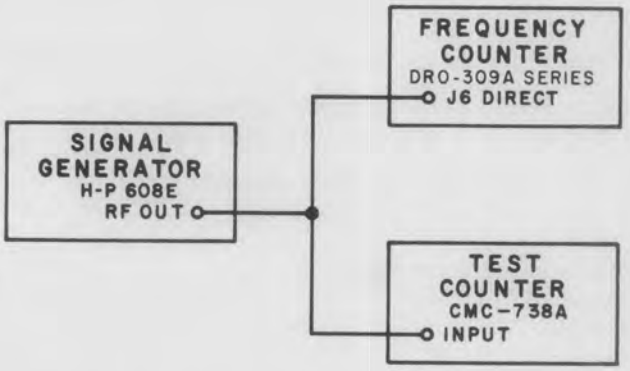


Figure 4-2. Equipment Setup for Readout Accuracy Test

4.4.7.2 Test Operations. -

(1) Observe the readouts of the two counters. Note that the least significant digit of the test counter represents 10 Hz, while the least significant digit displayed by the counter is 100 Hz.

(2) Verify that the two counters agree in readout frequency to within 100 Hz.

4.4.8 DAFC Tests. - These tests assure that the DAFC circuits can achieve lock to a desired frequency and provide proper correction voltages and correction rates. Proceed as follows:

4.4.8.1 Locking Operation. -

4.4.8.1.1 Initial Equipment Setup. -

(1) Interconnect the counter and VHF receiver with DAFC capability as shown in Figure 4-3.

(2) Set the front panel RANGE switch of the DRO-309A Series to 20-300 MHz. Set the front panel DAFC switch to OFF. Set the rear panel RANGE CONT and PRESET switches to INT.

(3) If the receiver has a tube type local oscillator, set the rear panel DAFC switch of the counter to mode 1. If the receiver has a solid state local oscillator, set the switch to mode 2.

(4) Tune the receiver to approximately the center of its tuning range.

Figure 4-3. Equipment Setup for the DAFC Lock Test

4.4.8.1.2 Test Operations. -

(1) Fine tune the receiver for an even megahertz frequency, such as XXX.000.

(2) Set the DAFC switch to FAST to lock the frequency.

(3) Using the fine tuning control of the receiver, quickly retune the receiver to a frequency approximately 10 kHz higher in frequency.

(4) Verify that after a delay of about 1 1/2 seconds, the readout quickly shifts back to the original lock frequency.

(5) Repeat steps (3) and (4), but tune the receiver to a lower frequency.

(6) Repeat steps (1) through (5) for all other characters that can be readout by the least significant digit, i.e., XXX.001, XXX.002, etc., to XXX.009.

(7) Repeat steps (1) through (5) for all other characters that can be readout by the next to least significant digit, i.e., XXX.010, XXX.020, etc., to XXX.090.

4.4.8.2 Automatic Rapid/Delayed Correction Speed. -

4.4.8.2.1 Initial Equipment Setup. -

(1) Remove the top cover from the counter. Remove the two mounting screws for card A3 and tilt the board up.

(2) Connect the oscilloscope probe to pin 13 of U11D. Refer to Figure 5-10 to identify the component.

(3) Set oscilloscope controls for a display of 2 msec/cm and 1V/cm. Use dc coupling and automatic internal triggering.

(4) Repeat all steps of paragraph 4.4.8.1.1.

4.4.8.2.2 Test Operations. -

(1) Fine tune the receiver for a readout of XXX.050 MHz.

(2) Set the DAFC switch to FAST to lock the frequency.

(3) Observe that the waveform shown in Figure 4-6c is momentarily obtained.

(4) Remove the connection from the LO input jack of the counter.

(5) Verify that after approximately 1 1/2 seconds the waveform changes to resemble Figure 4-6d.

4.4.8.3 Output Voltage Range. -

4.4.8.3.1 Initial Equipment Setup. -

(1) Interconnect equipment as shown in Figure 4-4.

(2) Set the front panel RANGE switch to 20-300 MHz and the DAFC switch to OFF. Set the rear panel DAFC switch to mode 1, and set the RANGE CONT and PRESET switches to INT.

(3) Set the digital multimeter controls to read dc voltage.

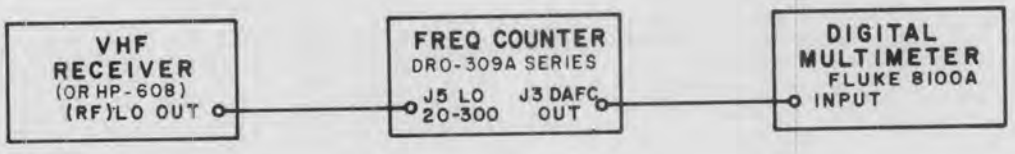


Figure 4-4. Equipment Setup for DAFC Range Test

4.4.8.3.2 Test Operations. -

(1) Tune the receiver for a readout of XXX.050. Set the front panel DAFC switch of the counter to FAST.

(2) Remove the connection between the receiver and the counter.

(3) Verify that the TUNING CORRECTION meter deflects toward the LOW mark.

(4) When the meter reaches end of scale and the output voltage stabilizes, read the voltage on the digital multimeter. The reading should be greater than +15 Vdc. -1,5 +22V

(5) Set the DAFC switch to OFF and repeat steps (1) and (2), but tune the receiver to XXX.950 kHz

(6) Observe that the TUNING CORRECTION meter deflects toward the HIGH mark and that the voltage reading is less than +5 Vdc. -2,3 +2,0

(7) Set the rear panel DAFC switch of the counter to mode 2.

(8) Repeat steps (1) through (4) except check for a reading of at least -3.0 Vdc. -4,3V

(9) Repeat steps (5) and (6), but check for a voltage reading of at least +2.5 Vdc. +2,7V

4.4.8.4 Correction Rate. -

4.4.8.4.1 Initial Equipment Setup. -

(1) Perform steps (1) through (3) of paragraph 4.4.8.3.1, except set the rear panel DAFC switch to mode 2.

4.4.8.4.2 Test Operations. -

(1) Perform step (1) of paragraph 4.4.8.3.2.

(2) Start the stopwatch and simultaneously remove the connection from the signal generator.

(3) When the digital multimeter indicates -3.0 Vdc, stop the stopwatch. A reading of less than 10 seconds should be obtained.

(4) Repeat steps (1) through (3) but use the SLOW setting on the DAFC switch. A typical result is approximately 30 seconds.

4.4.9 BCD Output. - These tests assure that the BCD output lines provide accurate data and that power supply and auxiliary functions operate properly.

4.4.9.1 Numerical Sequence.

4.4.9.1.1 Initial Equipment Setup. - Connect a printer, remote readout, or other readout device to BCD OUTPUT jack J2. Refer to paragraph 3.2.4 for interconnection information. Also connect the HP-612A as shown in Figure 4-1.

4.4.9.1.2 Test Operations. -

(1) Set the rear panel PRESET switch to OFF.

(2) Tune the HP-612A to 777.777 MHz.

(3) Verify that this readout appears on the counter and the remote readout.

(4) Tune the HP-612A to 888.888 MHz and repeat step (3).

4.4.9.2 Count Inhibit Input. -

4.4.9.2.1 Test Operations. -

(1) Obtain any stable readout.

(2) Ground pin #1 of rear panel connector J2.

(3) Disconnect the signal generator.

(4) Verify that the readout does not change until the ground at J2 is removed.

4.4.9.3 Store Pulse Output. -

4.4.9.3.1 Initial Equipment Setup. -

(1) Connect the oscilloscope to pin U of rear panel connector J2.

(2) Set the front panel RANGE control to 200-500 MHz.

(3) Set the oscilloscope controls for dc coupling with automatic internal negative triggering. Use a vertical sensitivity of 1V/cm and a time base of 1 msec/cm.

4.4.9.3.2 Test Operation. - Verify the presence of a negative going pulse with a width of approximately 0.4 msec and an amplitude of greater than 2V P-P.

4.4.9.4 Output Power. -

4.4.9.4.1 Initial Equipment Setup. - Set the controls of the digital multimeter to read dc voltage.

4.4.9.4.2 Test Operations. -

(1) Connect the multimeter probe to pin D of J2. Verify a reading of approximately +5 Vdc.

(2) Connect the multimeter probe to pin J of J2. Verify a reading of approximately -5 Vdc.

4.5 TROUBLESHOOTING

4.5.1 General. - Troubleshooting efforts should be directed toward localizing the problem to a defective module or circuit. This section contains aids for this process, including a troubleshooting chart, a table of typical voltage readings, and photographs of typical spectra and waveforms. The performance test (subsection 4.4) and the alignment procedures (subsection 4.6) are also of value in diagnosing the causes of malfunction. Background information needed for a thorough understanding of the theory of operation is provided by the circuit descriptions in Section II, the functional block diagram (Figure 2-1), and the schematic diagrams in Section VI.

4.5.2 Equipment Required. - Trouble isolation to the module or subassembly level can be accomplished by use of the following instruments or their equivalents:

(1) Signal Generator, Hewlett Packard Model 608E.

(2) Oscilloscope, Hewlett Packard Model 180A, with Model 1801A Dual Channel Vertical Amplifier and 1821A Time Base.

(3) Digital Multimeter, Fluke 8100A.

(4) VHF Receiver with DAFC Capability, such as the CEI Division Type 977, 555, etc.

(5) Assorted cables, connectors, and adapters.

NOTE

The following instruments are considered useful but nonessential for execution of troubleshooting procedures.

(6) Spectrum Analyser - RF Section, Hewlett Packard Model 8554L, with Spectrum Analyser - Display Section, Model 8552A, and Oscilloscope Main Frame, Model 140S.

4.5.3 Localization of Faults. - The primary methods of localizing failed modules and components are discussed below.

4.5.3.1 Visual Inspection. - A thorough visual inspection may be sufficient to locate the source of trouble. This method is valueable in avoiding additional damage which might result from continued operation of the equipment. Look for burned or crushed components, broken wires, loosened retaining brackets on plug-in modules, inproper mating of connectors, etc.

4.5.3.2 Troubleshooting Chart. - Table 4-3 gives a detailed listing of possible failure indications, with procedures to be followed in diagnosing faults. The first step is to decide which of the failure symptoms listed on the left side of the chart is applicable. Waveform and voltage measurements or signal injection are then indicated to isolate the faulty module or component. Faults on the gate generator board, A3, are diagnosed primarily by observation of waveforms. For the count, decode, and display card, A4, the readout on the numeric indicators may indicate the cause of the failure. Failure of the ac input circuitry or power supplies is usually indicated by complete failure of the readout.

4.5.3.3 Signal Injection. - Defective modules in the signal path may be quickly identified by applying signals at their inputs, working backwards along the signal path, through increasingly higher frequency ranges. Table 4-4 indicates injection points and type of signal to be applied. Most of the points indicated have an adjacent ground terminal which should be tied to the shield of the coaxial cable used to inject the signal. The rear panel PRESET switch should be set to OFF, the RANGE CONT switch should be set to INT, and the front panel RANGE switch should be set as indicated in the table.

4.5.3.4 Typical Spectra and Waveform Photographs. - Figure 4-5 and 4-6 show spectrum displays and waveforms from modules of the DRO-309A Series. Figure 4-5 illustrates the counting path. The spectra at the outputs of prescaler modules of A1, Figures 4-5a and 4-5b, and the waveforms from count, decode, and display card A4, Figures 4-5c through 4-5f, make it possible to trace a signal from an LO input jack through all counting circuits. (If a spectrum analyzer is not available, the signal injection procedures of paragraph 4.5.3.3 are indicated for prescaler troubleshooting.) The last waveform from the counting path is Figure 4-5f. This pulse is the BCD 8 output or carry from the first decade of counting on A4. The carry pulses from following decades have the same shape, but with the period multiplied by 10 for each additional decade. Figure 4-6 shows waveforms from gate generator A3 and power supply A2. Figures 4-6a and 4-6b show outputs of the gate generator timing circuits. A single photograph is shown to represent three waveforms -- reset, preset, and storage strobe. These waveforms are identical but staggered in time. Two waveforms, Figures 4-6c and 4-6d, illustrate the automatic rapid/delayed DAFC correction speeds. Additionally, two waveforms associated with power supplies are shown: Figure 4-6e illustrates operation of the voltage multiplier on A3, and 4-6f shows the waveform produced by the switching pass transistor in power supply module A2.

4.5.3.5 Typical Voltage Reading Chart. - Once a defective module has been located, the failed component may be determined by use of voltage readings. Table 4-5a lists voltage readings for transistors in the power supply and prescaler modules. Readings are approximate and intended only for troubleshooting purposes; some readings vary directly with ac input voltage. Figure 4-5b gives typical voltages at pins of the power supply module.

4.5.4 Failure Analysis. - Once the trouble has been localized, the unit can be returned to operating condition by substituting a spare module or subassembly known to be in good condition. Prior to performing corrective action on the faulty module, troubleshooting procedures should be reviewed to determine that the fault discovered is the actual cause of the trouble rather than a result.

4.5.5 Subassembly Removal, Repair, and Replacement. - All subassemblies of the DRO-309A Series are constructed on etched circuit cards. Several modules are plug-in cards. These modules may be removed by pulling them out of their sockets after releasing the retaining devices. Other modules are attached to the main chassis or a subchassis by mounting screws and are hard wired to a harness. Removal of these boards involves unsoldering leads from eyelets on the modules and removing the mounting screws. No special problems should be encountered in repair of cards A2, A3, and A4 if good rework practices are followed. Observe precautions to avoid application of excessive heat to component leads and etched circuit patterns. A minimum amount of solder should be employed.

NOTE

Prescaler P. C. boards A1A1, A1A2, and A1A3 are particularly susceptible to overheating during soldering, due to the low mass of the miniature components used. Use of a low wattage soldering iron with a small tip is essential. An iron consisting of the following components is recommended. All are manufactured by the Ungar Division of Eldon Industries:

No. 7155 Stepped Chisel Tiplet
No. 4035 Heating Unit
No. 776 Handle

Table 4-3. Troubleshooting Chart

Table 4-3a. Faults Indicated by Abnormal Readouts

TROUBLE INDICATION	PROBABLE FAULT	DIAGNOSTIC PROCEDURE
(1) All numeric indicators dark.	Blown fuse. Faulty power switch or 115/230 Vac switch. Defective power transformer. Failed A4U41 or A4Q2. Failed Switching regulator.	Replace. Check continuity through S1 and S2. Check continuity of windings. Check for +5 Vdc at A2TP1.
(2) One numeric indicator shows incomplete character.	Defective numeric indicator IC.	Substitute component.
(3) A numeric indicator has any gross failure indication; indicators to the left readout normally.	Defective storage IC on A4. Defective numeric indicator on A4.	Substitute component. Substitute component.
(4) A numeric indicator has any gross failure indication; indicators to the left also failed.	Failure of decade counter IC on A4.	Substitute component.
(5) Only readout is all zeros, with or without input.	Reset pulse from A3 failed; stays low (active).	Check waveform per Figure 4-6a.
(6) Only readout is a stable indeterminate number, with or without input.	Storage strobe pulse from A3 failed, stays high (inactive).	Check waveform per Figure 4-6a.
(7) Only readout is preset number with or without input.	Signal gate pulse from A3 failed, stays low (inactive).	Check waveform per Figure 4-6b.
(8) Erratic readout with or without input.	Storage strobe pulse from A3 failed, stays low (active).	Check waveform per Figure 4-6a.

Table 4-3a. Faults Indicated by Abnormal Readouts (Continued)

TROUBLE INDICATION	PROBABLE FAULT	DIAGNOSTIC PROCEDURE
	Signal gate pulse from A3 failed, stays high (active).	Check waveform per Figure 4-6b.
	Reset pulse from A3 failed, stays high (inactive).	Check waveform per Figure 4-6a.
(9) Readout with input is same as input frequency instead of lower by IF frequency.	Rear panel PRESET switch set to OFF.	Set switch per paragraph 3.2.5 or 3.2.6.
	Preset pulse from A3 failed, stays high (inactive).	Check waveform per Figure 4-6a.
(10) Only readout is preset number; except least significant digit responds to input.	Preset pulse from A3 failed, stays low (active).	Check waveform per Figure 4-6a.
(11) No response to input, VHF and UHF ranges.	Failed 325 MHz ÷ 4 or ÷ 8 A1A3.	Inject signals per paragraph 4.5.3.3.
(12) No response to input, any UHF ranges.	Failed 560 or 1060 MHz binary dividers (A1A2 or A1A1).	Same as (11).

Table 4-3b. Faults Indicated by DAFC Malfunction

TROUBLE INDICATION	PROBABLE FAULT	DIAGNOSTIC PROCEDURE
(1) DAFC runs away from desired frequency, or jumps 100 kHz and locks.	Rear panel DAFC switch set to wrong mode.	Set switch per paragraph 3.2.3.
(2) DAFC failed on one correction rate only.	Defective DAFC switch, S6.	Make continuity checks.
(3) DAFC will not lock, all correction rates.	Defective storage or comparator IC's on A3.	Substitute components.
	Defective FET A3Q4.	Substitute component.
(4) TUNING CORRECTION meter does not read zero when DAFC switch is set to OFF.	Erroneous DAFC zero adjustment.	Make adjustment per paragraph 4.6.4.
(5) Automatic rapid/delayed correction speed inoperative.	Defective speed control IC's A3U11, A3U12, A3U14.	Substitute components; test per paragraph 4.4.8.
(6) Mode 1 only has failed output voltage.	Defective mode inverter IC, A3U14B.	Same as (5).
	Vcc_2 failed on A3.	Check for +18 Vdc at A3CR18 cathode.

Table 4-4. Signal Injection Chart

Range	Injection Signal	Injection Point
0.1-50 MHz	70 MHz at 250 mV rms	A1A3E4
20-300 MHz	325 MHz at 50 mV rms	A1A3E1 and A1A2E8
200-500 MHz	560 MHz at 100 mV rms	A1A2E1
490-1000 MHz (DRO-309A and DRO-333)	1060 MHz at 50 mV rms	A1A1E1

Table 4-5. Typical Voltage Readings

Table 4-5a. Typical Transistor Element Voltages

Ref. Desig.	Type	Emitter	Base	Collector
A1A1Q1	2N3251	4.5	3.9	0.8
A1A1Q2	22840-2	0.0	0.7	4.5
A1A1Q3	2N3251	4.4	3.8	0.8
A1A1Q4	22840-2	0.0	0.8	4.4
A1A1Q5	22840-1	1.6	2.3	4.1
A1A1Q6	22840-1	1.6	2.3	4.4
A1A2Q1	2N3251	4.6	4.0	0.9
A1A2Q2	22840-2	0.0	0.8	4.6
A1A2Q3	22840-2	1.2	1.8	4.1
A1A2Q4	22840-2	1.2	1.8	4.2
A1A2Q5	2N3572	-0.7	0.0	4.8
A1A3Q1	2N3572	-1.7	-1.2	-0.7
A1A3Q2	2N3572	-0.7	0.0	4.8
A1A3Q3	2N5179	-1.0	-0.2	4.8
A2Q1	2N4037	-5.0	-5.6	-13
A2Q2	2N5039	Note 4	Note 4	12
A2Q3	2N2905A	12	Note 4	Note 4

NOTE: A1A1Q1 through Q6 used in DRO-309A and DRO-333 only.

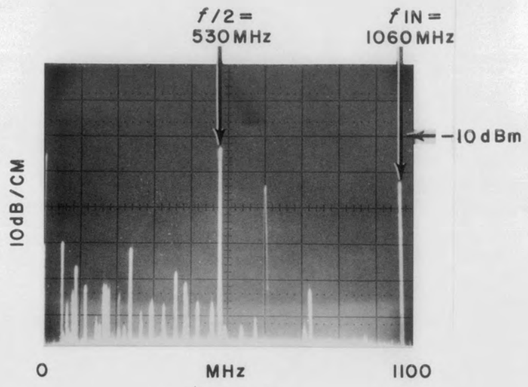


Figure 4-5a
Output of 1060 MHz
Binary Divider, A1A1E5

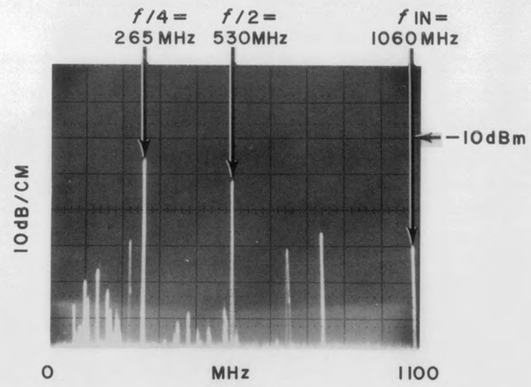


Figure 4-5b
Output of 560 MHz
Binary Divider, A1A2E6

NOTES:

(1) Refer to paragraph 4.5.2 for recommended test instruments.

(2) To obtain spectra 4-5a and 4-5b, apply an input of 1060 MHz at 100 mV rms to the DRO-309A and DRO-333 at J4 and set the RANGE switch to 490-1000 MHz. For the DRO-302B and DRO-315 apply 530 MHz at J3, and use the 200-500 MHz range.

(3) To obtain waveforms 4-5c through 4-5f, apply an input of 10 MHz at 100 mV rms at J6 and set the RANGE switch to 0.1-50 MHz.

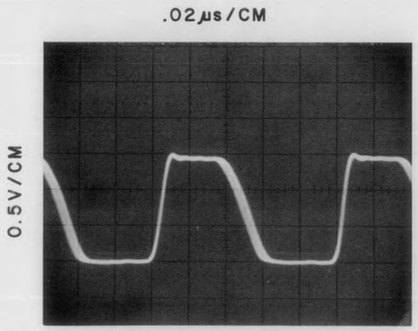


Figure 4-5c
Output of Video Amplifier of
Count, Decode and Display,
A4Q1 Base

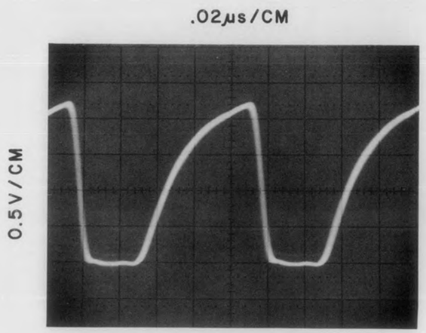


Figure 4-5d
Output of Trigger Transistor
of Count, Decode, and Display,
A4Q1 Collector

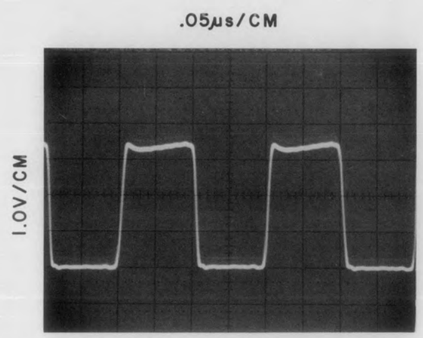


Figure 4-5e
Output of Count-By-Two of
Count, Decode and Display,
A4U2 Pin 11

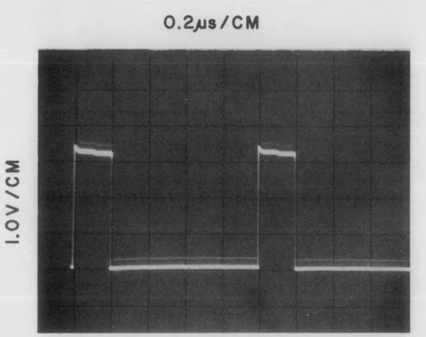


Figure 4-5f
Output of Count-By-Five
of Count, Decode and Display,
A4U3 Pin 12

Figure 4-5. Typical Spectra and Waveforms from the Counting Path

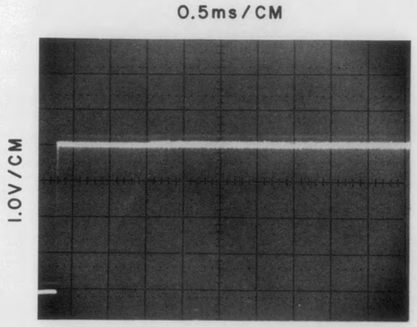


Figure 4-6a
Reset, Preset, or Storage
Strobe From Gate Generator,
A3U9A Pin 8,
A3U8B Pin 8, or A3U8A Pin 6

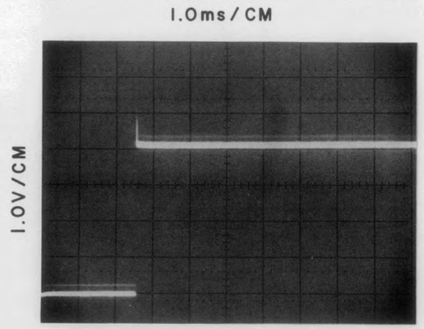


Figure 4-6b
Signal Gate From Gate
Generator, A3U13F Pin 2

NOTES:

(1) Waveforms 4-6a and 4-6b are taken with the RANGE switch set to 0.1-50 MHz; all others are 20-300 MHz.

(2) To obtain waveforms 4-6c and 4-6d, refer to paragraph 4.4.8.2.

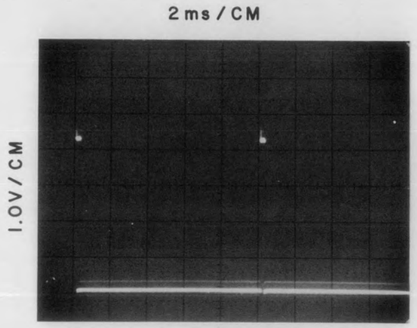


Figure 4-6c
DAFC Duty Cycle Strobe
on Gate Generator, Delayed
Speed, A3U11D, Pin 13

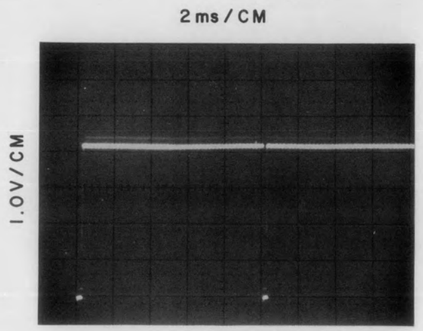


Figure 4-6d
DAFC Duty Cycle Strobe
on Gate Generator, Rapid
Speed, A3U11D Pin 13

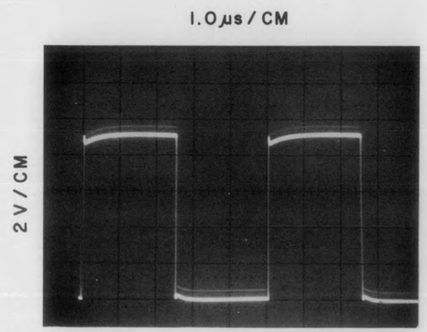


Figure 4-6e
Voltage Multiplier on Gate
Generator, Q6 Collector

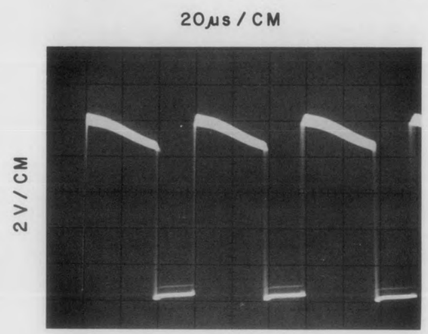


Figure 4-6f
Output of Pass Transistor of
Switching Regulator, A2Q2 Emitter

Figure 4-6. Typical Waveforms From the Gate Generator and Power Supply

Table 4-5b. Typical Module Pin Voltages Type 76192 Switching Regulator, A2

Pin	1	2 & 3	4	6	7 & 8	20, 21, 22
Voltages	12	10.5 Vac	-13	-5.0	0.0	5.0

NOTES: (1) Input power is 115 Vac 60 Hz.

(2) All readings are positive dc volts referenced to ground except as noted.

(3) All readings in A1 are taken with a 560 MHz, 100 mV rms signal applied to J3 with unit configured for common VHF/UHF input connector per paragraph 3.2.3.1. RANGE switch is set to 490-1000 MHz (200-500 MHz for DRO-302B and DRO-315). Voltmeter probe should be isolated from circuit under test by a series 1 kΩ resistor to decrease effect of shunt capacitance.

(4) DC readings not applicable; the switching waveform shown in Figure 4-6f is present.

4.6 ALIGNMENT AND ADJUSTMENT PROCEDURES

4.6.1 General. - The alignment procedures given here are suitable when making adjustments after replacing transistors or other components. Alignment should be performed only with suitable equipment by technicians familiar with the unit. Malfunctions indicated by the performance tests in subsection 4.4 may be corrected by execution of the alignment procedures. Only those controls specifically referred to within a series of steps given for aligning a particular circuit affect the alignment of that circuit. Those controls not mentioned in any one series of steps may be left in any position.

4.6.2 Test Equipment Required. - The following instruments, or their equivalents, are required to perform adjustments on the DRO-309A Series Frequency Counter:

(1) Digital Multimeter, Fluke 8100A

(2) Signal Generator, Hewlett Packard Model 608E

(3) Signal Generator, Hewlett Packard Model 612A.

4.6.3 Adjustment of Switching Regulator. - Proceed as follows:

4.6.3.1 Initial Equipment Setup. -

(1) Set controls of the digital multimeter to read dc voltage.

(2) Connect the multimeter probe to E11 of module A1A3, which is mounted on top of the chassis deck.

4.6.3.2 Adjustment Operation. - Read the regulator output voltage on the multimeter. Adjust A2R7, the only potentiometer on the module, for a reading of +5.00 Vdc.

4.6.4 Zero Adjustment of DAFC Voltage. - Proceed as follows:

4.6.4.1 Initial Equipment Setup. -

(1) Remove the top cover from the counter.

(2) Tilt up the top printed circuit card beneath the cover (A3) after releasing the retaining screws.

(3) Interconnect the counter and the Fluke 8100A Digital Multimeter as shown in Figure 4-7.

(4) Set the front panel DAFC switch of the counter to OFF. Set the rear panel DAFC switch to mode 2.

(5) Set the digital multimeter controls to read dc voltage.

4.6.4.2 Test Operations. -

(1) Refer to Figure 5-10 to identify potnetiometer A3R14.

(2) Adjust the potentiometer so that the digital multimeter reads less than ±0.1 Vdc.

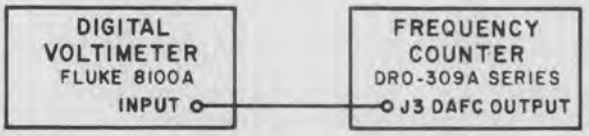


Figure 4-7. Equipment Setup for DAFC Zero Adjustment

4.6.5 Alignment of Prescaler Assembly. - Before proceeding, configure unit for separate UHF/VHF inputs; that is, connect internal plug P8 to J10 (see paragraph 3.2.3.1). Set the rear panel RANGE CONT switch to INT and the PRESET switch to OFF. Remove the cover from the prescaler assembly A1, which is located beneath the chassis deck.

4.6.5.1 VHF Alignment. -

4.6.5.1.1 Initial Equipment Setup. -

(1) Set the front panel RANGE switch of the DRO-309A to 20-300 MHz.

(2) Interconnect the counter and the Hewlett Packard Model 608E Signal Generator as shown in Figure 4-1. Make connection to J5, VHF LO (VHF/UHF) of the counter.

4.6.5.1.2 Adjustment Operations, Bias and AGC Threshold. -

(1) Adjust the signal generator controls for a CW output signal with a level of 100 mV rms.

(2) Tune the signal generator to 325 MHz, or to the highest frequency that will give a stable read-out on the counter.

(3) Increase the frequency of the signal generator output until the count just fails.

(4) Refer to Figure 5-8 to identify potentiometers A1A3R9 and A1A3R10.

(5) Adjust bias set potentiometer A1A3R9 to restore a stable count. Determine the range of rotation of the control that provides proper function and set the control to the center of this range.

(6) Repeat step (5), but adjust AGC threshold set potentiometer A1A3R10.

(7) Repeat steps (3), (5), and (6), until no further increase in maximum count frequency can be obtained. Note that an adjustment of A1A3R9 must always be followed by an adjustment of A1A3R10.

4.6.5.1.3 Adjustment Operations, Emitter Trimmer Capacitors. -

(1) Tune the signal generator to 180 MHz.

(2) Reduce the output level of the signal generator until the count displayed by the counter just fails.

(3) Refer to Figure 5-8 to locate trimmer capacitors A1A3C3 and A1A3C4.

(4) Adjust A1A3C4 to restore a stable count.

(5) Repeat steps (2) and (4) until no lower input level can be counted.

(6) Tune the signal generator to 325 MHz and repeat steps (2), (4), and (5), adjusting A1A3C3.

(7) Vary the signal level from 35 mV rms to 500 mV rms and verify that stable counting can be obtained.

4.6.5.2 Low UHF Alignment. -

4.6.5.2.1 Initial Equipment Setup. -

(1) Disconnect all inputs to the counter.

(2) Set the front panel RANGE switch to 200-500 MHz.

(3) Set controls of the multimeter to read dc voltage.

4.6.5.2.2 Adjustment Operations. -

(1) Refer to Figure 5-7 to locate components A1A2R10 and A1A2C10.

(2) Connect the multimeter probe to the junction of these two components.

(3) Adjust the potentiometer for a reading of +1.65 Vdc.

4.6.5.3 High UHF Alignment. -

4.6.5.3.1 Initial Equipment Setup. -

(1) Disconnect all inputs to the counter.

(2) Set the front panel RANGE switch 490-1000 MHz (DRO-309A and DRO-333). Set the rear panel PRESET switch to OFF, and the RANGE CONT switch to INT.

4.6.5.3.2 Adjustment Operation.

(1) Refer to Figure 5-6 to locate potentiometer A1A1R18.

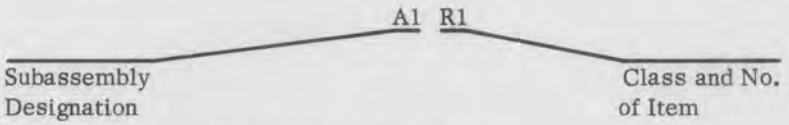
(2) Adjust the potentiometer until the numerical readout indicates approximately 950 MHz. The last three digits need not be stable.

SECTION V

REPLACEMENT PARTS LIST

5.1 UNIT NUMBERING METHOD

The unit numbering method of assigning reference designations (electrical symbol numbers) has been used to identify assemblies, subassemblies (and modules), and parts. An example of the unit method follows:



Identify from right to left as: First (1) resistor (R) of first (1) subassembly (A)

As shown on the main chassis schematic, components which are an integral part of the main chassis have no subassembly designation.

5.2 REFERENCE DESIGNATION PREFIX

Partial reference designations have been used on the equipment and on the illustrations in this manual. The partial reference designations consist of the class letter(s) and identifying item number. The complete reference designations may be obtained by placing the proper prefix before the partial reference designations. Reference Designation Prefixes are provided on drawings and illustrations in parenthesis within the figure titles.

5.3 LIST OF MANUFACTURERS

Mfr. Code	Name and Address
00779	AMP, Incorporated P. O. Box 3608 Harrisburg, Pennsylvania 17105
01037	Pyroferric-New York, Inc. 621 East 216th Street Bronx, New York 10467
01121	Allen-Bradley Company 1201 South 2nd Street Milwaukee, Wisconsin 53212
01295	Texas Instruments, Incorporated Semiconductor-Components Division 13500 North Central Expressway Dallas, Texas 75231
02114	Ferroxcube Corporation P. O. Box 359 Mt. Marion Road Saugerties, New York 12477
02735	RCA Corporation Solid State Division Route 202 Somerville, New Jersey 08876
04713	Motorola Semiconductor Products, Inc. 5005 East McDowell Road Phoenix, Arizona 85008
07263	Fairchild Camera and Instrument Corp. Semiconductor Division 464 Ellis Street Mountain View, California 94040
09353	C & K Components, Incorporated 103 Morse Street Watertown, Massachusetts 02172
09922	Burndy Corporation Richards Avenue Norwalk, Connecticut 06852
12969	Unitrode Corporation 580 Pleasant Street Watertown, Massachusetts 02172
13103	Thermalloy Company 8717 Diplomacy Row Dallas, Texas 75247

Mfr. Code	Name and Address
14632	Watkins-Johnson Company 700 Quince Orchard Road Gaithersburg, Maryland 20760
18324	Signetics Corporation 811 East Argues Avenue Sunnyvale, California 94086
19505	Applied Engineering Products Co. Division of Samarius Inc. 26 East Main Street Ansonia, Connecticut 06401
21604	The Buckeye Stamping Company 555 Marion Road Columbus, Ohio 43207
27014	National Semi-Conductor Corporation 2950 San Ysidro Way Santa Clara, California 95051
27193	Cutler-Hammer, Incorporated Special Products Division 402 North 27th Street Milwaukee, Wisconsin 53216
28480	Hewlett-Packard Company 1501 Page Mill Road Palo Alto, California 94304
49956	Raytheon Company 141 Spring Street Lexington, Massachusetts 02173
56289	Sprague Electric Company Marshall Street North Adams, Massachusetts 01247
71279	Cambridge Thermionic Corporation 455 Concord Avenue Cambridge, Massachusetts 02138
71400	Bussman Manufacturing Division of McGraw-Edison Company 2536 West University Street St. Louis, Missouri 63107
71700	General Cable Corporation Cornish Wire Company Division 101 Water Street Williamstown, Massachusetts 01267
71785	Cinch Manufacturing Company Howard B. Jones Division 1026 South Homan Avenue Chicago, Illinois 60624
72136	Electro Motive Manufacturing Co., Inc. South Park and John Streets Willimantic, Connecticut 06226
72982	Erie Technological Products, Inc. 644 West 12th Street Erie, Pennsylvania 16512
73138	Beckman Instruments, Inc. Helipot Division 2500 Harbor Boulevard Fullerton, California 92634
72899	JFD Electronics Company Division of Stratford Retreat House 15th at 62nd Street Brooklyn, New York 11219
75915	Littelfuse, Incorporated 800 East Northwest Highway Des Plaines, Illinois 60016
80058	Joint Electronic Type Designation System
80131	Electronic Industries Association 2001 Eye Street, N. W. Washington, D. C. 20006
81312	Winchester Electronics Division Litton Industries Incorporated Main Street and Hillside Avenue Oakville, Connecticut 06779
81349	Military Specifications
82389	Switchcraft, Incorporated 5555 North Elston Avenue Chicago, Illinois 60630
87034	Marco-Oak Industries, Division of Oak Electro/Netics Corporation 207 South Helena Street Anaheim, California 92803

Mfr. Code	Name and Address
88256	Litton Industries USECO Division 13536 Saticoy Street Van Nuys, California 91402
91418	Radio Materials Company 4242 West Bryn Mawr Avenue Chicago, Illinois 60646
91984	Maida Development Company 214 Academy Street Hampton, Virginia 23369
93332	Sylvania Electric Products, Inc. Semiconductor Products Division 100 Sylvan Road Woburn, Massachusetts 01801
95121	Quality Components, Inc. P. O. Box 113 St. Mary's, Pennsylvania 15857
97137	TRW Electronic Components Division Chicago, Illinois 60600
99848	Wilco Corporation 4030 West 10th Street P. O. Box 22248 Indianapolis, Indiana 46222

5.4 PARTS LIST

The parts list which follows contains all electrical parts used in the equipment and certain mechanical parts which are subject to unusual wear and damage. When ordering replacement parts from the Watkins-Johnson Co., specify the type and serial number of the equipment and the reference designation and description of each part ordered. The list of manufacturers provided in paragraph 5.3 and the manufacturer's part numbers for components are included as a guide to the user of the equipment in the field. These parts may not necessarily agree with the parts installed in the equipment, however, the parts specified in this list will provide satisfactory operation of the equipment. Replacement parts may be obtained from any manufacturer as long as the physical and electrical parameters of the part selected agree with the original indicated part. In the case of components defined by a military or industrial specification, a vendor which can provide the necessary component is suggested as a convenience to the user.

NOTE

As improved semiconductors become available it is the policy of CEI Division to incorporate them in proprietary products. For this reason some transistors, diodes, and integrated circuits installed in the equipment may not agree with those specified in the parts lists and schematic diagrams of this manual. However, the semiconductors designated in the manual may be substituted in every case with satisfactory results.

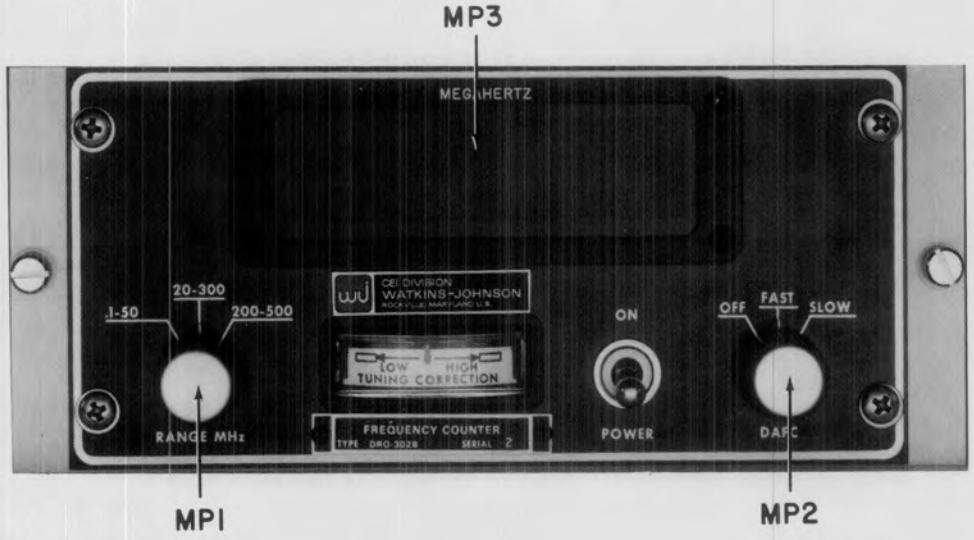


Figure 5-1. Type DRO-302B Frequency Counter, Front View, Location of Components

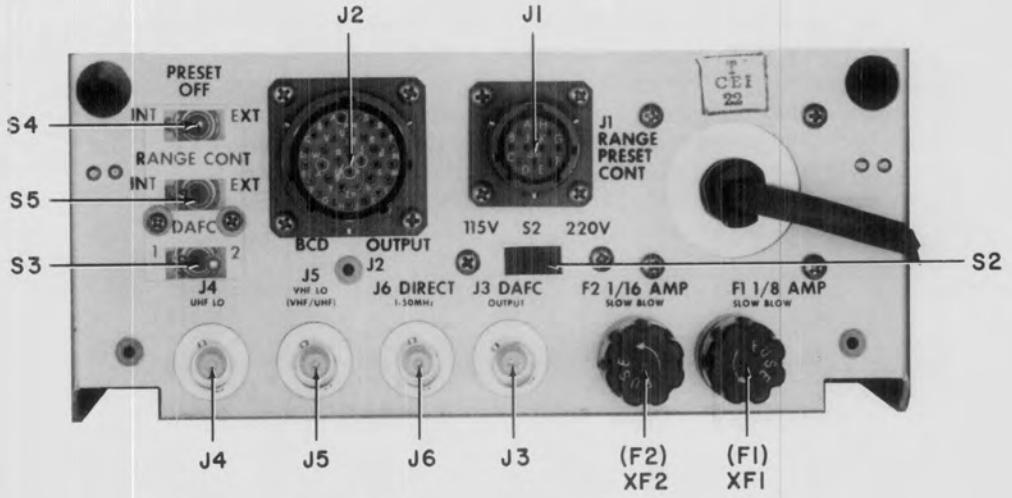


Figure 5-2. Type DRO-302B Frequency Counter, Rear View, Location of Components

5.4.1 Type DRO-309A & DRO-302B Frequency Counters, Main Chassis

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
A1	PRESCALER ASSEMBLY (DRO-309A ONLY)	1	79904-1	14632	
A1	PRESCALER ASSEMBLY (DRO-302B ONLY)	1	79904-2	14632	
A2	SWITCHING REGULATOR	1	76192	14632	
A3	GATE GENERATOR AND DAFC	1	79907	14632	
A4	COUNT, DECODE AND DISPLAY	1	79912-1	14632	
CR1	DIODE	2	1N995	80131	93332
CR2	Same as CR1				
C1	CAPACITOR, CERAMIC, FEEDTHRU: 0.05 μF, GMV, 300V	46	MS001DA503P	01121	
C2 thru C25	Same as C1				
C26	CAPACITOR, CERAMIC, FEEDTHRU: 1000 pF, GMV, 500V	1	2404-000X5U0-102P	72982	
C27	Same as C1				
C28	Same as C1				
C29	Same as C1				
C30	CAPACITOR, CERAMIC, FEEDTHRU: 5000 pF, 20%, 500V	1	2404-000X5U0-502M	72982	
C31 thru C48	Same as C1				
C49	CAPACITOR, ELECTROLYTIC, ALUMINUM: 1000 μF, -10+75%, 15V	1	34D108G015GL4	56289	
C50	CAPACITOR, ELECTROLYTIC, ALUMINUM: 8000 μF, -10+75%, 15V	1	39D808G015JT4	56289	
C51	CAPACITOR, ELECTROLYTIC, ALUMINUM: 150 μF, 10%, 15V	1	CS13BD157K	81349	
FL1	FILTER, LOW-PASS	1	JN33-694B	56289	
F1	FUSE, CARTRIDGE: 1/8 AMP, 3AG, SLOW	1	MDL1/8	71400	
F2	FUSE, CARTRIDGE: 1/16 AMP, 3AG, SLOW	1	MDL1/16	71400	
J1	CONNECTOR, RECEPTACLE	1	L12TE10S2N-A	09922	
J2	CONNECTOR, RECEPTACLE	1	L18TE32S2N-A	09922	
J3	CONNECTOR, RECEPTACLE	4	17825-1002	74868	
J4	Same as J3				
J5	Same as J3				
J6	Same as J3				
J7	CONNECTOR, RECEPTACLE	1	M10SLRN	81312	
J8	CONNECTOR, RECEPTACLE	2	UG-1468/U	80058	74868

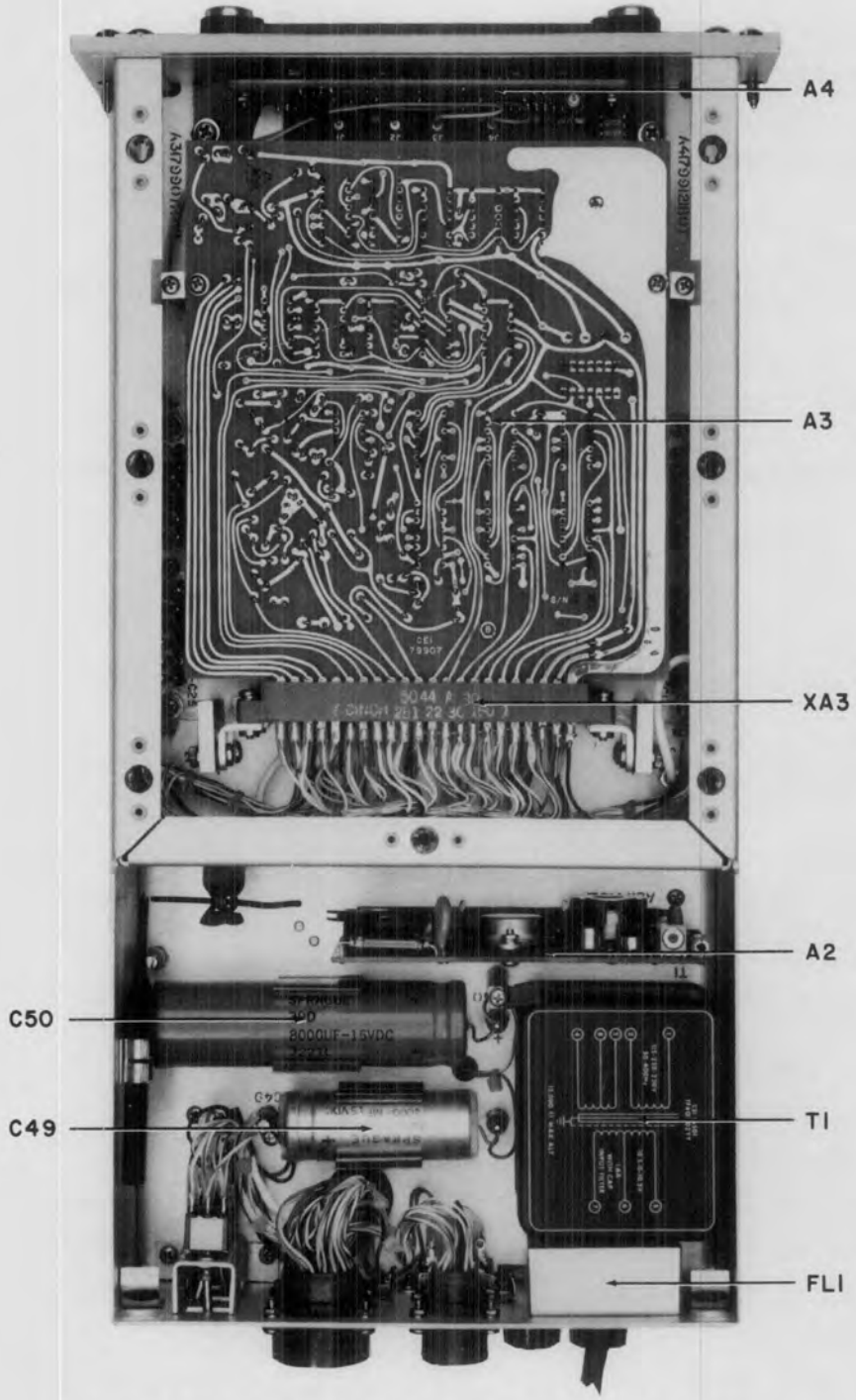


Figure 5-3. Type DRO-302B Frequency Counter, Top View, Location of Components

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
J9	CONNECTOR, RECEPTACLE	1	132	19505	
J10	Same as J8				
M1	METER, TUNING	1	15617-1	14632	
MP1	KNOB	2	PS70PL2	21604	
MP2	Same as MP1				
MP3	FILTER, LIGHT	1	12584-15	14632	
MP4	COVER	1	32829-1	14632	
P1	CONNECTOR, PLUG	3	UG-1465/U	80058	74868
P2	Same as P1				
P3	CONNECTOR, PLUG	3	UG-1466/U	80058	74868
P4	Same as P3				
P5	Same as P3				
P6	CONNECTOR, PLUG	2	60598-5	00779	
P7	Same as P6				
P8	Same as P1				
R1	RESISTOR, FIXED, COMPOSITION: 5.1 MΩ, 5%, 1/4W	1	RCR07G515JS	81349	01121
R2	RESISTOR, FIXED, COMPOSITION: 510 Ω, 5%, 1/4W	1	RCR07G511JS	81349	01121
R3	RESISTOR, FIXED, COMPOSITION: 1.0 kΩ, 5%, 1/4W	1	RCR07G102JS	81349	01121
R4	RESISTOR, FIXED, COMPOSITION: 100 Ω, 5%, 1/4W	1	RCR07G101JS	81349	01121
S1	SWITCH, TOGGLE	1	8280K16	27193	
S2	SWITCH, SLIDE	1	11A1211	82389	
S3	SWITCH, TOGGLE	2	7101	09353	
S4	SWITCH, TOGGLE	1	7303	09353	
S5	Same as S3				
S6	SWITCH, ROTARY	2	1128-43	14632	
S7	Same as S6				
T1	TRANSFORMER, POWER	1	16501	14632	
VR1	DIODE	1	1N758A	80131	04713
W1	CABLE ASSEMBLY	1	30020-1674	14632	
W2	CABLE ASSEMBLY	1	30020-1675	14632	
W3	CABLE ASSEMBLY	1	30020-1676	14632	
W4	CABLE ASSEMBLY	1	30020-1677	14632	
W5	CABLE ASSEMBLY	1	30020-1678	14632	
XA2	CONNECTOR, PRINTED CIRCUIT CARD	1	250-22-30-170	71785	
XA3	CONNECTOR, PRINTED CIRCUIT CARD	2	251-22-30-160	71785	
XA4	Same as XA3				

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
XF1	FUSEHOLDER	2	342004	75915	
XF2	Same as XF1				

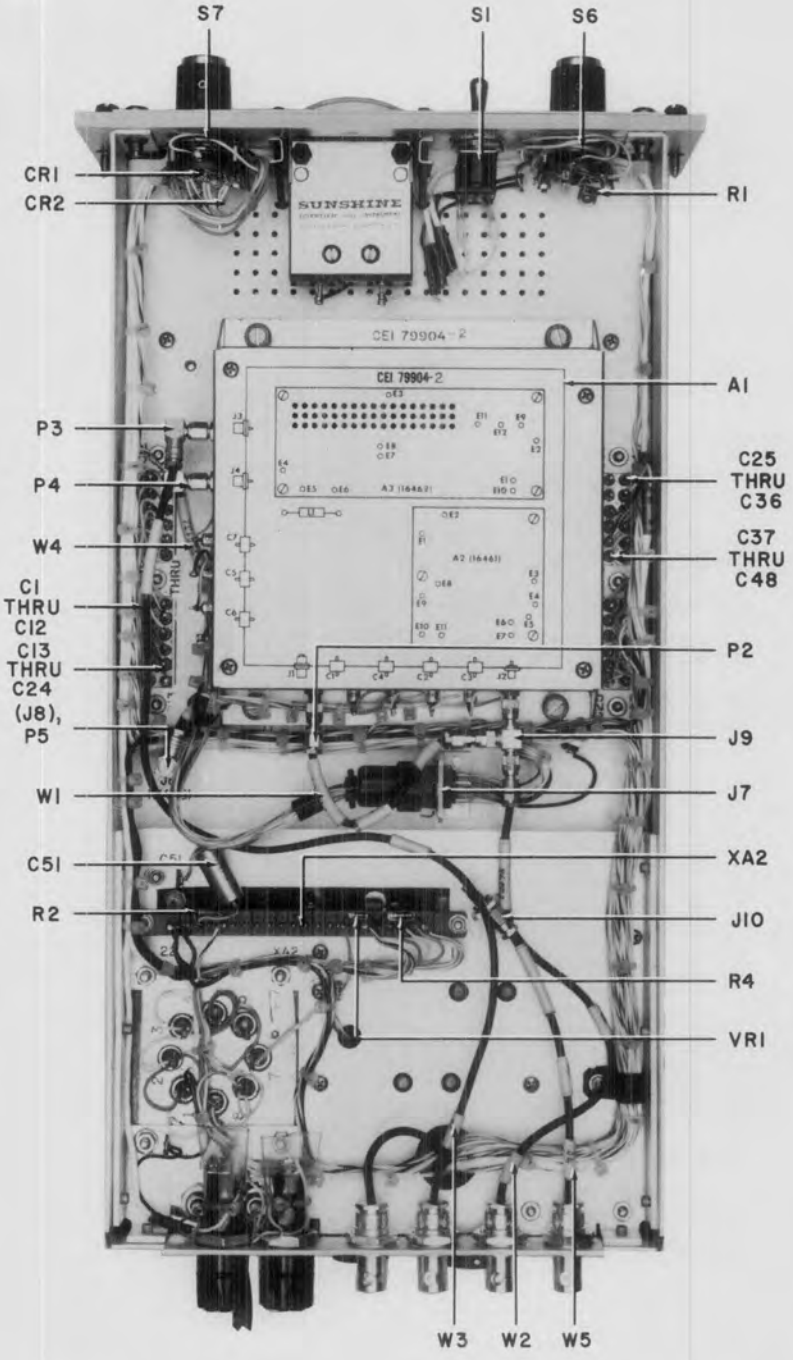


Figure 5-4. Type DRO-302B Frequency Counter, Bottom View, Location of Components

5.4.2 Type DRO-333 & DRO-315, Frequency Counters, Main Chassis

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
A1	PRESCALER ASSEMBLY (DRO-333 only)	1	79904-1	14632	
A1	PRESCALER ASSEMBLY (DRO-315 only)	1	79904-2	14632	
A2	SWITCHING REGULATOR	1	76192	14632	
A3	GATE GENERATOR	1	79907	14632	
A4	COUNT, DECODE,& DISPLAY	1	79912-1	14632	
CR1	DIODE	2	1N995	80131	
CR2	Same as CR1				
C1	CAPACITOR, CERAMIC, FEEDTHRU: .05 μF, GMV, 300V	46	MS001DA503P	01121	
C2 thru C25	Same as C1				
C26	CAPACITOR, CERAMIC, FEEDTHRU: 1000 pF, GMV 500V	1	2404-000X5U0-102P	72982	
C27 thru C29	Same as C1				
C30	CAPACITOR, CERAMIC, FEEDTHRU: 5000 pF, 20%, 500V	1	2404-000X5U0-502M	72982	
C31 thru C48	Same as C1				
C49	CAPACITOR, ELECTROLYTIC, ALUMINUM: 1000 μF, -10+75%, 15V	1	34D108G015GL4	56289	
C50	CAPACITOR, ELECTROLYTIC, ALUMINUM: 8000 μF, -10+75%, 15V	1	39D808G015JT4	56289	
C51	CAPACITOR, ELECTROLYTIC, TANTALUM: 150 μF, 10%, 15V	1	CS13BD157K	81349	56289
C52	CAPACITOR, FIXED, PAPER: 0.01 μF, 20%, 600V	4	102P515	56289	
C53 thru C55	Same as C52				
DS1	LAMP, NEON	7	A1H	87034	
F1	FUSE, CARTRIDGE: 1/8 AMP, 3AG	1	MDL1/8	71400	
F2	FUSE, CARTRIDGE: 1/16 AMP, 3AG	1	MDL1/16	71400	
J1	CONNECTOR, RECEPTACLE	1	L12TE10S2N-A	09922	
J2	CONNECTOR, RECEPTACLE	1	L18TE32S2N-A	09922	
J3	CONNECTOR, RECEPTACLE	4	17825-1002	74868	
J4	Same as J3				
J5	Same as J3				
J6	Same as J3				
J7	CONNECTOR, RECEPTACLE	1	M10SLRN	81312	

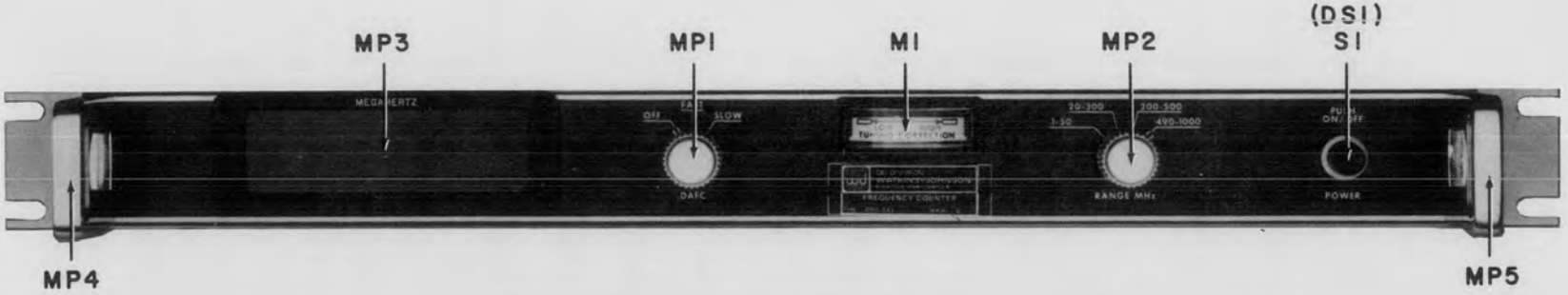


Figure 5-5. Type DRO-333 Frequency Counter, Front View, Location of Components

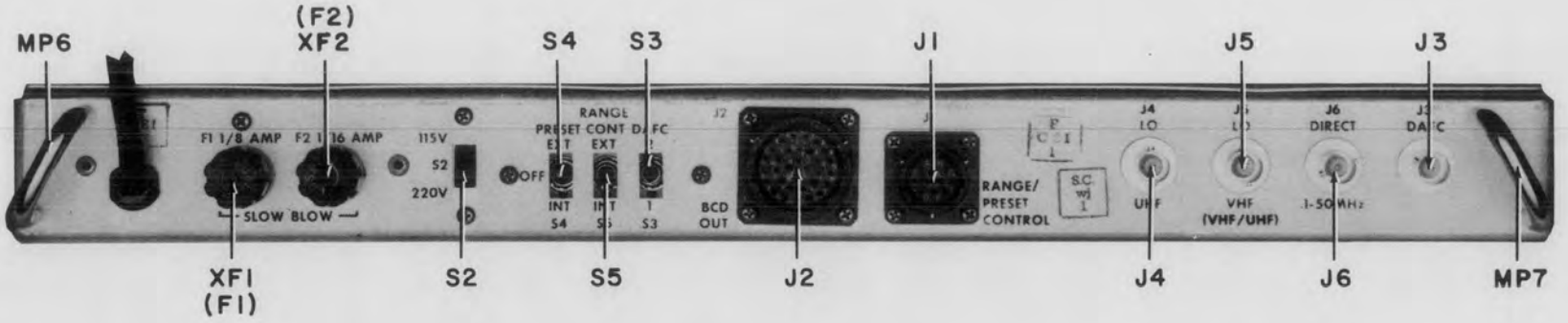


Figure 5-6. Type DRO-333 Frequency Counter, Rear View, Location of Components

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
J8	CONNECTOR, RECEPTACLE	2	UG-1468/U	80058	74868
J9	CONNECTOR, RECEPTACLE	1	132	19505	
J10	Same as J8				
J11	Same as P3				
L1	INDUCTOR	2	21210-84	14632	
L2	Same as L1				
M1	METER, TUNING	1	15617-1	14632	
MP1	KNOB	2	PS70PL2 (GREY)	21604	
MP2	Same as MP1				
MP3	FILTER, LIGHT	1	12584-15	14632	
MP4	HANDLE	2	32306-3	14632	
MP5	Same as MP4				
MP6	HANDLE	2	1070-12	88245	
MP7	Same as MP6				
MP8	COVER	1	41916-1	14632	
P1	CORD, POWER	1	3598-181-007	71700	
P2	CONNECTOR, PLUG	2	UG1465/U	80058	74868
P3	CONNECTOR, PLUG	4	UG1466/U	80058	74868
P4	Same as P3				
P5	Same as P3				
P6	CONNECTOR, PLUG	2	60598-5	00779	
P7	Same as P6				
P8	Same as P2				
R1	RESISTOR, FIXED, COMPOSITION: 5.1 MΩ, 5%, 1/4W	1	RCR07G515JS	81349	01121
R2	RESISTOR, FIXED, COMPOSITION: 510 Ω, 5%, 1/4W	1	RCR07G511JS	81349	01121
R3	RESISTOR, FIXED, COMPOSITION: 1.0 kΩ, 5%, 1/4W	1	RCR07G102JS	81349	01121
R4	RESISTOR, FIXED, COMPOSITION: 100 Ω, 5%, 1/4W	1	RCR07G101JS	81349	01121
R5	RESISTOR, FIXED, COMPOSITION: 27 kΩ, 5%, 1/4W	1	RCR07G273JS	81349	01121
S1	SWITCH, PUSH	1	671-6A1H	87034	01121
S2	SWITCH, SLIDE	1	11A1211	82389	01121
S3	SWITCH, TOGGLE	2	7101	09353	
S4	SWITCH, TOGGLE	1	7303	09353	
S5	Same as S3				
S6	SWITCH, ROTARY	2	1128-43	14632	
S7	Same as S6				
T1	TRANSFORMER, POWER	1	16931	14632	

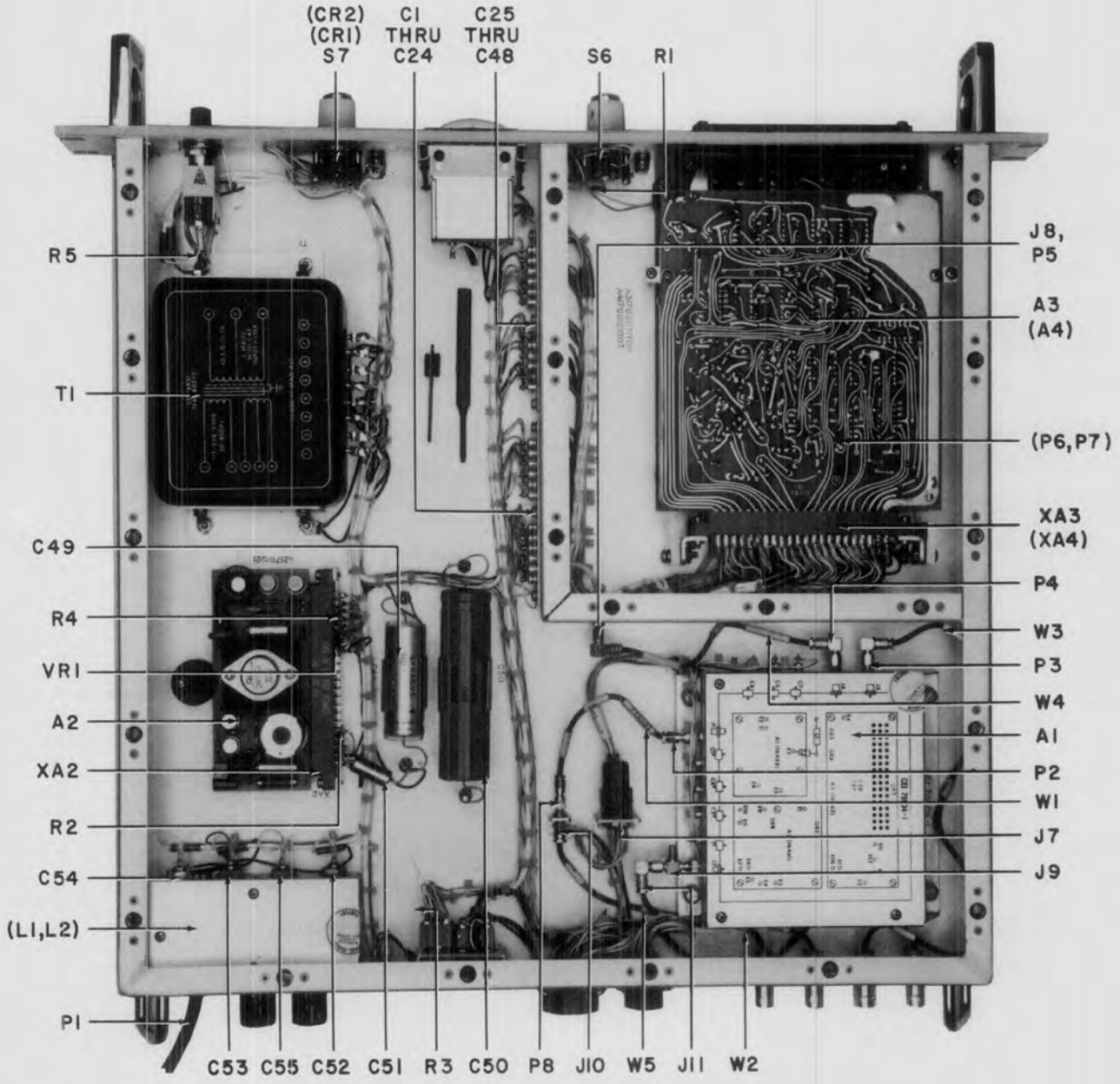


Figure 5-7. Type DRO-333 Frequency Counter, Top View, Location of Components

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
VR1	DIODE	1	1N758A	80131	04713
W1	CABLE ASSEMBLY	1	30020-1782	14632	
W2	CABLE ASSEMBLY	1	30020-1783	14632	
W3	CABLE ASSEMBLY	1	30020-1784	14632	
W4	CABLE ASSEMBLY	1	30020-1785	14632	
W5	CABLE ASSEMBLY	1	30020-1786	14632	
XA2	CONNECTOR, PRINTED CIRCUIT CARD	1	250-22-30-170	71785	
XA3	CONNECTOR, PRINTED CIRCUIT CARD	2	251-22-30-160	71785	
XA4	Same as CA3				
XF1	FUSEHOLDER	2	342004	75915	
XF2	Same as XF1				

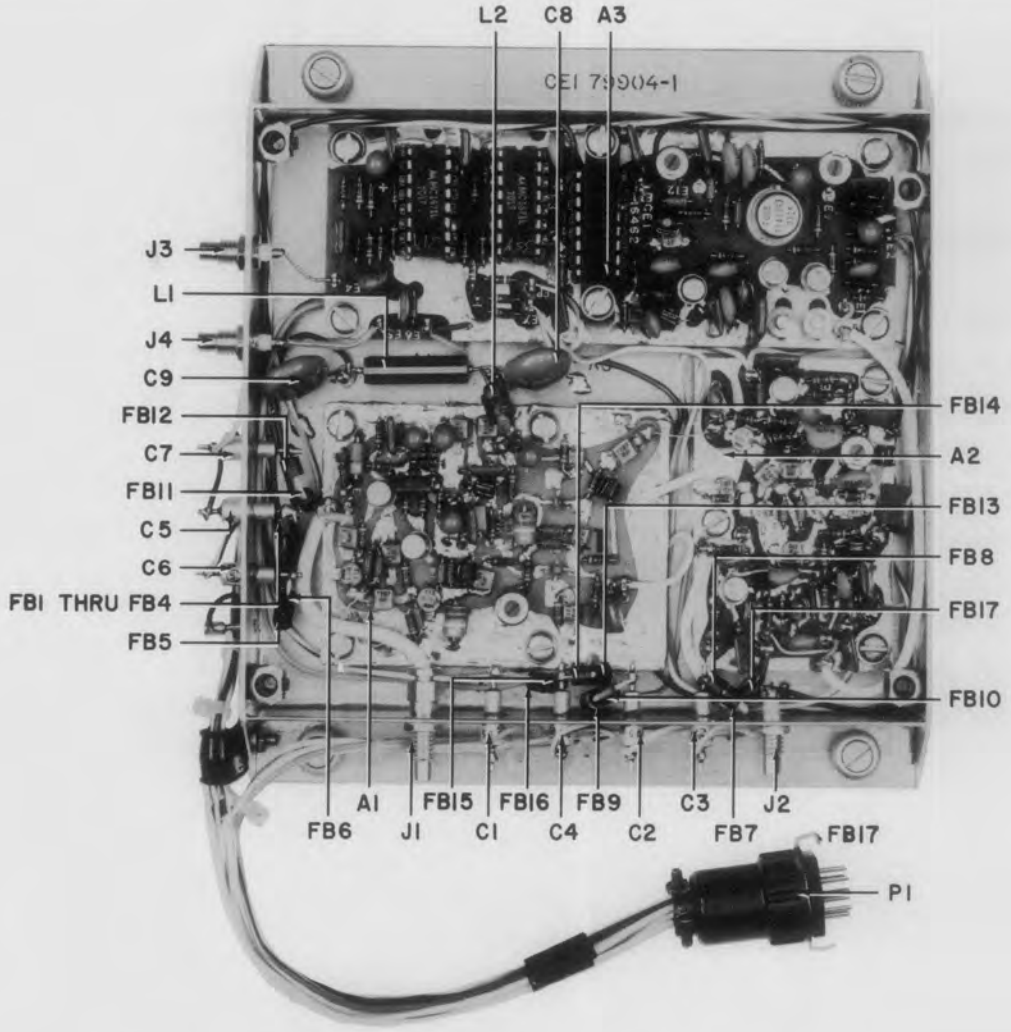


Figure 5-8. Type 79904-1 and 79904-2 Prescaler Assembly (A1), Location of Components

5.4.3 Type 79904-1 & 79904-2 Prescaler Assembly REF DESIG PREFIX A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
A1	1060 MHz BINARY DIVIDER (Type 79904-1 only)	1	16488-1	14632	
A2	560 MHz BINARY DIVIDER	1	16461-1	14632	
A3	325 MHz ECL, DIVIDE BY 2, 4, OR 8	1	16462	14632	
C1	CAPACITOR, CERAMIC, FEEDTHRU: 0.05 μF, GMV, 300V	7	MS001DA503P	01121	
C2 thru C7	Same as C1				
C8	CAPACITOR, ELECTROLYTIC, TANTALUM: 220 μF, 20%, 10V	2	196D227X0010MA3	56289	
C9	Same as C8				
FB1	FERRITE BEAD	16	56-590-65-4A	02114	
FB2 thru FB6	Same as FB1				
FB7	Same as FB1 (Type 79904-1 only)				
FB8	Same as FB1 (Type 79904-1 only)				
FB9 thru FB16	Same as FB1				
FB17	FERRITE BEAD	1	P5-1288	01037	
J1	CONNECTOR, PLUG	1	UG-1468/U	80058	74868
J2	CONNECTOR, RECEPTACLE	3	10-0104-002	19505	
J3	Same as J2				
J4	Same as J2				
L1	INDUCTOR	1	21210-112	14632	
L2	COIL, FIXED: 80 μH (Type 79904-1 only)	1	3080-15	99848	
MP1	COVER (Type 79904-1 only)	1	22849-1	14632	
MP1	COVER (Type 79904-2 only)	1	22849-2	14632	
P1	CONNECTOR, PLUG	1	M10PLSH19C	81312	

REF DESIG PREFIX A1A1 (DRO 302B & DRO 333 only)

5.4.3.1 Part 16488-1, 1060 MHz Binary Divider

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
CR1	DIODE	1	1N4446	80131	93332
CR2	DIODE	8	5082-2900	28480	
CR3 thru CR9	Same as CR2				
C1	CAPACITOR, ELECTROLYTIC, TANTALUM: 22 μF, 20%, 10V	3	196D226X0010JA1	56289	
C2	CAPACITOR, ELECTROLYTIC, TUBULAR: 0.33 pF, 10%, 500V	1	MC0.33PF,K	95121	
C3	CAPACITOR, CERAMIC, DISC: 100 pF, 10%, 300V	6	UY02101K	73899	
C4	CAPACITOR, ELECTROLYTIC, TANTALUM: 2.2 μF, 20%, 35V	1	196D225X0035JA1	56289	
C5	CAPACITOR, CERAMIC, DISC: 470 pF, 5%, 300V	2	UY03471J	73899	
C6	Same as C1				
C7	CAPACITOR, CERAMIC, DISC: 0.1 μF, 20%, 100V	4	8131M100-651-104M	72982	
C8	Same as C7				
C9	Same as C3				
C10	Same as C7				
C11	Same as C5				
C12	Same as C3				
C13	Same as C3				
C14	CAPACITOR, COMPOSITION, TUBULAR: 1.5 pF, 10%, 500V	2	MC1.5pF,K	95121	
C15	Same as C3				
C16	CAPACITOR, CERAMIC, DISC: 12 pF, 5%, 300V	2	UY01120J	73899	
C17	Same as C14				
C18	Same as C7				
C19	CAPACITOR, CERAMIC, DISC: 4.7 pF, ±0.25 pF, 300V	2	UY014R7C	73899	
C20	Same as C19				
C21	CAPACITOR, CERAMIC, DISC: 0.01 μF, 20%, 200V	1	8131A200Z5U0-103M	72982	
C22	Same as C3				
C23	Same as C16				
C24	Same as C1				
C25	CAPACITOR, CERAMIC, DISC: 200 pF, 500V	1	32-257578-40	91984	
C26	CAPACITOR, COMPOSITION, TUBULAR: 0.82 pF, 10%,	1	MC0.82pF,K	95121	
E1	TERMINAL, FORKED	5	140-1941-02-01	71279	
E2 thru E5	Same as E1				

REF DESIG PREFIX A1A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
FB1	FERRITE BEAD	2	56-590-65-4A	02114	
FB2	Same as FB1				
L1	COIL, FIXED	2	21209-11	14632'	
L2	Same as L1				
L3	COIL	1	16209-1	14632	
L4	COIL	1	16209-3	14632	
L5	COIL	1	16209-2	14632	
Q1	TRANSISTOR	2	2N3251	80131	04713
Q2	TRANSISTOR	2	22840-2	14632	
Q3	Same as Q1				
Q4	Same as Q2				
Q5	TRANSISTOR	2	22840-1	14632	
Q6	Same as Q5				
R1	RESISTOR, FIXED, COMPOSITION: 270 Ω, 5%, 1/8W	1	RCR05G271JS	81349	01121
R2	RESISTOR, FIXED, COMPOSITION: 680 Ω, 5%, 1/8W	1	RCR05G681JS	81349	01121
R3	RESISTOR, FIXED, COMPOSITION: 10 kΩ, 5%, 1/8W	1	RCR05G103JS	81349	01121
R4	RESISTOR, FIXED, COMPOSITION: 33 Ω, 5%, 1/8W	2	RCR05G330JS	81349	01121
R5	RESISTOR, FIXED, COMPOSITION: 470 Ω, 5%, 1/8W	4	RCR05G471JS	81349	01121
R6	NOT USED				
R7	RESISTOR, FIXED, COMPOSITION: 820 Ω, 5%, 1/8W	3	RCR05G821JS	81349	01121
R8	Same as R3				
R9	Same as R4				
R10	Same as R5				
R11	RESISTOR, FIXED, COMPOSITION: 10 Ω, 5%, 1/8W	1	RCR05G100JS	81349	01121
R12	RESISTOR, FIXED, COMPOSITION: 200 Ω, 5%, 1/8W	1	RCR05G201JS	81349	01121
R13	Same as R5				
R14*	Same as R7				
R15	RESISTOR, FIXED, COMPOSITION: 100 Ω, 5%, 1/8W	3	RCR05G101JS	81349	01121
R16*	Same as R7				
R17	Same as R15				
R18	RESISTOR, VARIABLE, FILM: 1 kΩ, 10%, 1/2W	1	62PR1K	73138	
R19	Same as R15				
R20	Same as R5				

* Nominal value; final value to be factory selected.

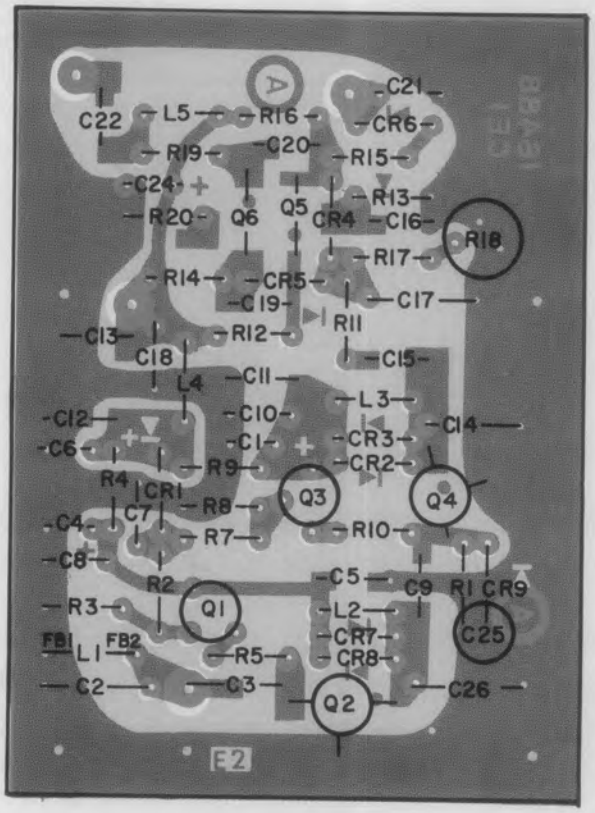


Figure 5-9. Part 16488-1 1060 MHz Binary Divider (A1A1), Location of Components

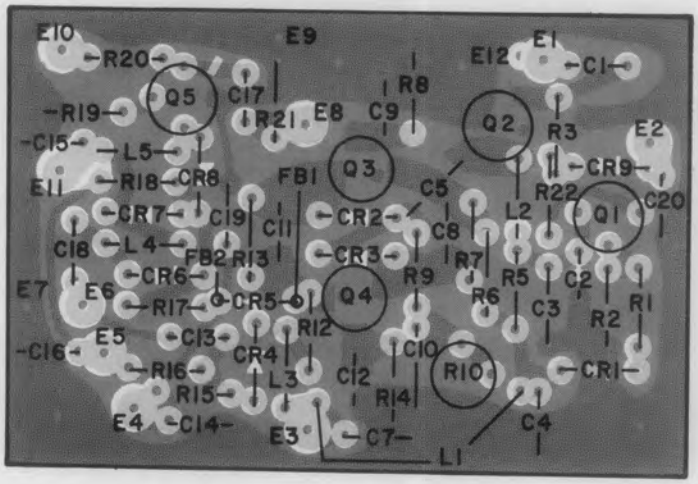


Figure 5-10. Part 16461-1 560 MHz Binary Divider (A1A2), Location of Components

5.4.3.2 Part 16461-1 560 MHz Binary Divider REF DESIG PREFIX A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
CR1	DIODE	3	1N4446	80131	93332
CR2	DIODE	3	5082-2900	28480	
CR3	Same as CR2				
CR4	DIODE	3	5082-3080	28480	
CR5	Same as CR1				
CR6	Same as CR4				
CR7	Same as CR1				
CR8	Same as CR4				
CR9	Same as CR2				
C1	CAPACITOR, CERAMIC, DISC: 1000 pF, GMV, 500V	5	SM1000PFP	91418	
C2	CAPACITOR, ELECTROLYTIC, TANTALUM: 2.2 μF, 20%, 35V	1	196D225X0035JA1	56289	
C3	CAPACITOR, CERAMIC, DISC: 470 pF, 20%, 1000V	2	B470PFM	91418	
C4	CAPACITOR, CERAMIC, DISC: 0.1 μF, 20%, 100V	2	8131M100-651-104M	72982	
C5	CAPACITOR, CERAMIC, DISC: 100 pF, 10%, 300V	1	UY02101K	73899	
C6	NOT USED				
C7	CAPACITOR, CERAMIC, DISC: 0.01 μF, 20%, 200V	4	8131A200Z5U0-103M	72982	
C8	CAPACITOR, CERAMIC, DISC: 4.7 pF, ±0.25 pF, 300V	2	UY014R7C	73899	
C9	CAPACITOR, CERAMIC, DISC: 15 pF, 5%, 300V	2	UY01150J	73899	
C10	Same as C3				
C11	Same as C8				
C12	Same as C9				
C13	Same as C1				
C14	Same as C7				
C15	Same as C7				
C16	Same as C7				
C17	Same as C1				
C18	Same as C1				
C19	Same as C1				
C20	Same as C4				
FB1	FERRITE BEAD	2	P5-1288	01037	
FB2	Same as FB1				
L1	COIL, FIXED	4	16209-3	14632	
L2	COIL, FIXED	1	22292-40	14632	
L3	Same as L1				
L4	Same as L1				

REF DESIG PREFIX A1A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
L5	Same as L1				
Q1	TRANSISTOR	1	2N3251	80131	04713
Q2	TRANSISTOR	3	22840-2	14632	
Q3	Same as Q2				
Q4	Same as Q2				
Q5	TRANSISTOR	1	2N3572	80131	01295
R1	RESISTOR, FIXED, COMPOSITION: 330 Ω, 5%, 1/8 W	1	RCR05G331JS	81349	01121
R2	RESISTOR, FIXED, COMPOSITION: 4.7 kΩ, 5%, 1/8 W	1	RCR05G472JS	81349	01121
R3	RESISTOR, FIXED, COMPOSITION: 47 Ω, 5%, 1/8 W	1	RCR05G470JS	81349	01121
R4	NOT USED				
R5	RESISTOR, FIXED, COMPOSITION: 18 Ω, 5%, 1/8 W	1	RCR05G180JS	81349	01121
R6	RESISTOR, FIXED, COMPOSITION: 200 Ω, 5%, 1/8 W	1	RCR05G201JS	81349	01121
R7	RESISTOR, FIXED, COMPOSITION: 1.5 kΩ, 5%, 1/8 W	2	RCR05G152JS	81349	01121
R8	RESISTOR, FIXED, COMPOSITION: 470 Ω, 5%, 1/8 W	4	RCR05G471JS	81349	01121
R9	RESISTOR, FIXED, COMPOSITION: 220 Ω, 5%, 1/8 W	1	RCR05G221JS	81349	01121
R10	RESISTOR, VARIABLE, FILM: 1 kΩ, 10%, 1/2W	1	62PAR1K	73138	
R11	NOT USED				
R12	RESISTOR, FIXED, COMPOSITION: 150 Ω, 5%, 1/8 W	1	RCR05G151JS	81349	01121
R13	Same as R7				
R14	Same as R8				
R15	RESISTOR, FIXED, COMPOSITION: 1.0 kΩ, 5%, 1/8W	2	RCR05G102JS	81349	01121
R16	RESISTOR, FIXED, COMPOSITION: 2.2 kΩ, 5%, 1/8W	2	RCR05G222JS	81349	01121
R17	Same as R8				
R18	Same as R16				
R19	RESISTOR, FIXED, COMPOSITION: 10 Ω, 5%, 1/8W	1	RCR05G100JS	81349	01121
R20	Same as R15				
R21	RESISTOR, FIXED, COMPOSITION: 270 Ω, 5%, 1/8W	1	RCR05G271JS	81349	01121
R22	Same as R8				

5.4.3.3 Part 16462 325 MHz ECL, Divide by 2, 4, or 8 REF DESIG PREFIX A1A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
CR1	DIODE	4	5082-3080	28480	
CR2	DIODE	2	1N4446	80131	93332
CR3	DIODE	3	5082-2900	28480	
CR4	Same as CR3				
CR5	Same as CR3				
CR6	Same as CR1				
CR7	Same as CR1				
CR8	Same as CR1				
CR9	Same as CR2				
C1	CAPACITOR, CERAMIC, DISC: 1000 pF, GMV, 500V	5	SM1000PFP	91418	
C2	Same as C1				
C3	CAPACITOR, VARIABLE, CERAMIC: 6-22 pF, 25V, N750	2	511-000-G6-22	72892	
C4	Same as C3				
C5	CAPACITOR, MICA, DIPPED: 68 pF, 5%, 500V	1	CM04ED680J03	81349	72136
C6	CAPACITOR, CERAMIC, DISC: 0.01 μF, 20%, 200V	5	8131A200Z5U0-103M	72982	
C7	CAPACITOR, CERAMIC, DISC: 0.1 μF, 20%, 100V	6	8131M100-651-104M	72982	
C8	CAPACITOR, ELECTROLYTIC, TANTALUM: 2.2 μF, 20%, 35V	1	196D225X0035JA1	56289	
C9	CAPACITOR, CERAMIC, DISC: 470 pF, 20%, 1000V	4	B470PFM	91418	
C10	Same as C6				
C11	Same as C1				
C12	Same as C7				
C13	Same as C9				
C14	Same as C1				
C15	CAPACITOR, CERAMIC, DISC: 12 pF, 5%, 300V	1	UY01120J	73899	
C16	Same as C9				
C17	CAPACITOR, CERAMIC, DISC: 10 pF, 5%, 300V	1	UY01100J	73899	
C18	Same as C9				
C19	CAPACITOR, CERAMIC, DISC: 15 pF, 5%, 300V	1	UY01150J	73899	
C20	Same as C7				
C21	Same as C6				
C22	CAPACITOR, ELECTROLYTIC, TANTALUM: 22 μF, 20%, 10V	2	196D226X0010JA1	56289	
C23	Same as C1				
C24	Same as C7				
C25	Same as C7				

REF DESIG PREFIX A1A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
C26	Same as C6				
C27	Same as C6				
C28	Same as C22				
C29	Same as C7				
L1	COIL, FIXED	3	16209-3	14632	
L2	Same as L1				
L3	Same as L1				
Q1	TRANSISTOR	2	2N3572	80131	01295
Q2	Same as Q1				
Q3	TRANSISTOR	1	2N5179	80131	04713
RA1	HEATSINK	1	16492-1	14632	
RA2	HEATSINK	1	16594-1	14632	
R1	RESISTOR, FIXED, COMPOSITION: 100 Ω, 5%, 1/8W	3	RCR05G101JS	81349	01121
R2	RESISTOR, FIXED, COMPOSITION: 1.0 kΩ, 5%, 1/8W	4	RCR05G102JS	81349	01121
R3	RESISTOR, FIXED, COMPOSITION: 820 Ω, 5%, 1/8W	1	RCR05G821JS	81349	01121
R4	RESISTOR, FIXED, COMPOSITION: 1.8 kΩ, 5%, 1/8W	1	RCR05G182JS	81349	01121
R5	RESISTOR, FIXED, COMPOSITION: 47 Ω, 5%, 1/8W	3	RCR05G470JS	81349	01121
R6	RESISTOR, FIXED, COMPOSITION: 150 Ω, 5%, 1/8W	2	RCR05G151JS	81349	01121
R7	Same as R2				
R8	RESISTOR, FIXED, COMPOSITION: 270 Ω, 5%, 1/8W	1	RCR05G271JS	81349	01121
R9	RESISTOR, VARIABLE, FILM: 500 Ω, 10%, 1/2W	2	62PR500	73138	
R10	Same as R9				
R11	RESISTOR, FIXED, COMPOSITION: 3.3 kΩ, 5%, 1/8W	1	RCR05G332JS	81349	01121
R12	Same as R2				
R13	RESISTOR, FIXED, COMPOSITION: 18 kΩ, 5%, 1/8W	1	RCR05G183JS	81349	01121
R14	RESISTOR, FIXED, COMPOSITION: 56 Ω, 5%, 1/8W	1	RCR05G560JS	81349	01121
R15	RESISTOR, FIXED, COMPOSITION: 470 Ω, 5%, 1/8W	4	RCR05G471JS	81349	01121
R16	RESISTOR, FIXED, COMPOSITION: 22 Ω, 5%, 1/8W	2	RCR05G220JS	81349	01121
R17	Same as R15				
R18	RESISTOR, FIXED, COMPOSITION: 560 Ω, 5%, 1/8W	2	RCR05G561JS	81349	01121
R19	Same as R5				
R20	Same as R15				
R21	Same as R18				
R22	Same as R1				
R23	RESISTOR, FIXED, COMPOSITION: 390 Ω, 5%, 1/8W	1	RCR05G391JS	81349	01121
R24	Same as R5				

REF DESIG PREFIX A1A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
R25	Same as R1 new value 510Ω				
R26	RESISTOR, FIXED, COMPOSITION: ~~510Ω~~ 1000Ω, 5%, 1/8W	1	RCR05G511JS	81349	01121
R27	Same as R2				
R28	RESISTOR, FIXED, COMPOSITION: 2.2 kΩ, 5%, 1/8W	1	RCR05G222JS	81349	01121
R29	Same as R15				
R30	Same as R16				
R31	Same as R6				
T1	TRANSFORMER	1	16597-1	14632	
U1	INTEGRATED CIRCUIT	1	U5B7741393	07263	
U2	INTEGRATED CIRCUIT	1	16916	14632	
U3	INTEGRATED CIRCUIT	2	MC1671L	04713	
U4	Same as U3				

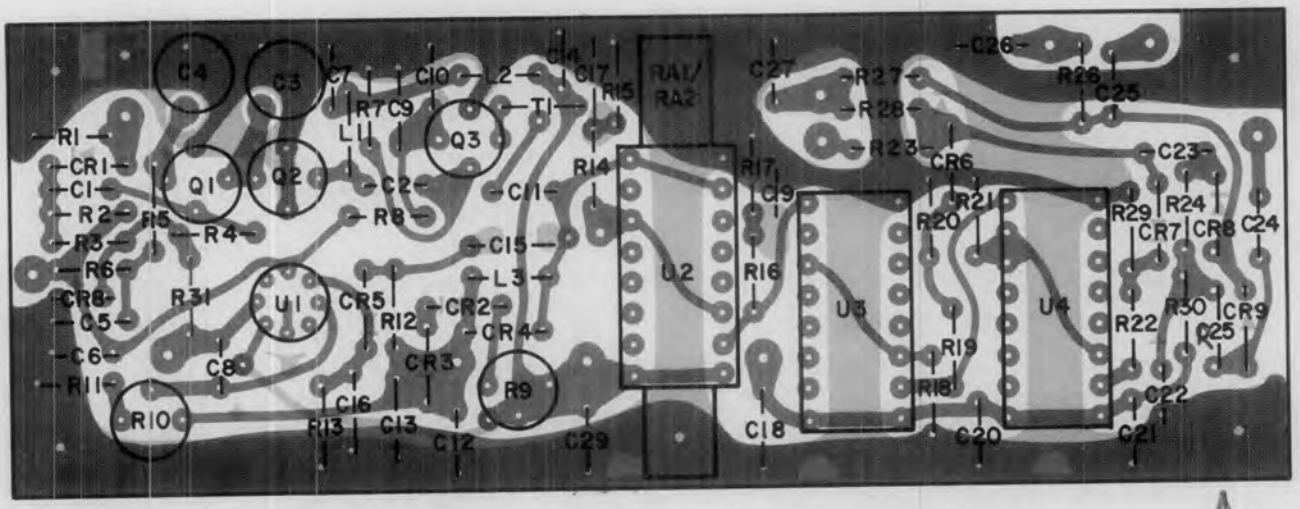


Figure 5-11. Part 16462 325 MHz ECL, Divide by 2, 4, or 8 (A1A3), Location of Components

C25 → R25 false reading

5.4.4 Type 76192, Switching Regulator REF DESIG PREFIX A2

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
CR1	DIODE	2	1N4998	80131	04713
CR2	Same as CR1				
CR3	DIODE	1	UTR3305	12969	
C1	CAPACITOR, ELECTROLYTIC, TANTALUM: 47 µF, 10%, 35V	1	CS13BF476K	81349	56289
C2	CAPACITOR, ELECTROLYTIC, TANTALUM: 4.7 µF, 10%, 35V	1	CS13BF475K	81349	56289
C3	CAPACITOR, CERAMIC, DISC: 0.01 µF, 20%, 200V	1	8131A200Z5UO-103M	72892	
C4	CAPACITOR, CERAMIC, DISC: 0.05 µF, 20%, 100V	1	29C212A7	56289	
C5	CAPACITOR, ELECTROLYTIC, TANTALUM: 150 µF, 10%, 15V	1	CS13BD157K	81349	01121
C6	CAPACITOR, ELECTROLYTIC, TANTALUM: ~~27~~ 100µF, 10%, ~~35~~ 20V	1	196D276X9035MA3	56289	
C7	CAPACITOR, CERAMIC, DISC: 0.1 µF, 20%, 100V	1	8131M100-651-104M	72982	
C8	CAPACITOR, MICA, DIPPED: 1000 pF, 5%, 100V	1	DM15-102J	72136	
L1	COIL, FIXED	2	21210-84	14632	
L2	COIL, FIXED	1	30316-3	14632	
L3	Same as L1				
Q1	TRANSISTOR	1	2N4037	80131	02735
Q2	TRANSISTOR	1	2N5039	80131	02735
Q3	TRANSISTOR	1	2N2905A	80131	04713
RA1	HEATSINK	1	2225B	13103	
RA2	HEATSINK	1	6103B	13103	
R1	RESISTOR, FIXED, COMPOSITION: 270 Ω, 5%, 1/4W	2	RCR07G271JS	81349	01121
R2	Same as R1				
R3	RESISTOR, FIXED, COMPOSITION: ~~68~~ 47Ω, 5%, 1/4W	1	RCR07G680JS	81349	01121
R4	RESISTOR, FIXED, COMPOSITION: 510 kΩ, 5%, 1/4W	1	RCR07G514JS	81349	01121
R5	RESISTOR, FIXED, COMPOSITION: 22 Ω, 5%, 1/4W	1	RCR07G220JS	81349	01121
R6	RESISTOR, FIXED, COMPOSITION: 4.3 kΩ, 5%, 1/4W	1	RCR07G432JS	81349	01121
R7	RESISTOR, VARIABLE, FILM: 1 kΩ, 10%, 1/2W	1	62PAR1K	73138	
R8	RESISTOR, FIXED, COMPOSITION: 2.4 kΩ, 5%, 1/4W	1	RCR07G242JS	81349	01121
TP1	JACK, TIP	1	TJ203R	49956	
U1	RECTIFIER ASSEMBLY	1	MDA950A3	04713	
U2	INTEGRATED CIRCUIT	1	LM305	27014	
VR1	DIODE	1	LVA56A	97137	

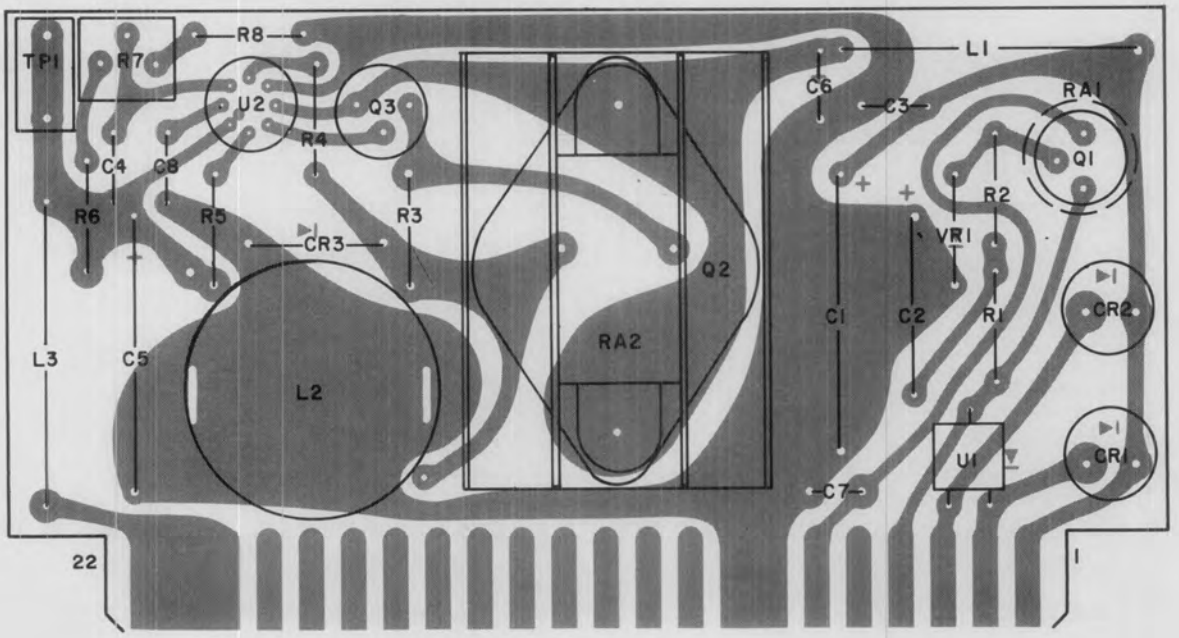


Figure 5-12. Type 76192 Switching Regulator (A2), Location of Components

5.4.5 Type 79907 Gate Generator and DAFC REF DESIG PREFIX A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
CR1	DIODE	12	1N995	80131	93332
CR2 thru CR6	Same as CR1				
CR7	DIODE	1	1N4446	80131	93332
CR8	DIODE	2	1N462A	80131	93332
CR9	Same as CR8				
CR10	DIODE	1	1N198A	80131	93332
CR11	NOT USED				
CR12	NOT USED				
CR13 thru CR18	Same as CR1				
C1	CAPACITOR, ELECTROLYTIC, TANTALUM: 4.7 μF, 10%, 35V	5	CS13BF475K	81349	56289
C2	CAPACITOR, CERAMIC, DISC: 0.1 μF, -20+80%, 25V	10	DFJ3	73899	
C3	Same as C1				
C4 thru C10	Same as C2				
C11	Same as C1				
C12	Same as C1				
C13	CAPACITOR, ELECTROLYTIC, TANTALUM: 10 μF, 10%, 20V	2	CS13BE106K	81349	56289
C14	Same as C13				
C15	Same as C2				
C16	Same as C2				
C17	Same as C1				
C18	NOT USED				
C19	CAPACITOR, CERAMIC, DISC: 0.1 μF, 20%, 100V	6	8131M100-651-104M	72982	
C20	NOT USED				
C21	Same as C19				
C22	Same as C19				
C23	Same as C19				
C24	Same as C19				
C25	Same as C19				
L1	COIL, FIXED; 500 μH, 10%	1	1500-15	99848	
Q1	TRANSISTOR	2	2N2222A	80131	04713
Q2	TRANSISTOR	1	2N3251	80131	04713

REF DESIG PREFIX A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
Q3	TRANSISTOR	1	2N929	80131	04713
Q4	TRANSISTOR	1	3N139 / 3N128 new	80131	02735
Q5	Same as Q1				
Q6	TRANSISTOR	1	2N709	80131	
R1	RESISTOR, FIXED, COMPOSITION: 10 kΩ, 5%, 1/4W	7	RCR07G103JS	81349	01121
R2 thru R6	Same as R1				
R7*	RESISTOR, FIXED, COMPOSITION: 750 kΩ, 5%, 1/4W	1	RCR07G754JS	81349	01121
R8	RESISTOR, FIXED, COMPOSITION: 4.7 kΩ, 5%, 1/4W	1	RCR07G472JS	81349	01121
R9	RESISTOR, FIXED, COMPOSITION: 6.2 kΩ, 5%, 1/4W	1	RCR07G622JS	81349	
R10	RESISTOR, FIXED, COMPOSITION: 15 kΩ, 5%, 1/4W	1	RCR07G153JS	81349	01121
R11	RESISTOR, FIXED, COMPOSITION: 33 Ω, 5%, 1/4W	1	RCR07G330JS	81349	01121
R12	RESISTOR, FIXED, COMPOSITION: 510 kΩ, 5%, 1/4W	1	RCR07G514JS	81349	01121
R13	NOT USED				
R14	RESISTOR, VARIABLE, FILM: 500 Ω, 10%, 1/2W	1	62PR500	73138	
R15	RESISTOR, FIXED, COMPOSITION: 1.0 kΩ, 5%, 1/4W	2	RCR07G102JS	81349	01121
R16	Same as R15				
R17	RESISTOR, FIXED, COMPOSITION: 200 kΩ, 5%, 1/4W	1	RCR07G204JS	81349	01121
R18	RESISTOR, FIXED, COMPOSITION: 100 kΩ, 5%, 1/4W	1	RCR07G104JS	81349	01121
R19	Same as R1				
R20	RESISTOR, FIXED, COMPOSITION: 30 kΩ, 5%, 1/4W	1	RCR07G303JS	81349	01121
R21	RESISTOR, FIXED, COMPOSITION: 2.0 kΩ, 5%, 1/4W	1	RCR07G202JS	81349	01121
R22	RESISTOR, FIXED, COMPOSITION: 18 kΩ, 5%, 1/4W	2	RCR07G183JS	81349	01121
R23	Same as R22				
R24	RESISTOR, FIXED, COMPOSITION: 470 Ω, 5%, 1/4W	1	RCR07G471JS	81349	01121
U1	INTEGRATED CIRCUIT	7	868292	14632	
U2	Same as U1				
U3	Same as U1				
U4	INTEGRATED CIRCUIT	1	SP322B	18324	
U5	INTEGRATED CIRCUIT	1	U6B901559X	07263	
U6	Same as U1				
U7	Same as U1				
U8	INTEGRATED CIRCUIT	1	86961	14632	
U9	INTEGRATED CIRCUIT	1	U6A996259X	07263	
U10	TEMPERATURE COMPENSATING CRYSTAL OSCILLATOR	1	32913-1	14632	

* Nominal value, Final value factory selected.

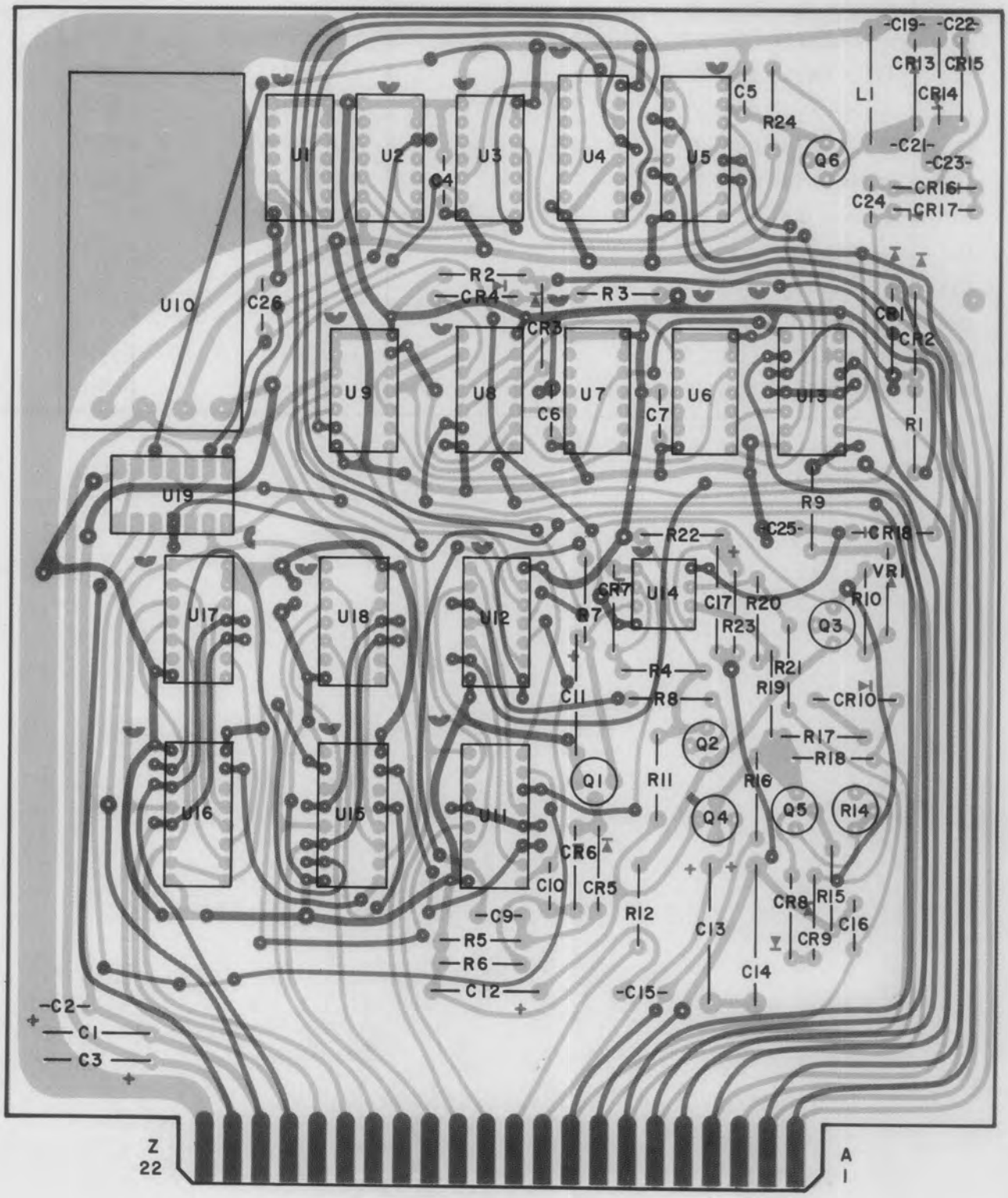


Figure 5-13. Type 79907 Gate Generator and DAFC (A3), Location of Components

REF DESIG PREFIX A3

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
U11	INTEGRATED CIRCUIT	1	U6B901459X	07263	
U12	INTEGRATED CIRCUIT	1	86946	14632	
U13	INTEGRATED CIRCUIT	1	867404	14632	
U14	INTEGRATED CIRCUIT MC 1458N	1	N5558V	27014	
U15	INTEGRATED CIRCUIT	2	8693L24	14632	
U16	Same as U15				
U17	Same as U1				
U18	Same as U1				
U19	Same as U1				
U19	INTEGRATED CIRCUIT	1	86936	14632	
VR1	DIODE	1	LVA56A	97137	

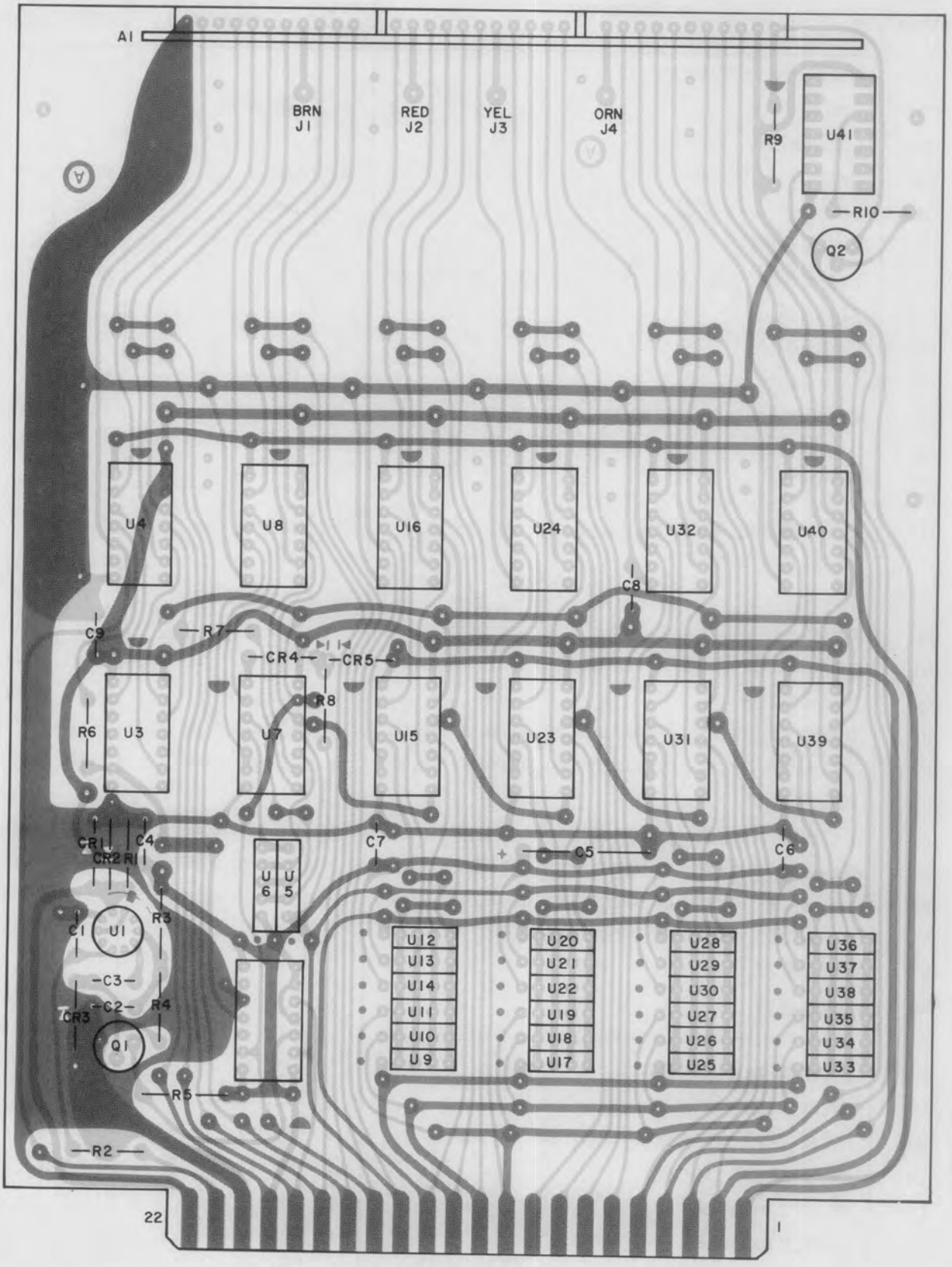


Figure 5-14. Type 79912-1 Count, Decode, and Display (A4), Location of Components

5.4.6 Type 79912-1, Count, Decode and Display REF DESIG PREFIX A4

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
A1	SOLID STATE NUMERIC DISPLAY	1	16513	14632	
CR1	DIODE	2	5082-2800	28480	
CR2	Same as CR1				
CR3	DIODE	1	1N4449	80131	93332
CR4	DIODE	2	1N4446	80131	93332
CR5	Same as CR4				
C1	CAPACITOR, CERAMIC, DISC: 0.1 μF, -20+80%, 25V	8	DFJ3	73899	
C2	Same as C1				
C3	Same as C1				
C4	Same as C1				
C5	CAPACITOR, ELECTROLYTIC, TANTALUM: 10 μF, 10%, 20V	1	CS13BE106K	81349	56289
C6 thru C9	Same as C1				
J1	CONNECTOR, RECEPTACLE	4	60599-3	00779	
J2	Same as J1				
J3	Same as J1				
J4	Same as J1				
Q1	TRANSISTOR	1	2N709A	80131	02735
Q2	TRANSISTOR	1	2N2222A	80131	04713
R1	RESISTOR, FIXED, COMPOSITION: 620 Ω, 5%, 1/4W	1	RCR07G621JS	81349	01121
R2	RESISTOR, FIXED, COMPOSITION: 47 Ω, 5%, 1/4W	2	RCR07G470JS	81349	01121
R3	Same as R2				
R4	RESISTOR, FIXED, COMPOSITION: 10 kΩ, 5%, 1/4W	1	RCR07G103JS	81349	01121
R5	RESISTOR, FIXED, COMPOSITION: 1.0 kΩ, 5%, 1/4W	3	RCR07G102JS	81349	01121
R6	RESISTOR, FIXED, COMPOSITION: 100 Ω, 5%, 1/4W	1	RCR07G101JS	81349	01121
R7	RESISTOR, FIXED, COMPOSITION: 200 Ω, 5%, 1/4W	1	RCR07G201JS	81349	01121
R8	Same as R5				
R9	Same as R5				
R10	RESISTOR, FIXED, COMPOSITION: 1.8 kΩ, 5%, 1/4W	1	RCR07G182JS	81349	01121
U1	INTEGRATED CIRCUIT	1	N5733K	18324	
U2	INTEGRATED CIRCUIT	1	RF3202DC	49956	
U3	INTEGRATED CIRCUIT	1	868290	14632	
U4	INTEGRATED CIRCUIT	11	868292	14632	
U5*	PRESET MODULE	1	31689-	14632	
U6	PRESET MODULE	5	31689-20	14632	
U7	INTEGRATED CIRCUIT	1	868280	14632	

* Preset Customer Selected.

REF DESIG PREFIX A4

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
U8	Same as U4				
U9	PRESET MODULE	1	31689-16	14632	
U10	PRESET MODULE	6	31689-10	14632	
U11	Same as U10				
U12	Same as U10				
U13*	PRESET MODULE	1	31689-	14632	
U14	Same as U6				
U15	Same as U4				
U16	Same as U4				
U17	PRESET MODULE	1	31689-18	14632	
U18	Same as U10				
U19	PRESET MODULE	1	31689-12	14632	
U20	Same as U10				
U21*	PRESET MODULE	1	31689-	14632	
U22	Same as U6				
U23	Same as U4				
U24	Same as U4				
U25	PRESET MODULE	1	31689-17	14632	
U26	PRESET MODULE	1	31689-14	14632	
U27	PRESET MODULE	5	31689-19	14632	
U28	Same as U10				
U29*	PRESET MODULE	1	31689-	14632	
U30	Same as U6				
U31	Same as U4				
U32	Same as U4				
U33	Same as U27				
U34	Same as U27				
U35	Same as U27				
U36	Same as U27				
U37*	PRESET MODULE	1	31689-	14632	
U38	Same as U6				
U39	Same as U4				
U40	Same as U4				
U41	Same as U4				

* Preset Customer Selected.

5.4.6.1 Part 16513, Solid State Numeric Display REF DESIG PREFIX A4A1

REF DESIG	DESCRIPTION	QTY. PER ASSY.	MANUFACTURER'S PART NO.	MFR. CODE	RECM. VENDOR
C1	CAPACITOR, ELECTROLYTIC, TANTALUM: 4.7 μF, 10%, 35V	1	CS13BF475K	81349	56289
C2	CAPACITOR, CERAMIC, DISC: 0.1 μF, -20+80%, 25V	1	DFJ3	73899	
U1	INTEGRATED CIRCUIT	6	5082-7300	28480	
U2	Same as U1				
U3	Same as U1				
U4	Same as U1				
U5	Same as U1				
U6	Same as U1				

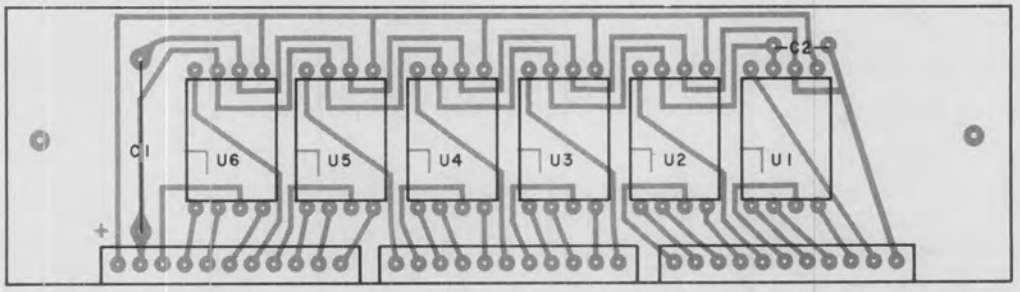
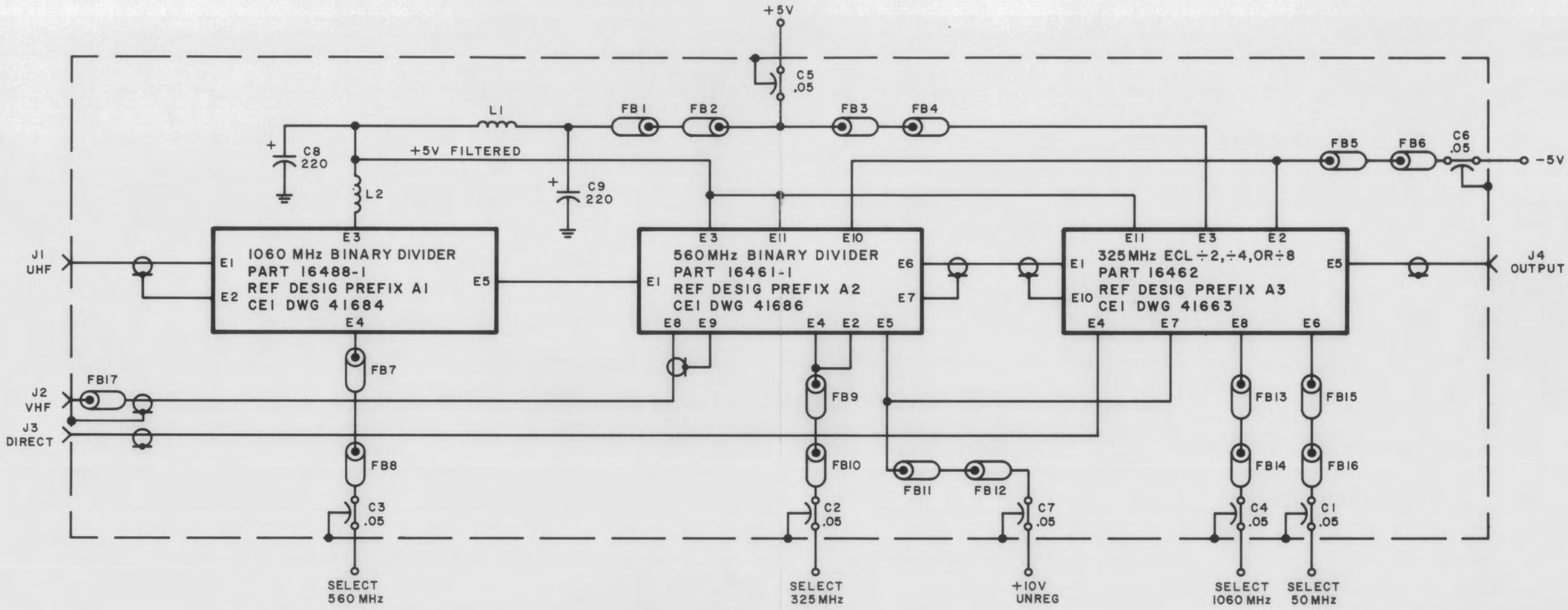


Figure 5-15. Part 16513 Solid State Numeric Display (A4A1), Location of Components

SECTION VI

SCHEMATIC DIAGRAMS



NOTES:
1. CAPACITANCE IS IN μF.
2. FOR WIRING TO PLUG, SEE DETAIL A.

DETAIL A

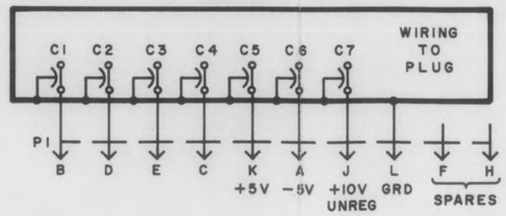
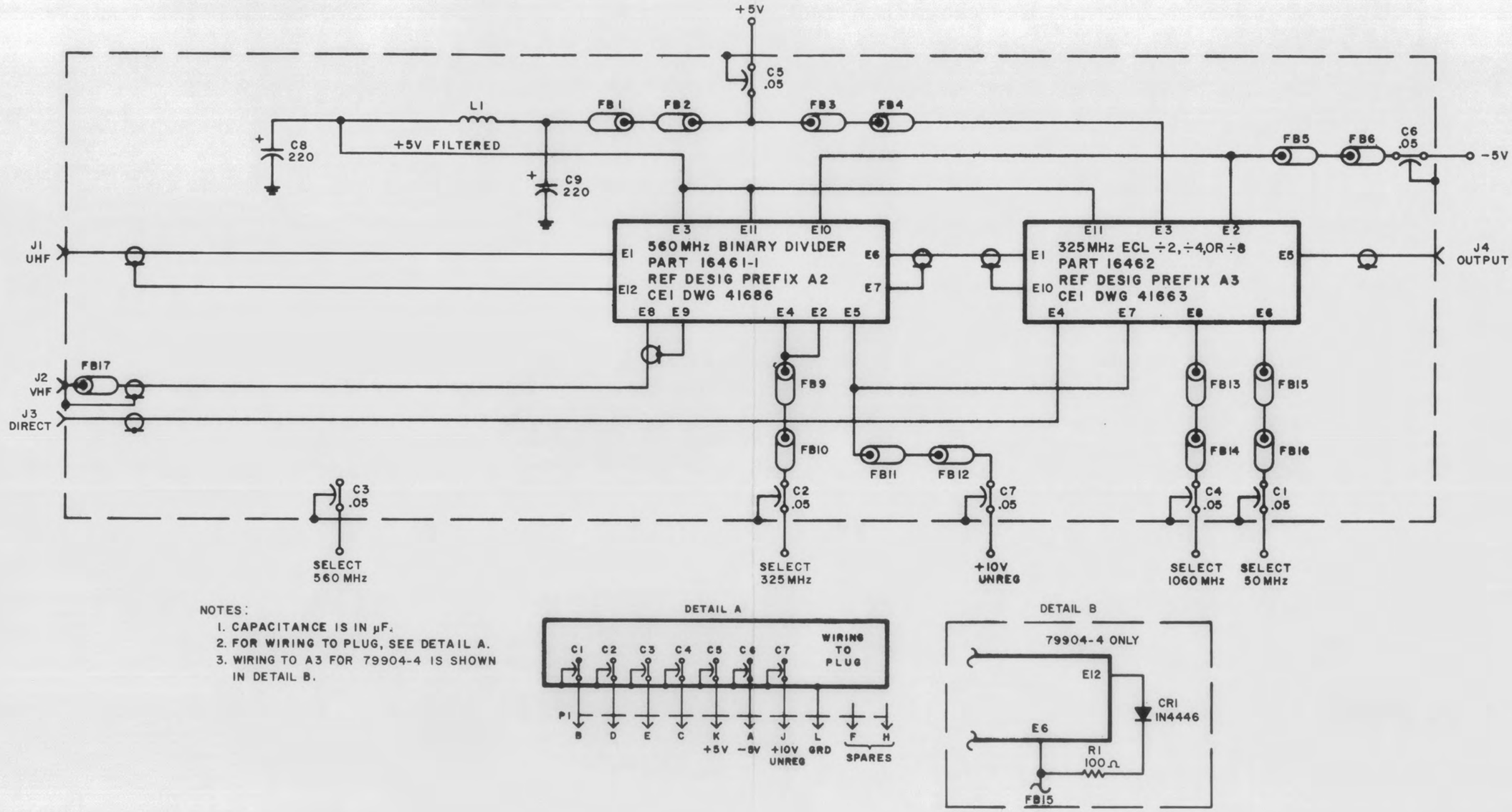


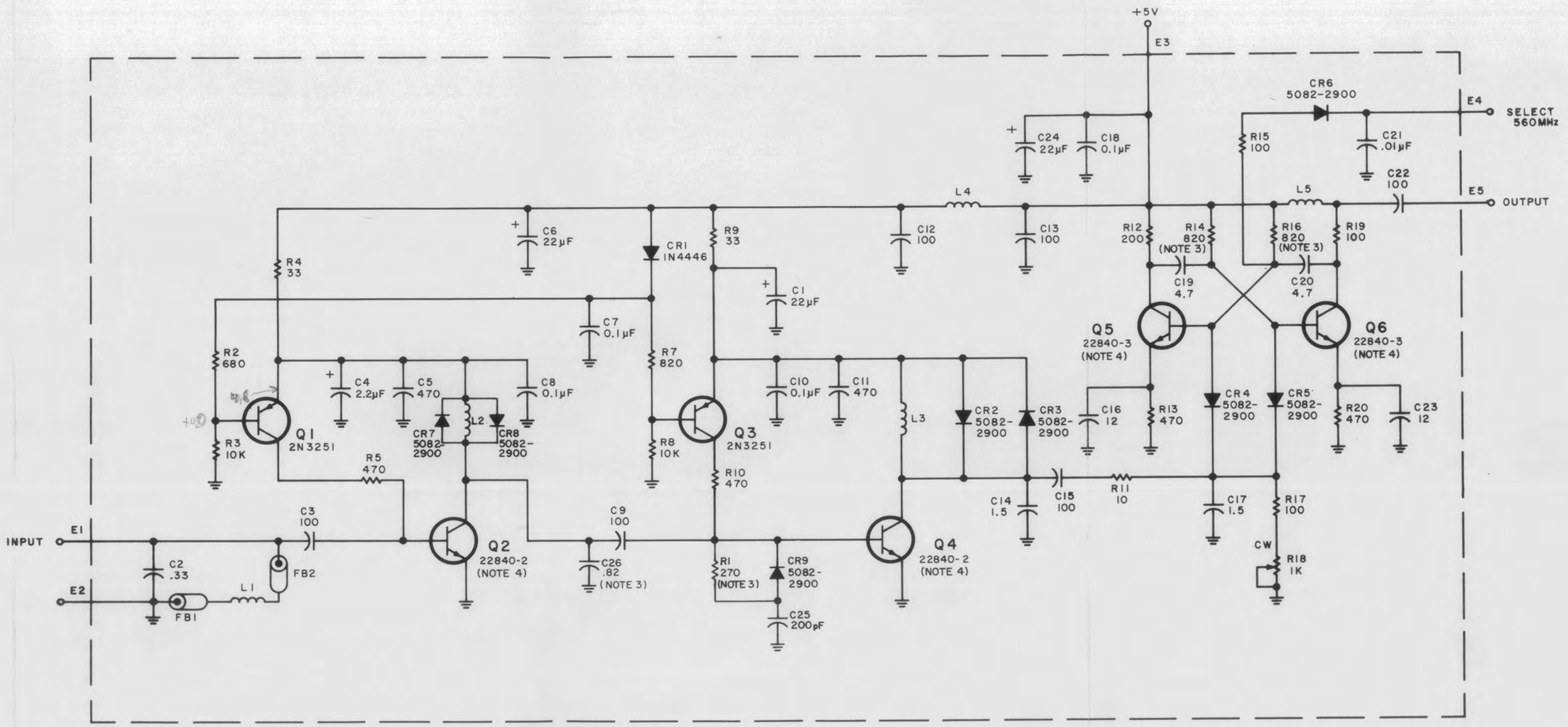
Figure 6-1. Type 79904-1 Prescaler Assembly (A1), Schematic Diagram (DRO-309A and DRO-333 only)



NOTES:

1. CAPACITANCE IS IN μF.
2. FOR WIRING TO PLUG, SEE DETAIL A.
3. WIRING TO A3 FOR 79904-4 IS SHOWN IN DETAIL B.

Figure 6-2. Type 79904-2 Prescaler Assembly (A1), Schematic Diagram (DRO-315 and DRO-302B only)



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ± 5%, 1/8 W.
   b) CAPACITANCE IS IN pF.
2. CW ON R18 DENOTES CLOCKWISE ROTATION OF ACTUATOR.
3. NOMINAL VALUE. FINAL VALUE FACTORY SELECTED
4. FOR Q2, Q4, Q5, & Q6 LEAD ARRANGEMENT SEE DETAIL A.

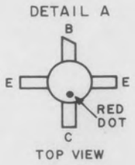
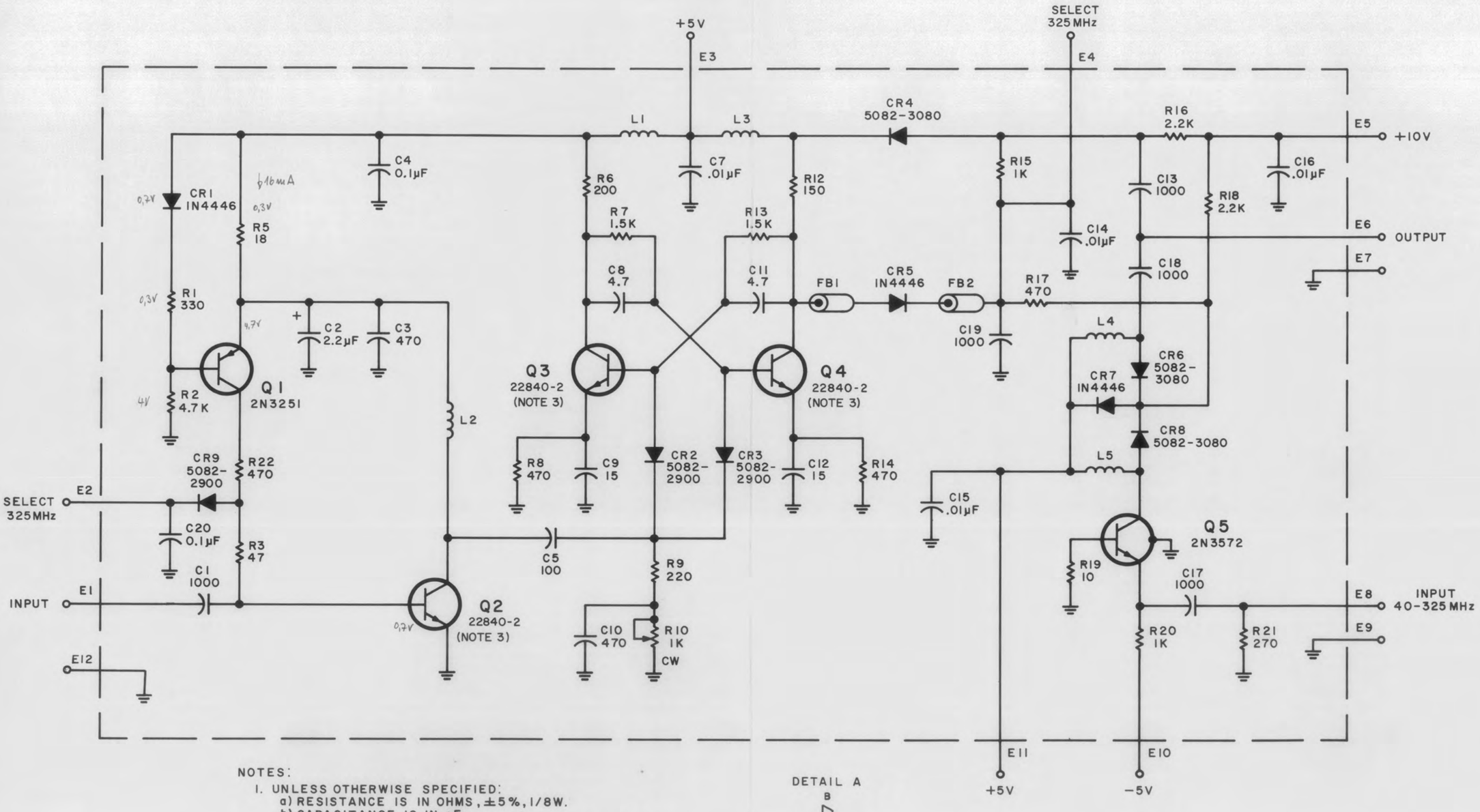


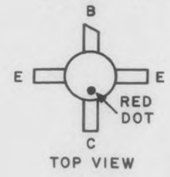
Figure 6-3. Part 16488-1 1060 MHz Binary Divider (A1A1), Schematic Diagram (DRO-309A and DRO-333 only)



NOTES:

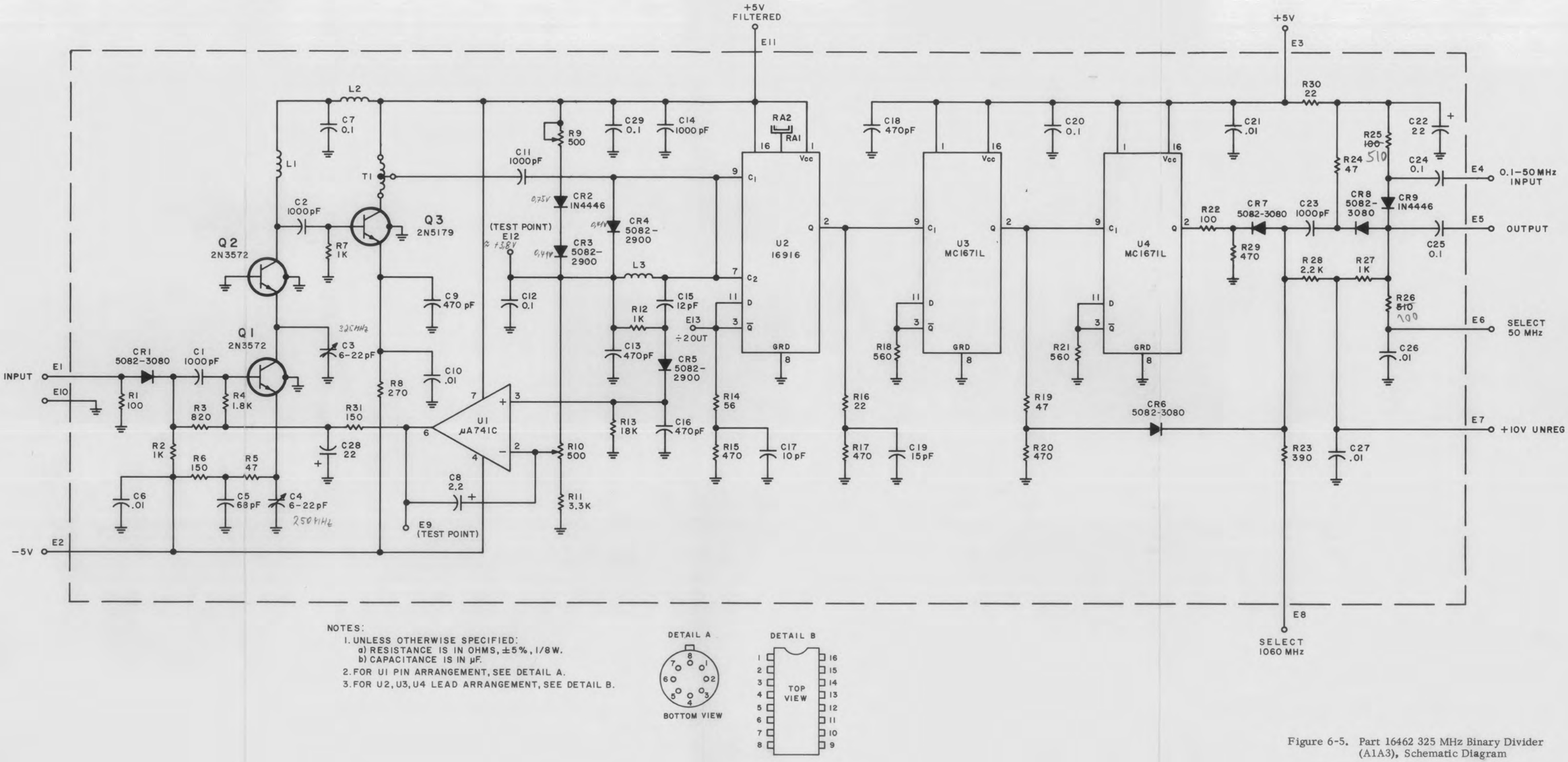
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN pF.
2. CW ON R10 DENOTES CLOCKWISE ROTATION OF ACTUATOR.
3. FOR Q2, Q3, Q4 LEAD ARRANGEMENT, SEE DETAIL A.

DETAIL A



TOP VIEW

Figure 6-4. Part 16461-1 560 MHz Binary Divider (A1A2), Schematic Diagram



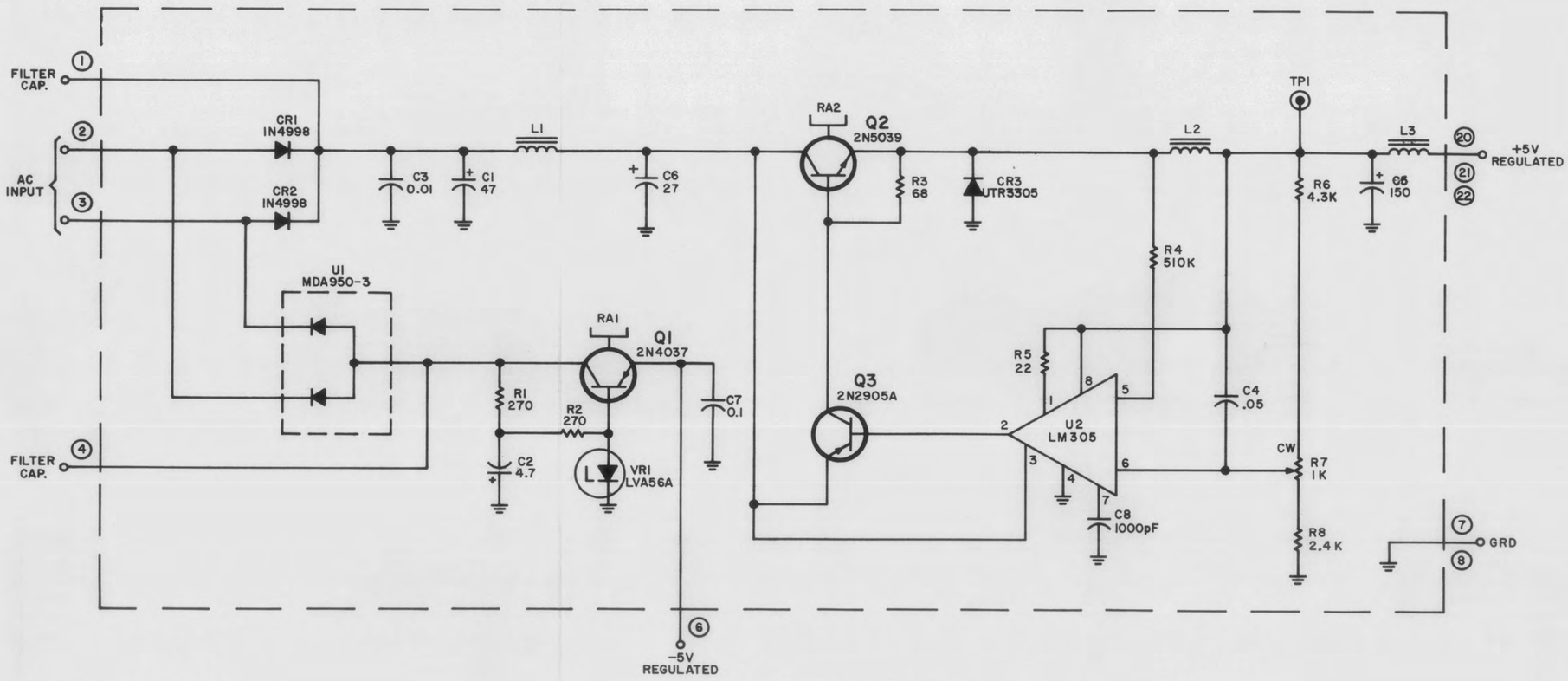
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, ±5%, 1/8W.
   b) CAPACITANCE IS IN µF.
2. FOR U1 PIN ARRANGEMENT, SEE DETAIL A.
3. FOR U2, U3, U4 LEAD ARRANGEMENT, SEE DETAIL B.

DETAIL A

DETAIL B

Figure 6-5. Part 16462 325 MHz Binary Divider (A1A3), Schematic Diagram

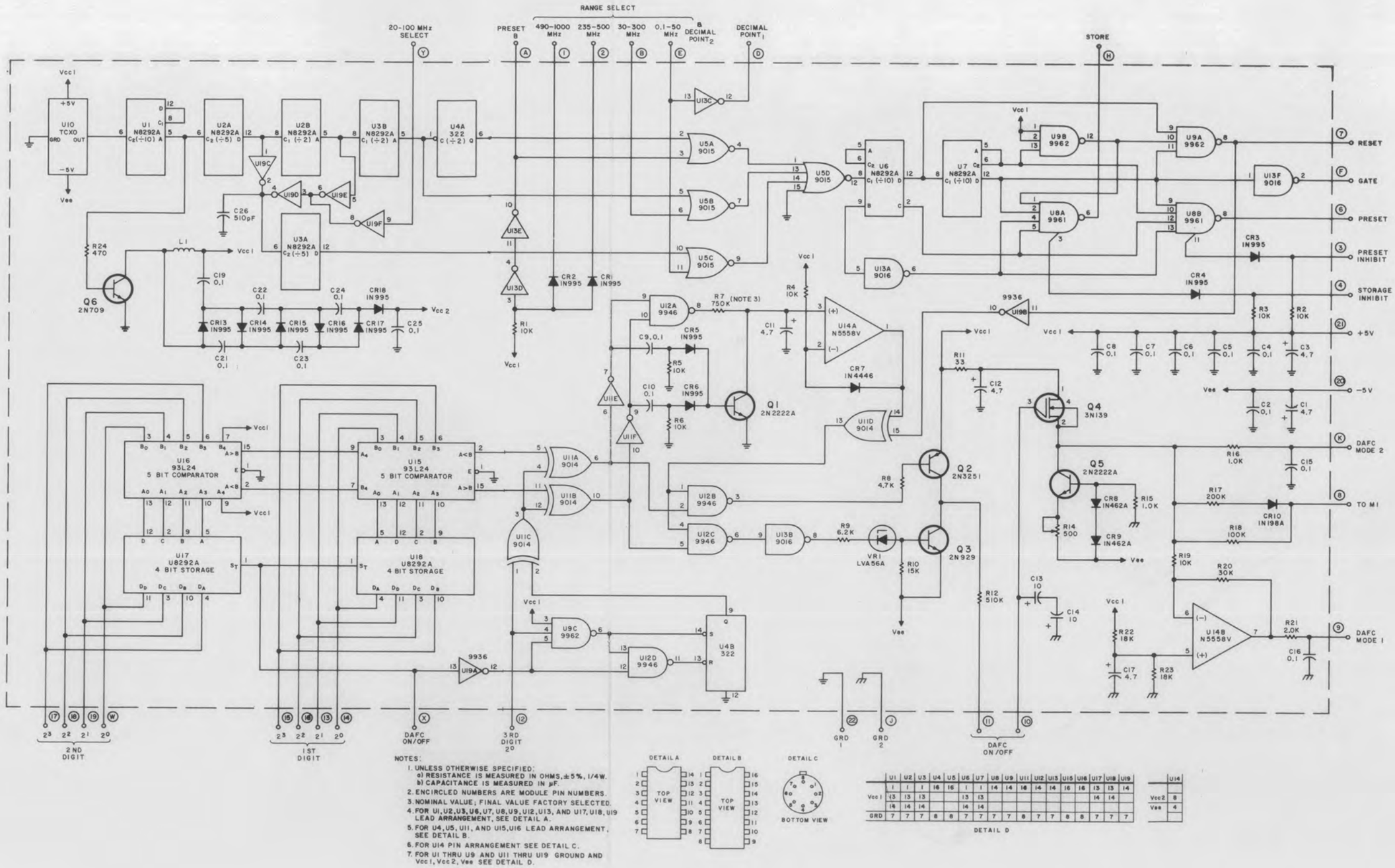


NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS MEASURED IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS MEASURED IN μF.
2. ENCIRCLED NUMBERS ARE MODULE PIN NUMBERS.
3. CW ON R7 DENOTES CLOCKWISE ROTATION OF ACTUATOR.
4. FOR U2 PIN ARRANGEMENT, SEE DETAIL A.

DETAIL A

BOTTOM VIEW

Figure 6-6. Type 76192 Switching Regulator (A2), Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS MEASURED IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS MEASURED IN μF.
2. ENCIRCLED NUMBERS ARE MODULE PIN NUMBERS.
3. NOMINAL VALUE; FINAL VALUE FACTORY SELECTED.
4. FOR U1, U2, U3, U6, U7, U8, U9, U12, U13, AND U17, U18, U19 LEAD ARRANGEMENT, SEE DETAIL A.
5. FOR U4, U5, U11, AND U15, U16 LEAD ARRANGEMENT, SEE DETAIL B.
6. FOR U14 PIN ARRANGEMENT SEE DETAIL C.
7. FOR U1 THRU U9 AND U11 THRU U19 GROUND AND Vcc1, Vcc2, Vee SEE DETAIL D.

DETAIL A

DETAIL B

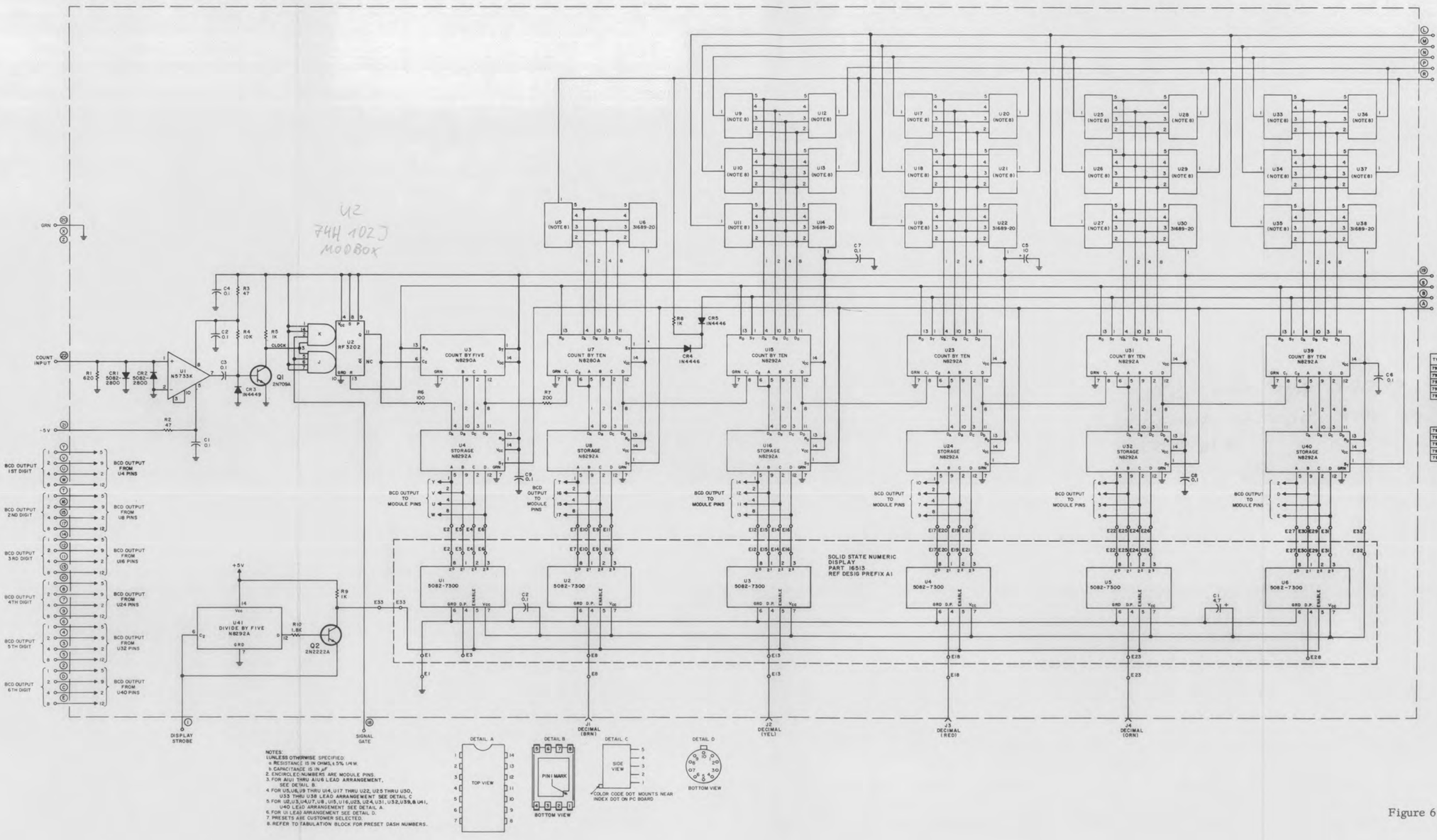
DETAIL C

DETAIL D

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U11	U12	U13	U15	U16	U17	U18	U19
	1	1	1	16	16	1	1	14	14	14	14	14	16	16	13	13	14
Vcc1	13	13	13			13	13								14	14	
	14	14	14			14	14										
GRD	7	7	7	8	8	7	7	7	7	8	7	7	8	8	7	7	7

	U14
Vcc2	8
Vee	4

Figure 6-7. Type 79907 Gate Generator and DAFC (A3), Schematic Diagram



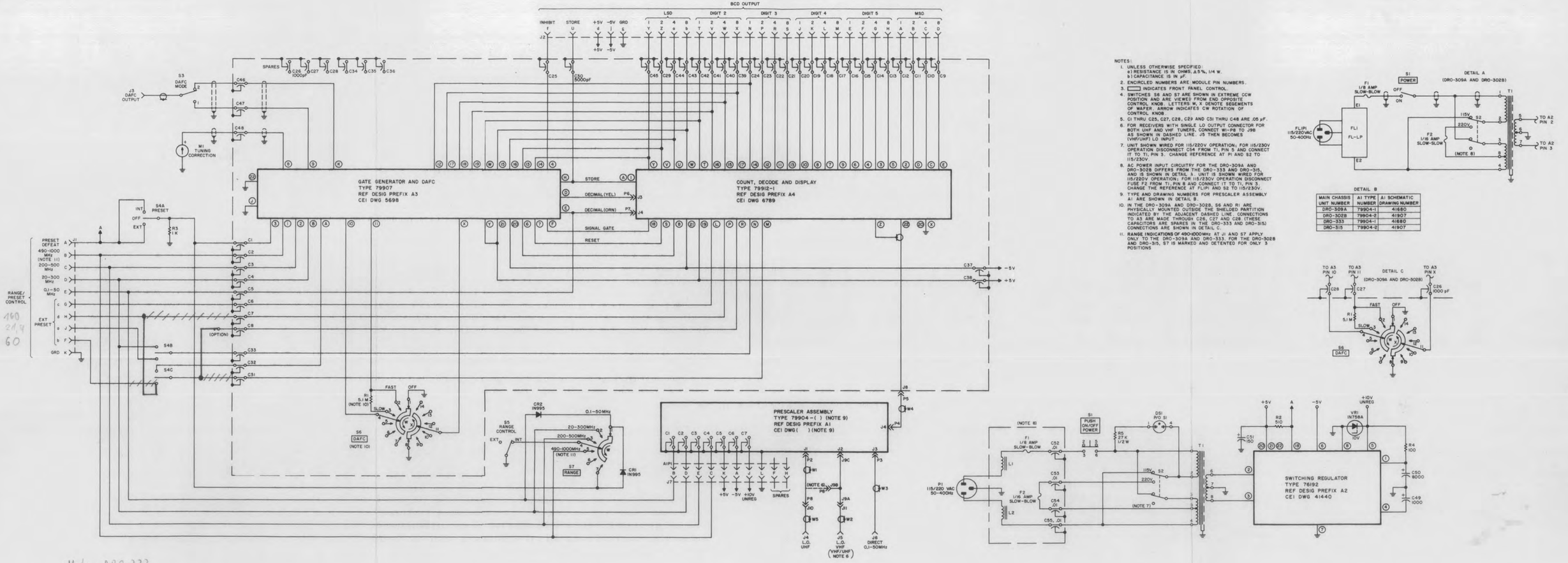
TABULATION A

TYPE NO.	PRESET	REF DESIG	3/689-	REF DESIG	3/689-	REF DESIG	3/689-	REF DESIG	3/689-	REF DESIG	3/689-	IF OFFSET
79912-1	a			U9	-16	U17	-18	U25	-17	U33	-19	0 2 1 4 0
79912-1	b			U10	-10	U18	-10	U26	-14	U34	-19	0 6 0 0 0
79912-1	c			U11	-10	U19	-12	U27	-19	U35	-19	0 0 5 0 0
79912-1	d			U12	-10	U20	-10	U28	-10	U36	-19	1 0 0 0 0
79912-1	e	U5	NOTE 7	U13	NOTE7	U21	NOTE 7	U29	NOTE 7	U37	NOTE7	- - - - -

79912-2	a			U9	-16	U17	-18	U25	-17	U33	-19	0 2 1 A 0
79912-2	b			U10	-10	U18	-10	U26	-14	U34	-19	0 6 0 0 0
79912-2	c			U11	-13	U19	-19	U27	-18	U35	-19	0 1 0 7 0
79912-2	d			U12	-15	U20	-10	U28	-19	U36	-19	0 0 9 5 0
79912-2	e	U5	-15	U13	-17	U21	-14	U29	-19	U37	-19	0 0 3 2 5

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, ±5% 1/4 W.
   b. CAPACITANCE IS IN μF.
2. ENCIRCLED NUMBERS ARE MODULE PINS.
3. FOR A1U1 THRU A1U8 LEAD ARRANGEMENT, SEE DETAIL B.
4. FOR U5, U6, U9 THRU U14, U17 THRU U22, U25 THRU U30, U33 THRU U38 LEAD ARRANGEMENT SEE DETAIL C.
5. FOR U2, U3, U4, U7, U8, U15, U16, U23, U24, U31, U32, U39, & U41, U40 LEAD ARRANGEMENT SEE DETAIL A.
6. FOR U1 LEAD ARRANGEMENT SEE DETAIL D.
7. PRESETS ARE CUSTOMER SELECTED.
8. REFER TO TABULATION BLOCK FOR PRESET DASH NUMBERS.

Figure 6-8. Type 79912-1 Count, Decode, and Display (A4), Schematic Diagram



Note: DRO-333
For 160 MHz Preset change wiring to blue lines

Figure 6-9. Types DRO-309A, DRO-302B, DRO-333, and DRO-315 Frequency Counters Main Chassis, Schematic Diagram