Table 1-1. Types 232-1 and 232-2 Tunable Filters, Specifications

Tuning Range	2 to 30 MHz
Noise Figure	6 dB, maximum
Input Impedance	50 ohms, nominal
Input VSWR	2.5:1, maximum
Output Center Frequency	232-1, 15 kHz; 232-2, 25 kHz
Output Bandwidth	5 kHz
Output Level	1V, rms, into 75-ohm load
Local Oscillator Radiation	10 μV, maximum
Image Rejection	60 dB, minimum
IF Rejection	60 dB, minimum
Internally Generated Spurious Signals	Not greater than 50 dB below nominal output level
Fine Tuning Range	±100 kHz, approximately
Gain Control Modes	Manual and AGC
Gain Control Range	80 dB, minimum, in either mode
Local Oscillator Output	50 mV, minimum, into 50-ohm load
COR Sensitivity	10 mV to 1.0V, front-panel adjustable
COR Attack Time	10 sec., approximately
COR Release Time	Less than 1.0 second
DAFC Stability	Holds receiver within ±100 Hz of set frequency for indefinite period
Input Power	115 or 230 Vac, 50-400 Hz
Power Consumption	6 watts, approximately
Dimensions	3.25 inches high, 8 inches wide, and 15.7 inches deep
Weight	6 pounds, approximately

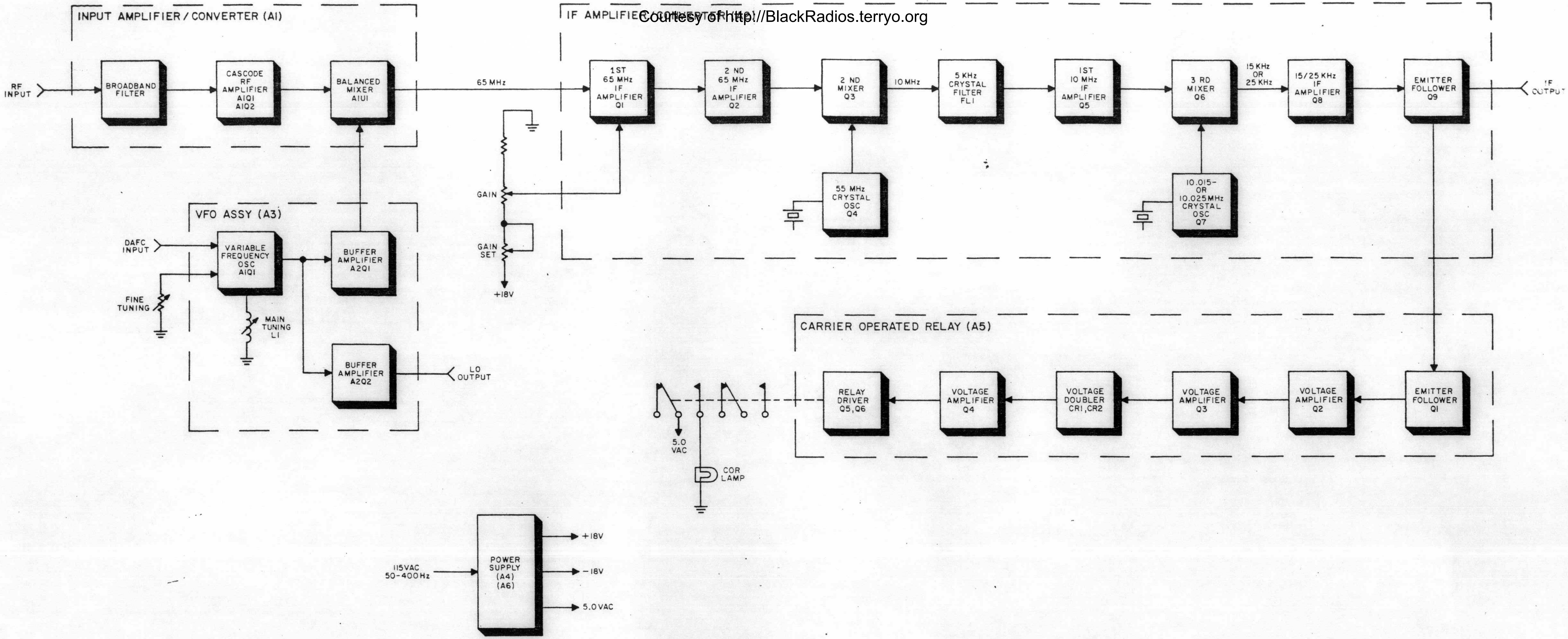


Figure 2-1. Types 232-1 and 232-2 Tunable Filters, Functional Block Diagram

SECTION I

GENERAL DESCRIPTION

1.1 ELECTRICAL CHARACTERISTICS

The CEI Types 232-1 and 232-2 Tunable Filters are designed to receive, amplify, and convert RF signals in the 2-MHz to 30-MHz frequency range to an undemodulated 15-kHz or 25-kHz IF output. The output signal bandwidth is 5 kHz. Both tunable filters utilize triple conversion. Initial conversion of the input signal is up to 65 MHz for maximum image rejection and minimum conducted local oscillator radiation. The second conversion is down to 10 MHz, and the third conversion is down to 15 kHz for the 232-1 and 25 kHz for the 232-2. The local oscillator in each of the filters can be locked in 100-Hz increments over the entire tuning range to an external frequency counter having DAFC (digital automatic frequency control). The stability of the filters then approaches that of the counter's internal reference source. A carrier operated relay (COR) circuit is included in the filters which provides a set of normally open and normally closed relay contacts on the rear apron. A threshold control and indicator lamp for the COR are mounted on the front panel. Release time of the relay is approximately 1.0 second after the loss of the activating carrier. Additional specifications for the 232-1 and 232-2 filters are listed in Table 1-1.

1.2 MECHANICAL CHARACTERISTICS

1.2.1 Figure 1-1 is a front-view of a typical 232-( ) Tunable Filter. Mounted on the front panel are the GAIN, FINE TUNING, and COR THRESHOLD controls, the COR lamp, the power toggle switch, and the main tuning knob and tape dial. The tuning control is equipped with a dial lock which is engaged when the LOCK level is depressed. Mounted on the rear apron of the filters are the RF input, DAFC input, LO output, and IF output jacks, all of which are BNC type receptacles, and the three-pin COR output connector. The rear apron also mounts the power cord and line fuse F1. The 232-( ) front panel and main chassis are constructed of aluminum. The front panel is overlaid with a black-anodized etched bezel.

1.2.2 The 232-( ) filters are constructed in a half-rack size and are designed for mounting in a CEI Type EF-201A equipment frame which will accommodate two units. Guide pins mounted in the frame mate with the two holes in the rear apron to properly align the filters. Two knurled screws on the 232-( ) front panel fasten to the frame front panel providing a secure mechanical connection. The equipment frame occupies only 3.5 inches of vertical space in a standard 19-inch rack. Overall dimensions of the filters are 3.25 inches high, 8 inches wide, and 15.7 inches deep. A typical 232-( ) weighs approximately 6 pounds.

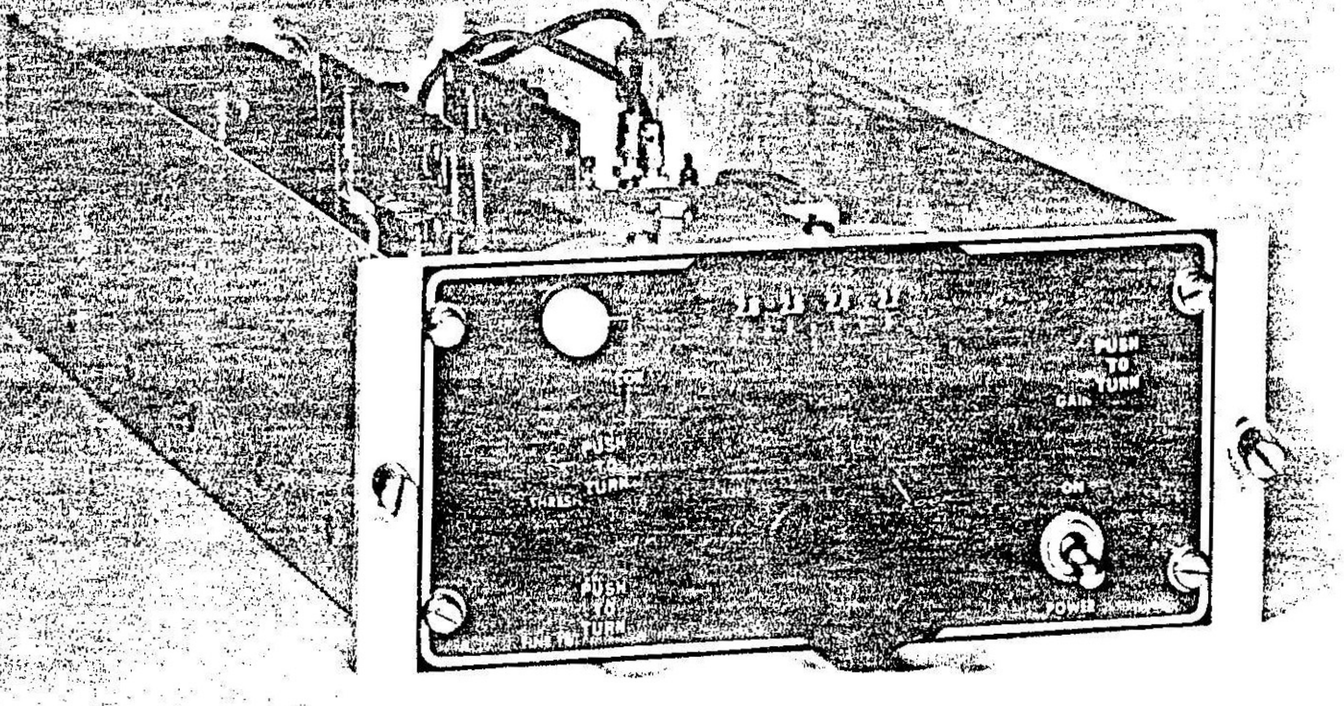


FIGURE I-I. TYPE 232-( ) TUNABLE FILTER, FRONT VIEW

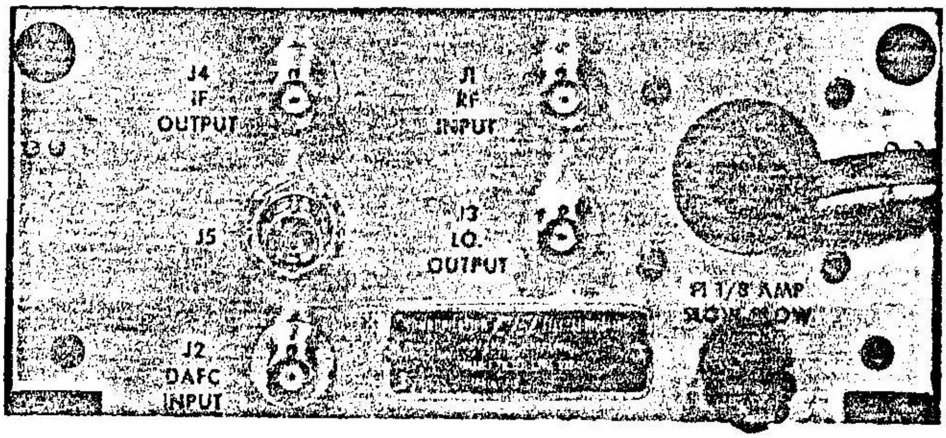


FIGURE 1-2. TYPE 232-( ) TUNABLE FILTER, REAR VIEW

SECTION II

CIRCUIT DESCRIPTION

2.1 GENERAL

A description of the circuits in the 232-( ) Tunable Filter is presented in the following paragraphs using the functional block diagram Figure 2-1, and the schematic diagrams, Figures 6-1 through 6-10. Note that the unit numbering method is used for electrical components, which means that parts on subassemblies and modules carry a prefix before the usual class letter and number of the item (such as A1C1 and A5Q1). These subassembly prefixes are omitted from callouts on the illustrations and from some references to the components in the text except in those cases where confusion might result from their omission.

2.2 FUNCTIONAL DESCRIPTION

2.2.1 The 232-1 and 232-2 Tunable Filters are triple conversion units designed to translate RF signals in the 2-MHz to 30-MHz frequency range to an undemodulated output centered at 15 kHz or 25 kHz.

2.2.2 Incoming signals to the 232-( ) are fed through a fixed-tuned, broadband filter having a 28-MHz bandwidth, to cascode RF amplifiers A1A1Q1 and A1A1Q2. The amplified output from this network is inductively coupled through a matching transformer and a resistive pad to balanced mixer module A1A1U1.

2.2.3 Transistor A3A1Q1 functions as the variable frequency oscillator in the filters. It is tuned across a range of 67 to 95 MHz by means of single-section inductuner A3L1. Fine tuning of the VFO is accomplished by means of a front-panel mounted potentiometer which applies a varying voltage to a varactor diode in the VFO tank circuit. Changes in the capacitance of the varactor are inversely proportional to the applied voltage, resulting in a tank circuit capacitance change and a shift in the VFO frequency. A second varactor operates in a similar manner when the DAFC mode is employed. The changing bias voltage in this case is provided by the associated electronic frequency counter. The oscillator output is fed through a buffer amplifier, A3A2Q2, to balanced mixer A1A1U1 in the input amplifier/converter.

2.2.4 The 65-MHz difference frequency produced by the mixing action in A1A1U1 is fed to A2Q1, the first of two IF amplifiers for this center frequency. This stage, a dual, insulated gate, field effect transistor (IGFET), is gain controlled by the front-panel GAIN potentiometer. Input signals are fed to gate no. 1 (pin 3) and the gain control voltage is applied to gate no. 2 (pin 2). Amplified output signals from the drain of A2Q1 are fed through a double-tuned circuit to A2Q2, a common emitter amplifier. Collector signals from this stage are fed through another double-tuned network to the second mixer, A2Q3, a dual IGFET. The mixer heterodynes the 65-MHz IF signal with the 55-MHz output from crystal oscillator A2Q4. The 10-MHz difference frequency produced in this mixer is fed through a single-tuned network and crystal filter A2FL1 to 10-MHz amplifier A2Q5, a third IGFET. The filter bandwidth is 5 kHz. IF signals at the 10-MHz center frequency are coupled from the drain of A2Q5 to the third mixer, A2Q6. This mixer heterodynes the 10-MHz IF signal with one of two different outputs from crystal oscillator A2Q7. In the 232-1 this is a 10.015-MHz signal, and in the 232-2 it is a 10.025-MHz output. The difference signal resulting from the mixing action is taken from the drain of A2Q6 and is coupled through voltage amplifier A2Q8 and output emitter follower A2Q9 to the rear-apron IF output jack and the COR threshold control. The latter component applies the signal to the carrier operated relay module.

2.2.5 The COR circuit consists of an input emitter follower, A5Q1, driving voltage amplifiers A5Q2 and A5Q3. A diode voltage doubler, A5CR1 and A5CR2, provides additional gain and then feeds the signal to voltage amplifier A5Q4. This stage in turn supplies the input signal to relay driver transistors A5Q5 and A5Q6. Two sets of normally open and two sets of normally closed relay contacts are available on a rear-apron terminal board.

2.2.6 The power supply for the 232-( ) filters consists of various main chassis components plus regulator modules A4 and A6 which supply +18 Vdc and -18 Vdc respectively.

2.3 TYPE 79559 INPUT AMPLIFIER/CONVERTER ASSEMBLY

The schematic diagram for the assembly is Figure 6-1; A1 is its reference designation prefix. The assembly contains a single etched circuit board which mounts the amplifier/converter. This board is a type 79558 input amplifier/converter and its schematic diagram is Figure 6-2. Parts on this board carry the reference designation prefix A1.

2.3.1 Input Filter. - Incoming RF signals are passed through a fixed tuned, broadband, high-pass, low-pass filter before being applied to the RF amplifiers. Inductors L1 through L3 plus capacitors C1 and C2, form a high-pass filter having a 2-MHz roll-off frequency. The remaining filter components, C3 through C6, and L4 through L6 four a low-pass filter with a 30-MHz cut-off frequency. The resultant response is extremely flat from 2 to 30 MHz.

2.3.2 RF Amplifiers. - Transistors Q1 and Q2 operate as RF amplifiers in a cascode circuit. Q1 is a common emitter amplifier whereas Q2 is operated in a grounded base configuration. Parasitic suppressor R7 feeds the signal from Q1 to Q2. Negative feedback to prevent oscillation is taken from the collector of Q2 and fed through C12 and R6 to the base of Q1. Amplified output signals from the collector of Q2 are coupled through impedance matching transformer T1 to balanced mixer, U1. Resistors R12, R13, and R14 terminate the input port of U1 in a purely resistive load for maximum transfer of the signal.

2.3.3 Balanced Mixer. - The balanced mixer, U1, is a completely self-contained, sealed module. It heterodynes the incoming RF signals with the output from variable frequency oscillator, A3A1Q1. The mixer suppresses the incoming signal and the local oscillator signal producing the sum and difference of the two. Since the input circuit in the IF amplifier is tuned to the difference frequency of 65 MHz, only this frequency is passed. This first IF frequency is fed directly to the input of the IF amplifier/converter.

2.4 TYPE 7754 VARIABLE FREQUENCY OSCILLATOR ASSEMBLY

The VFO assembly consists of the main tuning mechanism plus a part 15332 VFO and a part 15340 buffer amplifier. The schematic diagram for the entire assembly is Figure 6-4; its reference designation prefix is A3.

2.4.1 Part 15332 Variable Frequency Oscillator Board. - Figure 6-5 is the schematic diagram for this board; it carries the reference designation prefix A3A1. Transistor Q1 operates in a Clapp circuit. It is tuned by A3L1, a single-section inductuner which is ganged with the main tuning knob and gear train. Regenerative feedback to sustain oscillation is fed through C3 to the base of the stage. Fine tuning of the oscillator is accomplished by the front panel FINE TUNING potentiometer which operates in conjunction with varactor diode CR2. The capacitance of this component is inversely proportional to the reverse bias applied to it. Rotation of the FINE TUNING control in the clockwise direction increases the reverse bias applied to CR2 which decreases its capacitance and increases the oscillator frequency. A second varactor, CR1, performs the same function when the DAFC mode is employed. The reverse bias in this case is obtained from an associated frequency counter and fed to CR1 through rear-apron connector J2. The LO output signal is taken from the junction of C1 and C2 and fed to the input of buffer amplifier A3A2.

2.4.2 Part 15340 Buffer Amplifier. - Figure 6-6 is the schematic diagram for the buffer amplifier; A3A2 is its reference designation prefix. The LO signal is simultaneously coupled through dc blocking capacitors C1 and C2 to buffer amplifiers Q1 and Q2 respectively. Torroid transformers T1 and T2 form the collector loads for the two stages. These two components, along with their distributed capacity, develop the output signals. Capacitor C1 couples the output from Q1 through a resistive pad, having approximately 9 dB of attenuation, to output jack J2. This signal is then fed to the balanced mixer in the input amplifier/ converter. The output from Q2 is coupled through C10 and a similar resistive pad to jack J1, and then to the LO OUTPUT connector, J3, on the rear apron.

2.5 TYPE 79595 IF AMPLIFIER/CONVERTER

The schematic diagram for this subassembly is Figure 6-3; its reference designation prefix is A2.

2.5.1 65-MHz IF Amplifiers. - Transistor Q1, a dual IGFET, is the first IF amplifier for the 65-MHz center frequency. Incoming signals are fed to gate no. 1 of the stage from the low-pass input filter made up of C1 through C3 and L1. This circuit matches the output impedance of the balanced mixer to the input impedance of the first IF amplifier. Capacitor C3 tunes the input to 65 MHz. Blocking capacitor C4 couples the filter output to the signal gate of Q1. Amplified output signals are taken from the drain of the stage and fed through a double-tuned bandpass network to the base of the second 65-MHz amplifier, Q2. This transistor, operating in a common emitter configuration, amplifies and inverts the IF signal and feeds it through a double-tuned filter to the second mixer, Q3. Capacitor C15 feeds back out-of-phase signals from the junction of L5 and C18, to the base of Q2 to neutralize the stage.

2.5.2 55-MHz Oscillator and Second Mixer. - Conversion of the 65-MHz IF signal down to 10-MHz occurs in the second mixer stage, Q3. The IF signal is applied to gate no. 1 of this dual IGFET and the output of crystal oscillator Q4 is applied to gate no. 2. Heterodyning of the two signals produces the second IF frequency of 10 MHz which is taken from the drain of Q3. The crystal oscillator operates in a Clapp circuit with regenerative feedback taken at the junction of voltage dividing capacitors C53 and C54 and fed to the emitter through crystal Y1. The base of Q4 is held at RF ground by C51. Variable capacitor C55 peaks the oscillator to the crystal frequency while C56 couples the output to the mixer.

2.5.3 Crystal Filter. - Impedance matching capacitors C27 and C28 tap down the drain load of Q3 and couple the IF signal to crystal filter FL1. This unit sets the output bandwidth of the 232-( ) to 5 kHz. Test point TP1 is included at the output of the crystal filter to provide a means of monitoring the filter response by means of a wideband oscilloscope.

2.5.4 10-MHz IF Amplifier. - Blocking capacitor C30 couples the IF signal to gate no. 1 of 10-MHz IF amplifier Q5, a dual IGFET. The gain of this stage is also controlled by the front-panel GAIN potentiometer. A single-tuned network made up of L8 and C38 forms the drain load for Q5 and develops the amplified output signal which is coupled through dc blocking capacitor C39 to gate no. 1 of the third mixer, Q6.

2.5.5 Third Mixer/Crystal Oscillator. - Transistor Q6 functions as the third mixer. It is a dual IGFET which heterodynes the 10-MHz IF input signal with the output from crystal oscillator Q7. In the 232-1 filter the crystal frequency is 10.015 MHz. The crystal frequency in the 232-2 filter is 10.025 MHz. Q7 operates in a Colpitts configuration with regenerative emitter-to-base feedback through C57. The collector is held at RF ground by C59. Coupling capacitor C60 feeds the oscillator output, which is taken from the feedback circuit, to gate no. 2 of the mixer. The resultant difference frequency of either 15 kHz or 25 kHz is taken from the drain of Q6 and coupled through blocking capacitor C43, a pi-network impedance matching circuit (C44, C45, L9, R38) and blocking capacitor C47, to the base of voltage amplifier Q8.

2.5.6 Output Amplifier and Emitter Follower. - Transistor Q8 provides some additional voltage gain for the IF signal prior to applying it to output emitter follower Q9. The emitter follower insures that the IF output present at rear-apron jack J4 appears as a nominal 50-ohm impedance to the load. This IF output signal is also fed to the COR THRESHOLD control, R6, on the front panel.

2.6 TYPE 79563 CARRIER OPERATED RELAY

Figure 6-8 is the schematic diagram for this module; its reference designation prefix is A5.

2.6.1 The IF input signal to the COR is obtained from the arm of the THRESHOLD potentiometer. This input, which is positive going with increasing signal strength, is coupled through blocking capacitor C1 to the base of emitter follower Q1. Output signals from Q1 are fed directly to the base of voltage amplifier Q2. The negative going output which is developed across R5, is coupled through dc blocking capacitor C3 to the base of a second voltage amplifier, Q3. Since this input is negative going, the conduction through Q3 is reduced, producing a positive collector signal which is developed across R10. This output is filtered by C7 and fed to a voltage doubler circuit.

2.6.2 Capacitors C5 and C6 plus diodes CR1 and CR2 form a half-wave voltage doubler. This circuit provides a pulsating, negative dc output which is approximately twice the applied ac voltage peak. During positive half-cycles of the input signal diode CR1 conducts allowing C5 to charge to the peak voltage less the drop across the diode. During the negative half-cycles diode CR2 conducts and current flows from ground through C6. Since C5 is already charged to approximately the peak of the applied voltage, and since it is in series with the input, its potential is added to the applied voltage. Thus, C6 charges to the peak of the applied voltage less the drop across CR2, plus the charge stored by C5. This negative dc voltage is reflected through R13 and R16 to the base of Q4.

2.6.3 With no signal input to the module, transistor Q4 is conducting while Q5 and Q6 are cut off. The latter two stages function as a switch, relay driver, and time delay network. The voltage at the base of Q4 is zero under these conditions, whereas the emitter is clamped at -0.6 volts by diode CR3. With the COR THRESHOLD control fully clockwise and the threshold set potentiometer properly adjusted, an input signal level of only 10 mV is required to activate the relay. The applied input signal will cause the voltage on the base of Q4 to decrease below -0.6 volts cutting the transistor off. Once Q4 is cut off, a positive voltage at the junction of R20 and CR4 turns on Q5 and Q6. At the time Q4 cuts off, capacitor C8 discharges through CR4 and R20. The resultant bias applied to Q5 increases toward +18 volts at a rate determined by the RC time of the two components and results in a 10 second delay after the arrival of a signal before the relay transfers. Positive feedback through R21 and R16 occurs as soon as C8 begins to discharge, causing the base of Q4 to become even more negative assuring that the stage will reach full cut-off. This results in positive and rapid relay action. One set of normally open and one set of normally closed relay contacts are available at rear-apron multipin connector, J5. The normally open contacts appear between pins 1 and 2 and the normally closed contacts appear between pins 2 and 3. The front-panel COR lamp is illuminated by the application of 5.0 Vac through the other set of relay contacts.

2.7 POWER SUPPLY

2.7.1 The power supply for the 232-( ) tunable filters consists of various main chassis components plus regulator modules A4 and A6 which supply +18 Vdc and -18 Vdc respectively. The filters are designed to operate from a 115 Vac, 50-65-Hz source. From power line filter FL1, the ac input is fed through line fuse F1 and power switch S1 to the primary winding of transformer T1. The latter has two primary windings, one of which supplies the ac input for the two regulator modules. Three lamps in the tape dial window are illuminated from the remaining secondary winding.

2.7.2 Type 76162 +18 Vdc Power Supply Regulator. - The schematic diagram for this board is Figure 6-7; its reference designation prefix is A4. Transistor Q1 functions as a series regulator whose conduction is controlled by Q2, an emitter follower. Transistors Q3 and Q4 are connected in a differential amplifier configuration. The base of Q4 is held at a fixed potential by Zener diode CR2. The base of Q3 is connected to the regulated output through a sampling network consisting of fixed resistors R5 and R7, and potentiometer R6. The signals at the bases of the two stages are summed in the common emitter circuit to produce a signal at the collector of Q3 that is the difference between the two inputs. Thus, any fluctuation in the output voltage is sensed by Q3, amplified and inverted and fed to the base of Q2. For example, if the output voltage becomes more negative Q3 will conduct harder, causing an increased voltage drop across R2 and R3. This lowers the forward bias voltage and the current flow through Q2. As a result, the current flow through Q1 is reduced, returning the output voltage to its nominal value. Resistor R4 connects the base of Q3 to the input side of the regulator so that voltage fluctuations at this point can be sensed and compensated for by Q1. A differential amplifier is used in the comparison circuit as variations in base-emitter voltage due to temperature changes in one transistor will tend to cancel similar changes in the other. This configuration also permits the reference diode, CR2, to be placed in the base circuit rather than the emitter, as is the case with a one-stage error amplifier. Less current flows through the diode, resulting in a more stable reference voltage.

2.7.3 Type 76176 -18 Vdc Power Supply. - Figure 6-9 is the schematic diagram for the board; A6 is its reference designation prefix. This module employs a single transistor, Q1, operating as a series regulator. If the output tends to become more negative, the emitter-base junction will be reverse biased and the stage will conduct less returning the output to its nominal value.

SECTION III

INSTALLATION AND OPERATION

3.1 INSTALLATION

The 232-1 and 232-2 Tunable Filters are designed to mount in a CEI Type EF-201A Equipment Frame which occupies only 3.5 inches of vertical space and extends approximately 16 inches back into a standard 19-inch rack. Mounting dimensions are shown in Figure 3-1.

3.1.1 Power Connection. - Plug the power cord into a 115 Vac, 50-65-Hz source. The third pin of the power plug grounds the unit. If a three pin receptacle is not available use the adapter provided.

3.1.2 RF Connection. - Connect the source of 2-30-MHz RF signals to RF INPUT jack J1, a BNC-type receptacle.

3.1.3 DAFC Connection. - Connect the source of DAFC voltage to DAFC INPUT jack J2, also a BNC type receptacle.

3.1.4 LO Output. - The local oscillator output signal is available at jack J3 marked LO OUTPUT. This jack is a BNC type receptacle.

3.1.5 IF Output. - Undemodulated IF output signals are available at rear-apron connector J4. This output is centered on 15 kHz in the 232-1 and at 25 kHz in the 232-2.

3.1.6 COR Connection. - One set of normally open contacts from the COR relay is available between pins 1 and 2 of multipin connector J5. The normally closed contacts are available between pins 2 and 3.

3.2 OPERATION

The controls and indicators mounted on the front panel of the 232-( ) are described in the following paragraphs. These controls and indicators are shown in Figure 1-1.

3.2.1 Power Switch. - Placing the POWER toggle switch in the ON position applies power to the filter. The lamps in the tape dial will be illuminated when power is applied.

3.2.2 COR Threshold. - The COR threshold control determines the amplitude of the IF input signal applied to the COR module, and consequently the point at which the relay transfers. In order to change the sensitivity, the knob must be depressed before it is rotated. Clockwise rotation increases the circuit sensitivity.

3.2.3 COR Lamp. - When a signal of sufficient amplitude and duration activates the COR circuit and transfers the relay, the front panel COR lamp will be illuminated.

3.2.4 Fine Tuning. - Vernier tuning of the 232-( ) filter may be accomplished with the FINE TUNING control.

3.2.5 Gain Control. - The overall gain of the demodulator can be varied by the front-panel GAIN potentiometer.

3.2.6 Tuning Knob and Tape Dial. - The main tuning knob and tape dial are used to select the desired input between 2 and 30 MHz. The tuning mechanism is equipped with a dial lock to prevent movement once the desired frequency is selected. The lock is set by depressing the LOCK lever.

SECTION IV

MAINTENANCE

4.1 GENERAL

The CEI Types 232-1 and 232-2 Tunable Filters are designed to operate for long periods of time with just routine maintenance. The units require no special maintenance procedures and normally need only to be cleaned at periodic intervals. Down time will be minimized if trouble occurs if the maintenance technician is familiar with Section II in which the circuits are described, and with the alignment procedures in this section. Reference should also be made to the functional block diagram, Figure 2-1, and the schematic diagrams, Figures 6-1 through 6-10. Field maintenance should be confined to the replacement of fuses and plug-in modules. All other work should be carried out in a well equipped shop and performed by experienced technicians who are familiar with the tunable filters.

4.2 PLUG-IN MODULES

The plug-in modules can be easily removed by simply pulling them upward from the receptacles into which they are fitted. The numbers stenciled on the chassis adjacent to the receptacle pins correspond to the encircled numbers on the schematic diagrams at the points where the connecting leads pass through the lines outlining each module. Modules having different functions are keyed to prevent them from being damaged as a result of being placed in the wrong receptacle. All plug-in modules have their type numbers etched on the back of the cards. By referring to the schematic diagrams their reference designations can be found and thus their proper location in the unit.

4.3 TROUBLESHOOTING

Initial investigation should be directed toward localizing the trouble to a specific section of the filter. In the case of the plug-in modules a quick check can be made by plugging in a spare known to be good. If these substitutions do not cure the trouble, then a series chain consisting of A1 and A2 should be examined by feeding in a signal within the range of the unit, tuning the filter to the signal, and checking for an output from each stage. A complete lack of output could indicate a faulty VFO. Once the inoperative stage is located, voltage and resistance measurements will usually pin point the malfunctioning component. Typical transistor element voltages for the 232 filters are given in Table 4-1.

4.4 MAINTENANCE OF GEAR TRAIN ASSEMBLY

The gear train used in the 232 filters relies on stops built into the inductuner to halt rotation at the high and low ends of the tuning range. It is designed so that routine maintenance is not required. The occasional application of a few drops of light oil to the shaft bearings and the removal of accumulated dust is all that is necessary to assure proper operation.

4.4.1 Dial Lamp Replacement. - To replace a burned out dial lamp proceed as follows:

(1) Remove the two black screws that hold the dial escutcheon. Remove the escutcheon.

(2) Remove the light bar and light disperser by removing the retaining screws.

(3) Gently pull the light bar and printed circuit light board from the gear train.

(4) Rotate the light board up and detach it from the light bar by removing the two screws.

(5) Unsolder the burned out lamp and replace it with a new unit.

(6) Replace the light board by reversing steps (1) through (4).

4.4.2 Alignment of Dial Tape. - A calibrated steel tape is used as the tuning dial. It is geared to the inductuner in such a manner that it is unlikely that it will ever get out of position. However, to check the alignment, or to mechanically realign the dial, follow the steps given below.

(1) Turn the tuning knob clockwise until rotation stops.

(2) The mark to the right of the arrow should line up with the dial pointer. If it does, the tape is properly positioned. If not, proceed with step (3).

(3) Loosen the set screw on the drum drive gear (See Figure 5-1).

(4) Remove the clear plastic top from the tape chamber and by hand move the tape, independent of the gear train to align the mark under the dial pointer. Tighten the drive gear setscrew.

(5) Perform the dial calibration procedures described in paragraph 4.5.3.

4.5 ALIGNMENT PROCEDURES

4.5.1 General. - The alignment procedures given here are suitable when making periodic performance checks, or when making adjustments after replacing transistors or components. Only those controls specifically referred to within a series of steps given for aligning a particular circuit, affect the alignment of that circuit. Those controls not mentioned in any one series of steps may be left in any position. The alignment of this unit should be performed only with suitable equipments by technicians thoroughly familiar with the filter. If the limits and tolerances specified in the following procedures cannot be obtained then a factory alignment is necessary.

4.5.2 Test Equipment Required. - The following equipments or their equivalents are required to completely align the 232-1 and 232-2.

(1) Sweep Generator, Type Telonic SM-2000.

(2) Sweep Generator, Plug-In Head, Telonic Type LH-2

(3) Frequency Counter, Hewlett Packard Type 5245L

(4) Frequency Converter, Hewlett Packard Type 5253B

(5) AC VTVM, Hewlett Packard 400H

(6) Oscilloscope, Tektronix Type 503

(7) Assorted cables, connectors, and alignment tools.

4.5.3 Dial Calibration. - To calibrate the tape dial proceed as follows:

(1) Connect the input of the HP-5245L frequency counter to the LO OUTPUT jack on the rear apron of the 232-( ).

(2) Install the HP-5253B Frequency Converter into the counter.

(3) Set 232-( ) FINE TUNING control to midrange.

(4) Tune the 232-( ) to 2 MHz. The counter should read 67 MHz ±0.7 MHz. If not, adjust capacitor A3C1 for a reading within the 1% tolerance.

(5) Tune the 232-( ) to 30 MHz. The counter should read 95 MHz ±0.9 MHz. If not, slightly readjust A3C1 for a reading within the 1% tolerance.

(6) Check the dial at the 2-MHz end for proper calibration. Readjust A3C1 if necessary. Recheck the high-end of the dial. Continue this procedure until the readings at both the low and high ends are within the 1% tolerance.

4.5.4 Overall Alignment. - Proceed as follows:

(1) Connect equipment as shown in Figure 4-1.

(2) Set output frequency of sweep generator to 15 MHz.

(3) Tune 232-( ) to 15 MHz; rotate GAIN control fully clockwise.

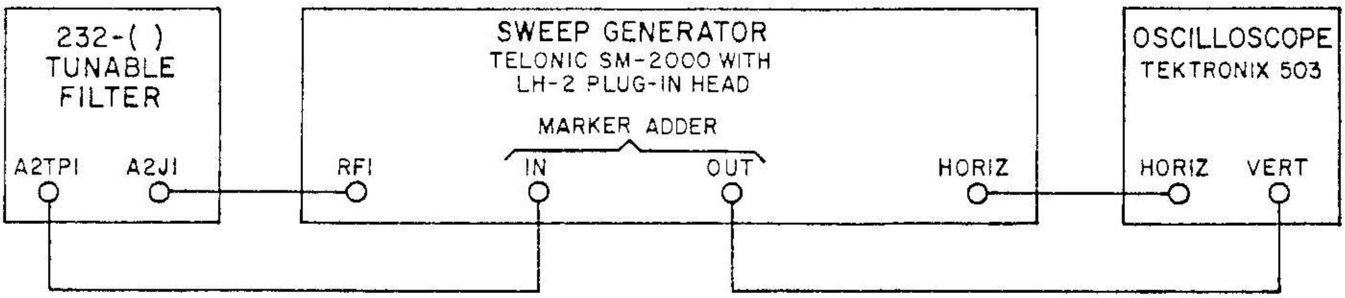


Figure 4-1. Equipment Setup, Type 232-( ) Tunable Filter, Overall Alignment

(4) Adjust the sweep generator and oscilloscope controls to display a response curve. The sweep rate will have to be decreased considerably to display the narrow bandwidth response.

(5) Adjust A2C55 for maximum base line shift.

(6) Adjust A2L7, A2L6, and A2L5, A2L3, A2L2, and A2C3 for a maximum amplitude, symmetrical response similar to the one shown in Figure 4-2.

(7) Disconnect the oscilloscope from the equipment setup.

(8) Connect the HP-400H AC VTVM to IF OUTPUT jack J4 on the rear apron.

NOTE

Terminate the IF output in a 10k ohm load prior to making the final adjustment described in step (9).

(9) Adjust inductor A2L8 for a maximum reading on the AC VTVM.

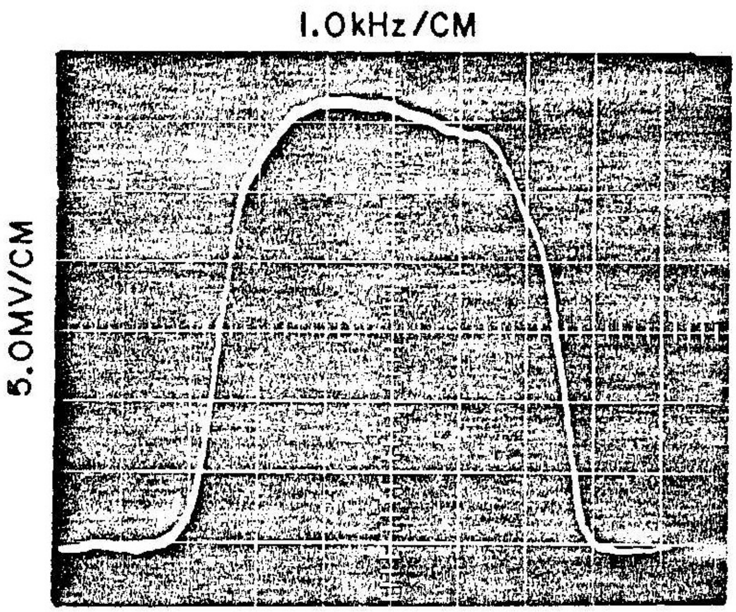


Figure 4-2. Typical Response,
Overall Filter Alignment

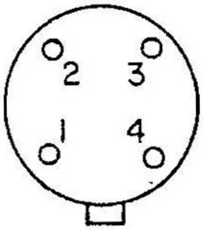
Table 4-1. Type 232-( ) Tunable Filter,
Typical Transistor Element Voltages

Ref. Desig.	Type	Gate 1	Gate 2	Drain	Source	Emitter	Base	Collector
A1A1Q1	2N5109					-8.50	-7.70	0.19
A1A1Q2	2N5109					1.89	2.63	10.11
A2Q1	3N140	1.08	2.95	16.7	1.23			
A2Q2	2N3933					3.00	3.74	16.23
A2Q3	3N140	1.11	2.30	17.02	1.40			
A2Q4	2N3933					3.11	3.04	14.54
A2Q5	3N140	1.09	3.26	16.50	1.23			
A2Q6	3N140	1.11	2.25	15.40	1.23			
A2Q7	2N3933					2.96	3.62	14.53
A2Q8	2N4074					3.58	4.21	6.95
A2Q9	2N4074					6.34	6.95	17.80
A3A1Q1	2N709A					6.58	7.68	18.15
A3A2Q1	2N3866					1.57	2.26	17.22
A3A2Q2	2N3866					1.94	2.65	18.15
A4Q1	2N3055					18.13	18.66	26.72
A4Q2	2N4074					18.66	19.26	26.71
A4Q3	2N4074					6.93	7.52	19.26
A4Q4	2N4074					6.93	7.55	17.39
A5Q1	2N4074					3.53	4.11	16.34
A5Q2	2N929					2.88	3.53	11.17
A5Q3	2N929					1.38	2.01	10.62
A5Q4	2N929					-0.66	0.0	11.52
A5Q5	2N929					0.67	1.27	0.72
A5Q6	2N4074					0.0	0.67	0.72
A6Q1	2N4037					-18.59	-19.21	-27.88

TEST CONDITIONS: All voltages are positive dc with respect to chassis unless otherwise noted. Readings taken with RCA WV-98C VTVM; 115 Vac applied, no signal input. Control Settings: GAIN, COR THRESHOLD, maximum CW; FINE TUNING midrange.

NOTES: 1. A bottom view diagram of the 3N140 is shown below.

3N140



1 Drain

2 Gate No. 2

3 Gate No. 1

4 Source

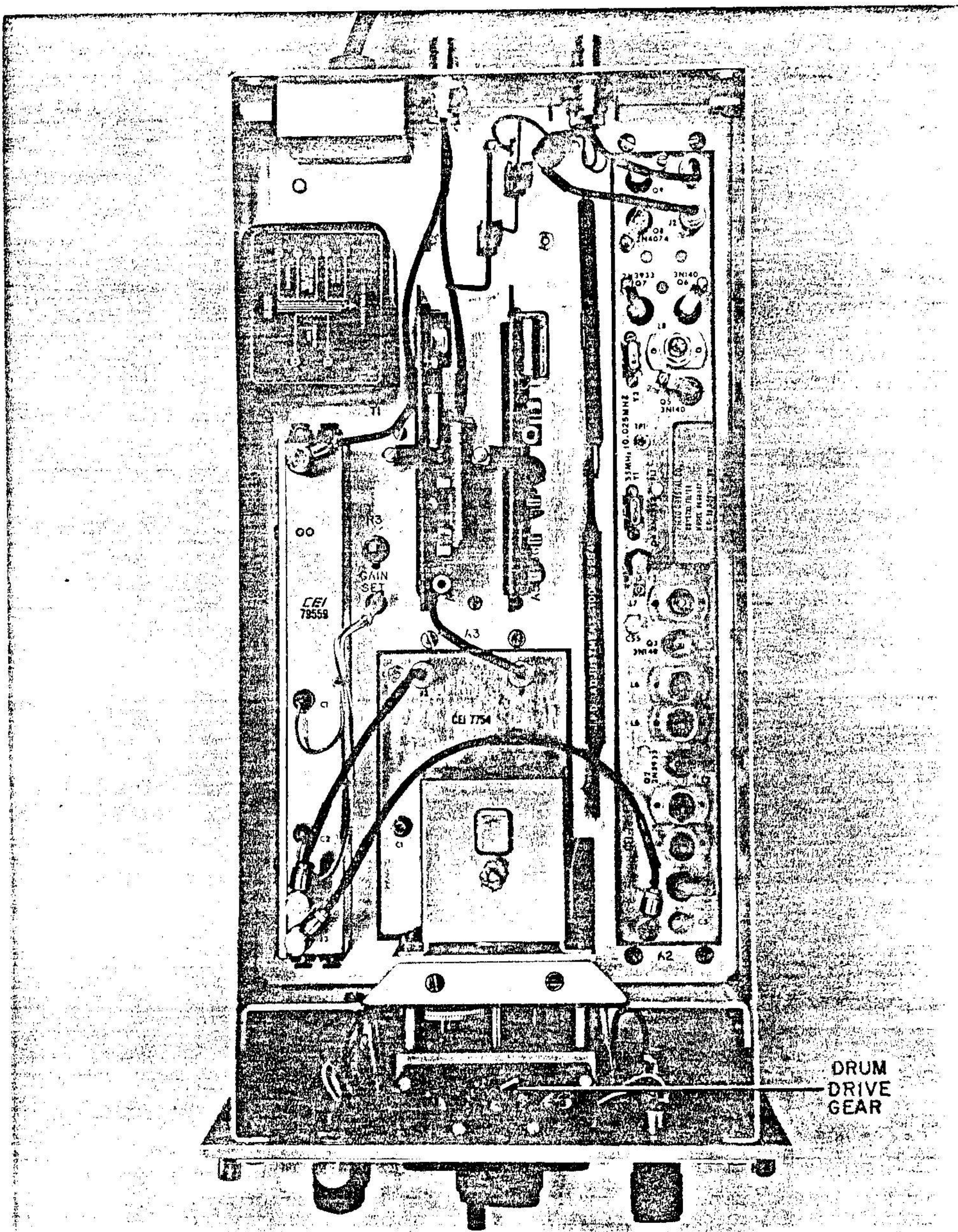


FIGURE 5-1. TYPE 232-( ) TUNABLE FILTER, TOP VIEW

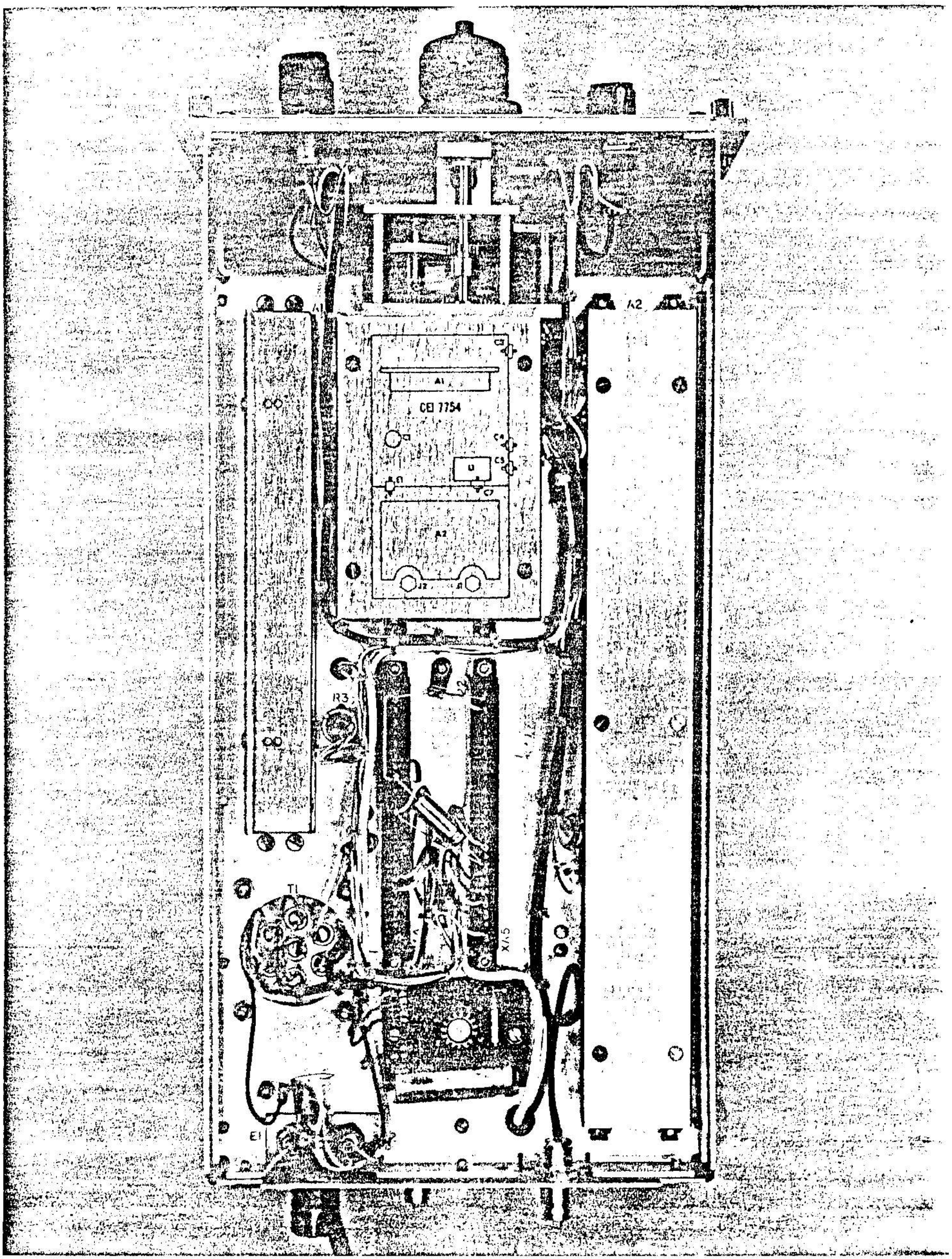
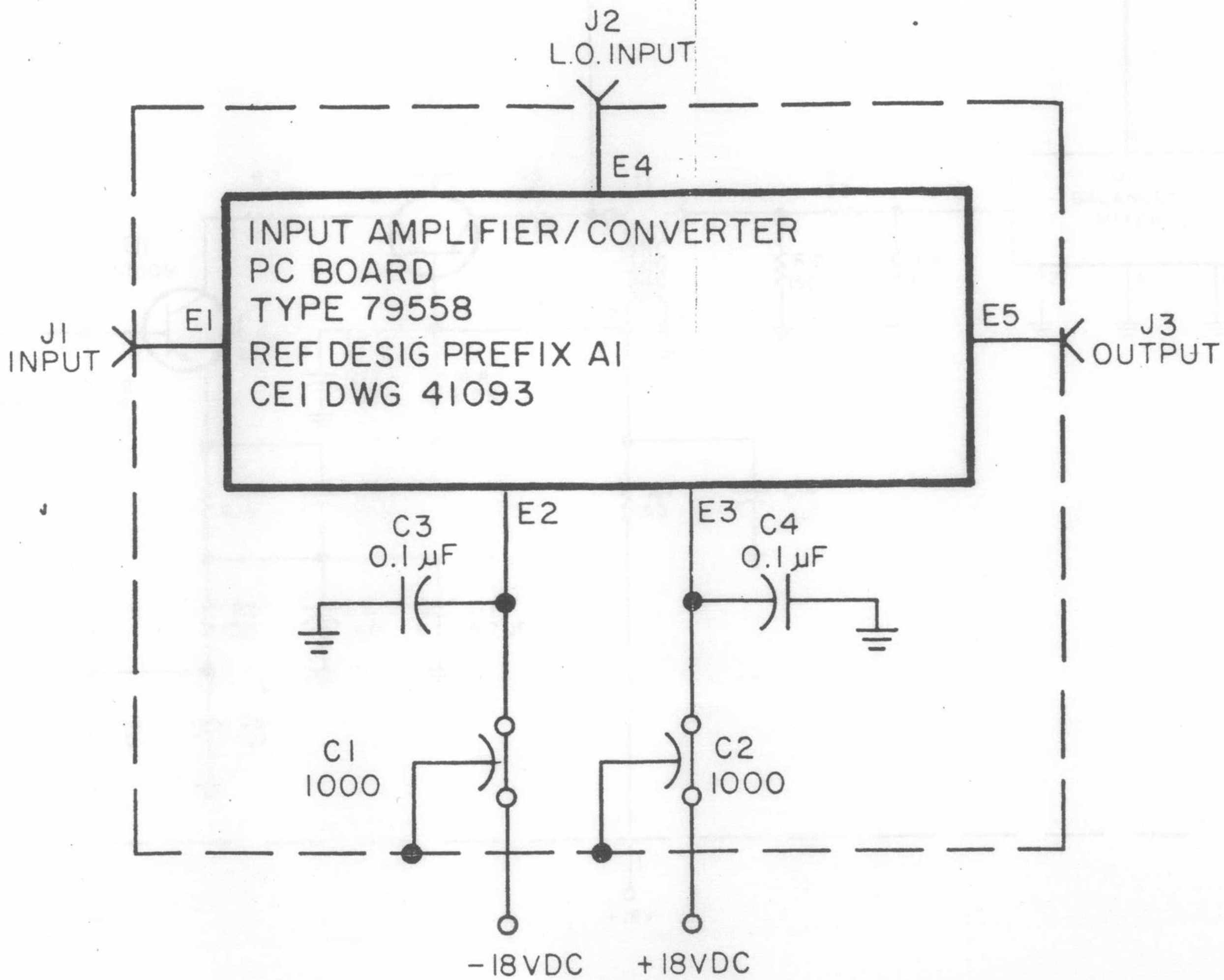
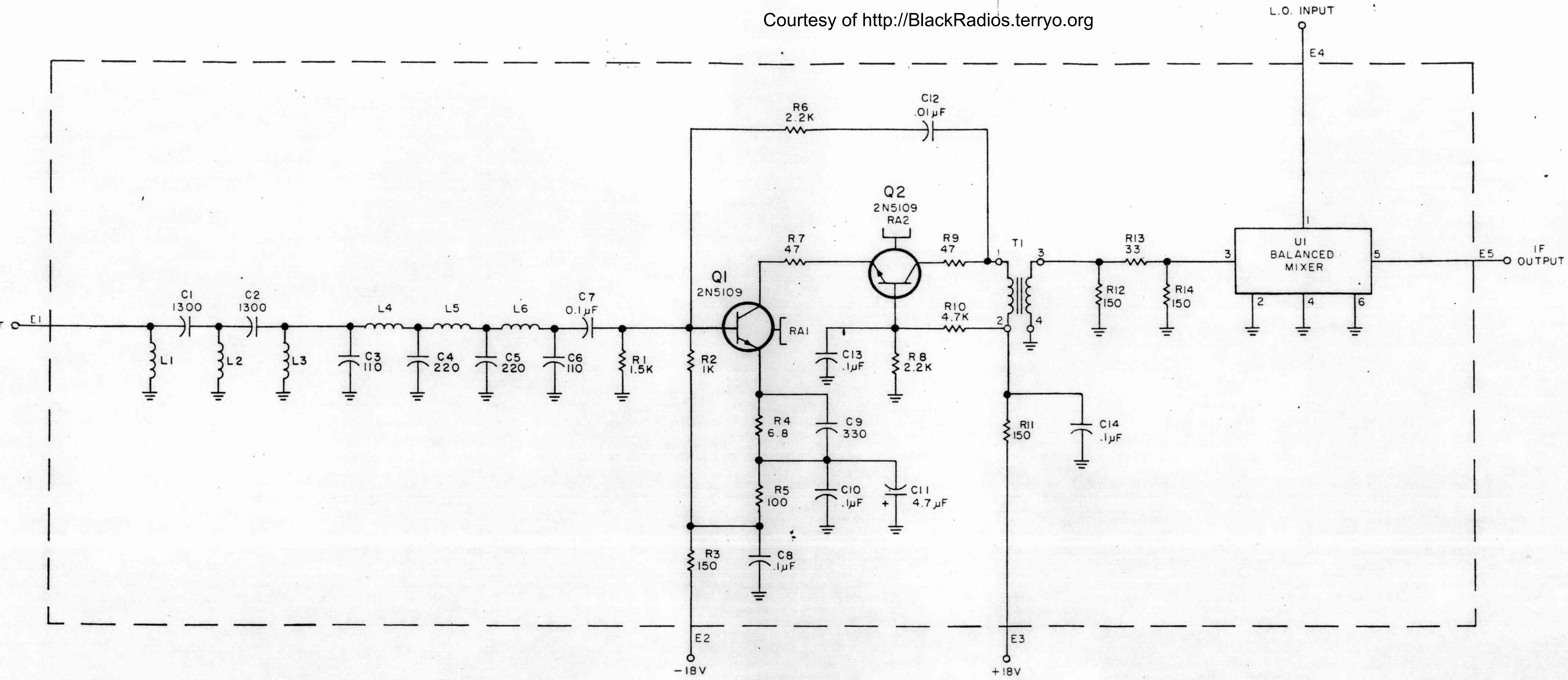


FIGURE 5-2. TYPE 232-( ) TUNABLE FILTER, BOTTOM VIEW



NOTE:
1. UNLESS OTHERWISE SPECIFIED:
a) CAPACITANCE IS MEASURED IN pF.

Figure 6-1. Type 79559 Input Amplifier/Converter Assembly, Schematic Diagram



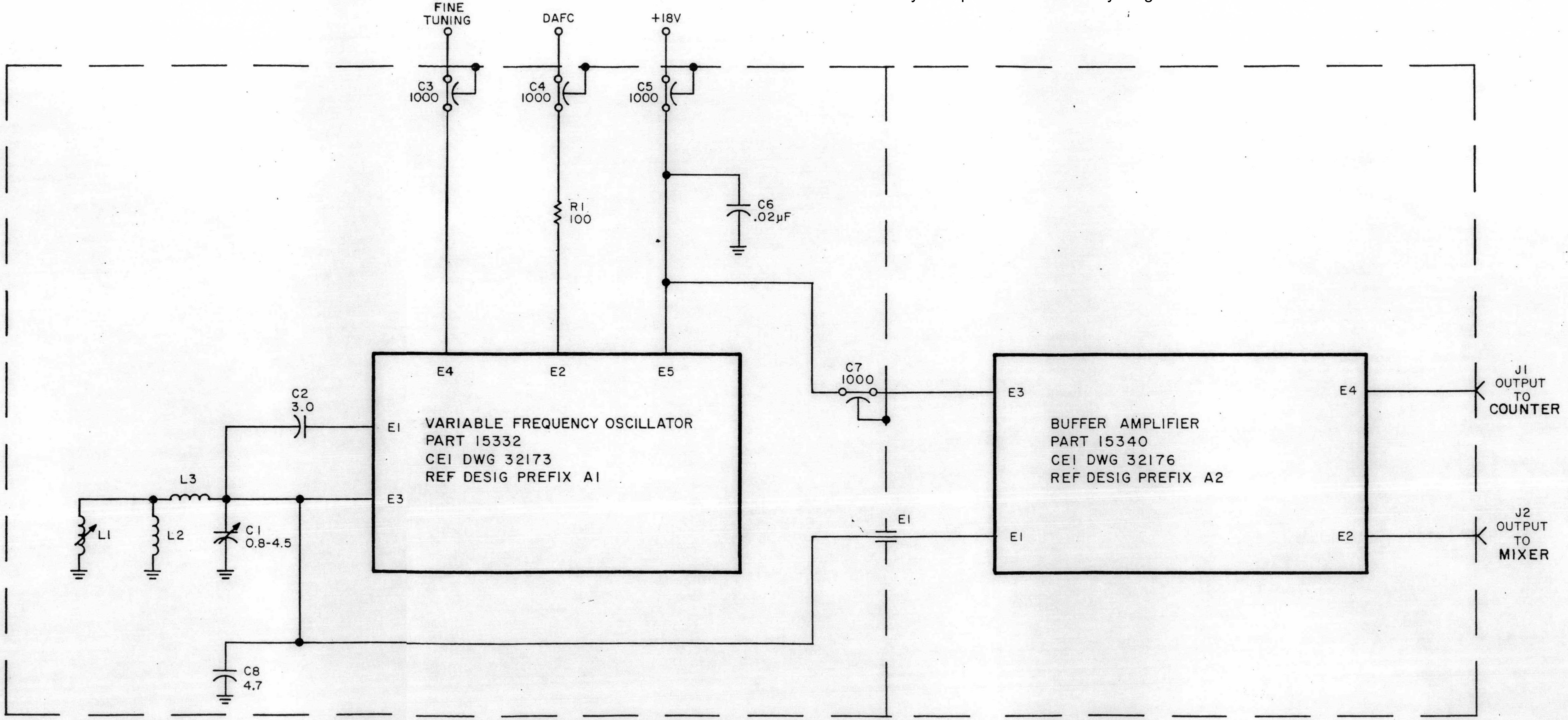
NOTES
1. UNLESS OTHERWISE SPECIFIED:
a) RESISTANCE IS MEASURED IN OHMS, ±5%, 1/4
b) CAPACITANCE IS MEASURED IN pF.

Figure 6-2. Type 79558 Input Amplifier/Converter PC Board, Schematic Diagram

NOTES

1. UNLESS OTHERWISE SPECIFIED
   a) RESISTANCE IS MEASURED IN OHMS, ±5%, 1/4W
   b) CAPACITANCE IS MEASURED IN pF
2. DIFFERENCE BETWEEN TYPES IS AT Y2. FREQUENCIES FOR Y2:
   TYPE 79595-1; 10.015MHz
   TYPE 79595-2; 10.025MHz

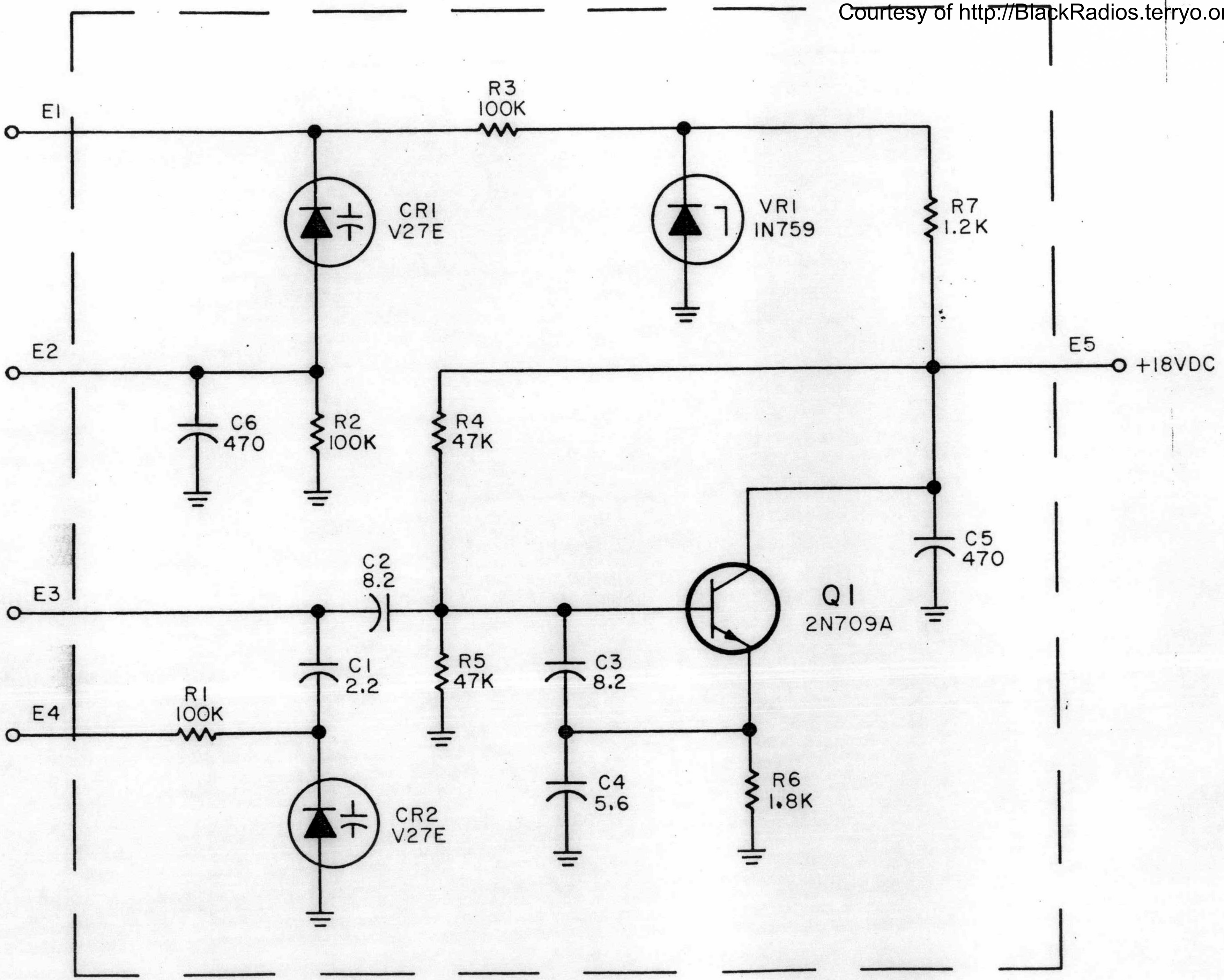
Figure 6-3. Type 79595 IF Amplifier/Converter Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) CAPACITANCE IS MEASURED IN pF.
   b) RESISTANCE IS MEASURED IN OHMS, 1/4W, 5%.

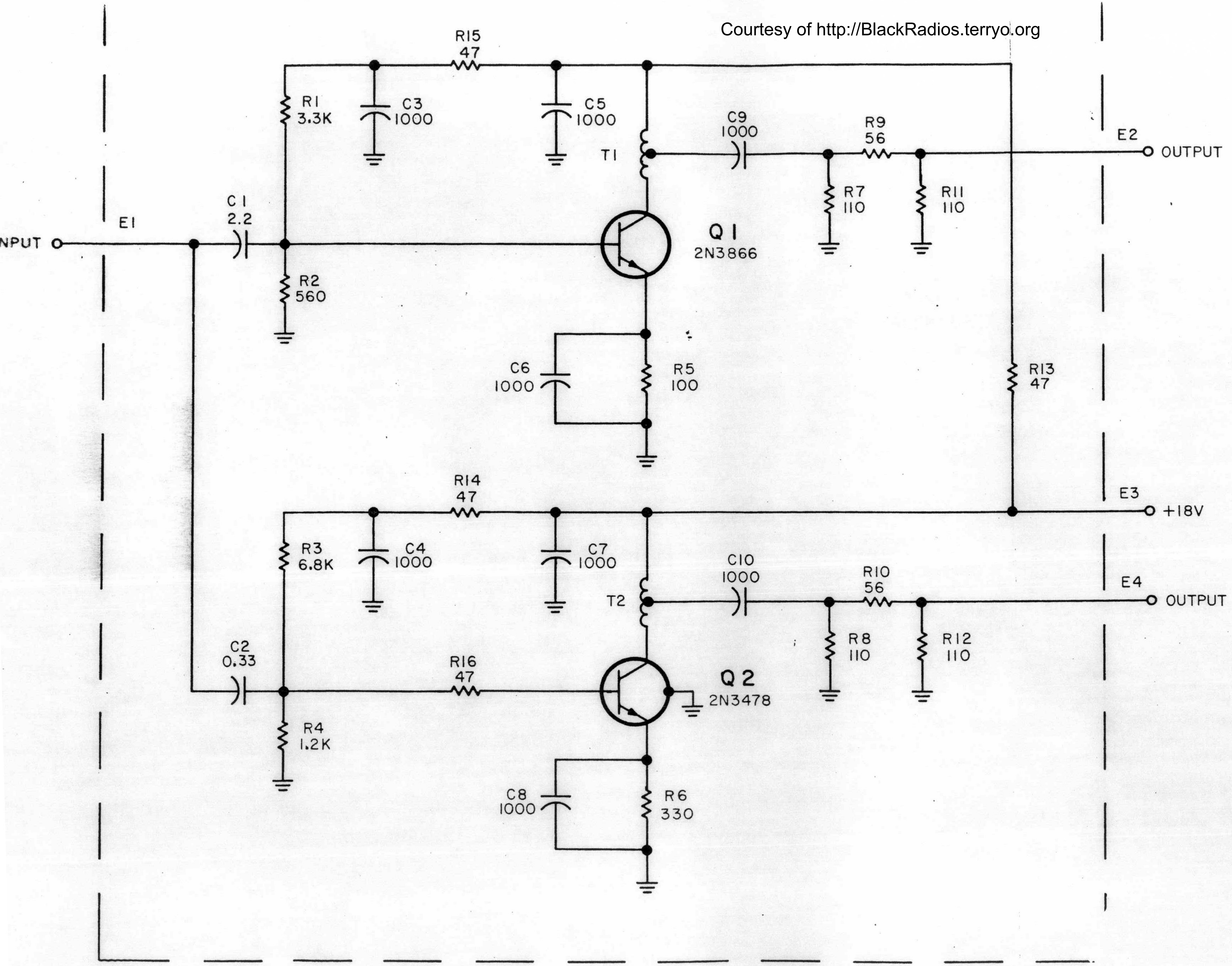
Figure 6-4. Type 7754 Variable Frequency Oscillator Assembly, Schematic Di



NOTES:

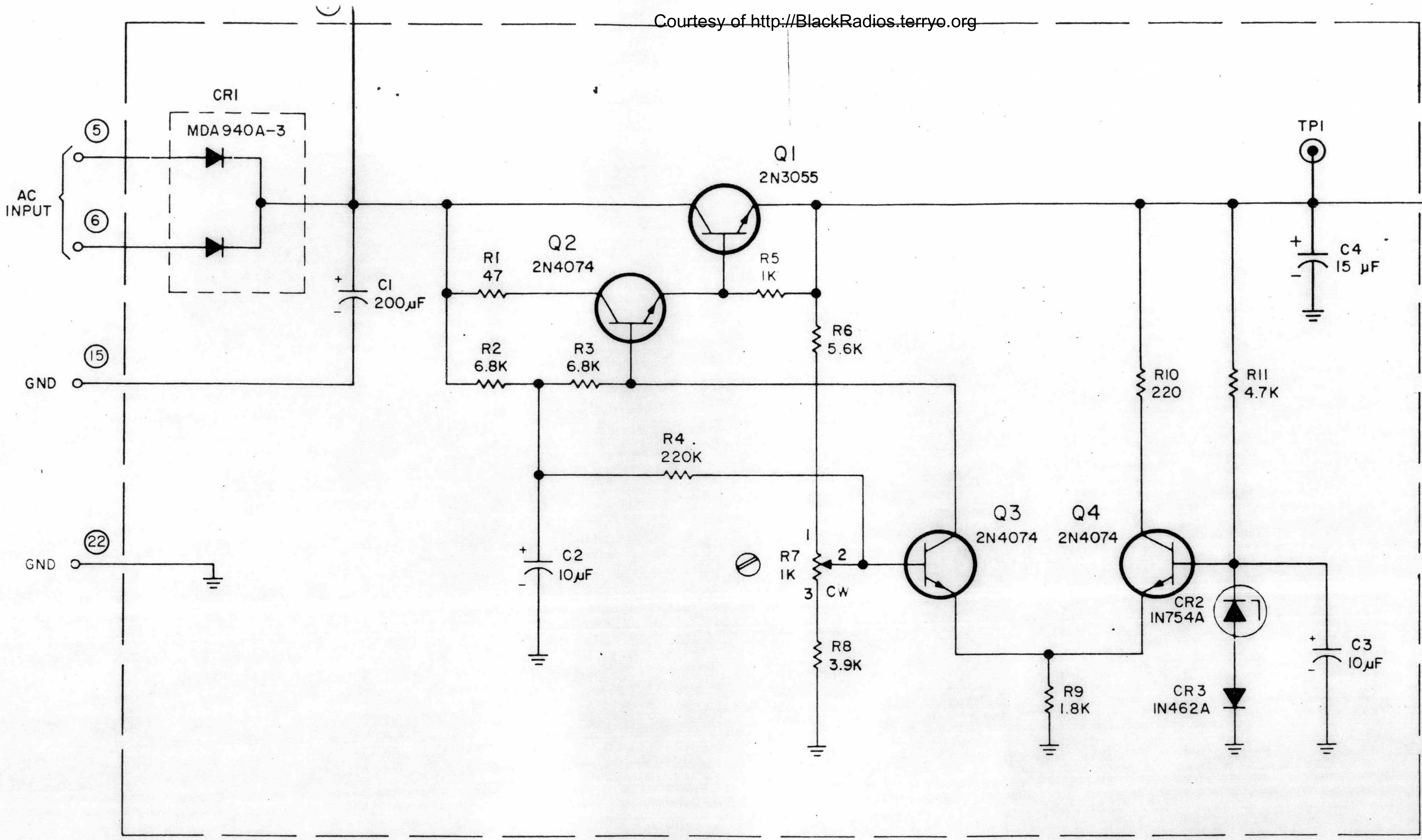
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS MEASURED IN OHMS, ±5%, 1/4W.
   b. CAPACITANCE IS MEASURED IN pF.

Figure 6-5. Part 15332 Variable Frequency Oscillator, Schematic Diagram



NOTES:

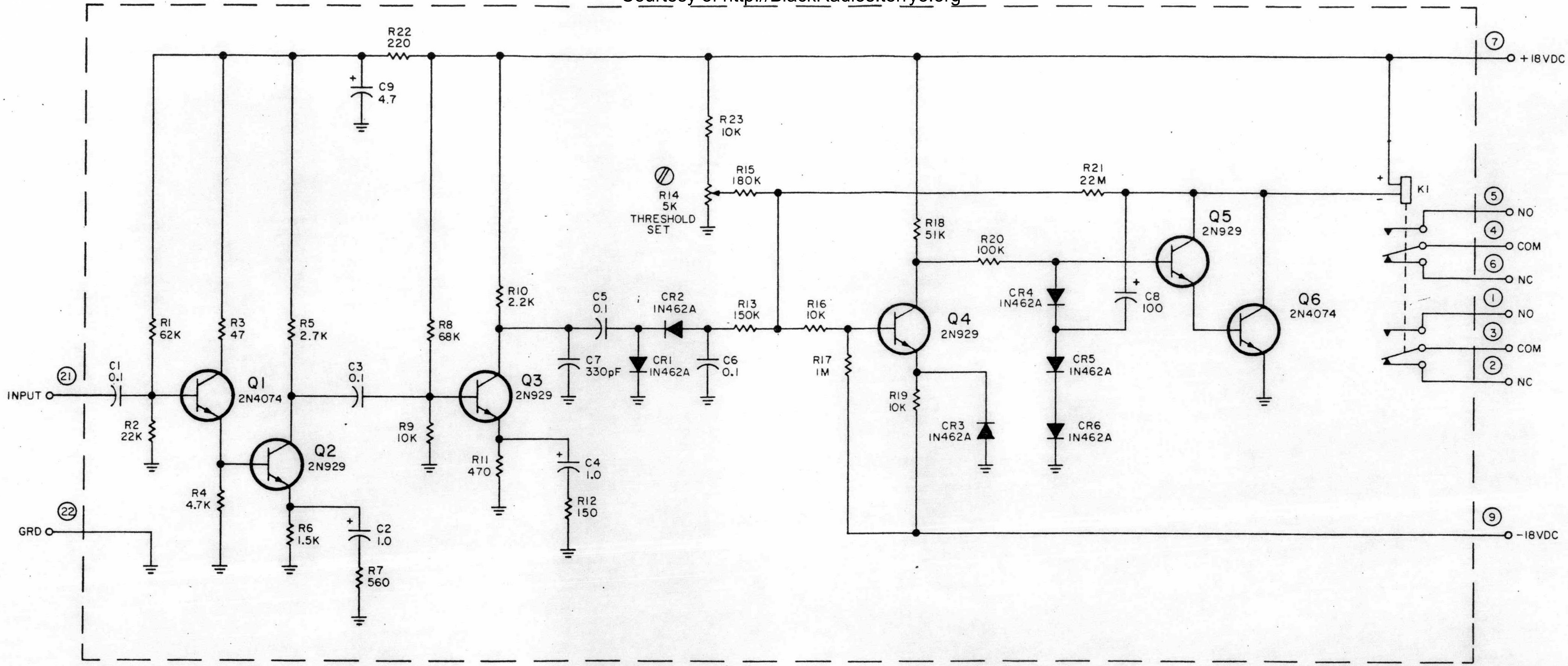
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS MEASURED IN OHMS, ±5%, 1/4W.
   b. CAPACITANCE IS MEASURED IN pF.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE IS MEASURED OHMS, ±5%, 1/4 W
2. ENCIRCLED NUMBERS ARE MODULE PIN NUMBERS
3. THE FOLLOWING NOTATIONS ARE USED ON POTENTIOMETERS
   CW INDICATES CLOCKWISE ROTATION
   ⊘ INDICATES SCREWDRIVER ADJUSTMENT

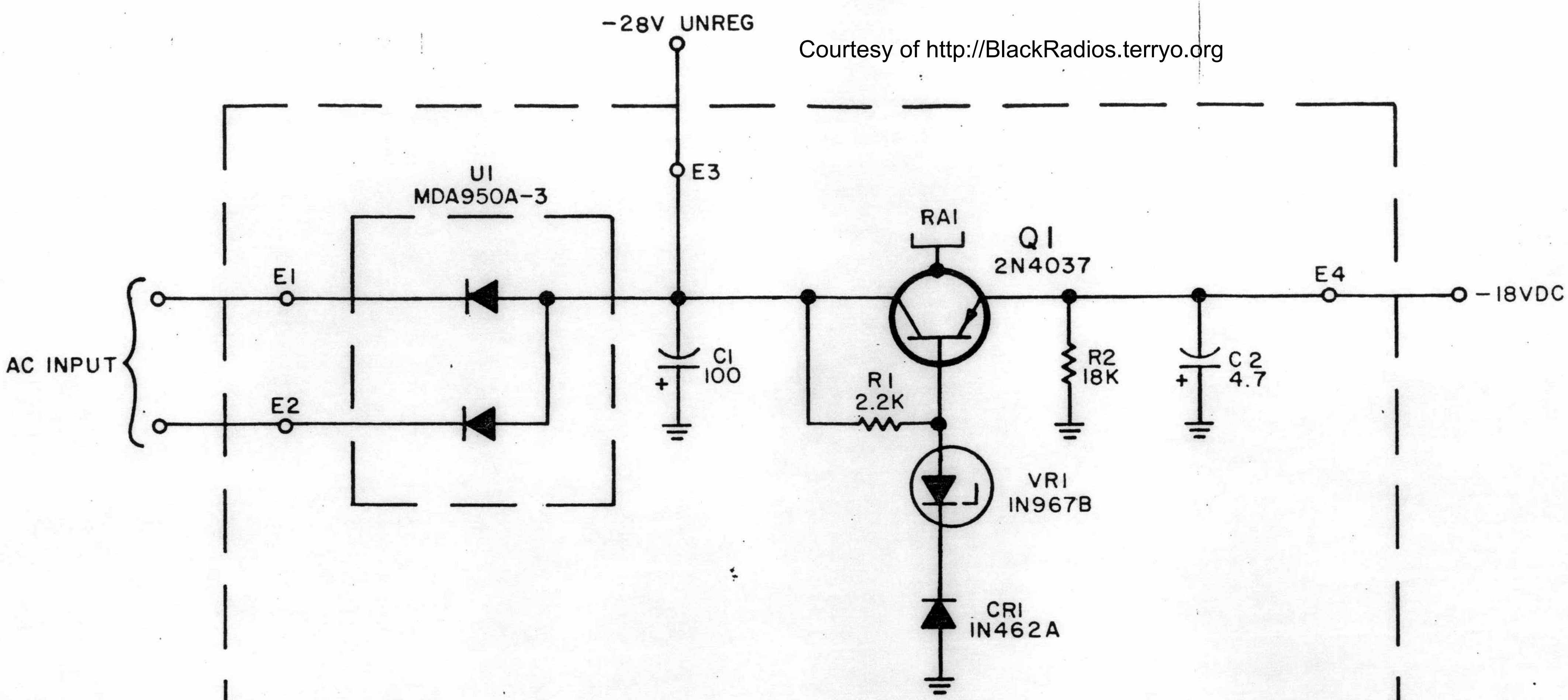
Figure 6-7. Type 76162 +18 Vdc Power Supply Regulator, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS MEASURED IN OHMS, 5%, 1/4W.
   b) CAPACITANCE IS MEASURED IN µF.
2. ENCIRCLED NUMBERS ARE MODULE PIN NUMBERS
3. THE FOLLOWING NOTATIONS ARE USED ON POTENTIOMETERS:
   a) ⊘ INDICATES SCREWDRIVER ADJUSTMENT.

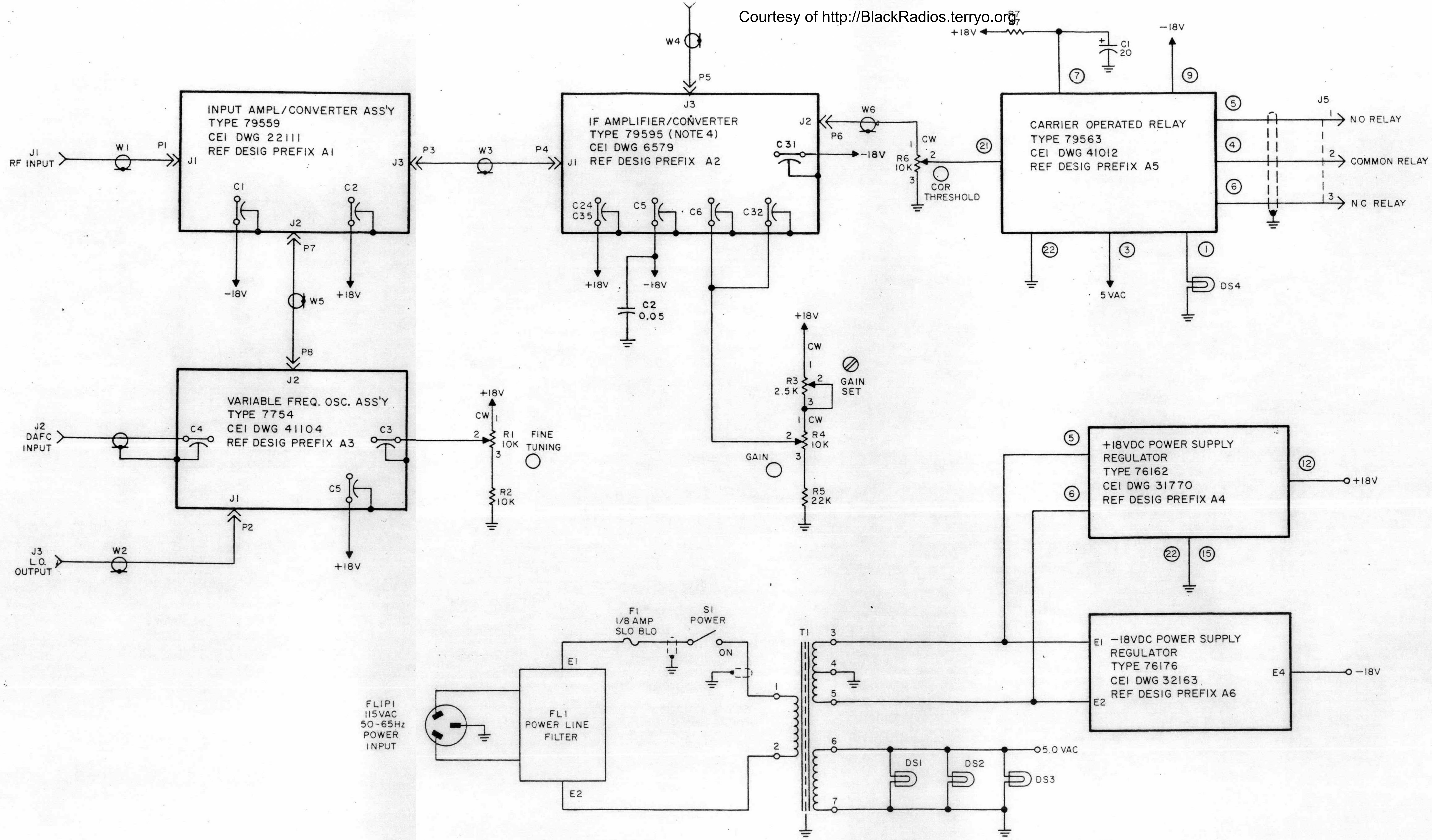
Figure 6-8. Type 79563 Carrier Operated Relay, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a.) RESISTANCE IS MEASURED IN OHMS, ±5%, 1/4W.
   b.) CAPACITANCE IS MEASURED IN μF.

Figure 6-9. Type 76176 -18 Vdc Power Supply Regulator, Schematic Diagram



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS MEASURED IN OHMS, ±5%, 1/4W.
   b) CAPACITANCE IS MEASURED IN uF.
2. ENCIRCLED NUMBERS ARE MODULE PIN NUMBERS.
3 THE FOLLOWING NOTATIONS ARE USED ON POTENTIOMETERS
   a) CW INDICATES CLOCKWISE ROTATION
   b) ◯ INDICATES FRONT PANEL CONTROL.
   c) ⊘ INDICATES SCREWDRIVER ADJUST
4. THE DIFFERENCE BETWEEN TYPES IS AT A2.
   TYPE 79595-1 IS USED ON TYPE 232-1.
   TYPE 79595-2 IS USED ON TYPE 232-2.